

# Renesas RA2A1 Group

# Renesas RA2A1 Group

Datasheet

Datasheet

## 32-Bit MCU

Renesas Advanced (RA) Family  
Renesas RA2 Series

瑞萨电子高级(RA)系列32位MCU

Renesas RA2 Series

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (<http://www.renesas.com>).

这些材料中包含的所有信息，包括产品和产品规格，均代表发布时的产品信息，瑞萨电子有限公司如有更改，恕不另行通知。请查看瑞萨电子有限公司通过各种方式发布的最新信息，包括瑞萨电子有限公司网站(<http://www.renesas.com>)。

Ultra-low power 48-MHz Arm® Cortex®-M23 core, up to 256-KB code flash memory, 32-KB SRAM, Capacitive Touch Sensing Unit, 16-bit A/D Converter, 24-bit sigma-delta A/D Converter, 12-bit D/A Converter, 8-bit D/A Converter, Operational Amplifier, security and safety features.

## Features

### ■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, and CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

### ■ Memory

- Up to 256-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- Up to 32-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Unit (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity

- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I<sup>2</sup>C bus interface (IIC) × 2
- Controller Area Network (CAN) module

### ■ Analog

- 16-bit A/D Converter (ADC16)
  - 1.2 Msps
  - Differential input mode
  - Single-ended input mode
- 24-bit Sigma-Delta A/D Converter (SDADC24)
  - 15.6 ksps
  - Differential input mode
  - Single-ended input mode
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) × 2
- High-Speed Analog Comparator (ACMPHS)
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 3
- Temperature Sensor (TSN)

### ■ Timers

- General PWM Timer 32-bit (GPT32)
- General PWM Timer 16-bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety

- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management

- Low power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption

- AES128/256
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSU)

### ■ Multiple Clock Sources

- Main clock oscillator (MOSC)
  - (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  - (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  - (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  - (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  - (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  - (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General Purpose I/O Ports

- Up to 49 input/output pins
  - Up to 3 CMOS input
  - Up to 46 CMOS input/output
  - Up to 9 input/output 5 V tolerant
  - Up to 3 high current (20 mA)

### ■ Operating Voltage

- VCC: 1.6 to 5.5 V

### ■ Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 36-pin BGA (5 mm × 5 mm, 0.8 mm pitch)
- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

超低功耗48-MHz Arm® Cortex®-M23内核、高达256-KB代码闪存、32-KBSRAM、电容式触控传感单元 16位AD转换器 24位sigma-delta AD转换器 12位DA转换器 8位DA转换器 运算放大器，安全和安全功能。

## Features

■ ArmCortex-M23内核 Armv8-M架构 最大工作频率: 48 MHz 具有8个区域的Arm内存保护单元(ArmMPU) 调试和跟踪: DWT、FPB和CoreSight MTB-M23 CoreSight调试端口: SW-DP

### ■ Memory

高达256KB代码闪存 8KB数据闪存 (100 000次程序擦除(PE)周期) 高达32KBSRAM 闪存高速缓存(FCACHE) 内存保护单元(MPU) 内存镜像功能(MMF) 128位唯一ID

### ■ Connectivity

USB2.0全速(USBFS)模块 带稳压器的片上收发器符合USB电池充电规范1.2 串行通信接口(SCI)×3UART简单IIC简单SPI 串行外设接口(SPI)×2 I2C总线接口(IIC)×2 控制器局域网(CAN)模块

### ■ Analog

16位AD转换器(ADC16)1.2Msps差分输入模式 单端输入模式 24位Sigma-DeltaAD转换器(SDAC24)15.6ksps差分输入模式单端输入模式 12位DA转换器(DAC12) 8位DA转换器(DAC8)×2 高速模拟比较器(ACMPHS) 低功耗模拟比较器(ACMPLP)×2 运算放大器(OPAMP)×3 温度传感器(TSN)

### ■ Timers

通用PWM定时器32位(GPT32) 通用PWM定时器16位(GPT16)×6 异步通用定时器(AGT)×2 看门狗定时器(WDT)

### ■ Safety

SRAM中的纠错码(ECC) SRAM奇偶校验错误检查 闪存区域保护 ADC自诊断功能 时钟频率精度测量电路(CAC) 循环冗余校验(CRC)计算器 数据操作电路(DOC) 端口GP T(POEG)的输出使能 独立看门狗定时器(IWDT) GPIO回读电平检测 寄存器写保护 主振荡器停止检测 非法内存访问

■系统和电源管理 低功耗模式 实时时钟(RTC) 事件链接控制器(ELC) 数据传输控制器(DTC) 按键中断功能(KINT) 上电复位 带电压的低电压检测(LVD)设置

■安全和加密 AES128/256 真随机数生成器(TRNG)

■人机界面(HMI) 电容式触摸传感单元(CTSU)

### ■多个时钟源

主时钟振荡器(MOSC) (当VCC=2.4到5.5V时为1到20MHz) (当VCC=1.8到5.5V时为1到8MHz) (当VCC=1.6到5.5V时为1到4MHz) 副时钟振荡器(SOSC)(32.768kHz) 高速片上振荡器(HOCO) (当VCC=2.4到5.5V时为24、32、48、64MHz) (当VCC=1.8到5.5V时为24、32、48MHz) (当VCC=1.6到5.5V时为24、32MHz) 中速片上振荡器(MOCO)(8MHz) 低速片上振荡器(LOCO)(32.768kHz) IWDT专用片上振荡器(15kHz) HOCOMOCOLOC的时钟微调功能 时钟输出支持

■通用IO端口 最多49个输入输出引脚 最多3个CMOS输入最多46个CMOS输入输出最多9个输入输出5V耐受最多3个高电流(20mA)

■工作电压 VCC: 1.6至5.5V

■工作温度和封装 Ta=-40°C至+85°C

36引脚BGA (5mm×5mm, 0.8mm间距) T a=-40°C至+105°C  
 - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)  
 - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)  
 - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)  
 - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

## 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 256-KB code flash memory
- 32-KB SRAM
- 16-bit A/D Converter (ADC16)
- 24-bit Sigma-Delta A/D Converter (SDADC24)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8)
- Operational Amplifier (OPAMP) with configurable switches
- Security features.

### 1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	<ul style="list-style-type: none"> <li>• Maximum operating frequency: up to 48 MHz</li> <li>• Arm Cortex-M23 core: <ul style="list-style-type: none"> <li>- Revision: r1p0-00rel0</li> <li>- Armv8-M architecture profile</li> <li>- Single-cycle integer multiplier</li> <li>- 17-cycle integer divider.</li> </ul> </li> <li>• Arm Memory Protection Unit (Arm MPU): <ul style="list-style-type: none"> <li>- Armv8 Protected Memory System Architecture</li> <li>- 8 protect regions.</li> </ul> </li> <li>• SysTick timer: <ul style="list-style-type: none"> <li>- Driven by SYSTICCLK (LOCO) or ICLK.</li> </ul> </li> </ul>

Table 1.2 Memory

Feature	Functional description
Code flash memory	256 KB of code flash memory. See section 43, Flash Memory in User's Manual.
Data flash memory	8 KB of data flash memory. See section 43, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 42, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: <ul style="list-style-type: none"> <li>• Single-chip mode</li> <li>• SCI or USB boot mode.</li> </ul> See section 3, Operating Modes in User's Manual.

## 1. Overview

MCU集成了多个系列软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外设，以促进设计可扩展性和基于平台的高效产品开发。

该系列中的MCU采用了高效ArmCortex®-M2332位内核，特别适合对成本敏感的低功耗应用，具有以下特性：

- 高达256KB的代码闪存
- 32-KB SRAM
- 16-bit A/D Converter (ADC16)
- 24-bit Sigma-Delta A/D Converter (SDADC24)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8)
- 具有可配置开关的运算放大器(OPAMP)
- 安全功能。

### 1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M23内核	最大工作频率：高达48MHz ArmCortex-M23内核；修订版：r1p0-00rel0Armv8-M架构配置 文件单周期整数乘法器17周期整数除法器。 Arm内存保护单元 (ArmMPU)：  Armv8ProtectedMemorySystemArchitecture8保护区。 SysTick计时器：  由SYSTICCLK(LOCO)或ICLK驱动。

Table 1.2 Memory

Feature	功能说明
代码闪存	256KB代码闪存。请参阅用户手册中的第43节，闪存。
数据闪存	8KB数据闪存。请参阅用户手册中的第43节，闪存。
内存镜像功能(MMF)	内存镜像功能(MMF)可配置为将代码闪存中所需的应用程序映像加载地址镜像到23位未使用的内存空间（内存镜像空间地址）中的应用程序映像链接地址。您的应用程序代码已开发并链接到从该MMF目标地址运行。您的应用程序代码不需要知道它存储在代码闪存中的加载位置。请参阅用户手册中的第5节，内存镜像功能(MMF)。
Option-setting memory	选项设置存储器确定复位后MCU的状态。见第7节，用户手册中的选项设置内存。
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。请参阅用户手册中的第42节，SRAM。

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种工作模式：单芯片模式 SCI或USB启动模式。请参阅用户手册中的第3节操作模式。

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	<p>13 resets:</p> <ul style="list-style-type: none"> <li>• RES pin reset</li> <li>• Power-on reset</li> <li>• Independent watchdog timer reset</li> <li>• Watchdog timer reset</li> <li>• Voltage monitor 0 reset</li> <li>• Voltage monitor 1 reset</li> <li>• Voltage monitor 2 reset</li> <li>• SRAM parity error reset</li> <li>• SRAM ECC error reset</li> <li>• Bus master MPU error reset</li> <li>• Bus slave MPU error reset</li> <li>• CPU stack pointer error reset</li> <li>• Software reset.</li> </ul> <p>See section 6, Resets in User's Manual.</p>
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	<ul style="list-style-type: none"> <li>• Main clock oscillator (MOSC)</li> <li>• Sub-clock oscillator (SOSC)</li> <li>• High-speed on-chip oscillator (HOCO)</li> <li>• Middle-speed on-chip oscillator (MOCO)</li> <li>• Low-speed on-chip oscillator (LOCO)</li> <li>• IWDT-dedicated on-chip oscillator</li> <li>• Clock out support.</li> </ul> <p>See section 9, Clock Generation Circuit in User's Manual.</p>
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 19, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. See section 12, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 24, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.3 系统(2之2)

Feature	功能说明
Resets	<p>13次复位: RES引脚复位上电复位独立看门狗定时器复位看门狗定时器复位电压监视器0复位电压监视器1复位电压监视器2复位SRAM奇偶校验错误复位SRAM ECC错误复位总线主控MPU错误复位总线从属MPU错误复位 CPU堆栈指针错误复位 软件复位。请参阅用户手册中的第6节, 重置。</p>
低电压检测(LVD)	低电压检测(LVD)功能监控输入到VCC引脚的电压电平, 并且可以使用软件程序选择检测电平。请参阅用户手册中的第8节, 低电压检测(LVD)。
Clocks	主时钟振荡器(MOSC) 子时钟振荡器(SOSC) 高速片上振荡器(HOCO) 中速片上振荡器(MOCO) 低速片上振荡器(LOCO) IWDT-专用片上振荡器 时钟输出支持。请参阅用户手册中的第9节, 时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在用作测量基准的时钟(测量基准时钟)生成的时间内对要测量的时钟(测量目标时钟)的脉冲进行计数, 并根据是否脉冲数在允许范围内。当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时, 将产生中断请求。请参阅用户手册中的第10节, 时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到NVIC/DTC模块。ICU还控制NMI中断。请参阅用户手册中的第13节, 中断控制器单元(ICU)。
按键中断功能(KINT)	通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚输入上升沿或下降沿, 可以生成按键中断。请参阅用户手册中的第19节, 按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗, 例如通过设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅用户手册中的第11节, 低功耗模式。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。请参见用户手册中的第12节, 寄存器写保护。
内存保护单元(MPU)	提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能用于内存保护。请参阅用户手册中的第15节, 内存保护单元(MPU)。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器, 可用于在计数器下溢时复位MCU, 因为系统已失控且无法刷新WDT。此外, 下溢可能会产生不可屏蔽的中断或中断。可以设置一个允许刷新周期来刷新计数器, 并作为检测系统何时失控的条件。请参阅用户手册中的第24节, 看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器, 必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或为定时器下溢生成不可屏蔽中断中断的功能。由于定时器使用独立的专用时钟源运行, 因此当系统失控时, 它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以在复位、下溢、刷新错误或寄存器中的计数值刷新时自动触发。请参阅用户手册中的第25节, 独立看门狗定时器(IWDT)。



Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 17, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 16, Data Transfer Controller (DTC) in User's Manual.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with one channel and a 16-bit timer with six channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 21, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 20, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 22, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC) in User's Manual.

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> <li>Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA))</li> <li>8-bit clock synchronous interface</li> <li>Simple IIC (master-only)</li> <li>Simple SPI</li> <li>Smart card interface.</li> </ul> The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI) in User's Manual.
I <sup>2</sup> C bus interface (IIC)	The 2-channel I <sup>2</sup> C bus interface (IIC) conforms with and provides a subset of the NXP I <sup>2</sup> C (Inter-Integrated Circuit) bus interface functions. See section 28, I <sup>2</sup> C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 30, Serial Peripheral Interface (SPI) in User's Manual.

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的中断请求作为事件信号, 将它们连接到不同的模块, 实现模块之间的直接交互, 无需CPU干预。请参阅用户手册中的第17节, 事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅用户手册中的第16节, 数据传输控制器(DTC)。

Table 1.6 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有1个通道的32位定时器和一个具有6个通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外, 可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参阅用户手册中的第21节, 通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	使用PortOutputEnableforGPT(POEG)功能将通用PWM定时器(GPT)输出引脚置于输出禁用状态。请参阅用户手册中的第20节, GPT(POEG)的端口输出启用。
异步通用Timer (AGT)	异步通用定时器(AGT)是一个16位定时器, 可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址, 可以通过AGT寄存器访问。请参阅用户手册中的第22节, 异步通用定时器(AGT)。
实时时钟(RTC)	实时时钟(RTC)有两种计数模式, 日历计数模式和二进制计数模式, 由寄存器设置控制。对于日历计数模式, RTC有一个从2000年到2099年的100年日历, 并自动调整闰年的日期。对于二进制计数模式, RTC会计算秒数并将信息保留为序列值。  二进制计数模式可用于公历(西方)以外的日历。请参阅用户手册中的第23节, 实时时钟(RTC)。

Table 1.7 通信接口 (2个中的1个)

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)可配置为五个异步和同步串行接口: 异步接口(UART和异步通信接口适配器(ACIA)) 8位时钟同步接口 简单IIC(仅限主机) 简单SPI 智能卡接口。智能卡接口符合ISO/IEC7816-3电子信号和传输协议标准。SCI0具有FIFO缓冲器以实现连续和全双工通信, 并且可以使用片上波特率发生器独立配置数据传输速度。请参阅用户手册中的第27节, 串行通信接口(SCI)。
I <sup>2</sup> C总线接口(IIC)	2通道I <sup>2</sup> C总线接口(IIC)符合并提供NXP I <sup>2</sup> C(内部集成电路)总线接口功能的子集。请参阅用户手册中的第28节, I <sup>2</sup> C总线接口(IIC)。
串行外设接口(SPI)	两个独立的串行外设接口(SPI)通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。请参阅用户手册中的第30节, 串行外设接口(SPI)。

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 29, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a device controller. The module supports full-speed and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of five pipes. Pipe 0 and pipe 4 to pipe 7 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. The MCU supports Battery Charging Specification revision 1.2. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply 3.3 V. See section 26, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.8 Analog (1 of 2)

Feature	Functional description
16-bit A/D Converter (ADC16)	A successive approximation 16-bit A/D Converter (ADC16) is provided. Up to 17 single-ended/4 differential analog input channels are selectable. Reference voltage of SDADC24, temperature sensor output, and internal reference voltage are selectable for conversion. The calibration function calculates capacitor array DAC and gain/offset correction values under the usage conditions to enable accurate A/D conversion. See section 32, 16-Bit A/D Converter (ADC16) in User's Manual.
24-bit Sigma-Delta A/D Converter (SDADC24)	A 24-bit Sigma-Delta A/D Converter (SDADC24) with a programmable gain instrumentation amplifier is provided. Up to 10 single-ended/5 differential analog input channels are selectable. The 2 single-ended/1 differential analog input channels of these analog input channels are inputs from internal OPAMP. Analog input multiplexer is input to the sigma-delta A/D converter by the programmable gain instrumentation amplifier (PGA). The A/D conversion result is filtered by the SINC3 digital filter, and then stored in an output register. The calibration function calculates gain error and offset error correction values under the usage conditions to enable accurate A/D conversion. See section 33, 24-Bit Sigma-Delta A/D Converter (SDADC24) in User's Manual.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) is provided. See section 34, 12-Bit D/A Converter (DAC12) in User's Manual.
8-bit D/A Converter (DAC8)	An 8-bit D/A Converter (DAC8) is provided. See section 35, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC16 for conversion and can be further used by the end application. See section 36, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a reference voltage with an analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from either an input to the IVREFi (i = 0 to 2) pin, an output from internal D/A converter, or from the internal reference voltage (Vref) generated internally in the MCU. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 38, High-Speed Analog Comparator (ACMPHS) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference voltage with an analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 39, Low-Power Analog Comparator (ACMPLP) in User's Manual.

Table 1.7 通信接口 (2个中的2个)

Feature	功能说明
控制器局域网(CAN)模块	控制器局域网(CAN)模块提供了在电磁噪声应用中使用基于消息的协议在多个从机和主机之间接收和传输数据的功能。CAN模块符合ISO11898-1(CAN2.0A/CAN2.0B)标准,最多支持32个邮箱,可配置为普通邮箱和FIFO模式下的发送或接收。支持标准(11位)和扩展(29位)消息格式。请参阅用户手册中的第29节,控制器局域网(CAN)模块。
USB2.0全速(USBFS)模块	USB2.0全速(USBFS)模块可以作为设备控制器运行。该模块支持通用串行总线规范2.0中定义的全速和低速传输。该模块有一个内部USB收发器,支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器,最多提供五个管道。可以根据用于通信的外围设备或根据您的系统为管道0和管道4到管道7分配任何端点编号。MCU支持电池充电规范1.2版。由于MCU可以在5V下供电,USBLDO稳压器为内部USB收发器提供3.3V电源。请参阅用户手册中的第26节,USB2.0全速模块(USBFS)。

Table 1.8 模拟(1of2)

Feature	功能说明
16-bit A/D Converter (ADC16)	提供了一个逐次逼近型16位模数转换器(ADC16)。最多可选择17个单端4个差分模拟输入通道。SDADC24的参考电压、温度传感器输出和内部参考电压可选择进行转换。校准功能在使用条件下计算电容器阵列DAC和增益偏移校正,以实现准确的AD转换。请参阅用户手册中的第32节,16位AD转换器(ADC16)。
24-bit Sigma-Delta A/D Converter (SDADC24)	提供带有可编程增益仪表放大器的24位Sigma-DeltaAD转换器(SDADC24)。最多可选择10个单端5个差分模拟输入通道。这些模拟输入通道的2个单端1个差分模拟输入通道是来自内部OPAMP的输入。模拟输入多路复用器通过可编程增益仪表放大器(PGA)输入到sigma-deltaAD转换器。AD转换结果经SINC3数字滤波器滤波,然后存入输出寄存器。校准功能计算使用条件下的增益误差和偏移误差校正,以实现精确的AD转换。请参阅用户手册中的第33节,24位Sigma-DeltaAD转换器(SDADC24)。
12-bit D/A Converter (DAC12)	提供了一个12位DA转换器(DAC12)。请参阅第34节,12位DA转换器(DAC12) User's Manual.
8-bit D/A Converter (DAC8)	提供了一个8位DA转换器(DAC8)。请参阅第35节,8位DA转换器(DAC8) User's Manual.
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度,以确保器件可靠运行。传感器输出与管芯温度成正比的电压,管芯温度与输出电压呈线性关系。输出电压被提供给ADC16进行转换,并且可以被最终应用进一步使用。请参阅用户手册中的第36节,温度传感器(TSN)。
高速模拟比较器(ACMPHS)	高速模拟比较器(ACMPHS)将参考电压与模拟输入电压进行比较。比较结果可以通过软件读取,也可以对外输出。参考电压可以从IVREFi(i=0至2)引脚的输入、内部DA转换器的输出或MCU内部生成的内部参考电压(Vref)中选择。这种灵活性在需要在模拟信号之间执行go-no-go比较而并不一定需要AD转换的应用中很有用。请参见用户手册中的第38节,高速模拟比较器(ACMPHS)。
低功耗模拟比较器(ACMPLP)	低功耗模拟比较器(ACMPLP)将参考电压与模拟输入电压进行比较。比较结果可以通过软件读取,也可以对外输出。参考电压可以从CMPREFi(i=0,1)引脚的输入、内部8位DA转换器输出或MCU内部生成的内部参考电压(Vref)中选择。可以在开始操作之前设置ACMPLP响应速度。设置高速模式会减少响应延迟时间,但会增加电流消耗。设置低速模式会增加响应延迟时间,但会降低电流消耗。请参阅用户手册中的第39节,低功耗模拟比较器(ACMPLP)。

Table 1.8 Analog (2 of 2)

Feature	Functional description
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A total of three differential operational amplifier units with two input pins and one output pin are provided. All units have switches that can select input signals. Additionally, operational amplifier 0 has a switch that can select the output pin. See section 37, Operational Amplifier (OPAMP) in User's Manual.

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSUS)	The Capacitive Touch Sensing Unit (CTSUS) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSUS to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 40, Capacitive Touch Sensing Unit (CTSUS) in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 31, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 41, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
AES	See section 44, AES Engine in User's Manual.
True Random Number Generator (TRNG)	See section 45, True Random Number Generator (TRNG) in User's Manual.

Table 1.8 模拟 (2个中的2个)

Feature	功能说明
运算放大器(OPAMP)	运算放大器(OPAMP)可用于放大小的模拟输入电压并输出放大后的电压。总共提供了三个差分运算放大器单元,具有两个输入引脚和一个输出引脚。所有单元都有可以选择输入信号的开关。此外,运算放大器0有一个可以选择输出引脚的开关。请参阅用户手册中的第37节运算放大器(OPAMP)。

Table 1.9 人机界面

Feature	功能说明
电容式触控感应单元(CTSUS)	电容式触摸传感单元(CTSUS)测量触摸传感器的静电电容。静电电容的变化由软件确定,使CTSUS能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围,因此手指不会直接接触电极。请参阅用户手册中的第40节,电容式触摸感应单元(CTSUS)。

Table 1.10 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外,还可以使用各种生成CRC的多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用,例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅用户手册中的第31节,循环冗余校验(CRC)计算器。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。见第41节,用户手册中的数据操作电路(DOC)。

Table 1.11 Security

Feature	功能说明
AES	请参阅用户手册中的第44节,AES引擎。
真随机数生成器(TRNG)	请参阅用户手册中的第45节,真随机数生成器(TRNG)。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

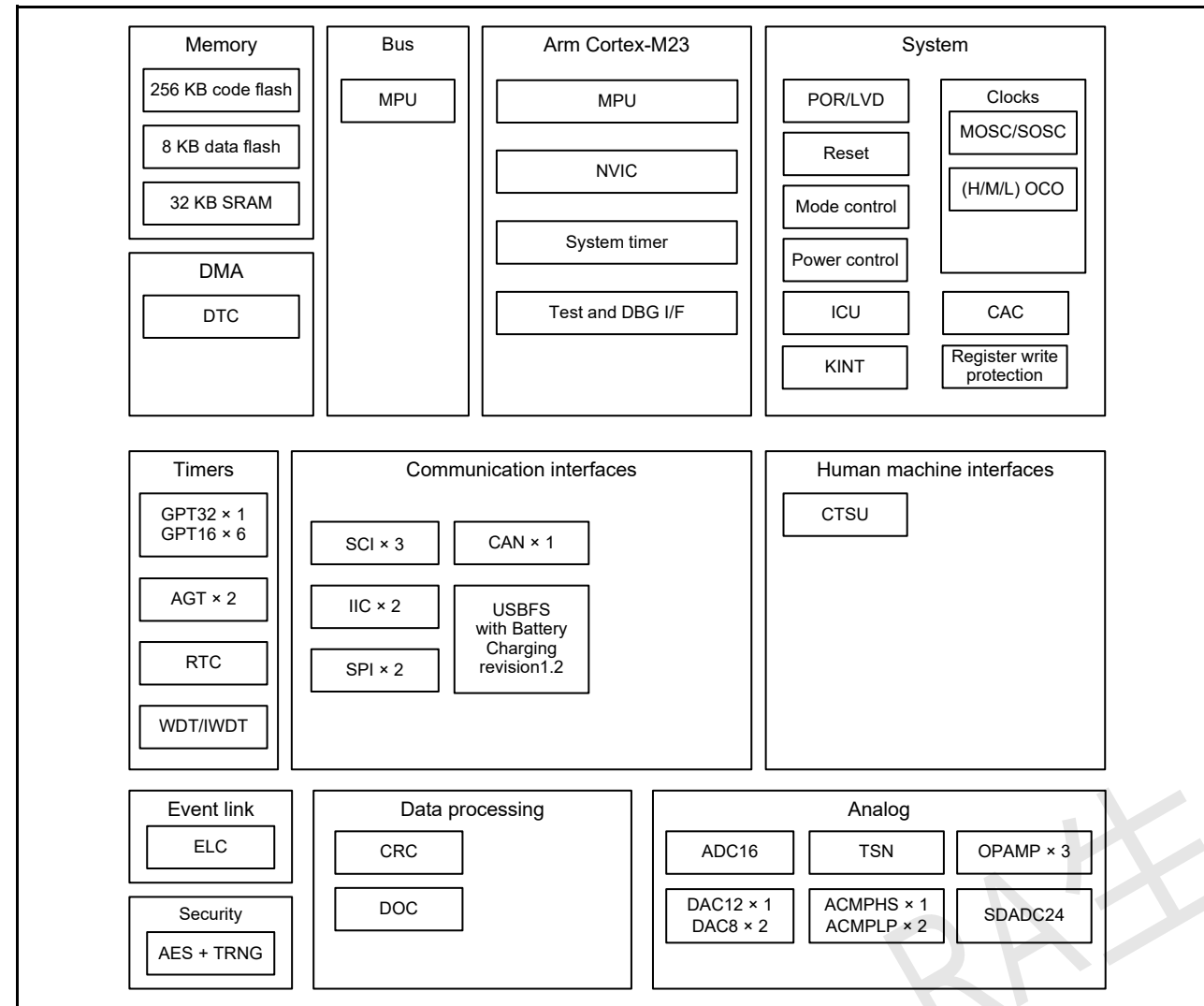


Figure 1.1 Block diagram

1.2 框图

图1.1显示了MCU超集的框图，该组中的一些单独的设备具有功能的子集。

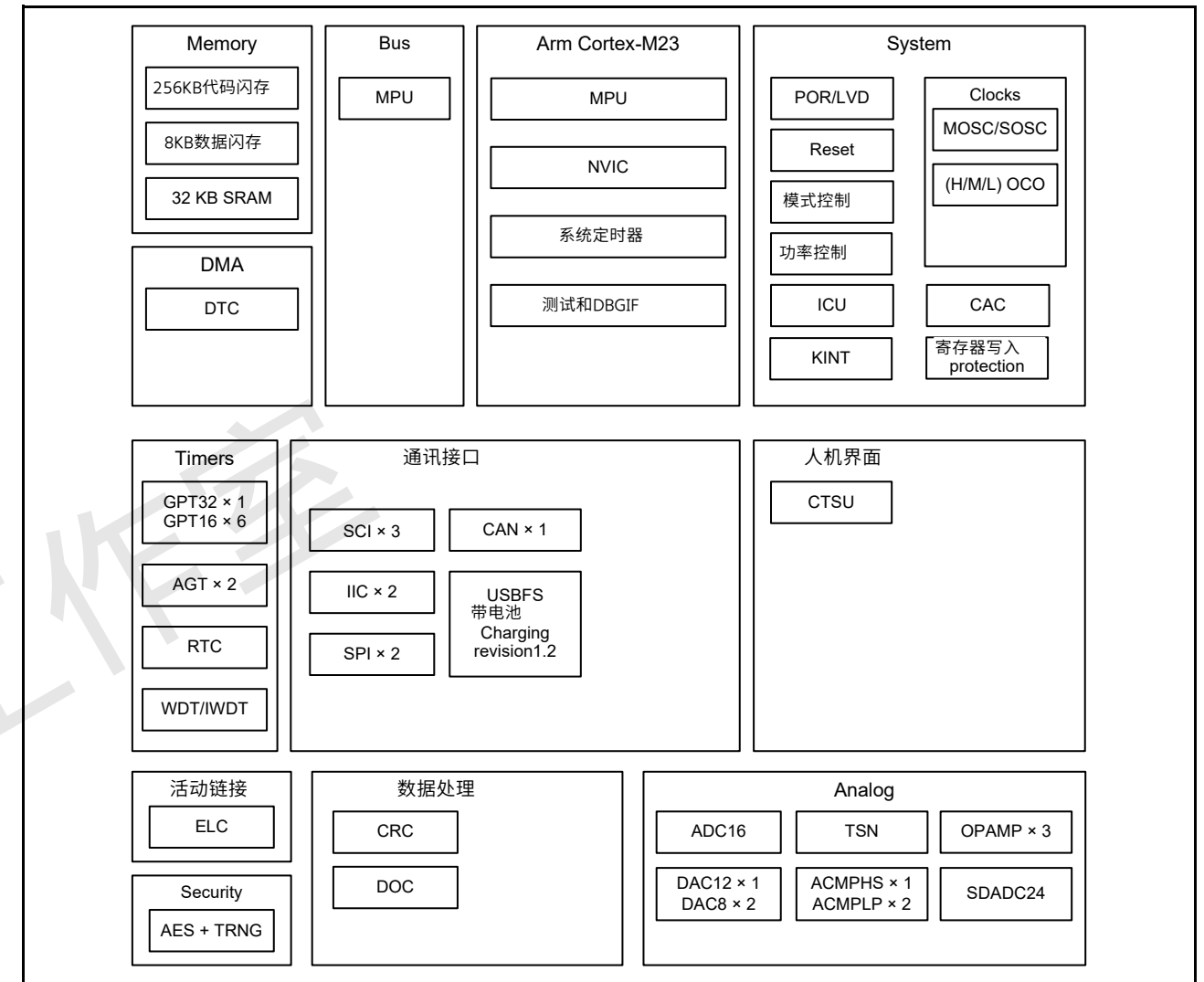


Figure 1.1 框图



### 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

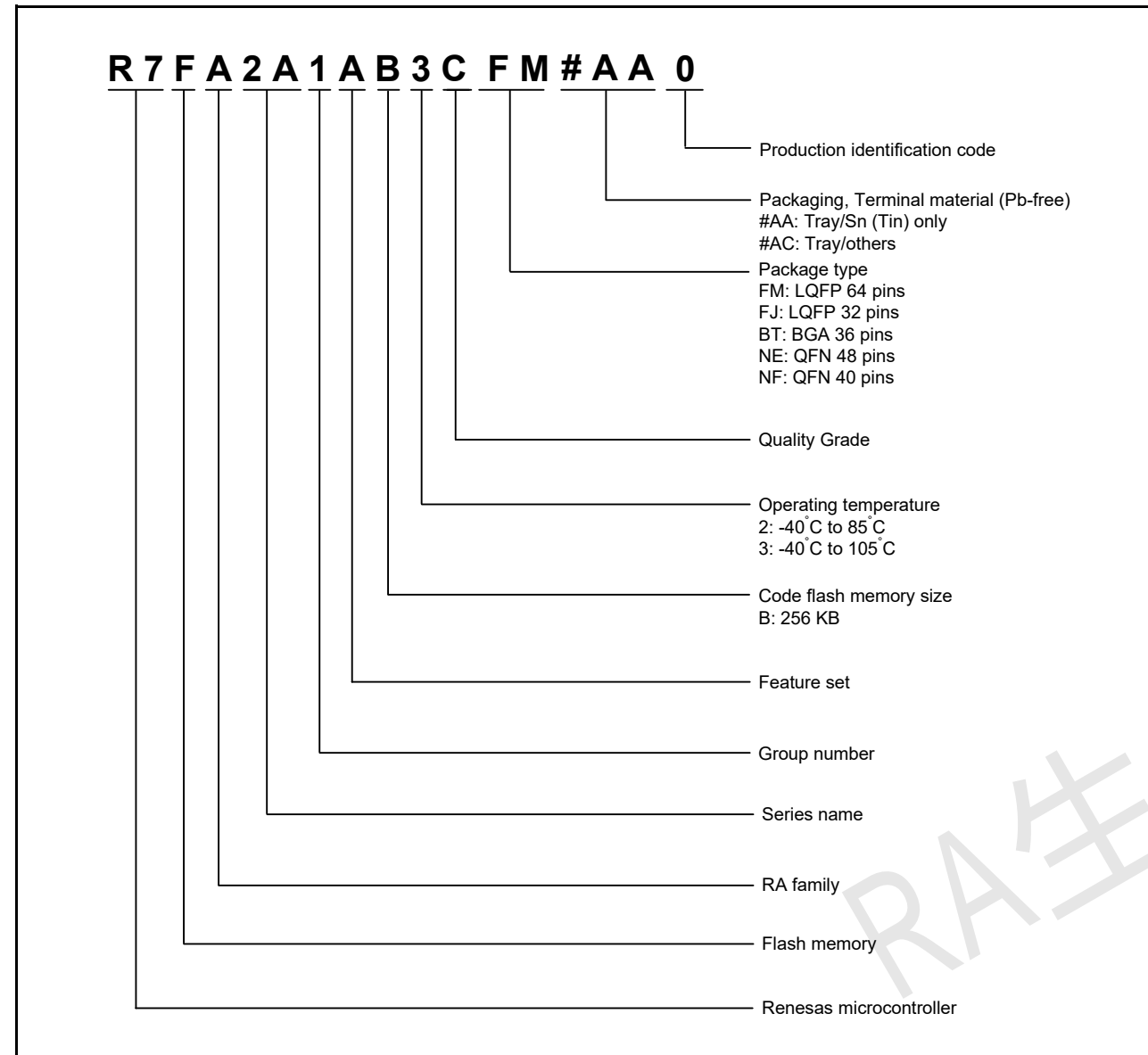


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2A1AB3CFM	R7FA2A1AB3CFM#AA0	PLQP0064KB-C	256 KB	8 KB	32 KB	-40 to +105°C
R7FA2A1AB3CNE	R7FA2A1AB3CNE#AC0	PWQN0048KB-A				-40 to +105°C
R7FA2A1AB3CNF	R7FA2A1AB3CNF#AC0	PWQN0040KC-A				-40 to +105°C
R7FA2A1AB2CBT	R7FA2A1AB2CBT#AC0	PLBG0036GA-A				-40 to +85°C
R7FA2A1AB3CFJ	R7FA2A1AB3CFJ#AA0	PLQP0032GB-A				-40 to +105°C

### 1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.12显示了产品列表。

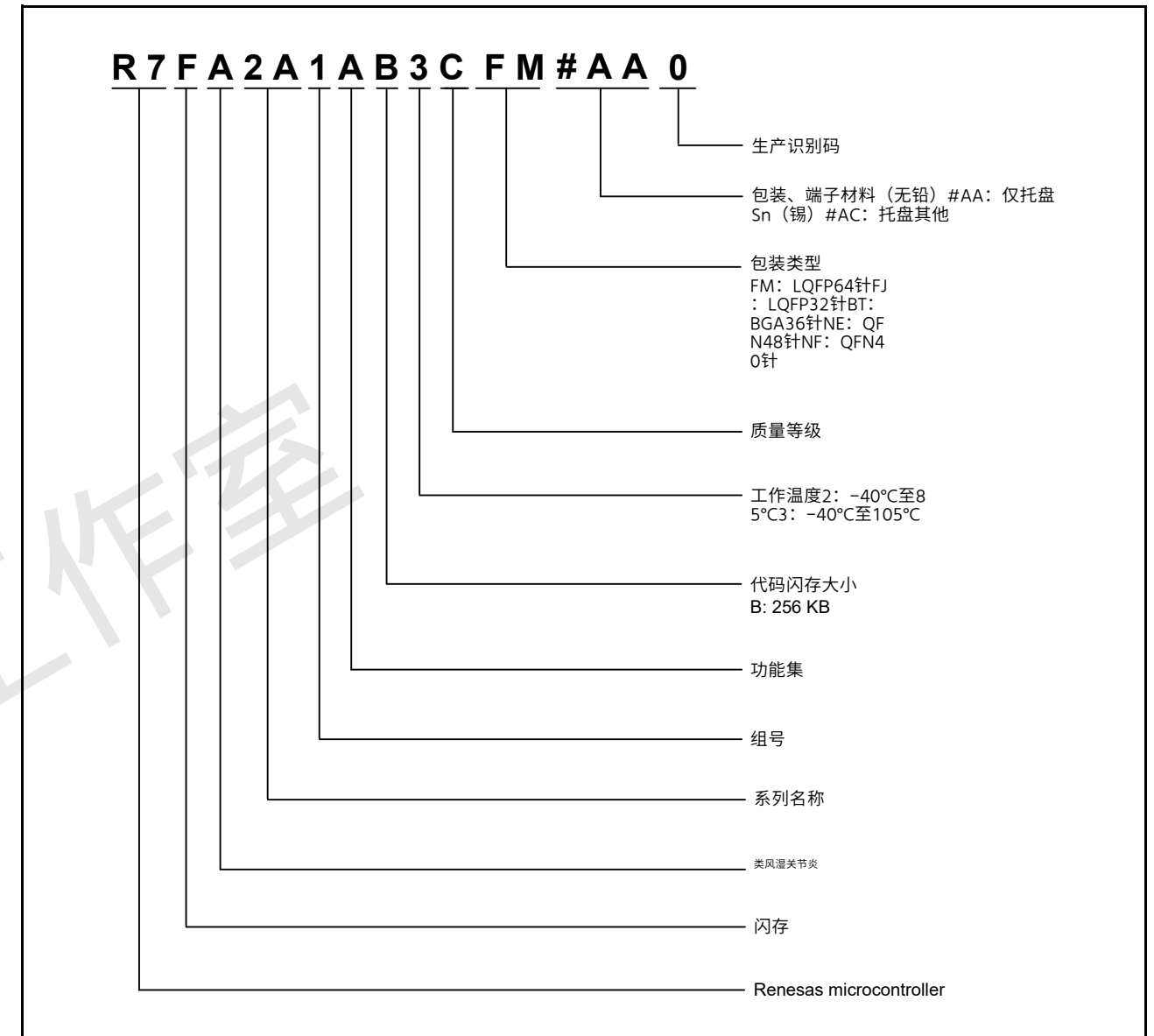


Figure 1.2 零件编号方案

Table 1.12 产品列表

产品部件号	可订购部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA2A1AB3CFM	R7FA2A1AB3CFM#AA0	PLQP0064KB-C	256 KB	8 KB	32 KB	-40 to +105°C
R7FA2A1AB3CNE	R7FA2A1AB3CNE#AC0	PWQN0048KB-A				-40 to +105°C
R7FA2A1AB3CNF	R7FA2A1AB3CNF#AC0	PWQN0040KC-A				-40 to +105°C
R7FA2A1AB2CBT	R7FA2A1AB2CBT#AC0	PLBG0036GA-A				-40 to +85°C
R7FA2A1AB3CFJ	R7FA2A1AB3CFJ#AA0	PLQP0032GB-A				-40 to +105°C

## 1.4 Function Comparison

Table 1.13 Function comparison

Part numbers	R7FA2A1AB3CFM	R7FA2A1AB3CNE	R7FA2A1AB3CNF	R7FA2A1AB2CBT	R7FA2A1AB3CFJ	
Pin count	64	48	40	36	32	
Package	LQFP	QFN	QFN	BGA	LQFP	
Code flash memory	256 KB					
Data flash memory	8 KB					
SRAM	32 KB					
	Parity	16 KB				
	ECC	16 KB				
System	CPU clock	48 MHz				
	Sub-clock oscillator	Yes			No	
	ICU	Yes				
	KINT	8	6	4	4	3
Event control	ELC	Yes				
DMA	DTC	Yes				
Timers	GPT32	1				
	GPT16	6	6	4	3	4
	AGT	2				
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	3				
	IIC	2				
	SPI	2		1	2	
	CAN	Yes				
	USBFS	Yes			No	
Analog	ADC16	17 (4*1)	12 (3*1)	8 (1*1)	5 (1*1)	5 (1*1)
	SDADC24	8 (4*1)	6 (3*1)	4 (2*1)	2 (1*1)	2 (1*1)
	DAC12	1				
	DAC8	2	2*2	2*3		
	ACMPHS	1				
	ACMPLP	2				
	OPAMP	3	2	1	1	1
	TSN	Yes				
HMI	CTSU	26	16	11	9	11
Data processing	CRC	Yes				
	DOC	Yes				
Security	AES and TRNG					

Note 1. The number of channels of the differential analog input.

Note 2. Pin output function of DA8\_1 cannot be used.

Note 3. Pin output function of DA8\_0 and DA8\_1 cannot be used.

## 1.4 功能比较

Table 1.13 功能对比

零件号	R7FA2A1AB3CFM	R7FA2A1AB3CNE	R7FA2A1AB3CNF	R7FA2A1AB2CBT	R7FA2A1AB3CFJ	
针数	64	48	40	36	32	
Package	LQFP	QFN	QFN	BGA	LQFP	
代码闪存	256 KB					
数据闪存	8 KB					
SRAM	32 KB					
	Parity	16 KB				
	ECC	16 KB				
System	中央处理器时钟	48 MHz				
	Sub-clock oscillator	Yes			No	
	ICU	Yes				
	KINT	8	6	4	4	3
事件控制	ELC	Yes				
DMA	DTC	Yes				
Timers	GPT32	1				
	GPT16	6	6	4	3	4
	AGT	2				
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	3				
	IIC	2				
	SPI	2		1	2	
	CAN	Yes				
	USBFS	Yes			No	
Analog	ADC16	17 (4*1)	12 (3*1)	8 (1*1)	5 (1*1)	5 (1*1)
	SDADC24	8 (4*1)	6 (3*1)	4 (2*1)	2 (1*1)	2 (1*1)
	DAC12	1				
	DAC8	2	2*2	2*3		
	ACMPHS	1				
	ACMPLP	2				
	OPAMP	3	2	1	1	1
	TSN	Yes				
HMI	CTSU	26	16	11	9	11
数据处理	CRC	Yes				
	DOC	Yes				
Security	AES and TRNG					

注1.差分模拟输入的通道数。

注2.DA8\_1的引脚输出功能不能使用。

注3.DA8\_0和DA8\_1的引脚输出功能不能使用。

## 1.5 Pin Functions

Table 1.14 Pin functions (1 of 4)

Function	Signal	I/O	Description	
Power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect it to VSS by a 0.1- $\mu$ F capacitor. Place the capacitor close to the pin.	
	VCL	I/O	Connect this pin to VSS through a smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).	
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.	
	EXTAL	Input		
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.	
	XCOUT	Output		
	CLKOUT	Output		Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.	
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.	
CAC	CACREF	Input	Measurement reference clock input pin	
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin	
	SWCLK	Input	Serial wire clock pin	
Interrupt	NMI	Input	Non-maskable interrupt request pin	
	IRQ0 to IRQ7	Input	Maskable interrupt request pins	
GPT	GTETRGA, GTETRGB	Input	External trigger input pin	
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, output compare, or PWM output pin	
	GTIU	Input	Hall sensor input pin U	
	GTIV	Input	Hall sensor input pin V	
	GTIW	Input	Hall sensor input pin W	
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)	
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)	
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)	
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)	
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)	
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)	
	AGT	AGTEE0, AGTEE1	Input	External event input enable
		AGTIO0, AGTIO1	I/O	External event input and pulse output
AGTO0, AGTO1		Output	Pulse output	
AGTOA0, AGTOA1		Output	Output compare match A output	
AGTOB0, AGTOB1		Output	Output compare match B output	
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock	

## 1.5 引脚功能

Table 1.14 引脚功能(1of4)

Function	Signal	I/O	Description	
电源	VCC	Input	电源引脚。将此引脚连接到系统电源。通过一个0.1 $\mu$ F电容将其连接到VSS。将电容器靠近引脚放置。	
	VCL	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS。将电容器靠近引脚放置。	
	VSS	Input	接地引脚。连接到系统电源(0V)。	
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。	
	EXTAL	Input		
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。	
	XCOUT	Output		
	CLKOUT	Output		时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。	
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。	
CAC	CACREF	Input	测量参考时钟输入引脚	
On-chip debug	SWDIO	I/O	串行线调试数据输入输出引脚	
	SWCLK	Input	串行线时钟引脚	
Interrupt	NMI	Input	不可屏蔽中断请求引脚	
	IRQ0 to IRQ7	Input	可屏蔽中断请求引脚	
GPT	GTETRGA, GTETRGB	Input	外部触发输入引脚	
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	输入捕捉、输出比较或PWM输出引脚	
	GTIU	Input	霍尔传感器输入引脚U	
	GTIV	Input	霍尔传感器输入引脚V	
	GTIW	Input	霍尔传感器输入引脚W	
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出 (正U相)	
	GTOULO	Output	用于BLDC电机控制的3相PWM输出 (负U相)	
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出 (正V相)	
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出 (负V相)	
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出 (正W相)	
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出 (负W相)	
	AGT	AGTEE0, AGTEE1	Input	外部事件输入使能
		AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出
AGTO0, AGTO1		Output	脉冲输出	
AGTOA0, AGTOA1		Output	输出比较匹配A输出	
AGTOB0, AGTOB1		Output	输出比较匹配B输出	
RTC	RTCOUT	Output	1Hz/64Hz时钟的输出引脚	

Table 1.14 Pin functions (2 of 4)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.

Table 1.14 引脚功能(2of4)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	时钟输入输出引脚 (时钟同步模式)
	RXD0, RXD1, RXD9	Input	接收数据的输入引脚 (异步模式时钟同步模式)
	TXD0, TXD1, TXD9	Output	传输数据的输出引脚 (异步模式时钟同步模式)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	输入输出引脚用于控制发送和接收的开始 (异步模式时钟同步模式), 低电平有效
	SCL0, SCL1, SCL9	I/O	IIC时钟的输入输出引脚 (简单IIC)
	SDA0, SDA1, SDA9	I/O	IIC数据的输入输出引脚 (简单IIC)
	SCK0, SCK1, SCK9	I/O	时钟的输入输出引脚 (简单SPI)
	MISO0, MISO1, MISO9	I/O	用于从机传输数据的输入输出引脚 (简单SPI)
	MOSI0, MOSI1, MOSI9	I/O	用于数据主传输的输入输出引脚 (简单SPI)
	SS0, SS1, SS9	Input	片选输入引脚 (简单SPI), 低电平有效
IIC	SCL0, SCL1	I/O	时钟输入输出引脚
	SDA0, SDA1	I/O	数据输入输出引脚
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	输入或输出从主机输出的数据
	MISOA, MISOB	I/O	从机输入或输出数据输出
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚
CAN	CRX0	Input	接收数据
	CTX0	Output	传输数据
USBFS	VSS_USB	Input	接地引脚
	VCC_USB_LDO	Input	USB LDO稳压器的电源引脚
	VCC_USB	I/O	输入: USB收发器的电源引脚。输出: USB LDO稳压器输出引脚。该引脚应连接到外部电容器。
	USB_DP	I/O	USB片上收发器的D+IO引脚。该引脚应连接到USB总线的D+引脚。
	USB_DM	I/O	USB片上收发器的DIO引脚。该引脚应连接到USB总线的Dpin。
	USB_VBUS	Input	USB电缆连接监视器引脚。该引脚应连接到USB总线的VBUS。当USB模块作为设备控制器运行时, 可以检测到VBUS引脚状态 (连接或断开)。



Table 1.14 Pin functions (3 of 4)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the ADC16, DAC12, DAC8, ACMPHS, ACMPLP, and OPAMP
	AVSS0	Input	Analog ground pin for the ADC16, DAC12, DAC8, ACMPHS, ACMPLP, and OPAMP
	AVCC1	Input	Analog voltage supply pin for the SDADC24
	AVSS1	Input	Analog ground pin for the SDADC24
	VREFH0	Input	Analog reference voltage supply pin for the ADC16. Connect this pin to AVCC0 when not using the ADC16.
	VREFL0	Input	Analog reference ground pin for the ADC16. Connect this pin to AVSS0 when not using the ADC16.
	VREFH	Input	Analog reference voltage supply pin for the DAC12
	VREFL	Input	Analog reference ground pin for the DAC12
ADC16	AN000 to AN008, AN016 to AN023	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
SDADC24	ANS0P to ANSD3P	Input	Input pins for the analog signals to be processed by the SDADC24
	ANS0N to ANSD3N	Input	Input pins for the analog signals to be processed by the SDADC24
	ADREG	Output	Regulator capacitance for the SDADC24
	SBIAS	Output	Sensor power supply
	VREFI	Input	External reference voltage supply pin for the SDADC24
DAC12	DA12_0	Output	Output pin for the analog signals to be processed by the 12-bit D/A converter
DAC8	DA8_0, DA8_1	Output	Output pins for the analog signals to be processed by the 8-bit D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPHS	IVREF0 to IVREF2	Input	Reference voltage input pin
	IVCMP0 to IVCMP2	Input	Analog voltage input pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP2+	Input	Analog voltage input pins
	AMP0- to AMP2-	Input	Analog voltage input pins
	AMP0O to AMP2O	Output	Analog voltage output pins
CTSU	TS00 to TS25	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins

Table 1.14 引脚功能(3of4)

Function	Signal	I/O	Description
模拟电源	AVCC0	Input	ADC16、DAC12、DAC8、ACMPHS、ACMPLP, and OPAMP
	AVSS0	Input	ADC16、DAC12、DAC8、ACMPHS、ACMPLP和OPAMP的模拟接地引脚
	AVCC1	Input	SDADC24的模拟电压电源引脚
	AVSS1	Input	SDADC24的模拟接地引脚
	VREFH0	Input	ADC16的模拟参考电压电源引脚。将此引脚连接到不使用ADC16时的AVCC0。
	VREFL0	Input	ADC16的模拟参考接地引脚。不使用ADC16时, 将此引脚连接到AVSS0。
	VREFH	Input	DAC12的模拟参考电压电源引脚
	VREFL	Input	DAC12的模拟参考接地引脚
ADC16	AN000 to AN008, AN016 to AN023	Input	AD转换器要处理的模拟信号的输入引脚
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚, 低电平有效
SDADC24	ANS0P to ANSD3P	Input	SDADC24处理的模拟信号的输入引脚
	ANS0N to ANSD3N	Input	SDADC24处理的模拟信号的输入引脚
	ADREG	Output	SDADC24的稳压器电容
	SBIAS	Output	传感器电源
	VREFI	Input	SDADC24的外部参考电压电源引脚
DAC12	DA12_0	Output	由12位DA转换器处理的模拟信号的输出引脚
DAC8	DA8_0, DA8_1	Output	由8位DA转换器处理的模拟信号的输出引脚
比较器输出	VCOUT	Output	比较器输出引脚
ACMPHS	IVREF0 to IVREF2	Input	参考电压输入引脚
	IVCMP0 to IVCMP2	Input	模拟电压输入引脚
ACMPLP	CMPREF0, CMPREF1	Input	参考电压输入引脚
	CMPIN0, CMPIN1	Input	模拟电压输入引脚
OPAMP	AMP0+ to AMP2+	Input	模拟电压输入引脚
	AMP0- to AMP2-	Input	模拟电压输入引脚
	AMP0O to AMP2O	Output	模拟电压输出引脚
CTSU	TS00 to TS25	Input	电容式触摸检测引脚 (触摸引脚)
	TSCAP	-	触摸驱动器的辅助电源引脚
KINT	KR00 to KR07	Input	按键中断输入引脚

Table 1.14 Pin functions (4 of 4)

Function	Signal	I/O	Description
I/O ports	P000 to P003, P012 to P015	I/O	General-purpose input/output pins
	P100 to P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments.

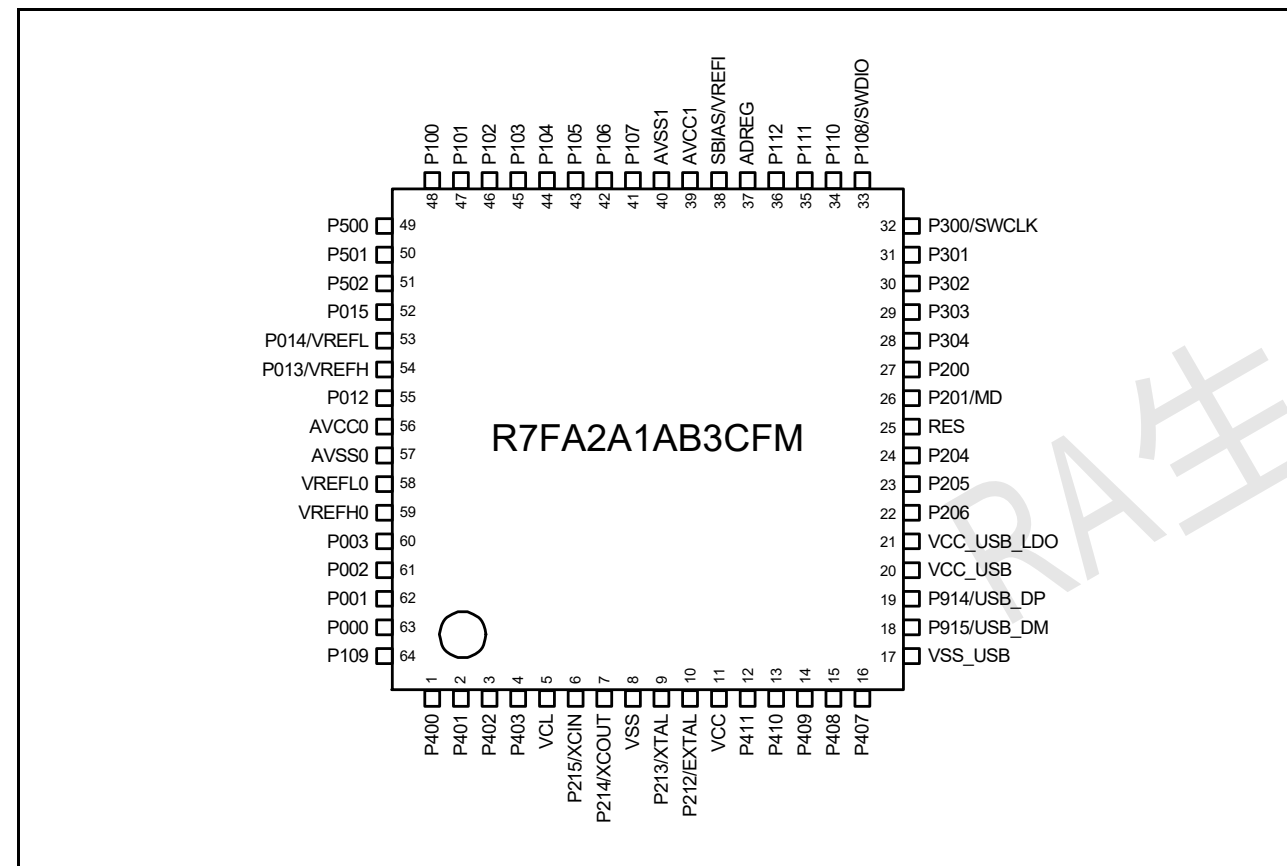


Figure 1.3 Pin assignment for LQFP 64-pin

Table 1.14 引脚功能 (4个, 共4个)

Function	Signal	I/O	Description
I/O ports	P000 to P003, P012 to P015	I/O	General-purpose input/output pins
	P100 to P112	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	通用输入引脚
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 引脚分配

图1.3至图1.7显示了引脚分配。

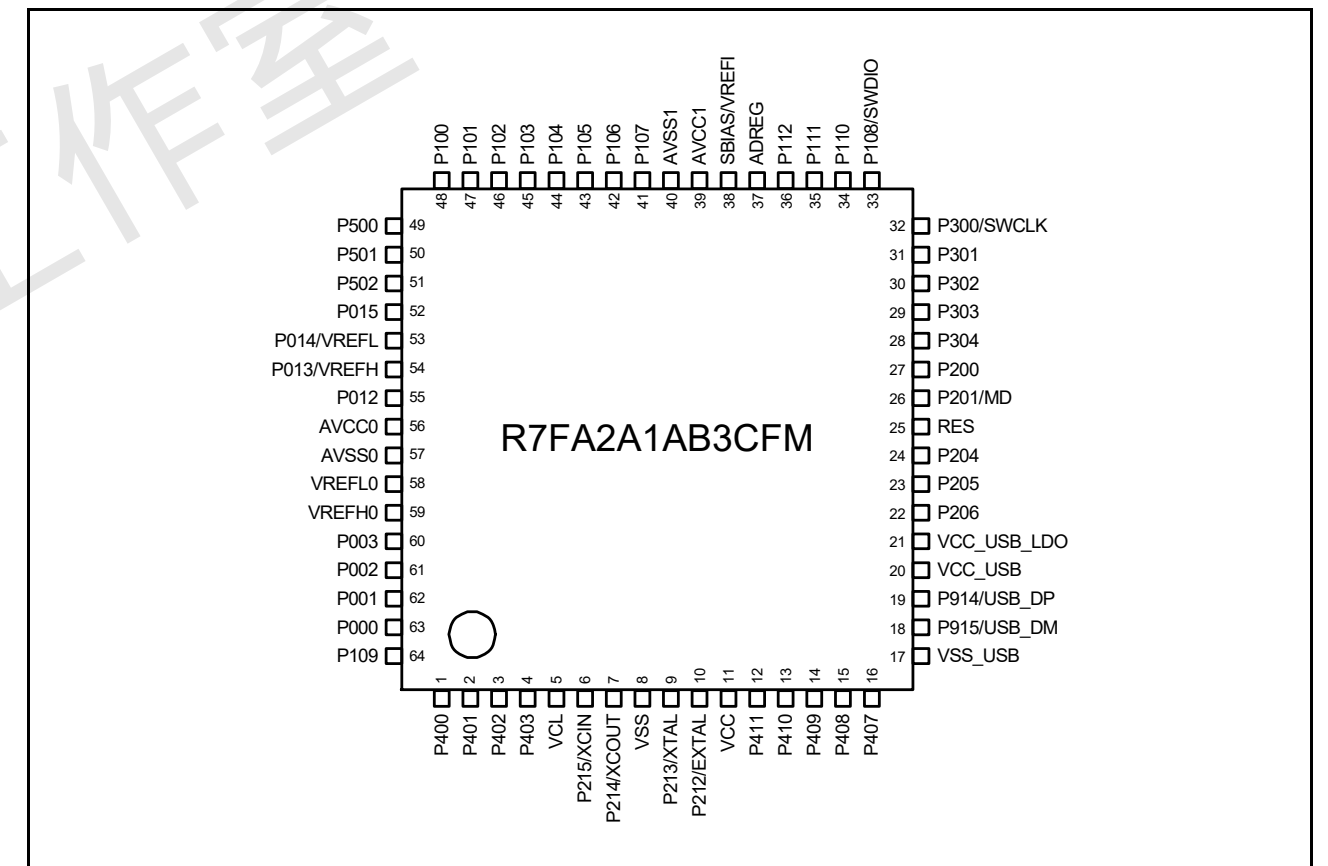


Figure 1.3 LQFP64引脚的引脚分配

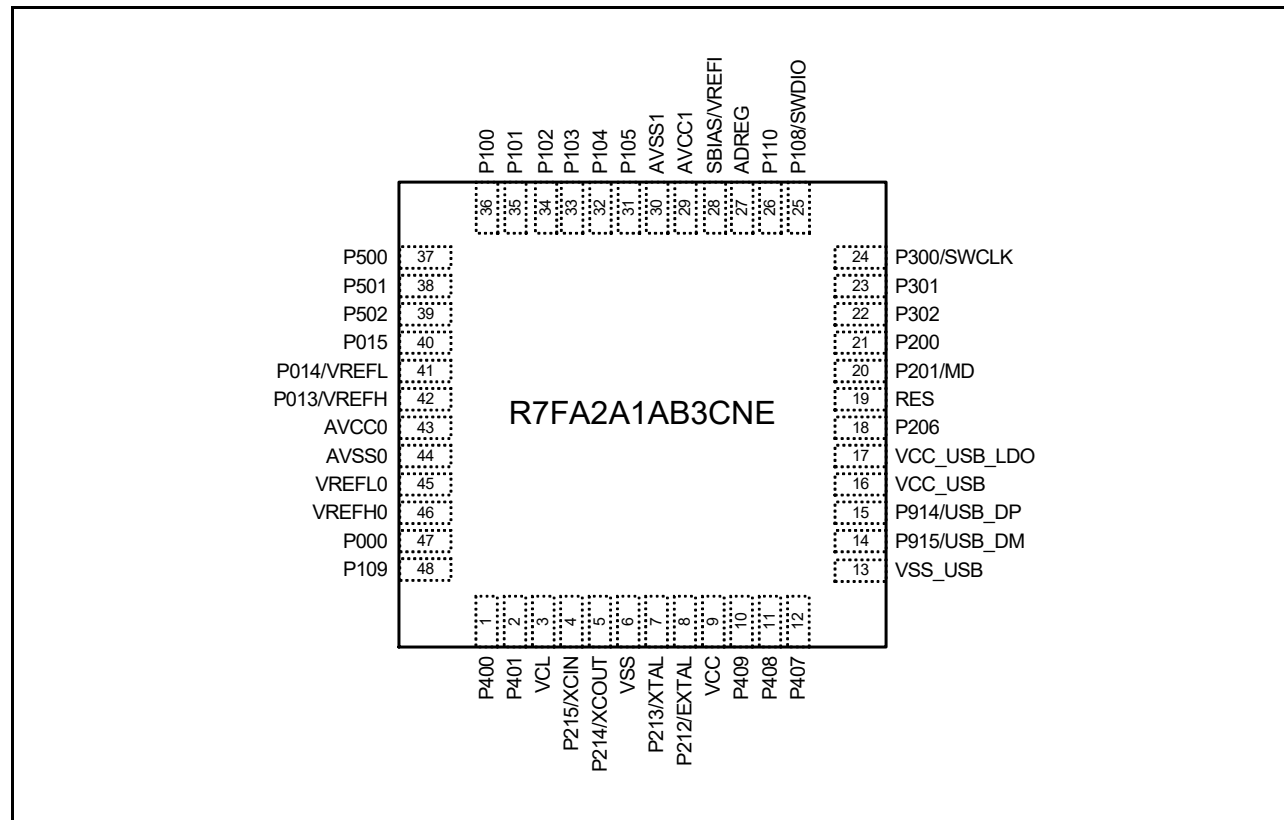


Figure 1.4 Pin assignment for QFN 48-pin

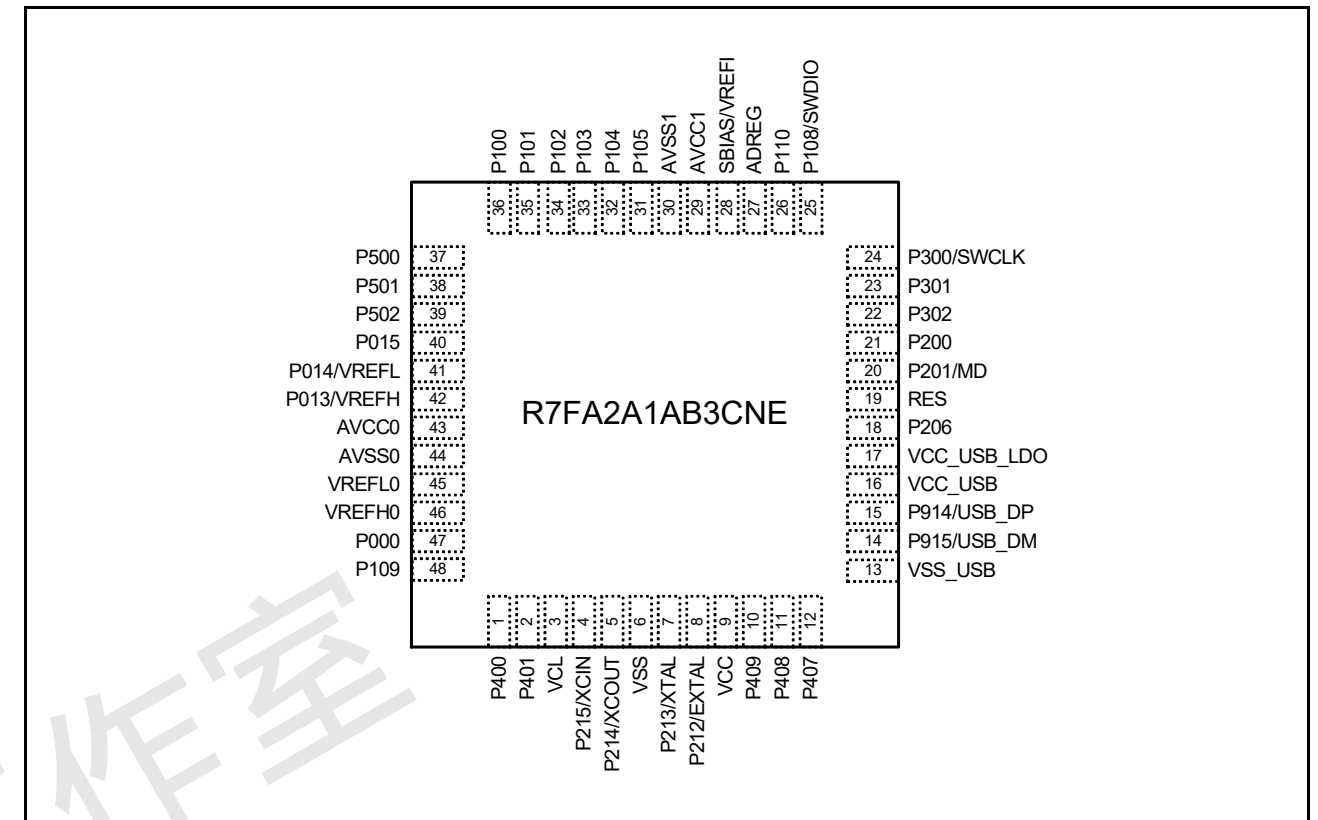


Figure 1.4 QFN48引脚的引脚分配

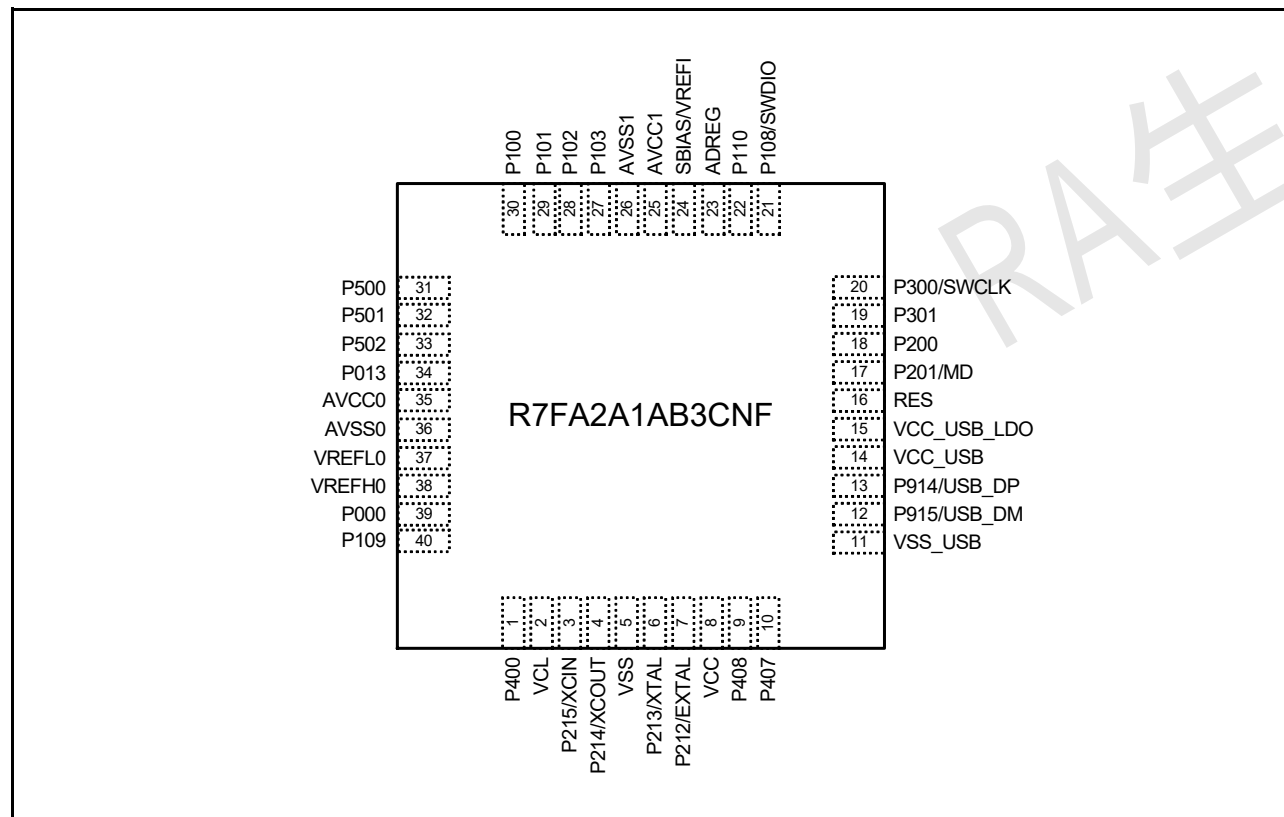


Figure 1.5 Pin assignment for QFN 40-pin

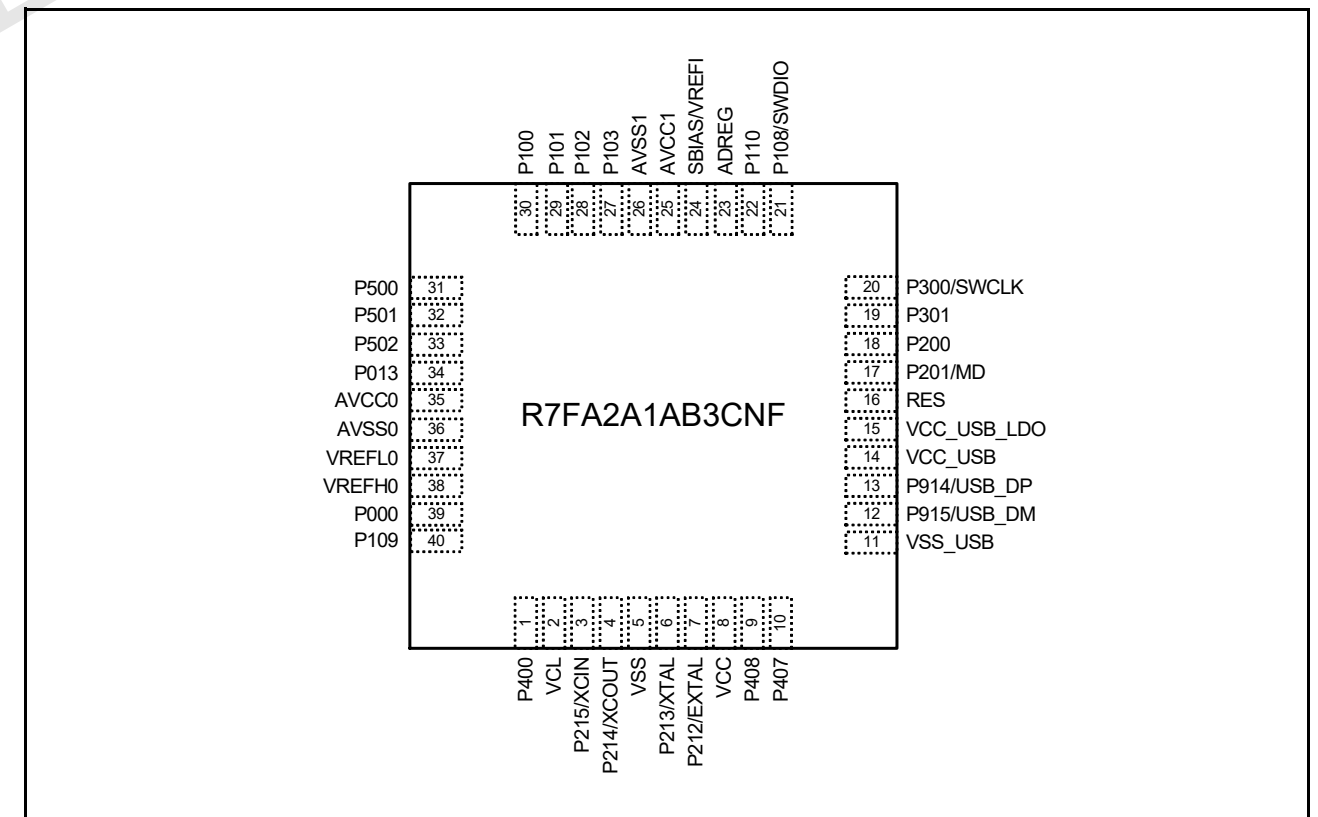


Figure 1.5 QFN40引脚的引脚分配

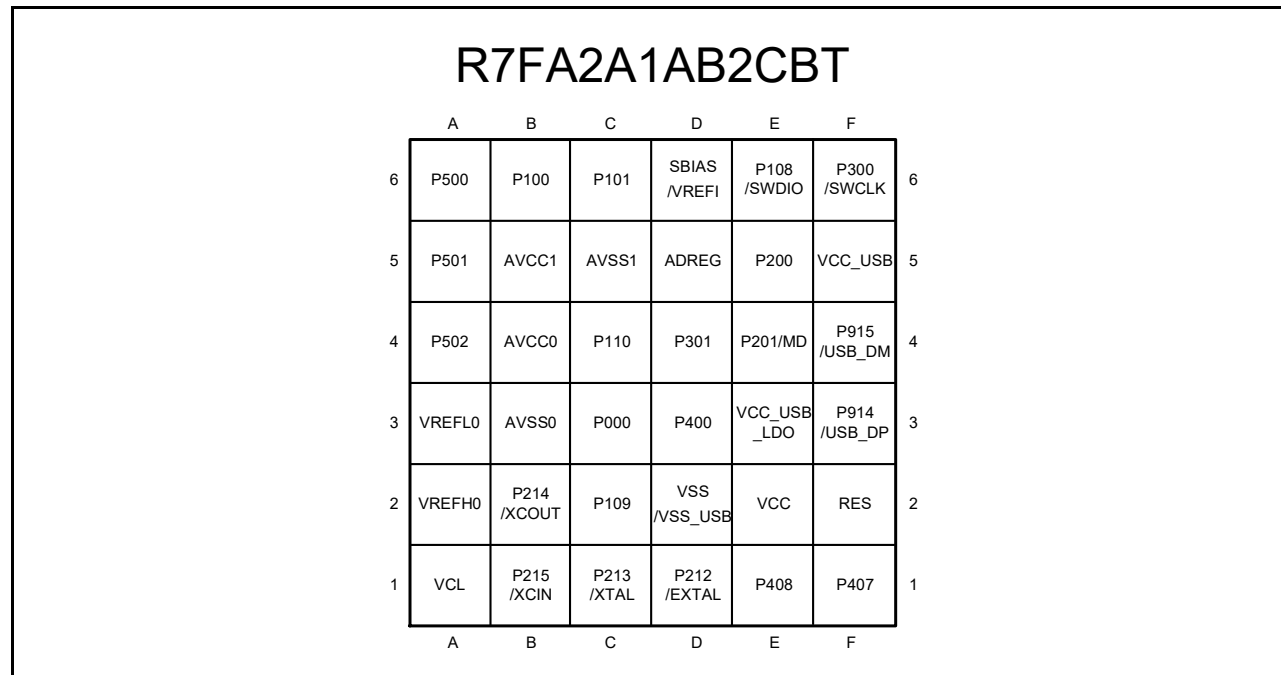


Figure 1.6 Pin assignment for BGA 36-pin (top view, pad side down)

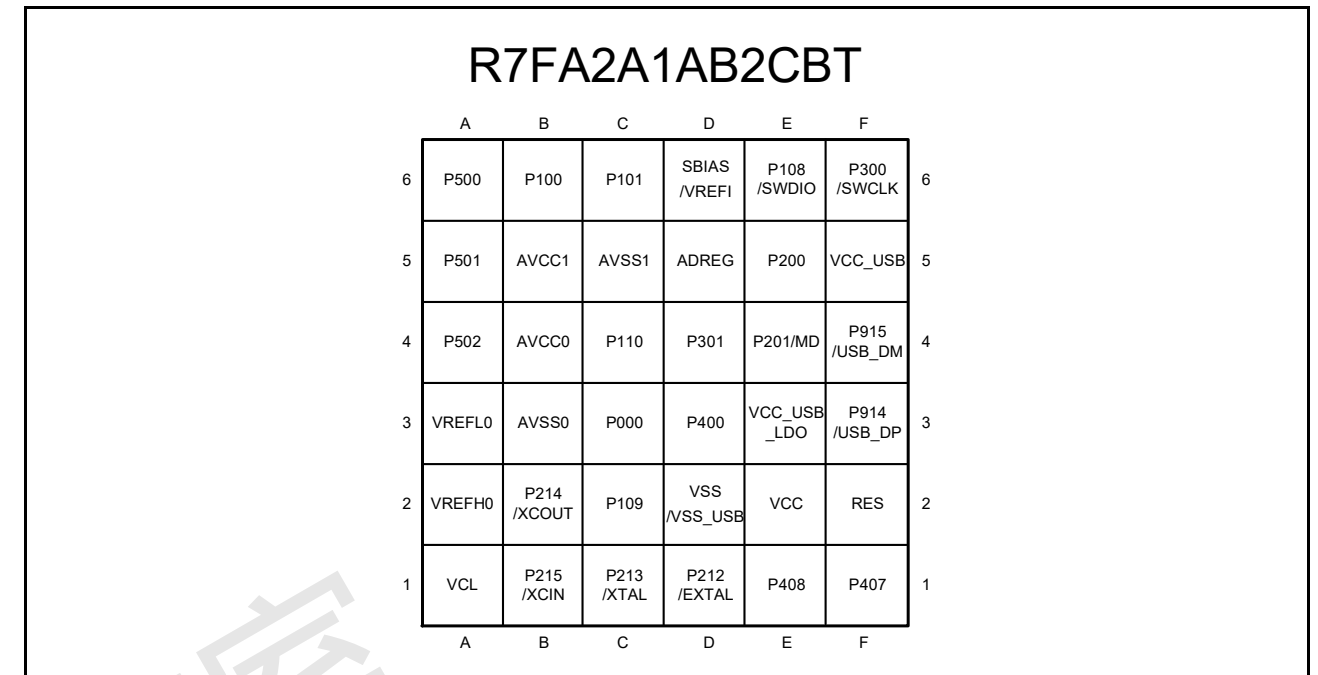


Figure 1.6 BGA36引脚的引脚分配 (俯视图, 焊盘面朝下)

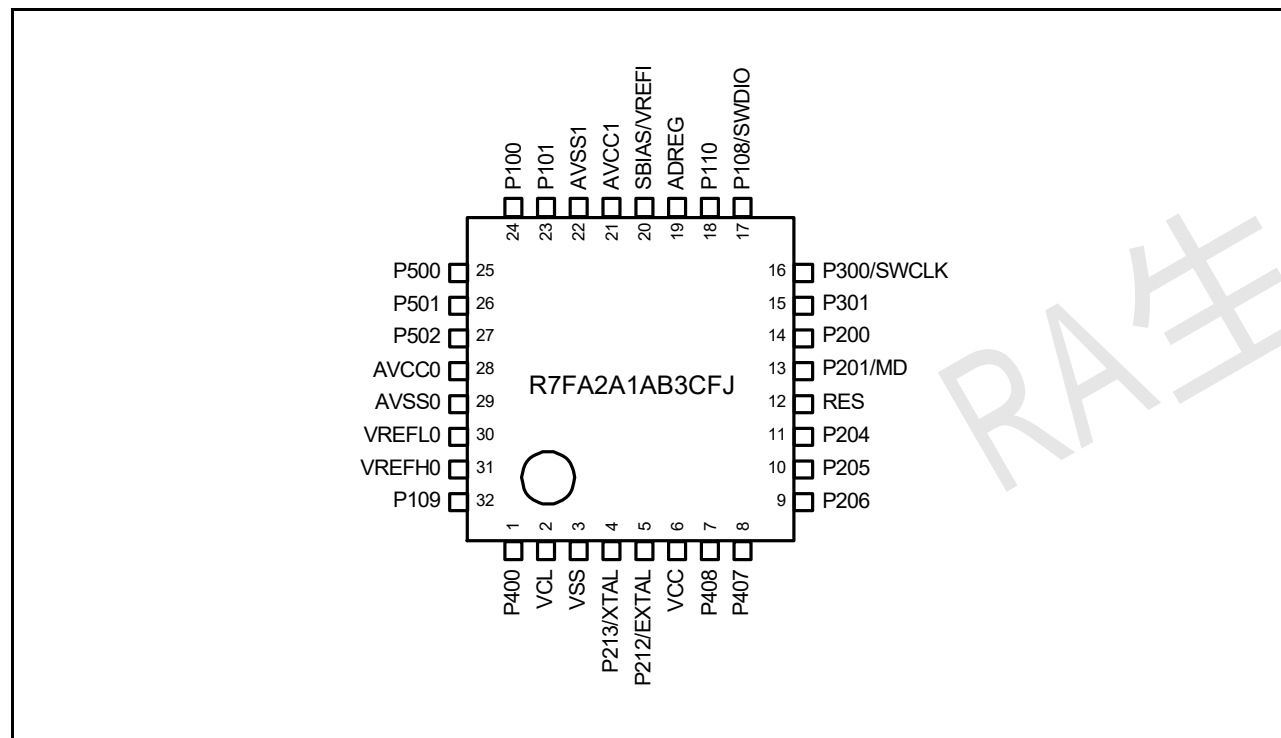


Figure 1.7 Pin assignment for LQFP 32-pin

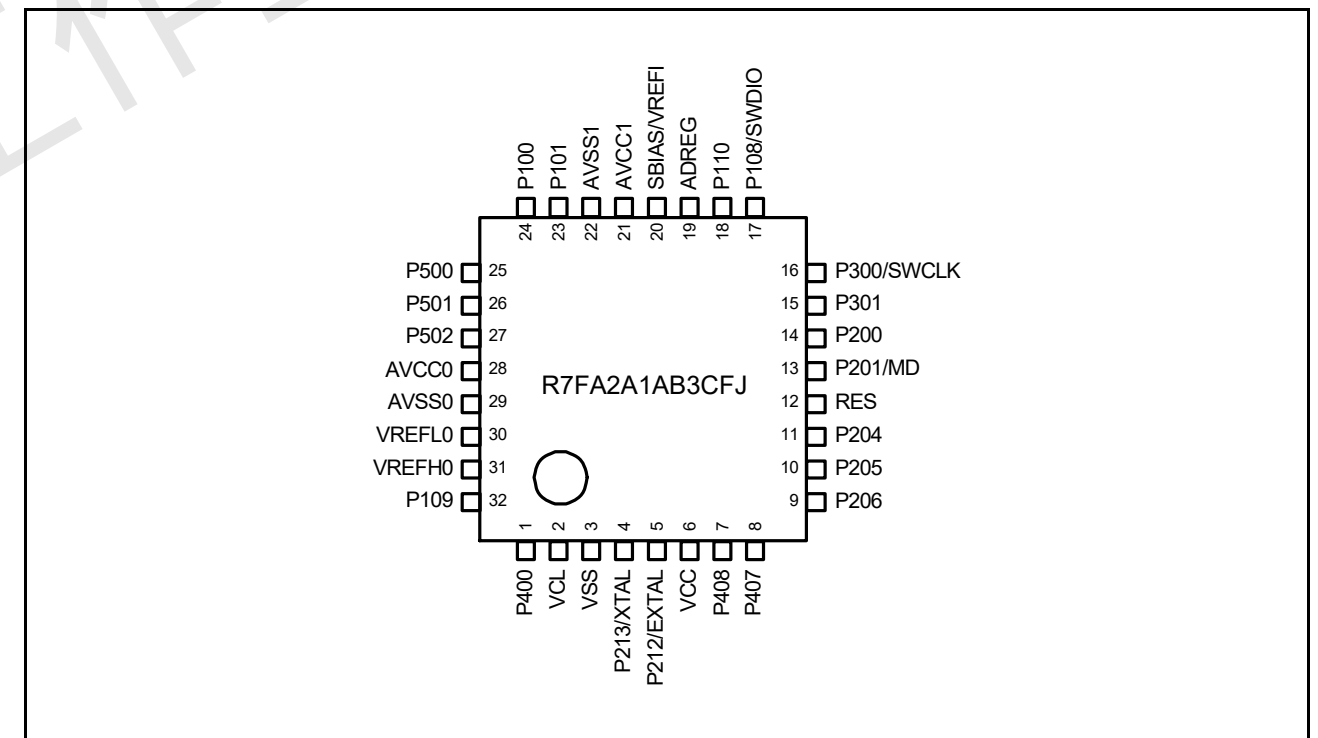


Figure 1.7 LQFP32引脚的引脚分配



1.7 Pin Lists

Pin number				Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analog				HMI	
LQFP64	QFN48	QFN40	BGA36			AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU
1	1	1	D3	1	P400	AGTEE0_A	GTETRGA_A	GTIOC1A_A	RTCCOUT_C									TS00	KR02/IRQ0_A
2	2	-	-	-	P401	AGTEE1_A	GTIU_A	GTIOC4A_A										TS01	KR03/IRQ5_B
3	-	-	-	-	P402		GTIV_A	GTIOC0A_D										TS02	
4	-	-	-	-	P403		GTIW_A	GTIOC0B_C										TS03	
5	3	2	A1	2	VCL														
6	4	3	B1	-	XCIN	P215													
7	5	4	B2	-	XCOUT	P214													
8	6	5	D2	3	VSS														
9	7	6	C1	4	XTAL	P213	AGTEE1_B	GTETRGA_B	GTIOC0A_B										IRQ2_B
10	8	7	D1	5	EXTAL	P212	AGTIO0_A	GTETRGA_B	GTIOC0B_B										IRQ3_B
11	9	8	E2	6	VCC														
12	-	-	-	-	P411			GTIOC5A_A											TS04
13	-	-	-	-	P410			GTIOC5B_A											TS05
14	10	-	-	-	P409	AGTO1_A		GTIOC0A_C											TSCAP_E/IRQ7_A
15	11	9	E1	7		P408	AGTO0_A	GTOUUP_A	GTIOC0A_A										TS06/IRQ1_A
16	12	10	F1	8	CACREF_B	P407	AGTIO0_C	GTOULO_A	GTIOC0B_A										TSCAP_D/IRQ1_B
17	13	11	D2	-	VSS_USB														
18	14	12	F4	-		P915													USB_DM
19	15	13	F3	-		P914													USB_DP
20	16	14	F5	-	VCC_USB														
21	17	15	E3	-	VCC_USB_LDO														
22	18	-	-	9		P206	AGTIO0_B	GTOVUP_A	GTIOC3A_A										TS07/IRQ6_A
23	-	-	-	10		P205		GTOVL_O_A	GTIOC3B_A										TS08/IRQ0_C
24	-	-	-	11		P204													TS09
25	19	16	F2	12	RES														
26	20	17	E4	13	MD	P201													
27	21	18	E5	14		P200													NMI
28	-	-	-	-		P304			GTIOC6A_A										TS10/KR07
29	-	-	-	-		P303			GTIOC6B_A										TS11/KR06
30	22	-	-	-	CACREF_A	P302	AGTOA1_A	GTOVLO_B	GTIOC3B_B										TS12/KR05/IRQ4_B

1.7 引脚列表

Pin number				Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analog		HMI					
针号	QFN48	QFN40	BGA36			AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt	
1	1	1	D3	1	P400	AGTEE0_A	GTETRGA_A	GTIOC1A_A	RTCCOUT_C										TS00	KR02/IRQ0_A	
2	2	-	-	-	P401	AGTEE1_A	GTIU_A	GTIOC4A_A												TS01	KR03/IRQ5_B
3	-	-	-	-	P402		GTIV_A	GTIOC0A_D												TS02	
4	-	-	-	-	P403		GTIW_A	GTIOC0B_C												TS03	
5	3	2	A1	2	VCL																
6	4	3	B1	-	XCIN	P215															
7	5	4	B2	-	XCOUT	P214															
8	6	5	D2	3	VSS																
9	7	6	C1	4	XTAL	P213	AGTEE1_B	GTETRGA_B	GTIOC0A_B											IRQ2_B	
10	8	7	D1	5	EXTAL	P212	AGTIO0_A	GTETRGA_B	GTIOC0B_B											IRQ3_B	
11	9	8	E2	6	VCC																
12	-	-	-	-	P411			GTIOC5A_A												TS04	
13	-	-	-	-	P410			GTIOC5B_A												TS05	
14	10	-	-	-	P409	AGTO1_A		GTIOC0A_C												TSCAP_E/IRQ7_A	
15	11	9	E1	7		P408	AGTO0_A	GTOUUP_A	GTIOC0A_A											TS06/IRQ1_A	
16	12	10	F1	8	CACREF_B	P407	AGTIO0_C	GTOULO_A	GTIOC0B_A											TSCAP_D/IRQ1_B	
17	13	11	D2	-	VSS_USB																
18	14	12	F4	-		P915														USB_DM	
19	15	13	F3	-		P914														USB_DP	
20	16	14	F5	-	VCC_USB																
21	17	15	E3	-	VCC_USB_LDO																
22	18	-	-	9		P206	AGTIO0_B	GTOVUP_A	GTIOC3A_A											TS07/IRQ6_A	
23	-	-	-	10		P205		GTOVL_O_A	GTIOC3B_A											TS08/IRQ0_C	
24	-	-	-	11		P204														TS09	
25	19	16	F2	12	RES																
26	20	17	E4	13	MD	P201															
27	21	18	E5	14		P200														NMI	
28	-	-	-	-		P304			GTIOC6A_A											TS10/KR07	
29	-	-	-	-		P303			GTIOC6B_A											TS11/KR06	
30	22	-	-	-	CACREF_A	P302	AGTOA1_A	GTOVLO_B	GTIOC3B_B											TS12/KR05/IRQ4_B	

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analog				HMI																			
LQFP64	QFN48	QFN40	BGA36	LQFP32			AGT	GPT_OPS, POEG	GPT	RTC	USBS, CAN	SCI	IC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt																	
31	23	19	D4	15		P301													TS13	KR04/IRQ5_A																		
32	24	20	F6	16	SWCLK	P300																																
33	25	21	E6	17	SWDIO	P108																																
34	26	22	C4	18	CLKOUT_A	P110	AGTOB0_A	GTOWL_O_A	GTIOC2_B_B				CTX0_C	TXD0_D/MISO0_D/SDA0_D/RXD9_B/MISO9_B/SCL9_B	SDA1_D	RSPCKA_A	ADTRG0_A		CMPREF1	TSCAP_A	IRQ2_A																	
35	-	-	-	-		P111									SCL1_C	RSPCKA_B				TS14	IRQ6_B																	
36	-	-	-	-	CLKOUT_B	P112									SDA1_C	SSLA0_B					TSCAP_B	IRQ7_B																
37	27	23	D5	19	ADREG																																	
38	28	24	D6	20	SBIAS/VREFI																																	
39	29	25	B5	21	AVCC1																																	
40	30	26	C5	22	AVSS1																																	
41	-	-	-	-		P107															AN023	ANS03N																
42	-	-	-	-		P106																AN022	ANS03P															
43	31	-	-	-		P105																MOSIB_C	AN021	ANS02N														
44	32	-	-	-		P104																	MISOB_C	AN020	ANS02P													
45	33	27	-	-		P103																		RSPCKB_C	AN019	ANS01N												
46	34	28	-	-		P102																			CTSD9_RT/S9_D/SS9_D	SSLB0_C	AN018	ANS01P										
47	35	29	C6	23		P101																			RXD9_C/MISO9_C/SCL9_C		AN017	ANS00N	IVREF2	TS22	IRQ5_C							
48	36	30	B6	24		P100																			TXD9_D/MISO9_D/SDA9_D		AN016	ANS00P	IVCMP2	TS23	IRQ4_C							
49	37	31	A6	25		P500																			RXD0_D/MISO0_D/SCL0_D		AN000	DA12_0	IVCMP0	AMP0+	TS24	IRQ3_C						
50	38	32	A5	26		P501																			TXD0_E/MISO0_E/SDA0_E		AN001		IVREF0	AMP0-	TS25	IRQ2_C						
51	39	33	A4	27		P502																			CTS0_RT/S0_E/SS0_E		AN002			AMP00	IRQ1_C							
52	40	-	-	-		P015																										AN003		AMP10				
53	41	-	-	-	VREFL	P014																											AN004		IVREF1	AMP1-		
54	42	34	-	-	VREFH	P013																												AN005	DA8_0	IVCMP1	AMP1+	
55	-	-	-	-		P012																												AN008		AMP20		
56	43	35	B4	28	AVCC0																																	
57	44	36	B3	29	AVSS0																																	
58	45	37	A3	30	VREFLO																																	
59	46	38	A2	31	VREFHO																																	
60	-	-	-	-		P003																																
61	-	-	-	-		P002																																
62	-	-	-	-		P001																																
63	47	39	C3	-		P000	AGTIO1_A		GTIOC4_B_B																													
64	48	40	C2	32		P109	AGTIOA0_A	GTETR_GB_A	GTIOC1_B_B																													

Note: Several pin names have the added suffix of \_A, \_B, \_C, \_D, \_E and \_F. The suffix can be ignored when assigning functionality.

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analog				HMI			
LQFP64	QFN48	QFN40	BGA36	LQFP32			AGT	GPT_OPS, POEG	GPT	RTC	USBS, CAN	SCI	IC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt	
31	23	19	D4	15		P301															TS13	KR04/IRQ5_A
32	24	20	F6	16	SWCLK	P300																
33	25	21	E6	17	SWDIO	P108																
34	26	22	C4	18	CLKOUT_A	P110	AGTOB0_A	GTOWL_O_A	GTIOC2_B_B				CTX0_C	TXD0_D/MISO0_D/SDA0_D/RXD9_B/MISO9_B/SCL9_B	SDA1_D	RSPCKA_A	ADTRG0_A		CMPREF1	TSCAP_A	IRQ2_A	
35	-	-	-	-		P111																
36	-	-	-	-	CLKOUT_B	P112																
37	27	23	D5	19	ADREG																	
38	28	24	D6	20	SBIAS/VREFI																	
39	29	25	B5	21	AVCC1																	
40	30	26	C5	22	AVSS1																	
41	-	-	-	-		P107																
42	-	-	-	-		P106																
43	31	-	-	-		P105																
44	32	-	-	-		P104																
45	33	27	-	-		P103																
46	34	28	-	-		P102																
47	35	29	C6	23		P101																
48	36	30	B6	24		P100																
49	37	31	A6	25		P500																
50	38	32	A5	26		P501																
51	39	33	A4	27		P502																
52	40	-	-	-		P015																
53	41	-	-	-	VREFL	P014																
54	42	34	-	-	VREFH	P013																
55	-	-	-	-		P012																
56	43	35	B4	28	AVCC0																	
57	44	36	B3	29	AVSS0																	
58	45	37	A3	30	VREFLO																	
59	46	38	A2	31	VREFHO																	
60	-	-	-	-		P003																
61	-	-	-	-		P002																
62	-	-	-	-		P001																
63	47	39	C3	-		P000	AGTIO1_A		GTIOC4_B_B													
64	48	40	C2	32		P109	AGTIOA0_A	GTETR_GB_A	GTIOC1_B_B													

Note: 几个管脚名称添加了\_A、\_B、\_C、\_D、\_E和\_F的后缀。分配功能时可以忽略后缀。

## 2. Electrical Characteristics

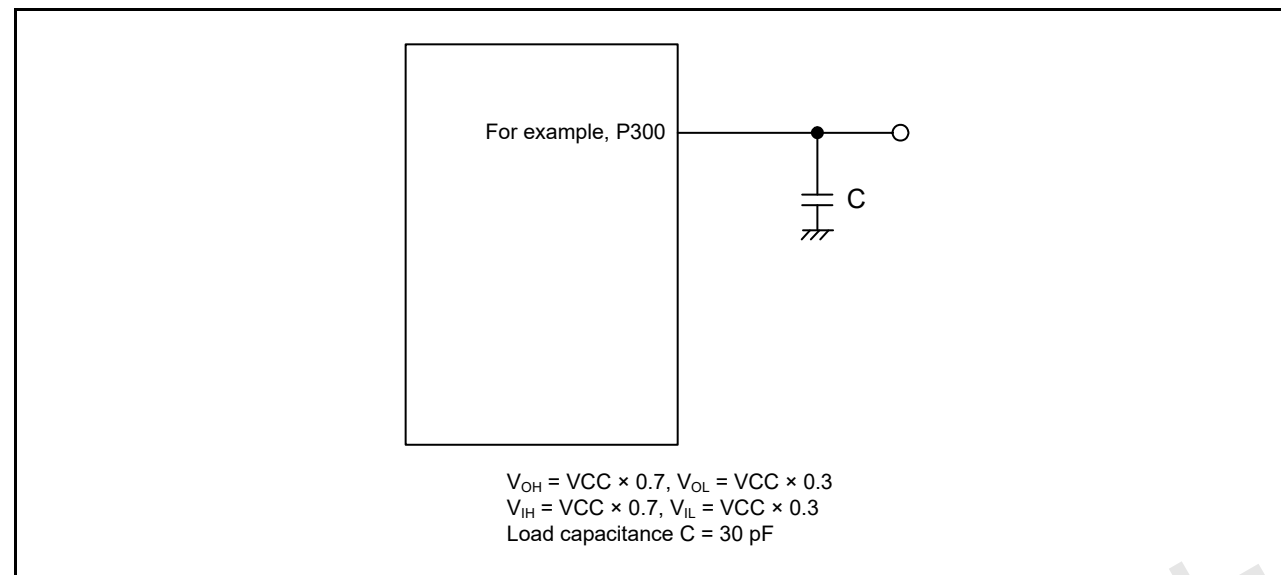
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC^{*1} = AVCC0 = AVCC1 = VCC\_USB^{*2} = VCC\_USB\_LDO^{*2} = 1.6$  to  $5.5$  V
- $VREFH = VREFH0 = 1.6$  to  $AVCC0$
- $VSS = AVSS0 = AVSS1 = VREFL = VREFL0 = VSS\_USB = 0$  V
- $T_a = T_{opr}$ .

Note 1. The typical condition is set to  $VCC = 3.3$  V.

Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.



**Figure 2.1** Input or output timing measurement conditions

The measurement conditions for the timing specifications of each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

### 2.1 Absolute Maximum Ratings

**Table 2.1** Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit	
Power supply voltage	VCC	-0.5 to +6.5	V	
Input voltage	5 V-tolerant ports*1	$V_{in}$	-0.3 to +6.5	V
	P002, P003, P012 to P015, P500 to P502	$V_{in}$	-0.3 to $AVCC0 + 0.3$	V
	P100 to P107	$V_{in}$	-0.3 to $AVCC1 + 0.3$	V
	Others	$V_{in}$	-0.3 to $VCC + 0.3$	V
Reference power supply voltage	VREFH0	-0.3 to +6.5	V	
	VREFH	-0.3 to +6.5	V	
	VREFI	-0.3 to $AVCC1 + 0.3$	V	
Analog power supply voltage	AVCC0, AVCC1*5	-0.5 to +6.5	V	

## 2. 电气特性

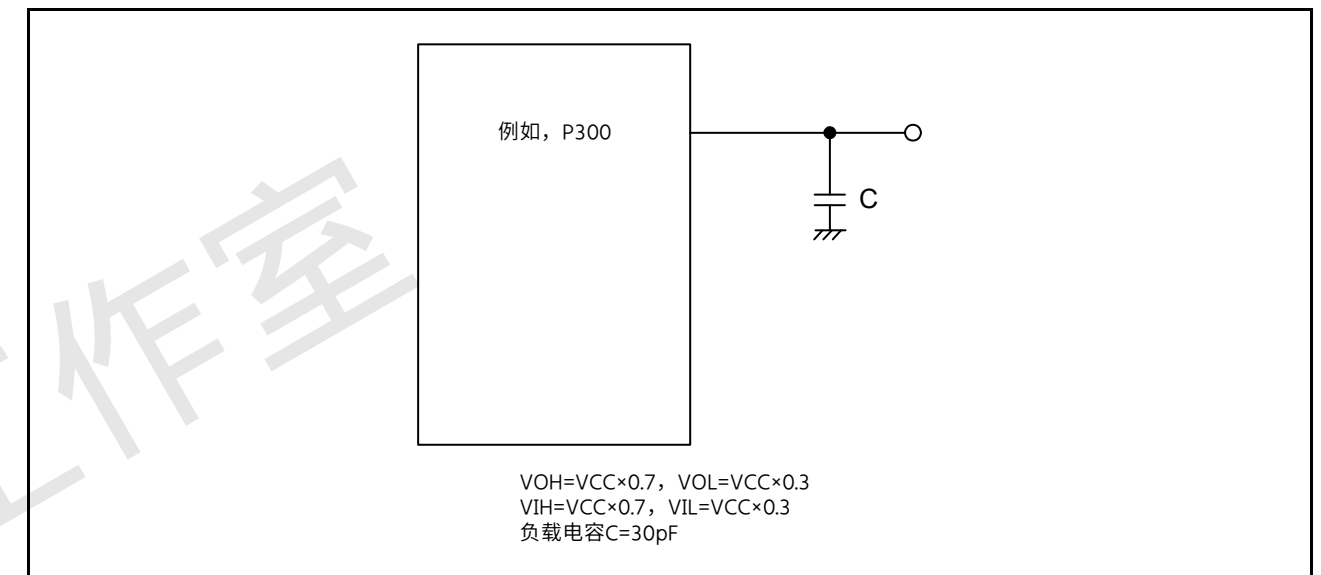
除非另有规定，MCU的电气特性在以下条件下定义：

- $VCC^{*1} = AVCC0 = AVCC1 = VCC\_USB^{*2} = VCC\_USB\_LDO^{*2} = 1.6$  to  $5.5$  V
- $VREFH = VREFH0 = 1.6$  to  $AVCC0$
- $VSS = AVSS0 = AVSS1 = VREFL = VREFL0 = VSS\_USB = 0$  V
- $T_a = T_{opr}$ .

Note 1. 典型条件设置为 $VCC=3.3V$ 。

Note 2. 不使用USBFS时。

图2.1显示了时序条件。



**Figure 2.1** 输入或输出定时测量条件

推荐每个外设的时序规格的测量条件，以获得最佳的外设操作。但是，请确保调整每个引脚的驱动能力以满足您的系统条件。

用于相同功能的每个功能引脚必须选择相同的驱动能力。如果各功能管脚的IO驱动能力混用，则无法保证各功能的AC规格。

### 2.1 绝对最大额定值

**Table 2.1** 绝对最大额定值(1of2)

Parameter	Symbol	Value	Unit	
电源电压	VCC	-0.5 to +6.5	V	
输入电压	5 V-tolerant ports*1	$V_{in}$	-0.3 to +6.5	V
	P002, P003, P012 to P015, P500 to P502	$V_{in}$	-0.3 to $AVCC0 + 0.3$	V
	P100 to P107	$V_{in}$	-0.3 to $AVCC1 + 0.3$	V
	Others	$V_{in}$	-0.3 to $VCC + 0.3$	V
参考电源电压	VREFH0	-0.3 to +6.5	V	
	VREFH	-0.3 to +6.5	V	
	VREFI	-0.3 to $AVCC1 + 0.3$	V	
模拟电源电压	AVCC0, AVCC1*5	-0.5 to +6.5	V	

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
USB power supply voltage	VCC_USB	-0.5 to +6.5	V
	VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	V <sub>AN</sub>	When AN000 to AN008 are used	-0.3 to AVCC0 + 0.3
		When AN016 to AN023 are used	-0.3 to AVCC1 + 0.3
		When ANSD0P to ANSD3P and ANSD0N to ANSD3N are used	-0.3 to AVCC1 + 0.3
Operating temperature*2 *3 *4	T <sub>opr</sub>	-40 to +85 -40 to +105	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

- Note 1. Ports P000, P111, P112, P205, P206, P301, P401, P407, and P409 are 5 V tolerant. Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
- Note 2. See [section 2.2.1, Tj/Ta Definition](#).
- Note 3. Contact Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
- Note 4. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#).
- Note 5. Use AVCC0 and AVCC1 under the same conditions:  
AVCC0 = AVCC1

**Caution:** Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the VCC\_USB and VSS\_USB pins, between the VREFH and VREFL pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC16. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- VCC and VSS: about 0.1 μF
- AVCC0 and AVSS0: about 0.1 μF
- AVCC1 and AVSS1: about 0.1 μF
- VREFH and VREFL: about 0.1 μF
- VREFH0 and VREFL0: about 10 μF.

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 μF capacitor. Connect the VREFH0 pin to a VREFL0 pin by 1 μF (-25% to +25%) capacitor when VREFADC is selected as the high potential reference voltage of the ADC16. Connect the ADREG pin to a AVSS1 pin by a 0.47 μF (-50% to +20%) capacitor. Connect the SBIAS/VREFI pin to a AVSS1 pin by a 0.22 μF (-20% to +20%) capacitor. Every capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions (1 of 2)

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB_LDO	-	5.5	V
	VSS	-	0	-	-	V

Table 2.1 绝对最大额定值(2of2)

Parameter	Symbol	Value	Unit
USB电源电压	VCC_USB	-0.5 to +6.5	V
	VCC_USB_LDO	-0.5 to +6.5	V
模拟输入电压	V <sub>AN</sub>	使用AN000至AN008时	-0.3 to AVCC0 + 0.3
		使用AN016至AN023时	-0.3 to AVCC1 + 0.3
		使用ANS0P到ANS03P和ANS0N到ANS03N时	-0.3 to AVCC1 + 0.3
Operating temperature*2 *3 *4	T <sub>opr</sub>	-40 to +85 -40 to +105	°C
贮存温度	T <sub>stg</sub>	-55 to +125	°C

- Note 1. 端口P000、P111、P112、P205、P206、P301、P401、P407和P409可承受5V电压。请勿在设备未通电时输入信号或IO上拉电源。输入此类信号或IO上拉导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件劣化。
- Note 2. 请参见第2.2.1节，Tj/Ta定义。
- Note 3. 有关Ta=+85°C至+105°C时降额操作的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。
- Note 4. 工作温度的上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分Numbering。
- Note 5. 在相同条件下使用AVCC0和AVCC1：  
AVCC0 = AVCC1

**Caution:** 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

为排除因噪声干扰而导致的任何故障，请在VCC和VSS引脚之间、AVCC0和AVSS0引脚之间、AVCC1和AVSS1引脚之间、VCC\_USB和VSS\_USB引脚之间、VREFH和VREFL引脚之间插入具有高频特性的电容器，当VREFH0被选为ADC16的高电位参考电压时，VREFH0和VREFL0引脚之间。将以下值的电容器尽可能靠近每个电源引脚并使用最短和最重的走线：VCC和VSS：约0.1μFAVCC0和AVSS0：约0.1μFAVCC1和AVSS1：约0.1μFVREFH和VREFL：约0.1μFVREFH0和VREFL0：约10μF。此外，连接电容器作为稳定电容。

通过一个4.7μF电容将VCL引脚连接到VSS引脚。Connect the VREFH0 pin to a VREFL0 pin by 1 μF (25% to +25%) capacitor when VREFADC is selected as the high potential reference voltage of the ADC16. 通过一个0.47 μF (50%至+20%) 电容将ADREG引脚连接到AVSS1引脚。通过一个0.22 μF (20%至+20%) 电容将SBIASVREF I引脚连接到AVSS1引脚。每个电容器都必须靠近引脚放置。

Table 2.2 推荐的操作条件 (2个中的1个)

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC*1, *2	不使用USBFS时	1.6	-	5.5	V
		使用USBFS时 USB稳压器 Disable	VCC_USB	-	3.6	V
		使用USBFS时 USB稳压器 Enable	VCC_USB_LDO	-	5.5	V
	VSS	-	0	-	-	V



Table 2.2 Recommended operating conditions (2 of 2)

Parameter	Symbol	Value	Min	Typ	Max	Unit
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	AVCC1*1, *2		-	AVCC0	-	V
	AVSS1		-	0	-	V
	VREFH0	When used as ADC16 Reference	1.7	-	AVCC0	V
	VREFL0		-	0	-	V
	VREFH	When used as DAC12 Reference	1.7	-	AVCC0	V
	VREFL		-	0	-	V
	VREFI	When used as SDADC24 Reference*3	0.8	-	2.4	V

- Note 1. Use AVCC0, AVCC1, and VCC under the following conditions:  
AVCC0, AVCC1, and VCC can be set individually within the operating range when  $VCC \geq 2.2\text{ V}$  and  $AVCC0 = AVCC1 \geq 2.2\text{ V}$ .  
 $AVCC0 = AVCC1 = VCC$  when  $VCC < 2.2\text{ V}$  or  $AVCC0 = AVCC1 < 2.2\text{ V}$ .
- Note 2. When powering on the VCC and AVCC0 and AVCC1 pins, power them on at the same time or the VCC pin first and then the AVCC0 and AVCC1 pins.
- Note 3. The condition when using external input for the reference voltage of SDADC24.

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T<sub>a</sub>) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T <sub>j</sub>	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode
			105*1		

- Note: Make sure that  $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$ , where total power consumption =  $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times VCC$ .
- Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#). If the part number shows the operation temperature at 85°C, then the maximum value of T<sub>j</sub> is 105°C, otherwise it is 125°C.

Table 2.2 推荐的操作条件 (2个中的2个)

Parameter	Symbol	Value	Min	Typ	Max	Unit
USB电源电压	VCC_USB	不使用USBFS时	-	VCC	-	V
		使用USBFS时 USB稳压器 Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	不使用USBFS时	-	VCC	-	V
		使用USBFS时 USB稳压器 Disable	-	VCC	-	V
		使用USBFS时 USB稳压器 Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
模拟电源电压	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	AVCC1*1, *2		-	AVCC0	-	V
	AVSS1		-	0	-	V
	VREFH0	当用作 ADC16 Reference	1.7	-	AVCC0	V
	VREFL0		-	0	-	V
	VREFH	当用作 DAC12 Reference	1.7	-	AVCC0	V
	VREFL		-	0	-	V
	VREFI	当用作 SDADC24 Reference*3	0.8	-	2.4	V

- Note 1. 在以下条件下使用AVCC0、AVCC1和VCC:  
当 $VCC \geq 2.2\text{ V}$ 且 $AVCC0 = AVCC1 \geq 2.2\text{ V}$ 时, AVCC0、AVCC1和VCC可以在工作范围内单独设置。  
当 $VCC < 2.2\text{ V}$ 或 $AVCC0 = AVCC1 < 2.2\text{ V}$ 时,  $AVCC0 = AVCC1 = VCC$ 。
- Note 2. VCC和AVCC0和AVCC1引脚上电时, 同时上电或先上电VCC再上电。  
AVCC0和AVCC1引脚。
- Note 3. SDADC24的参考电压使用外部输入时的条件。

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

条件: 工作温度(T<sub>a</sub>)-40至+105°C的产品

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T <sub>j</sub>	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode
			105*1		

- Note: 确保 $T_j = T_a + \theta_{ja} \times \text{总功耗(W)}$ , 其中总功耗= $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times VCC$ 。
- Note 1. 工作温度上限为85°C或105°C, 具体取决于产品。有关详细信息, 请参阅第1.3节, 部分编号。如果零件编号显示工作温度为85°C, 则T<sub>j</sub>的最大值为105°C, 否则为125°C。

2.2.2 I/O  $V_{IH}$ ,  $V_{IL}$ Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$ 

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	$V_{IH}$	$VCC \times 0.7$	-	5.8	V
		$V_{IL}$	-	-	$VCC \times 0.3$	
		$\Delta V_T$	$VCC \times 0.05$	-	-	
	RES, NMI Other peripheral input pins excluding IIC	$V_{IH}$	$VCC \times 0.8$	-	-	
		$V_{IL}$	-	-	$VCC \times 0.2$	
		$\Delta V_T$	$VCC \times 0.1$	-	-	
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	$V_{IH}$	2.2	-	-	VCC = 3.6 to 5.5 V
		$V_{IH}$	2.0	-	-	VCC = 2.7 to 3.6 V
		$V_{IL}$	-	-	0.8	VCC = 2.7 to 5.5 V
	5 V-tolerant ports*3	$V_{IH}$	$VCC \times 0.8$	-	5.8	-
		$V_{IL}$	-	-	$VCC \times 0.2$	
	P002, P003, P012 to P015, P500 to P502	$V_{IH}$	$AVCC0 \times 0.8$	-	-	
		$V_{IL}$	-	-	$AVCC0 \times 0.2$	
	P100 to P107	$V_{IH}$	$AVCC1 \times 0.8$	-	-	
		$V_{IL}$	-	-	$AVCC1 \times 0.2$	
	P914, P915	$V_{IH}$	$VCC\_USB \times 0.8$	-	$VCC\_USB + 0.3$	
		$V_{IL}$	-	-	$VCC\_USB \times 0.2$	
	EXTAL Input ports pins except for P002, P003, P012 to P015, P100 to P107, P500 to P502, P914, P915	$V_{IH}$	$VCC \times 0.8$	-	-	
		$V_{IL}$	-	-	$VCC \times 0.2$	

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_C, SCL1\_B, SCL1\_C, SDA1\_B, SDA1\_C (total 9 pins)

Note 2. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins)

Note 3. P000, P111, P112, P205, P206, P301, P401, P407, P409 (total 9 pins)

2.2.2 I/O  $V_{IH}$ Table 2.4 I/O  $V_{IH}$ 

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
施密特触发器 输入电压	IIC (except for SMBus)*1	$V_{IH}$	$VCC \times 0.7$	-	5.8	V
		$V_{IL}$	-	-	$VCC \times 0.3$	
		$\Delta V_T$	$VCC \times 0.05$	-	-	
	RES, NMI 除IIC外的其他外设输入引 脚	$V_{IH}$	$VCC \times 0.8$	-	-	
		$V_{IL}$	-	-	$VCC \times 0.2$	
		$\Delta V_T$	$VCC \times 0.1$	-	-	
输入电压 (施 密特触发器输 入引脚除外)	IIC (SMBus)*2	$V_{IH}$	2.2	-	-	VCC = 3.6 to 5.5 V
		$V_{IH}$	2.0	-	-	VCC = 2.7 to 3.6 V
		$V_{IL}$	-	-	0.8	VCC = 2.7 to 5.5 V
	5 V-tolerant ports*3	$V_{IH}$	$VCC \times 0.8$	-	5.8	-
		$V_{IL}$	-	-	$VCC \times 0.2$	
	P002, P003, P012 to P015, P500 to P502	$V_{IH}$	$AVCC0 \times 0.8$	-	-	
		$V_{IL}$	-	-	$AVCC0 \times 0.2$	
	P100 to P107	$V_{IH}$	$AVCC1 \times 0.8$	-	-	
		$V_{IL}$	-	-	$AVCC1 \times 0.2$	
	P914, P915	$V_{IH}$	$VCC\_USB \times 0.8$	-	$VCC\_USB + 0.3$	
		$V_{IL}$	-	-	$VCC\_USB \times 0.2$	
	EXTAL 输入端口引脚除了 P002, P003, P012 to P015, P100 to P107, P500 to P502, P914, P915	$V_{IH}$	$VCC \times 0.8$	-	-	
		$V_{IL}$	-	-	$VCC \times 0.2$	

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_C, SCL1\_B, SCL1\_C, SDA1\_B, SDA1\_C (total 9 pins)

Note 2. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins)

Note 3. P000, P111, P112, P205, P206, P301, P401, P407, P409 (total 9 pins)

2.2.3 I/O I<sub>OH</sub>, I<sub>OL</sub>

**Table 2.5 I/O I<sub>OH</sub>, I<sub>OL</sub>**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit		
Permissible output current (average value per pin)	Ports P212, P213	-	I <sub>OH</sub>	-	-	-4.0	mA
		I <sub>OL</sub>	-	-	4.0	mA	
	Ports P407, P408, P409	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
		Middle drive for IIC Fast mode and SPI*4	I <sub>OH</sub>	-	-	-8.0	mA
			I <sub>OL</sub>	-	-	8.0	mA
	Middle drive*2 VCC = 3.0 to 5.5 V	I <sub>OH</sub>	-	-	-20.0	mA	
		I <sub>OL</sub>	-	-	20.0	mA	
	Ports P914, P915	I <sub>OH</sub>	-	-	-4.0	mA	
		I <sub>OL</sub>	-	-	4.0	mA	
	Other output pins*3	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
Middle drive*2		I <sub>OH</sub>	-	-	-8.0	mA	
		I <sub>OL</sub>	-	-	8.0	mA	
Permissible output current (max value per pin)	Ports P212, P213	-	I <sub>OH</sub>	-	-	-4.0	mA
		I <sub>OL</sub>	-	-	4.0	mA	
	Ports P407, P408, P409	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
		Middle drive for IIC Fast mode and SPI*4	I <sub>OH</sub>	-	-	-8.0	mA
			I <sub>OL</sub>	-	-	8.0	mA
	Middle drive*2 VCC = 3.0 to 5.5 V	I <sub>OH</sub>	-	-	-20.0	mA	
		I <sub>OL</sub>	-	-	20.0	mA	
	Ports P914, P915	I <sub>OH</sub>	-	-	-4.0	mA	
		I <sub>OL</sub>	-	-	4.0	mA	
	Other output pins*3	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
Middle drive*2		I <sub>OH</sub>	-	-	-8.0	mA	
		I <sub>OL</sub>	-	-	8.0	mA	
Permissible output current (max value total pins)	Total of ports P002, P003, P012 to P015, P500 to P502	ΣI <sub>OH</sub> (max)	-	-	-30	mA	
		ΣI <sub>OL</sub> (max)	-	-	30	mA	
	Total of ports P100 to P107	ΣI <sub>OH</sub> (max)	-	-	-30	mA	
		ΣI <sub>OL</sub> (max)	-	-	30	mA	
	Total of ports P914, P915	ΣI <sub>OH</sub>	-	-	-4.0	mA	
		ΣI <sub>OL</sub>	-	-	4.0	mA	
	Total of all output pin*5	ΣI <sub>OH</sub> (max)	-	-	-60	mA	
		ΣI <sub>OL</sub> (max)	-	-	60	mA	

- Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
- Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
- Note 3. Except for Ports P200, P214, P215, which are input ports.
- Note 4. This is the value when middle driving ability for IIC Fast mode and SPI is selected with the Port Drive Capability bit in PmnPFS register.
- Note 5. For details on the permissible output current used with CTSU, see [section 2.12, CTSU Characteristics](#).

**Caution:** To protect the reliability of the MCU, the output current values should not exceed the values in [Table 2.5](#). The average output current indicates the average current value measured during 100 μs.

2.2.3 我爱我哦

**Table 2.5 我爱我哦**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit		
允许输出电流 (每个引脚的平均值)	Ports P212, P213	-	I <sub>OH</sub>	-	-	-4.0	mA
		I <sub>OL</sub>	-	-	4.0	mA	
	Ports P407, P408, P409	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
		IIC中间驱动器快速模式和SPI*4	I <sub>OH</sub>	-	-	-8.0	mA
			I <sub>OL</sub>	-	-	8.0	mA
	Middle drive*2 VCC = 3.0 to 5.5 V	I <sub>OH</sub>	-	-	-20.0	mA	
		I <sub>OL</sub>	-	-	20.0	mA	
	Ports P914, P915	I <sub>OH</sub>	-	-	-4.0	mA	
		I <sub>OL</sub>	-	-	4.0	mA	
	其他输出引脚*3	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
Middle drive*2		I <sub>OH</sub>	-	-	-8.0	mA	
		I <sub>OL</sub>	-	-	8.0	mA	
允许输出电流 (每个引脚的最大值)	Ports P212, P213	-	I <sub>OH</sub>	-	-	-4.0	mA
		I <sub>OL</sub>	-	-	4.0	mA	
	Ports P407, P408, P409	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
		IIC中间驱动器快速模式和SPI*4	I <sub>OH</sub>	-	-	-8.0	mA
			I <sub>OL</sub>	-	-	8.0	mA
	Middle drive*2 VCC = 3.0 to 5.5 V	I <sub>OH</sub>	-	-	-20.0	mA	
		I <sub>OL</sub>	-	-	20.0	mA	
	Ports P914, P915	I <sub>OH</sub>	-	-	-4.0	mA	
		I <sub>OL</sub>	-	-	4.0	mA	
	其他输出引脚*3	Low drive*1	I <sub>OH</sub>	-	-	-4.0	mA
			I <sub>OL</sub>	-	-	4.0	mA
Middle drive*2		I <sub>OH</sub>	-	-	-8.0	mA	
		I <sub>OL</sub>	-	-	8.0	mA	
允许输出电流 (最大总引脚数)	P002、P003、P012至P015、P500至端口总数	ΣI <sub>OH</sub> (max)	-	-	-30	mA	
		ΣI <sub>OL</sub> (max)	-	-	30	mA	
	P100至P107端口总数	ΣI <sub>OH</sub> (max)	-	-	-30	mA	
		ΣI <sub>OL</sub> (max)	-	-	30	mA	
	P914、P915端口总数	ΣI <sub>OH</sub>	-	-	-4.0	mA	
		ΣI <sub>OL</sub>	-	-	4.0	mA	
	所有输出引脚的总数*5	ΣI <sub>OH</sub> (max)	-	-	-60	mA	
		ΣI <sub>OL</sub> (max)	-	-	60	mA	

- Note 1. 这是使用PmnPFS寄存器中的端口驱动能力位选择低驱动能力时的值。
- Note 2. 这是使用PmnPFS寄存器中的端口驱动能力位选择中等驱动能力时的值。
- Note 3. 端口P200、P214、P215除外，它们是输入端口。
- Note 4. 这是通过PmnPFS寄存器中的端口驱动能力位选择IIC快速模式和SPI的中等驱动能力时的值。

Note 5. 有关与CTSU一起使用的允许输出电流的详细信息，请参阅第2.12节，CTSU特性。  
**Caution:** 为保护MCU的可靠性，输出电流值不应超过表2.5中的值。平均输出电流表示在100μs期间测量的平均电流值。

2.2.4 I/O  $V_{OH}$ ,  $V_{OL}$ , and Other Characteristics**Table 2.6** I/O  $V_{OH}$ ,  $V_{OL}$  (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 4.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1	$V_{OL}$	-	-	0.4	V $I_{OL} = 3.0 \text{ mA}$
		$V_{OL}^{*2,*5}$	-	-	0.6	$I_{OL} = 6.0 \text{ mA}$
Ports P407, P408, P409	Low drive	$V_{OH}$	VCC - 0.8	-	-	$I_{OH} = -2.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 2.0 \text{ mA}$
	Middle drive for IIC Fast mode and SPI*5	$V_{OH}$	VCC - 0.8	-	-	$I_{OH} = -4.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 4.0 \text{ mA}$
	Middle drive*2,*3	$V_{OH}$	VCC - 1.0	-	-	$I_{OH} = -20 \text{ mA}$
		$V_{OL}$	-	-	1.0	$I_{OL} = 20 \text{ mA}$
Ports P002, P003, P012 to P015, P500 to P502	Low drive	$V_{OH}$	AVCC0 - 0.8	-	-	$I_{OH} = -2.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 2.0 \text{ mA}$
	Middle drive	$V_{OH}$	AVCC0 - 0.8	-	-	$I_{OH} = -4.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 4.0 \text{ mA}$
Ports P100 to P107	Low drive	$V_{OH}$	AVCC1 - 0.8	-	-	$I_{OH} = -2.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 2.0 \text{ mA}$
	Middle drive	$V_{OH}$	AVCC1 - 0.8	-	-	$I_{OH} = -4.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 4.0 \text{ mA}$
Ports P914, P915	$V_{OH}$	VCC_USB - 0.8	-	-	$I_{OH} = -2.0 \text{ mA}$	
	$V_{OL}$	-	-	0.8	$I_{OL} = 2.0 \text{ mA}$	
Other output pins*4	Low drive	$V_{OH}$	VCC - 0.8	-	-	$I_{OH} = -2.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 2.0 \text{ mA}$
	Middle drive*6	$V_{OH}$	VCC - 0.8	-	-	$I_{OH} = -4.0 \text{ mA}$
		$V_{OL}$	-	-	0.8	$I_{OL} = 4.0 \text{ mA}$

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for P200, P214, P215, which are input ports.

Note 5. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in PmnPFS register for P407, P408, and P409.

Note 6. Except for P212, P213.

## 2.2.4 IOVOH VOL和其他特性

**Table 2.6** IOVOH VOL(1)

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 4.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
输出电压	IIC*1	$V_{OL}$	-	-	0.4	V 我OL=3.0毫安
		$V_{OL}^{*2,*5}$	-	-	0.6	我OL=6.0毫安
Ports P407, P408, P409	低驱动	$V_{OH}$	VCC - 0.8	-	-	IOH=-2.0毫安
		$V_{OL}$	-	-	0.8	我OL=2.0毫安
	IIC中间驱动器快速模式和SPI*5	$V_{OH}$	VCC - 0.8	-	-	IOH=-4.0毫安
		$V_{OL}$	-	-	0.8	我OL=4.0毫安
	Middle drive*2,*3	$V_{OH}$	VCC - 1.0	-	-	IOH=-20毫安
		$V_{OL}$	-	-	1.0	我OL=20毫安
Ports P002, P003, P012 to P015, P500 to P502	低驱动	$V_{OH}$	AVCC0 - 0.8	-	-	IOH=-2.0毫安
		$V_{OL}$	-	-	0.8	我OL=2.0毫安
	中间驱动器	$V_{OH}$	AVCC0 - 0.8	-	-	IOH=-4.0毫安
		$V_{OL}$	-	-	0.8	我OL=4.0毫安
端口P100至P107	低驱动	$V_{OH}$	AVCC1 - 0.8	-	-	IOH=-2.0毫安
		$V_{OL}$	-	-	0.8	我OL=2.0毫安
	中间驱动器	$V_{OH}$	AVCC1 - 0.8	-	-	IOH=-4.0毫安
		$V_{OL}$	-	-	0.8	我OL=4.0毫安
Ports P914, P915	$V_{OH}$	VCC_USB - 0.8	-	-	IOH=-2.0毫安	
	$V_{OL}$	-	-	0.8	我OL=2.0毫安	
其他输出引脚*4	低驱动	$V_{OH}$	VCC - 0.8	-	-	IOH=-2.0毫安
		$V_{OL}$	-	-	0.8	我OL=2.0毫安
	Middle drive*6	$V_{OH}$	VCC - 0.8	-	-	IOH=-4.0毫安
		$V_{OL}$	-	-	0.8	我OL=4.0毫安

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins).

Note 2. 这是使用PmnPFS寄存器中的端口驱动能力位选择中等驱动能力时的值。

Note 3. 基于特性数据，未经生产测试。

Note 4. P200、P214、P215除外，它们是输入端口。

Note 5. 这是通过PmnPFS寄存器中的端口驱动能力位选择IIC和SPI的中等驱动能力时的值 P407, P408, and P409.

Note 6. P212、P213除外。



**Table 2.7 I/O V<sub>OH</sub>, V<sub>OL</sub> (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 2.7 to 4.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC*1	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 3.0 mA
		V <sub>OL</sub> *2,*5	-	-	0.6		I <sub>OL</sub> = 6.0 mA
Ports P407, P408, P409	Low drive	V <sub>OH</sub>	VCC - 0.5	-	-		I <sub>OH</sub> = -1.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 1.0 mA
	Middle drive for IIC Fast mode and SPI*5	V <sub>OH</sub>	VCC - 0.5	-	-		I <sub>OH</sub> = -2.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 2.0 mA
	Middle drive*2,*3	V <sub>OH</sub>	VCC - 1.0	-	-		I <sub>OH</sub> = -20 mA VCC = 3.3 V
		V <sub>OL</sub>	-	-	1.0		I <sub>OL</sub> = 20 mA VCC = 3.3 V
Ports P002, P003, P012 to P015, P500 to P502	Low drive	V <sub>OH</sub>	AVCC0 - 0.5	-	-		I <sub>OH</sub> = -1.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 1.0 mA
	Middle drive	V <sub>OH</sub>	AVCC0 - 0.5	-	-		I <sub>OH</sub> = -2.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 2.0 mA
Ports P100 to P107	Low drive	V <sub>OH</sub>	AVCC1 - 0.5	-	-		I <sub>OH</sub> = -1.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 1.0 mA
	Middle drive	V <sub>OH</sub>	AVCC1 - 0.5	-	-		I <sub>OH</sub> = -2.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 2.0 mA
Ports P914, P915	V <sub>OH</sub>	VCC_USB - 0.5	-	-		I <sub>OH</sub> = -1.0 mA	
	V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 1.0 mA	
Other output pins*4	Low drive	V <sub>OH</sub>	VCC - 0.5	-	-		I <sub>OH</sub> = -1.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 1.0 mA
	Middle drive*6	V <sub>OH</sub>	VCC - 0.5	-	-		I <sub>OH</sub> = -2.0 mA
		V <sub>OL</sub>	-	-	0.5		I <sub>OL</sub> = 2.0 mA

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for P200, P214, P215, which are input ports.

Note 5. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in PmnPFS register for P407, P408, and P409.

Note 6. Except for P212, P213.

**Table 2.7 IOVOH VOL(2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 2.7 to 4.0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
输出电压	IIC*1	V <sub>OL</sub>	-	-	0.4	V	我OL=3.0毫安
		V <sub>OL</sub> *2,*5	-	-	0.6		我OL=6.0毫安
Ports P407, P408, P409	低驱动	V <sub>OH</sub>	VCC - 0.5	-	-		IOH=1.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=1.0毫安
	IIC中间驱动器快速模式和SPI*5	V <sub>OH</sub>	VCC - 0.5	-	-		IOH=2.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=2.0毫安
	Middle drive*2,*3	V <sub>OH</sub>	VCC - 1.0	-	-		我OH=20毫安 VCC=3.3V
		V <sub>OL</sub>	-	-	1.0		我OL=20毫安 VCC=3.3V
Ports P002, P003, P012 to P015, P500 to P502	低驱动	V <sub>OH</sub>	AVCC0 - 0.5	-	-		IOH=1.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=1.0毫安
	中间驱动器	V <sub>OH</sub>	AVCC0 - 0.5	-	-		IOH=2.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=2.0毫安
端口P100至P107	低驱动	V <sub>OH</sub>	AVCC1 - 0.5	-	-		IOH=-1.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=1.0毫安
	中间驱动器	V <sub>OH</sub>	AVCC1 - 0.5	-	-		IOH=2.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=2.0毫安
Ports P914, P915	V <sub>OH</sub>	VCC_USB - 0.5	-	-		IOH=1.0毫安	
	V <sub>OL</sub>	-	-	0.5		我OL=1.0毫安	
其他输出引脚*4	低驱动	V <sub>OH</sub>	VCC - 0.5	-	-		IOH=1.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=1.0毫安
	Middle drive*6	V <sub>OH</sub>	VCC - 0.5	-	-		IOH=2.0毫安
		V <sub>OL</sub>	-	-	0.5		我OL=2.0毫安

Note 1. SCL0\_A, SCL0\_B, SCL0\_C, SDA0\_A, SDA0\_B, SDA0\_C, SCL1\_A, SCL1\_B, SCL1\_C, SDA1\_A, SDA1\_B, SDA1\_C, SDA1\_D (total 13 pins).

Note 2. 这是使用PmnPFS寄存器中的端口驱动能力位选择中等驱动能力时的值。

Note 3. 基于特性数据，未经生产测试。

Note 4. P200、P214、P215除外，它们是输入端口。

Note 5. 这是通过PmnPFS寄存器中的端口驱动能力位选择IIC和SPI的中等驱动能力时的值 P407, P408, and P409.

Note 6. P212、P213除外。

**Table 2.8 I/O V<sub>OH</sub>, V<sub>OL</sub> (3)**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	Ports P407, P408, P409	Low drive	V <sub>OH</sub>	VCC - 0.3	-	-	V	I <sub>OH</sub> = -0.5 mA
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 0.5 mA	
		Middle drive for IIC Fast mode and SPI*2	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> = -1.0 mA	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 1.0 mA	
		Ports P002, P003, P012 to P015, P500 to P502	Low drive	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> = -0.5 mA
				V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 0.5 mA
	Middle drive		V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> = -1.0 mA	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 1.0 mA	
	Ports P100 to P107	Low drive	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> = -0.5 mA	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 0.5 mA	
		Middle drive	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> = -1.0 mA	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 1.0 mA	
Ports P914, P915		V <sub>OH</sub>	VCC_USB - 0.3	-	-	I <sub>OH</sub> = -0.5 mA		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 0.5 mA		
Other output pins*1	Low drive	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> = -0.5 mA		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 0.5 mA		
	Middle drive*3	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> = -1.0 mA		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> = 1.0 mA		

Note 1. Except for ports P200, P214, P215, which are input ports.

Note 2. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in the PmnPFS register for P407, P408, and P409.

Note 3. Except for P212, P213.

**Table 2.9 I/O other characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	I <sub>in</sub>	-	-	1.0	μA	V <sub>in</sub> = 0 V V <sub>in</sub> = VCC
Three-state leakage current (off state)	5 V-tolerant ports	I <sub>TSL</sub>	-	-	1.0	μA	V <sub>in</sub> = 0 V V <sub>in</sub> = 5.8 V
	Other ports		-	-	1.0		
Input pull-up resistor	All ports (except for P200, P214, P215, P914, P915)	R <sub>U</sub>	10	20	50	kΩ	V <sub>in</sub> = 0 V
Input capacitance	P012 to P015, P200, P502, P914, P915	C <sub>in</sub>	-	-	30	pF	V <sub>in</sub> = 0 V f = 1 MHz T <sub>a</sub> = 25°C
	Other input pins		-	-	15		

**Table 2.8 IOV<sub>OH</sub> VOL(3)**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件	
输出电压	Ports P407, P408, P409	低驱动	V <sub>OH</sub>	VCC - 0.3	-	-	V	I <sub>OH</sub> =0.5毫安
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =0.5毫安	
		IIC中间驱动器快速模式和SPI*2	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> =1.0毫安	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =1.0毫安	
		Ports P002, P003, P012 to P015, P500 to P502	低驱动	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> =0.5毫安
				V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =0.5毫安
	中间驱动器		V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> =1.0毫安	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =1.0毫安	
	端口P100至P107	低驱动	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> =0.5毫安	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =0.5毫安	
		中间驱动器	V <sub>OH</sub>	AVCC0 - 0.3	-	-	I <sub>OH</sub> =1.0毫安	
			V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =1.0毫安	
Ports P914, P915		V <sub>OH</sub>	VCC_USB - 0.3	-	-	I <sub>OH</sub> =0.5毫安		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =0.5毫安		
其他输出引脚*1	低驱动	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> =0.5毫安		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =0.5毫安		
	Middle drive*3	V <sub>OH</sub>	VCC - 0.3	-	-	I <sub>OH</sub> =-1.0毫安		
		V <sub>OL</sub>	-	-	0.3	I <sub>OL</sub> =1.0毫安		

注1.端口P200、P214、P215除外，它们是输入端口。

注2.这是IIC和SPI的中等驱动能力通过端口驱动能力位选择时的值 PmnPFS寄存器用于P407、P408和P409。

注3.P212、P213除外。

**Table 2.9 IO其他特征**

Conditions: VCC = AVCC0 = AVCC1 = VCC\_USB = VCC\_USB\_LDO = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入漏电流	RES, 端口P200、P214、P215	I <sub>in</sub>	-	-	1.0	μA	V <sub>in</sub> = 0 V V <sub>in</sub> = VCC
三态漏电流 (关闭状态)	5 V-tolerant ports	I <sub>TSL</sub>	-	-	1.0	μA	V <sub>in</sub> = 0 V V <sub>in</sub> = 5.8 V
	其他端口		-	-	1.0		
输入上拉电阻	所有端口 (P200、P214、P215、P914、P915除外)	R <sub>U</sub>	10	20	50	kΩ	V <sub>in</sub> = 0 V
输入电容	P012 to P015, P200, P502, P914, P915	C <sub>in</sub>	-	-	30	pF	V <sub>in</sub> = 0 V f = 1 MHz T <sub>a</sub> = 25°C
	其他输入引脚		-	-	15		

2.2.5 Output Characteristics for I/O Pins (Low Drive Capacity)

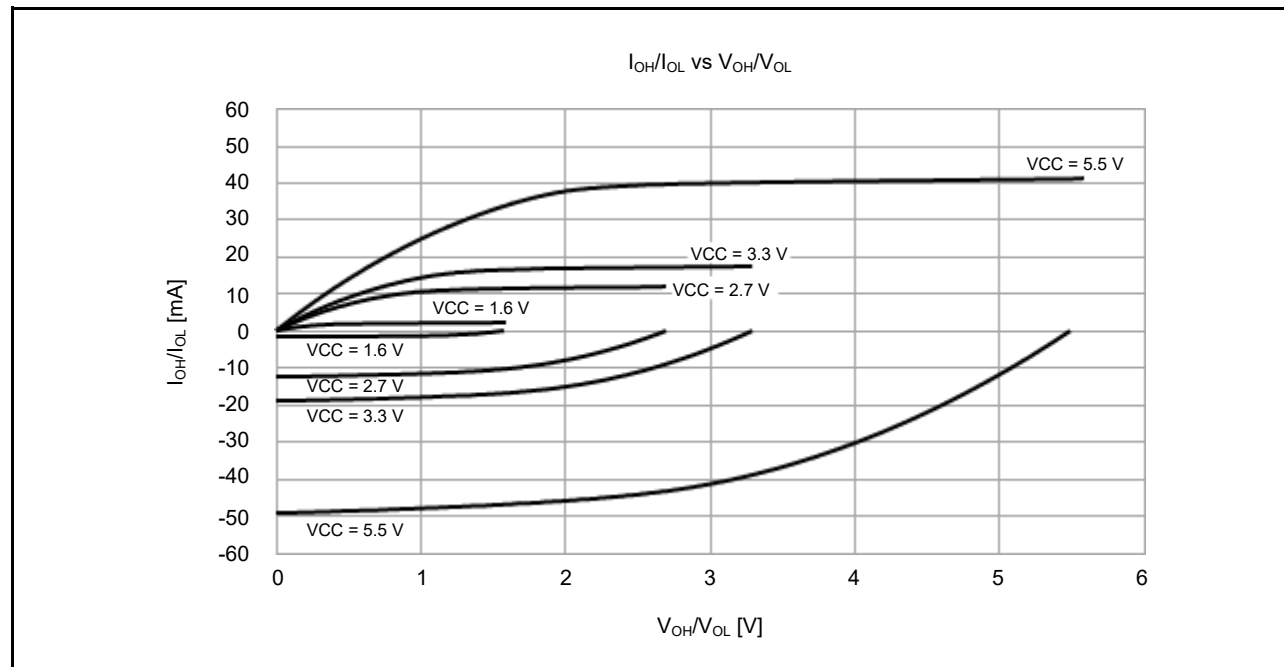


Figure 2.2  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when low drive output is selected (reference data, except for P914 and P915)

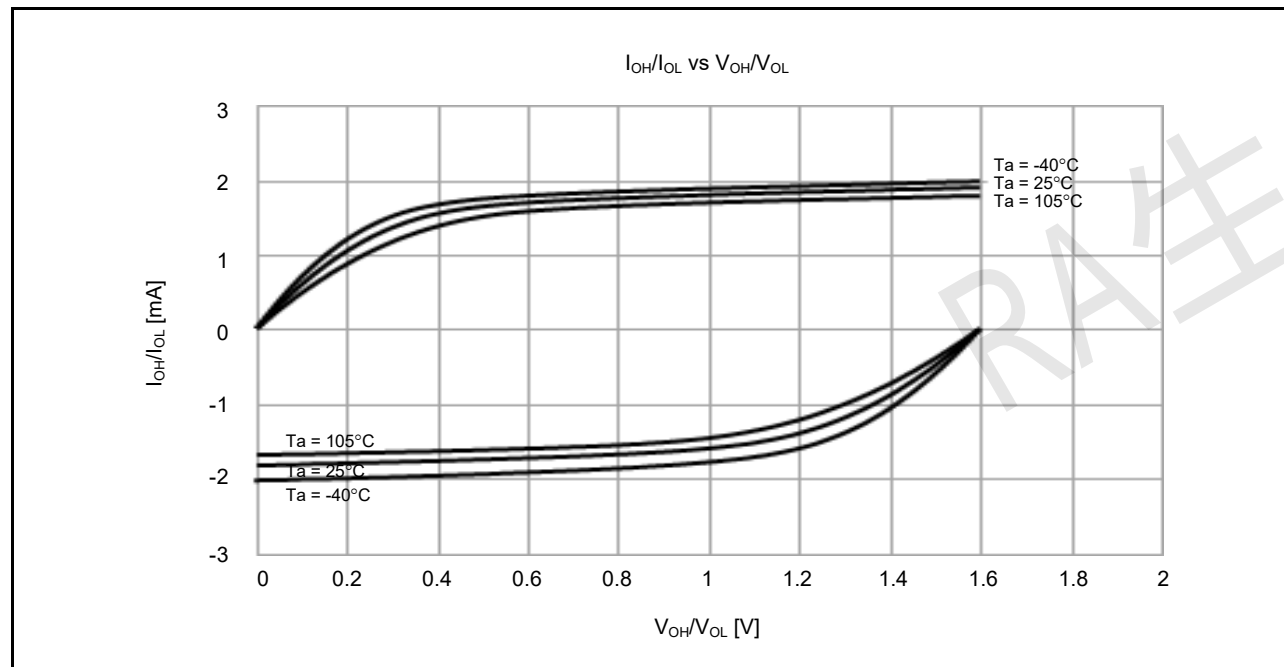


Figure 2.3  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 1.6V$  when low drive output is selected (reference data, except for P914 and P915)

2.2.5 IO引脚的输出特性（低驱动容量）

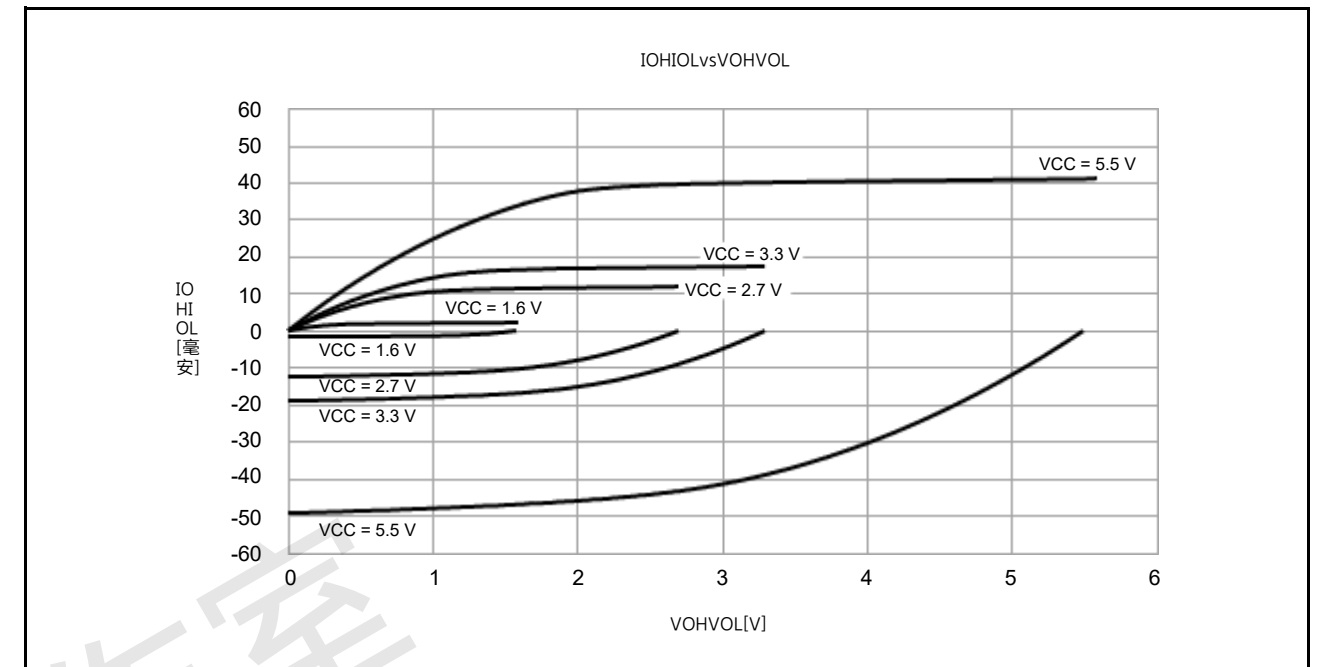


Figure 2.2 选择低驱动输出时,  $T_a=25^\circ\text{C}$ 时的 $V_{OH}/V_{OL}$ 和 $I_{OH}/I_{OL}$ 电压特性（参考数据, P914和P915除外）

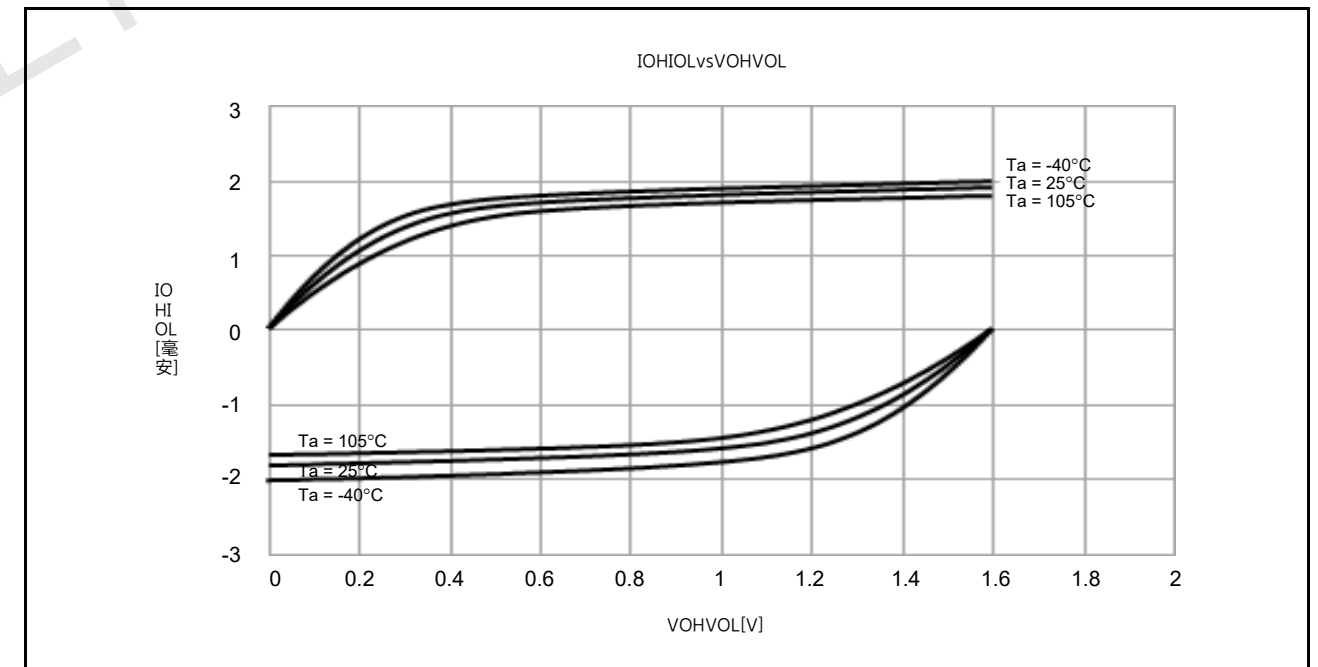


Figure 2.3 选择低驱动输出时,  $V_{OH}/V_{OL}$ 和 $I_{OH}/I_{OL}$ 在 $V_{CC}=1.6V$ 时的温度特性（参考数据, P914和P915除外）

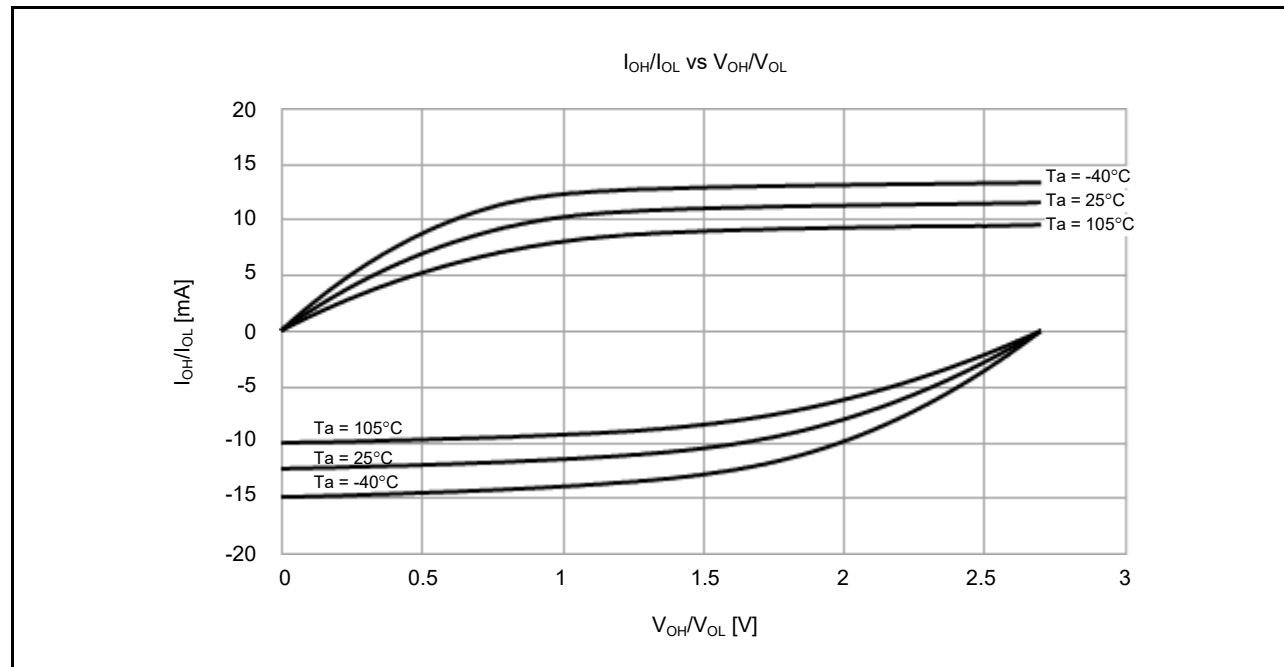


Figure 2.4  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7\text{ V}$  when low drive output is selected (reference data, except for P914 and P915)

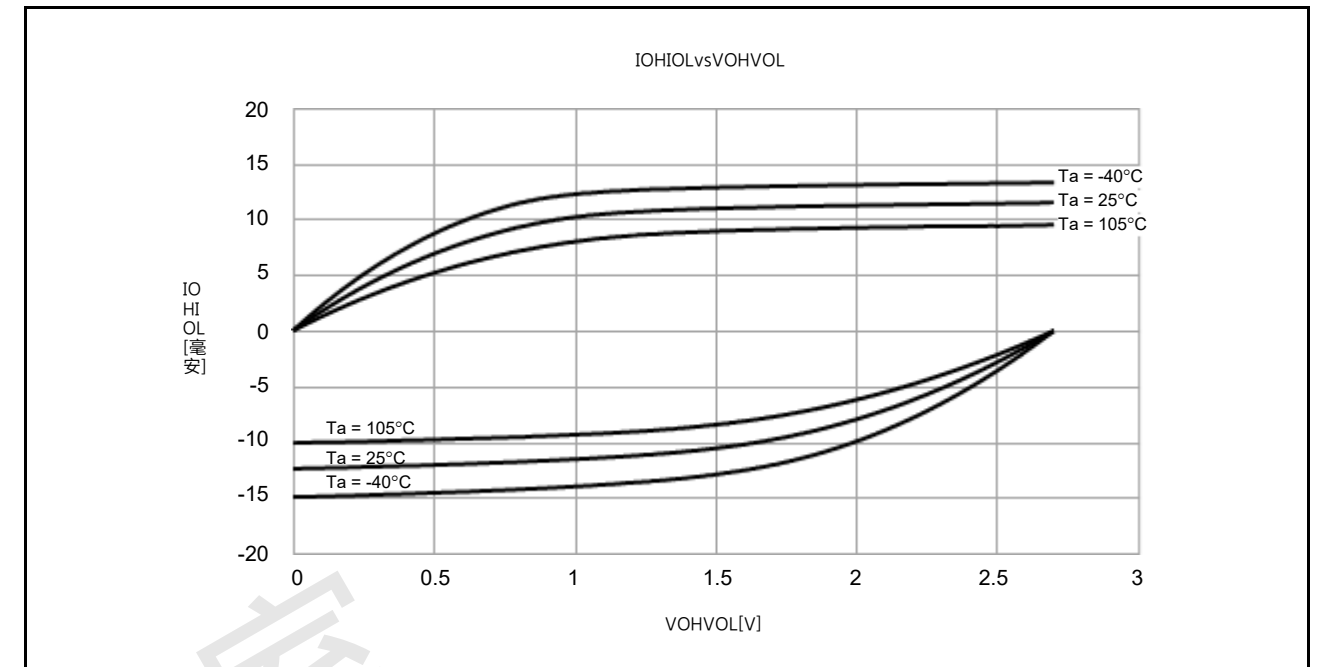


Figure 2.4 选择低驱动输出时， $VOHVOL$ 和 $IOHIOL$ 在 $V_{CC}=2.7V$ 时的温度特性（参考数据，P914和P915除外）

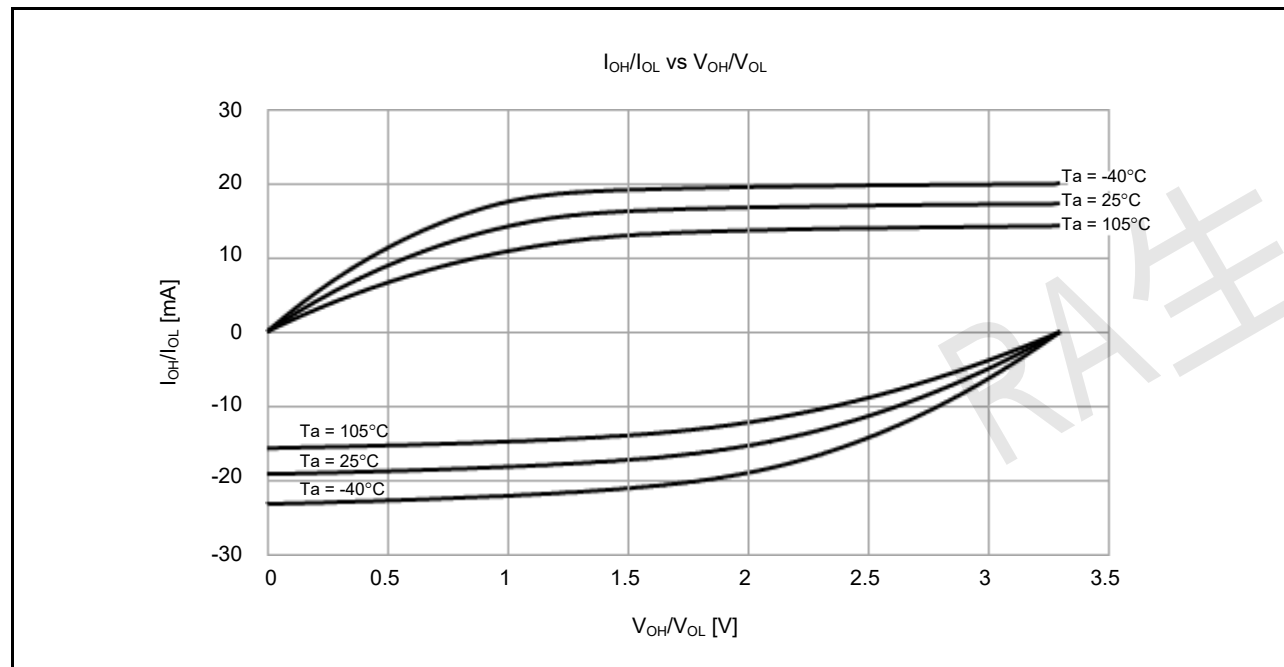


Figure 2.5  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.3\text{ V}$  when low drive output is selected (reference data, except for P914 and P915)

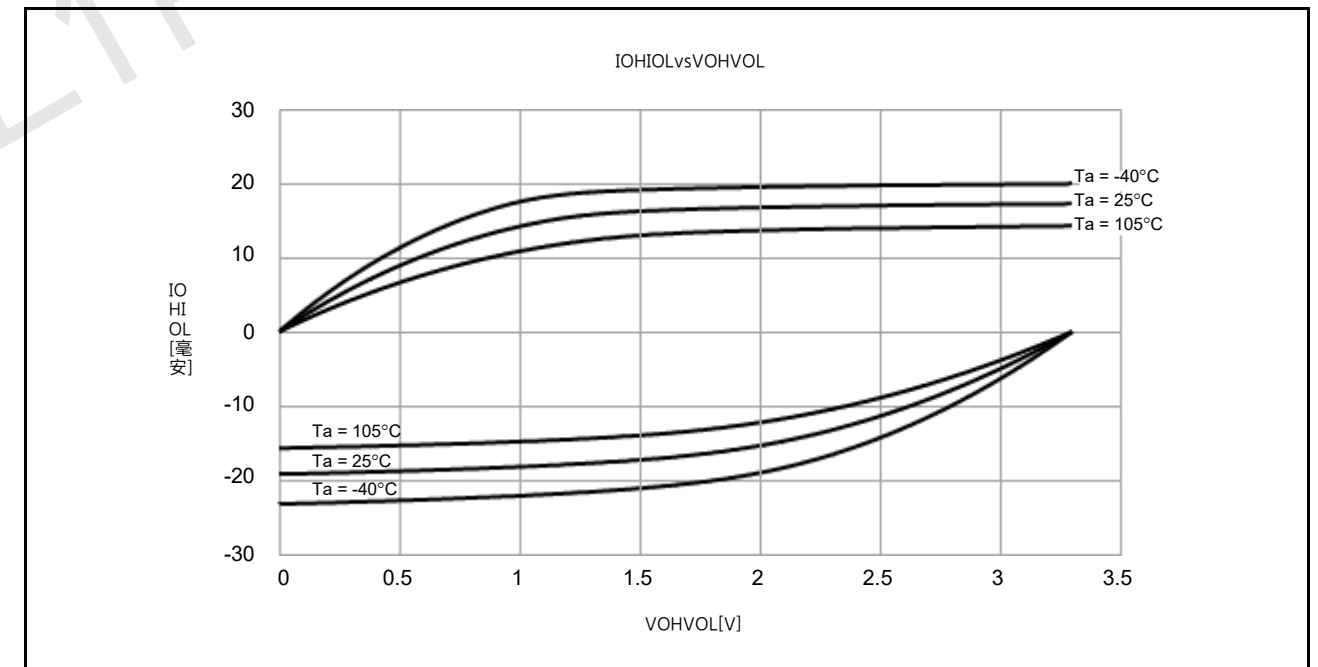


Figure 2.5 选择低驱动输出时， $VOHVOL$ 和 $IOHIOL$ 在 $V_{CC}=3.3V$ 时的温度特性（参考数据，P914和P915除外）



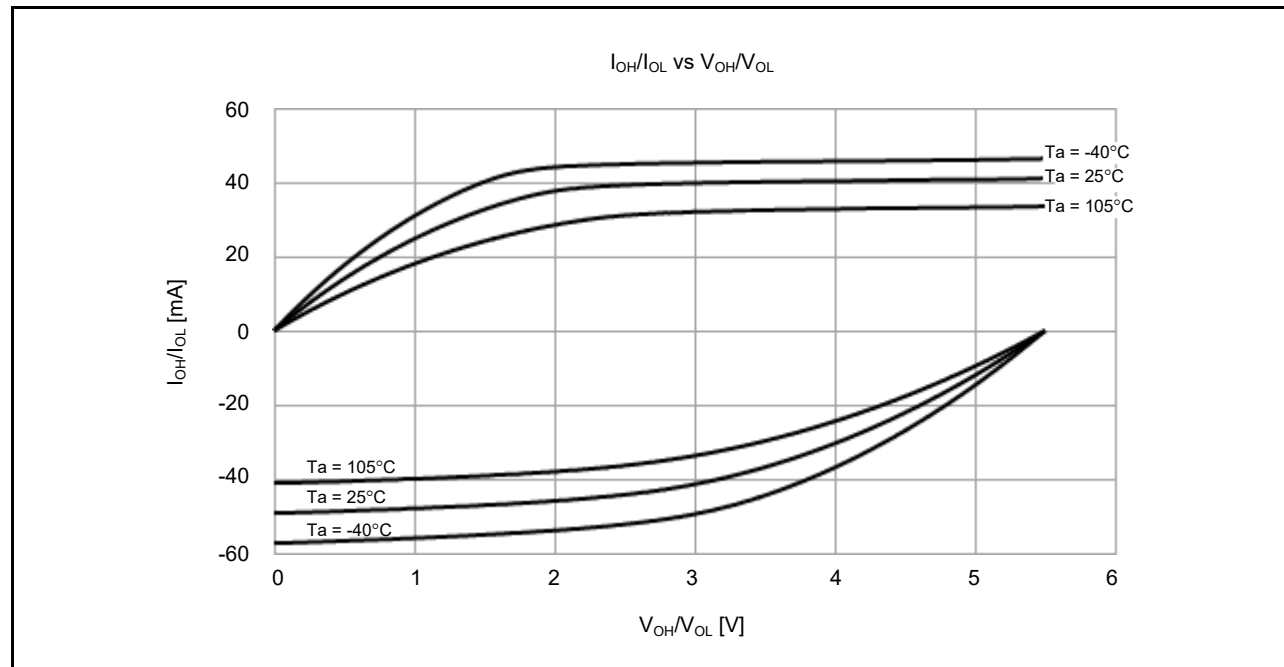


Figure 2.6  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 5.5\text{ V}$  when low drive output is selected (reference data, except for P914 and P915)

2.2.6 Output Characteristics for I/O Pins (Middle Drive Capacity)

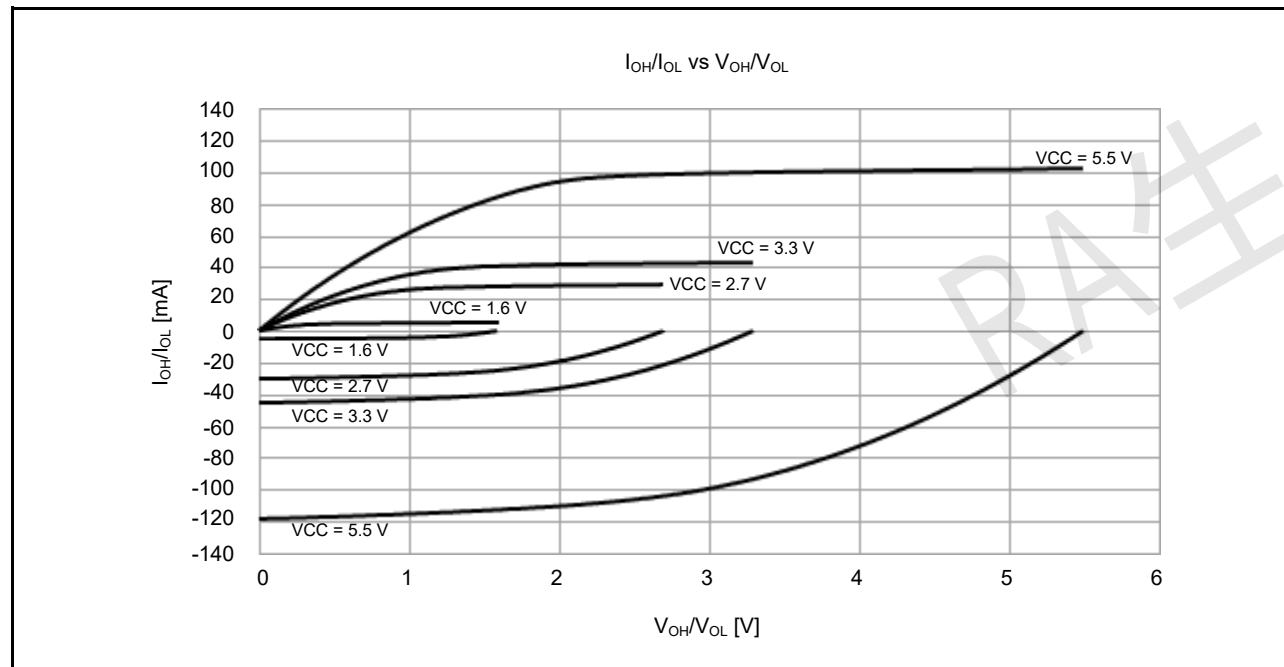


Figure 2.7  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when middle drive output is selected (reference data, except for P914 and P915)

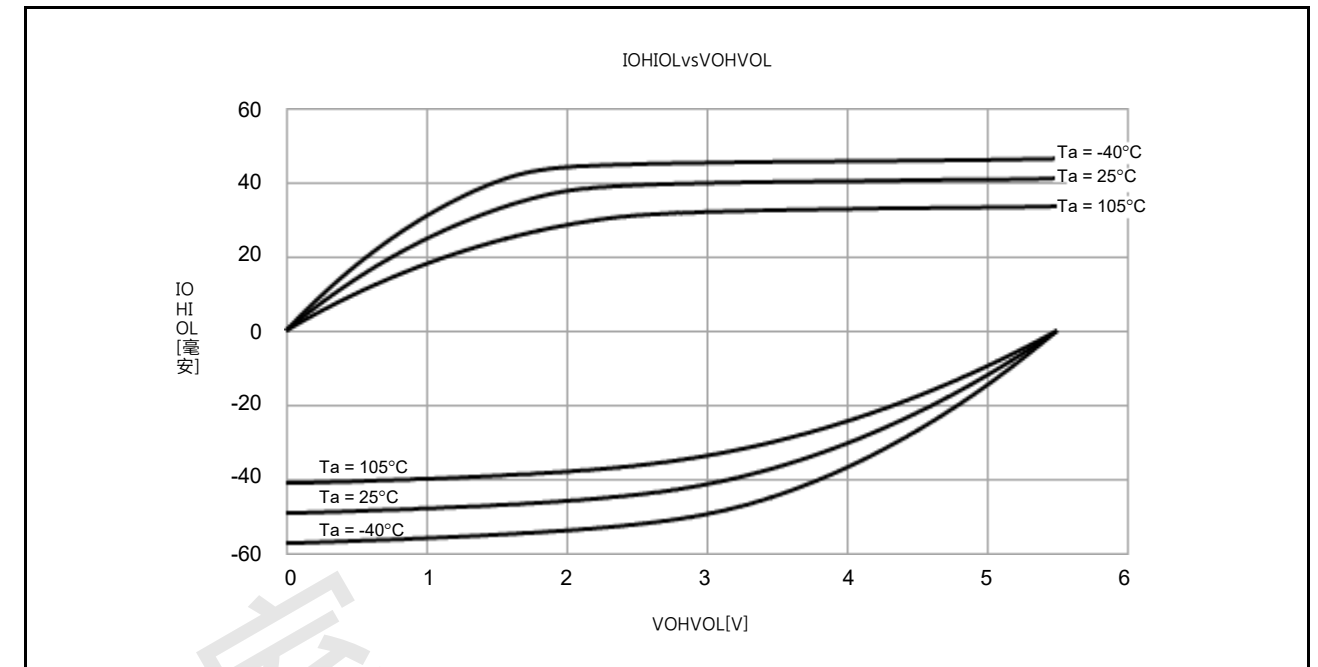


Figure 2.6 选择低驱动输出时， $V_{OHVOL}$ 和 $I_{OHVOL}$ 在 $V_{CC}=5.5\text{V}$ 时的温度特性（参考数据，P914和P915除外）

2.2.6 IO引脚的输出特性（中等驱动容量）

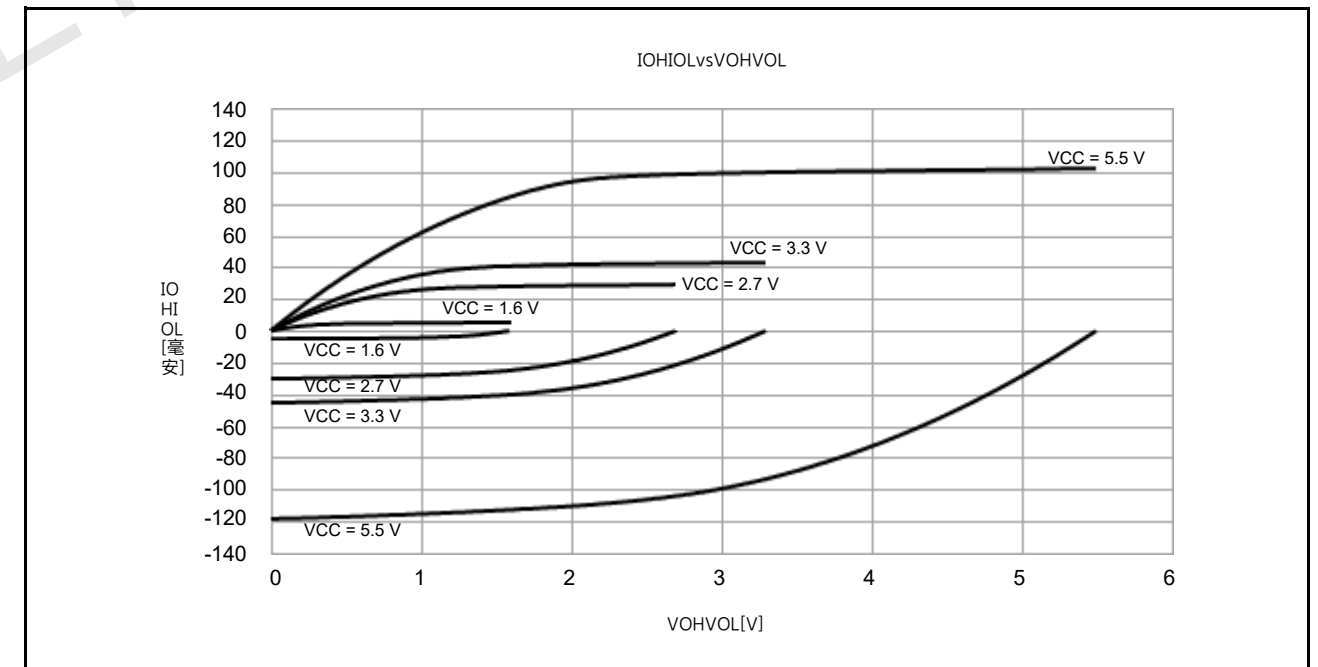


Figure 2.7 选择中间驱动输出时， $T_a=25^\circ\text{C}$ 时的 $V_{OHVOL}$ 和 $I_{OHVOL}$ 电压特性（参考数据，P914和P915除外）

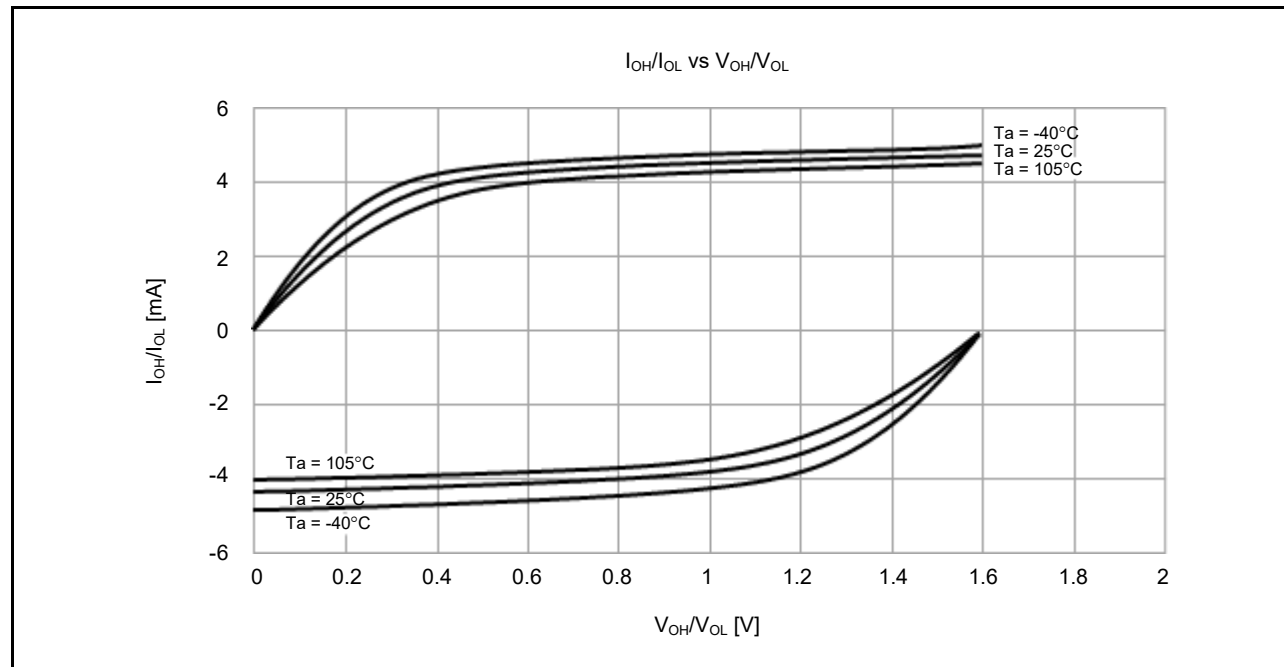


Figure 2.8  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 1.6\text{ V}$  when middle drive output is selected (reference data, except for P914 and P915)

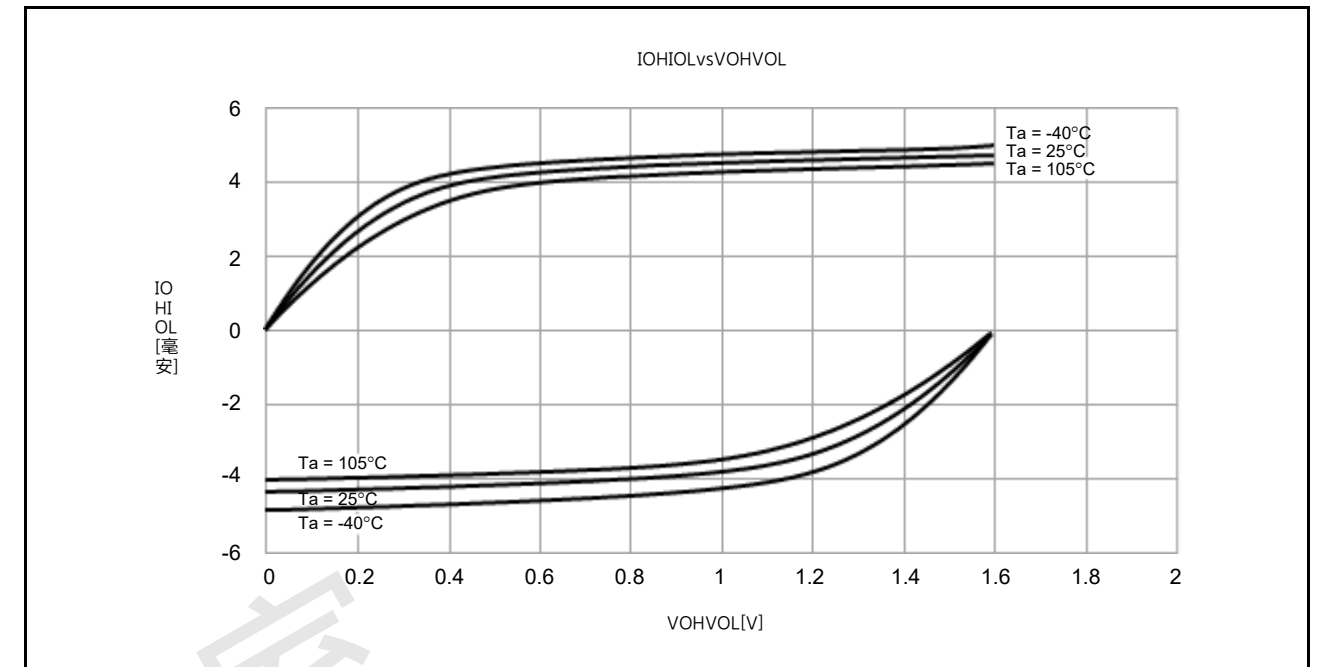


Figure 2.8  $VOHVOL$ 和 $IOH/IOL$ 选择中间驱动输出时 $V_{CC}=1.6V$ 时的温度特性 (参考数据, P914和P915除外)

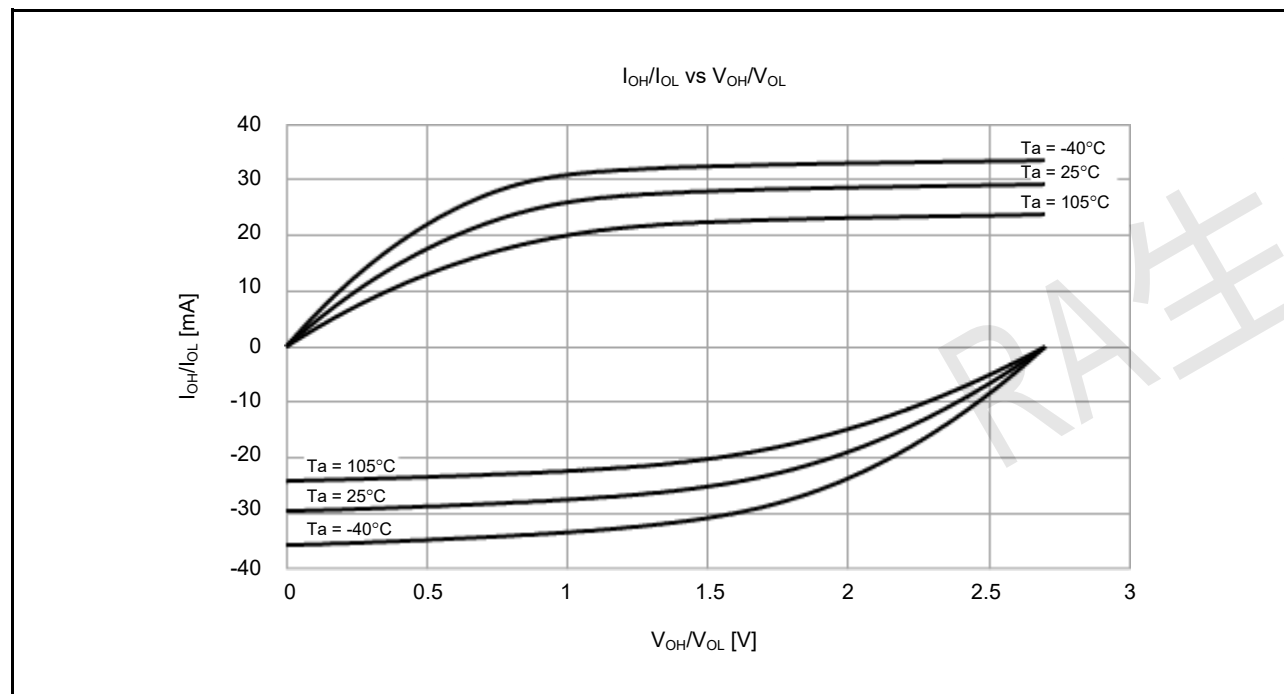


Figure 2.9  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7\text{ V}$  when middle drive output is selected (reference data, except for P914 and P915)

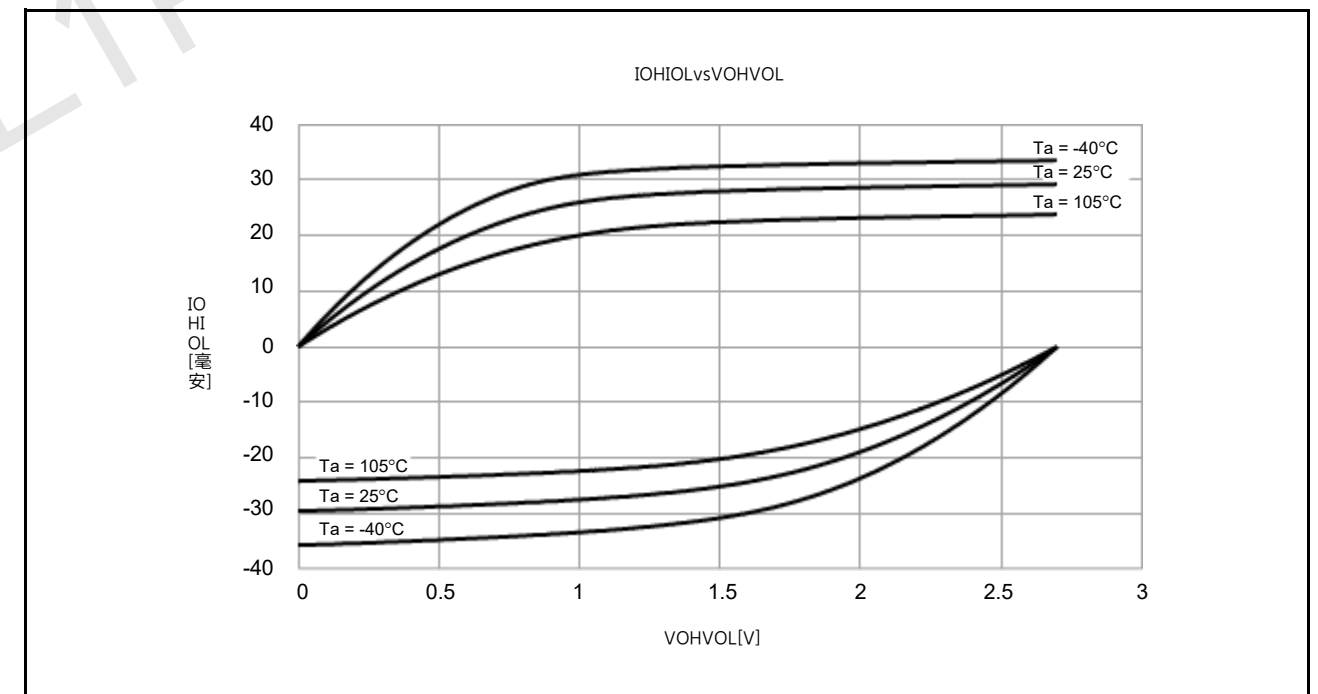


Figure 2.9 选择中间驱动输出时,  $VOHVOL$ 和 $IOH/IOL$ 在 $V_{CC}=2.7V$ 时的温度特性 (参考数据, P914和P915除外)

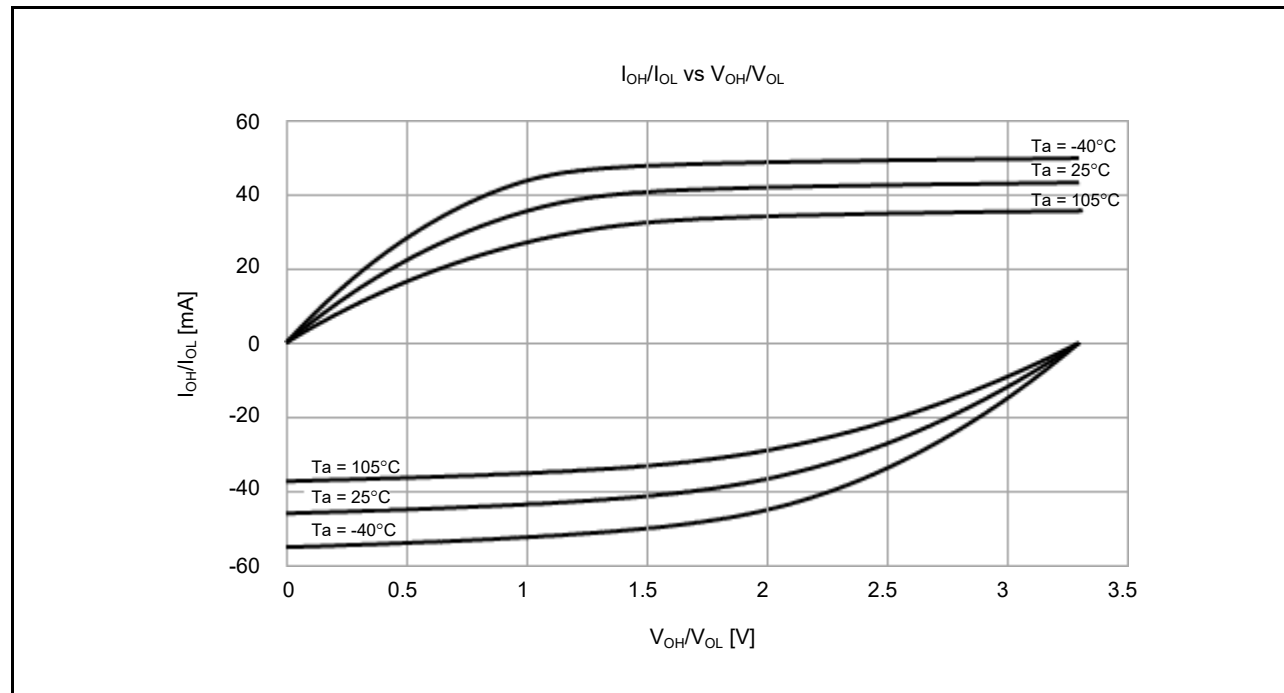


Figure 2.10  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.3\text{ V}$  when middle drive output is selected (reference data, except for P914 and P915)

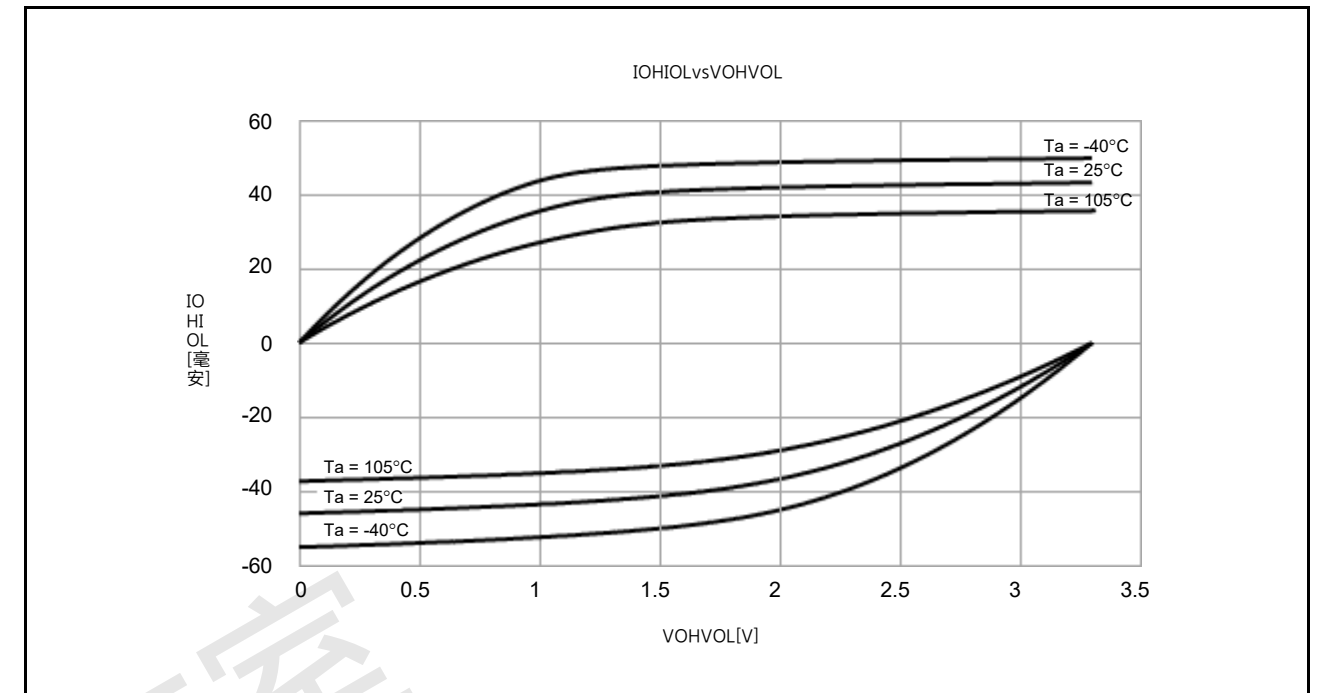


Figure 2.10 选择中间驱动输出时,  $VOHVOL$ 和 $IOHIOL$ 在 $V_{CC}=3.3\text{V}$ 时的温度特性 (参考数据, P914和P915除外)

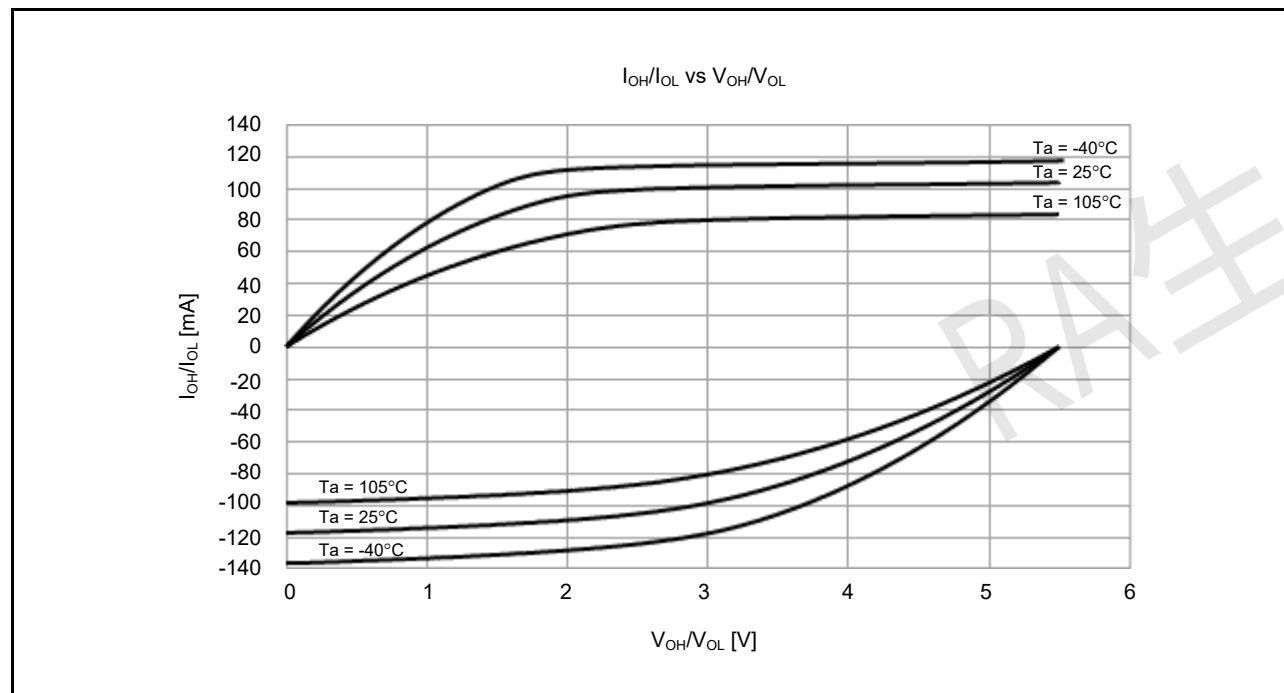


Figure 2.11  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 5.5\text{ V}$  when middle drive output is selected (reference data, except for P914 and P915)

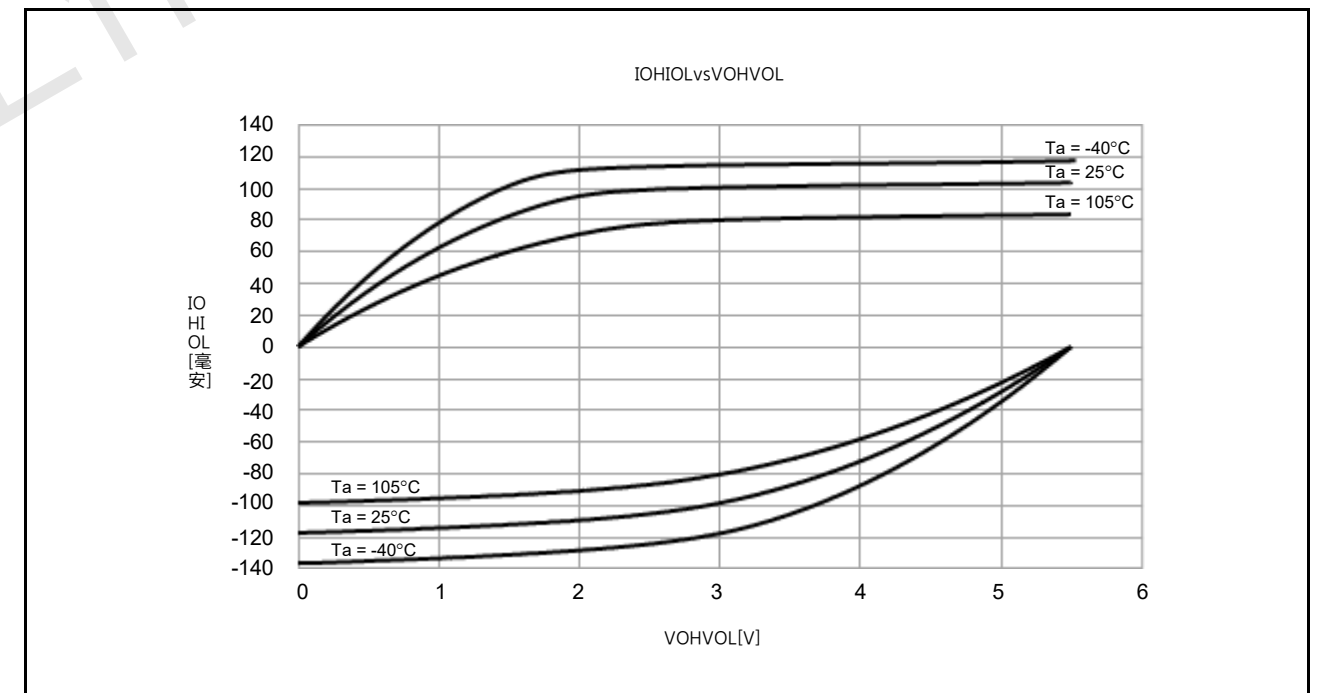


Figure 2.11 选择中间驱动输出时,  $VOHVOL$ 和 $IOHIOL$ 在 $V_{CC}=5.5\text{V}$ 时的温度特性 (参考数据, P914和P915除外)

2.2.7 Output Characteristics for P407, P408 and P409 I/O Pins (Middle Drive Capacity)

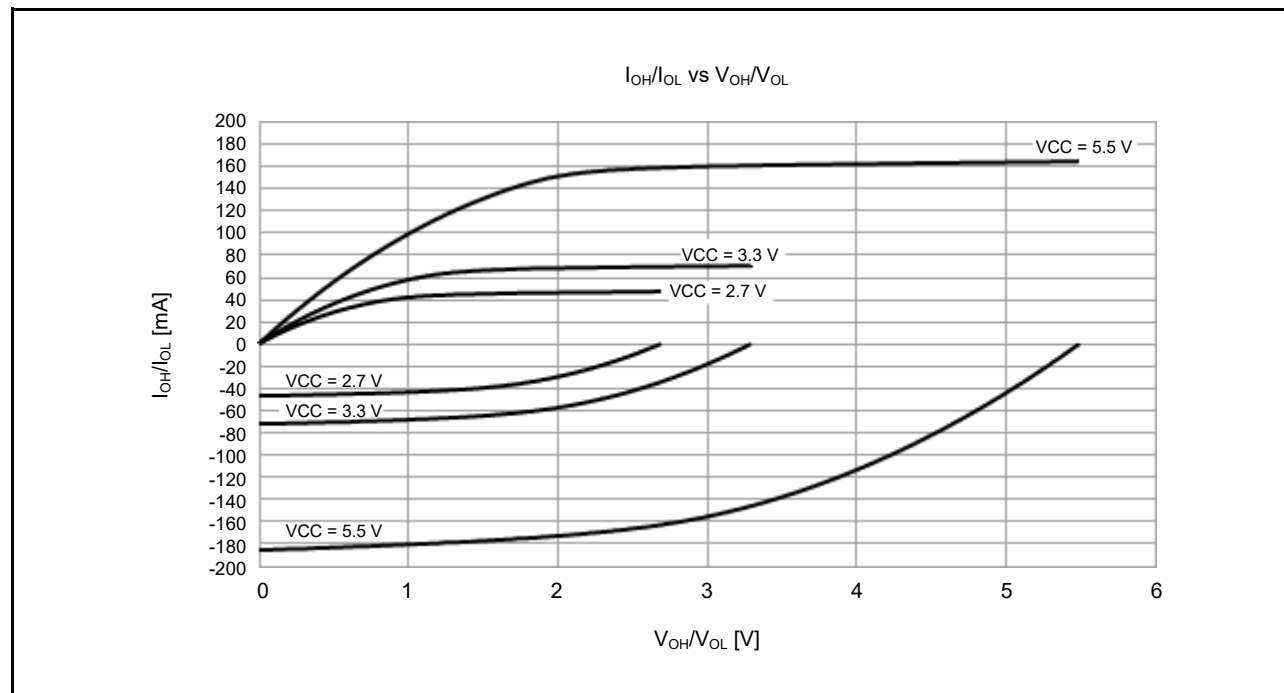


Figure 2.12  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when middle drive output is selected (reference data)

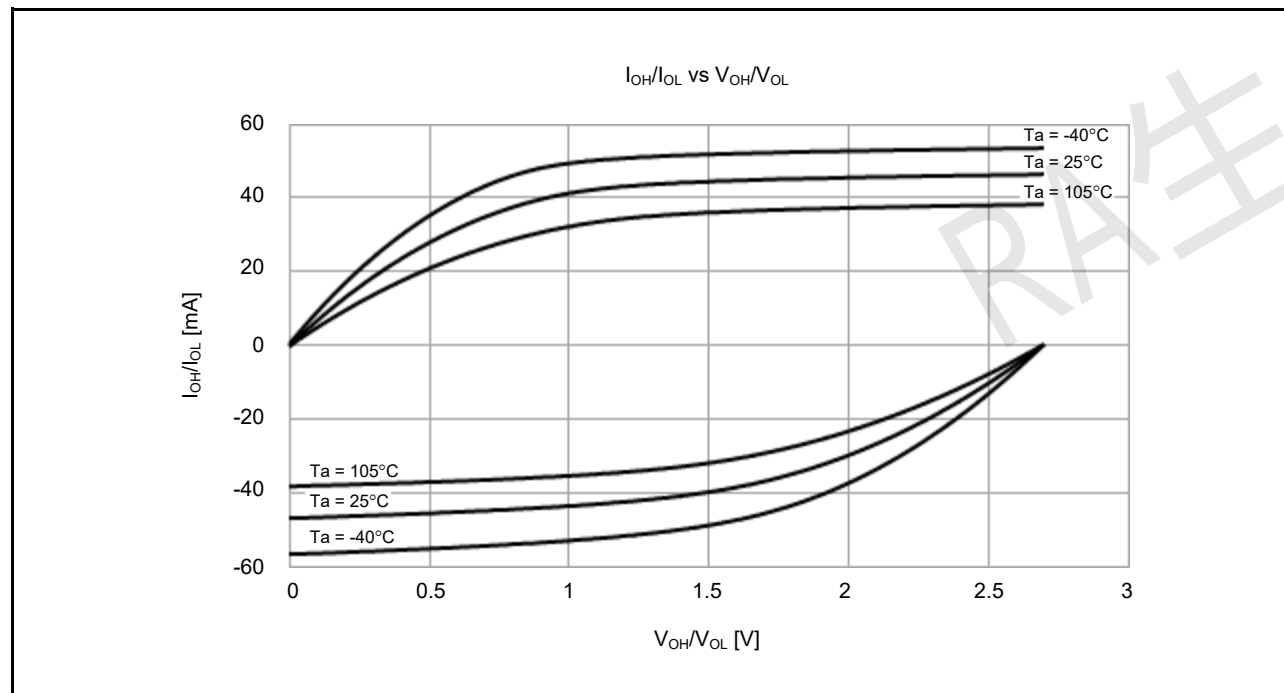


Figure 2.13  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7\text{V}$  when middle drive output is selected (reference data)

2.2.7 P407、P408和P409IO引脚的输出特性（中间驱动器）Capacity)

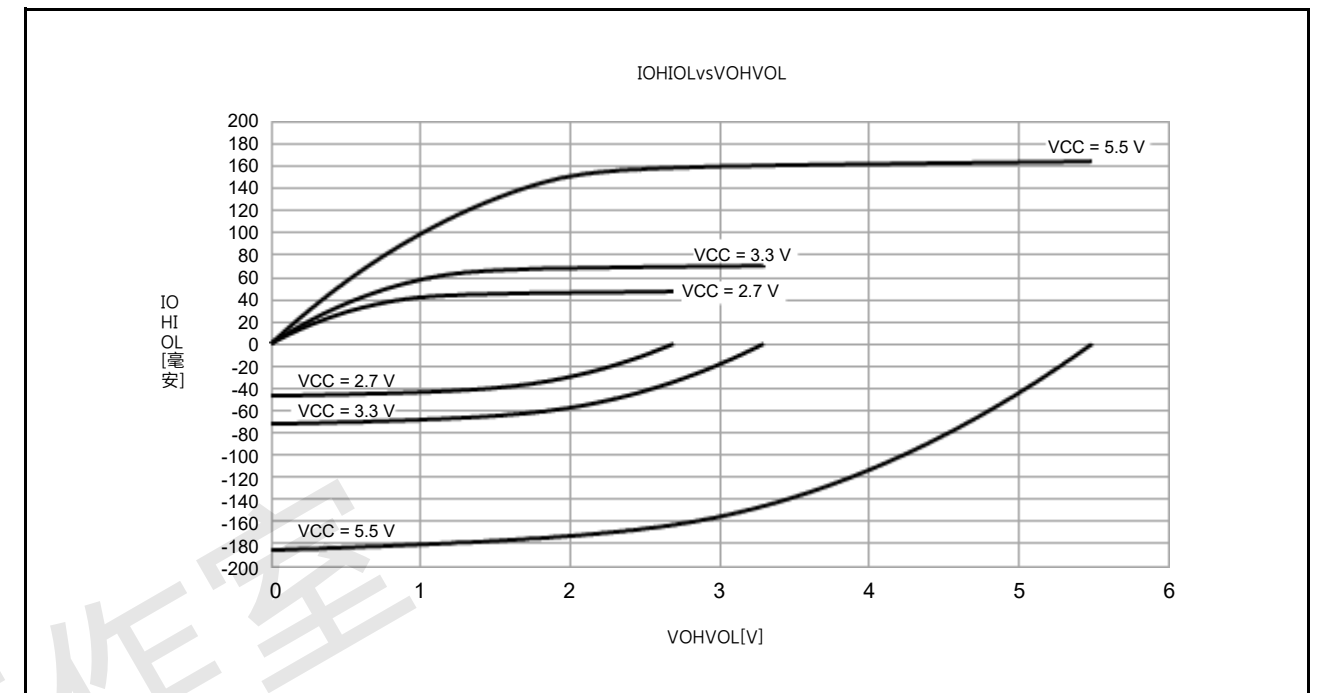


Figure 2.12 选择中间驱动输出时 $T_a=25^\circ\text{C}$ 时的 $V_{OH}/V_{OL}$ 和 $I_{OH}/I_{OL}$ 电压特性（参考数据）

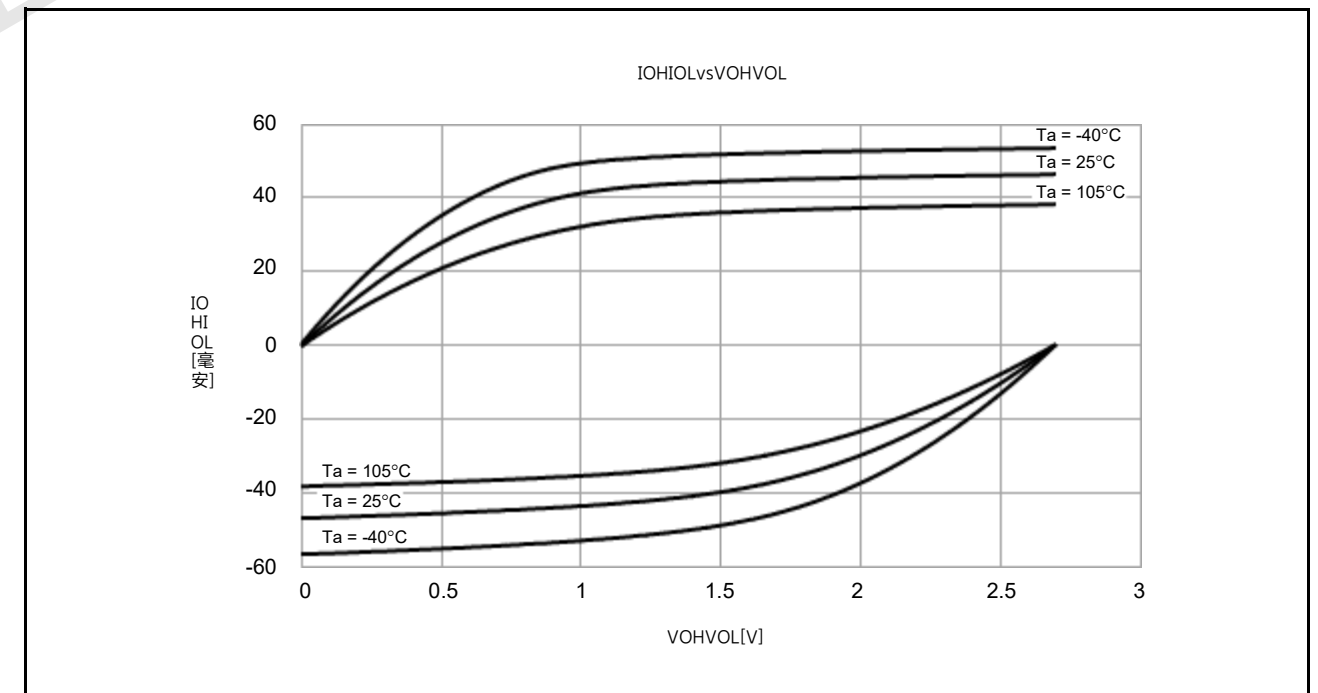


Figure 2.13 选择中间驱动输出时， $V_{CC}=2.7\text{V}$ 时的 $V_{OH}/V_{OL}$ 和 $I_{OH}/I_{OL}$ 温度特性（参考数据）

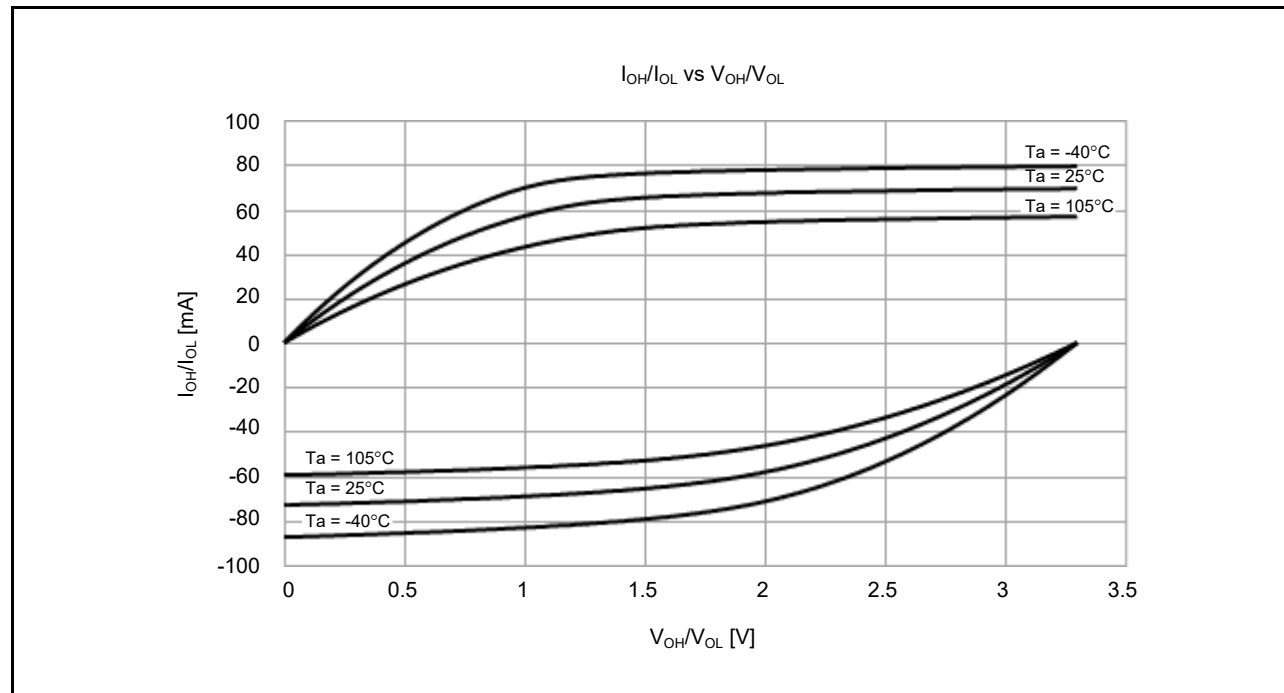


Figure 2.14  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.3\text{ V}$  when middle drive output is selected (reference data)

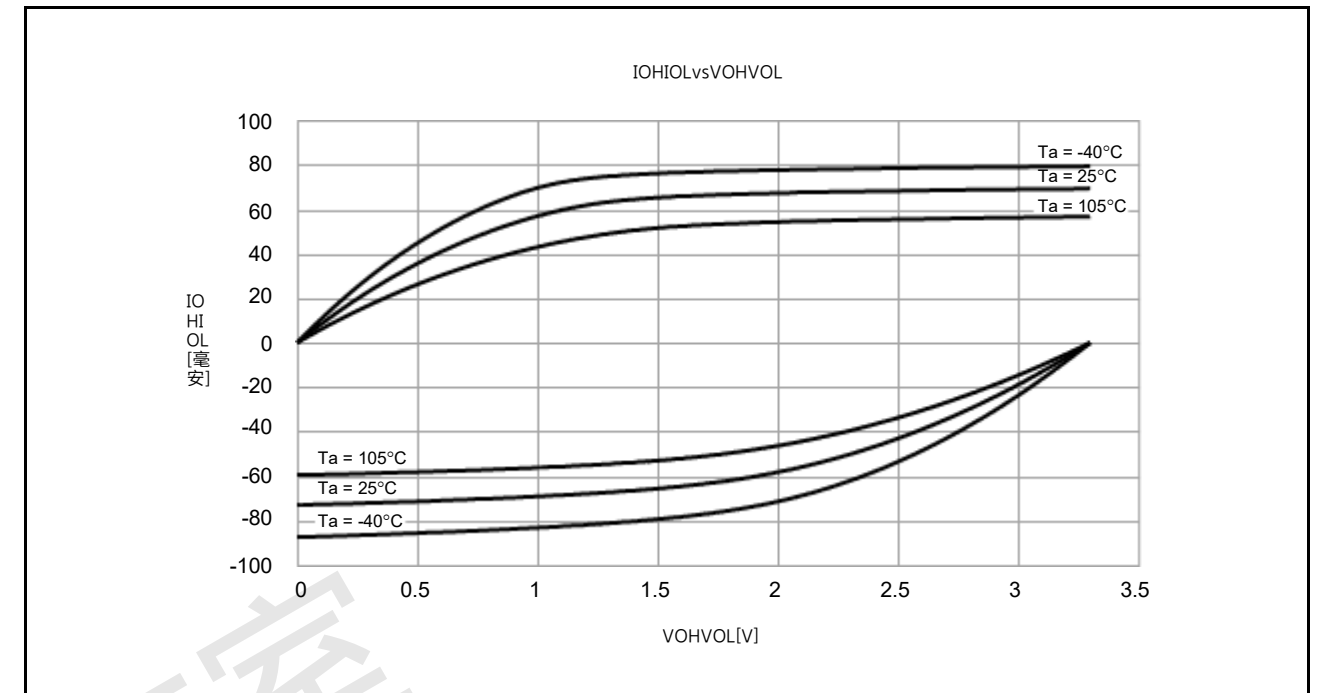


Figure 2.14 选择中间驱动输出时,  $V_{CC}=3.3\text{V}$ 时的 $V_{OHVOL}$ 和 $I_{OHVOL}$ 温度特性 (参考数据)

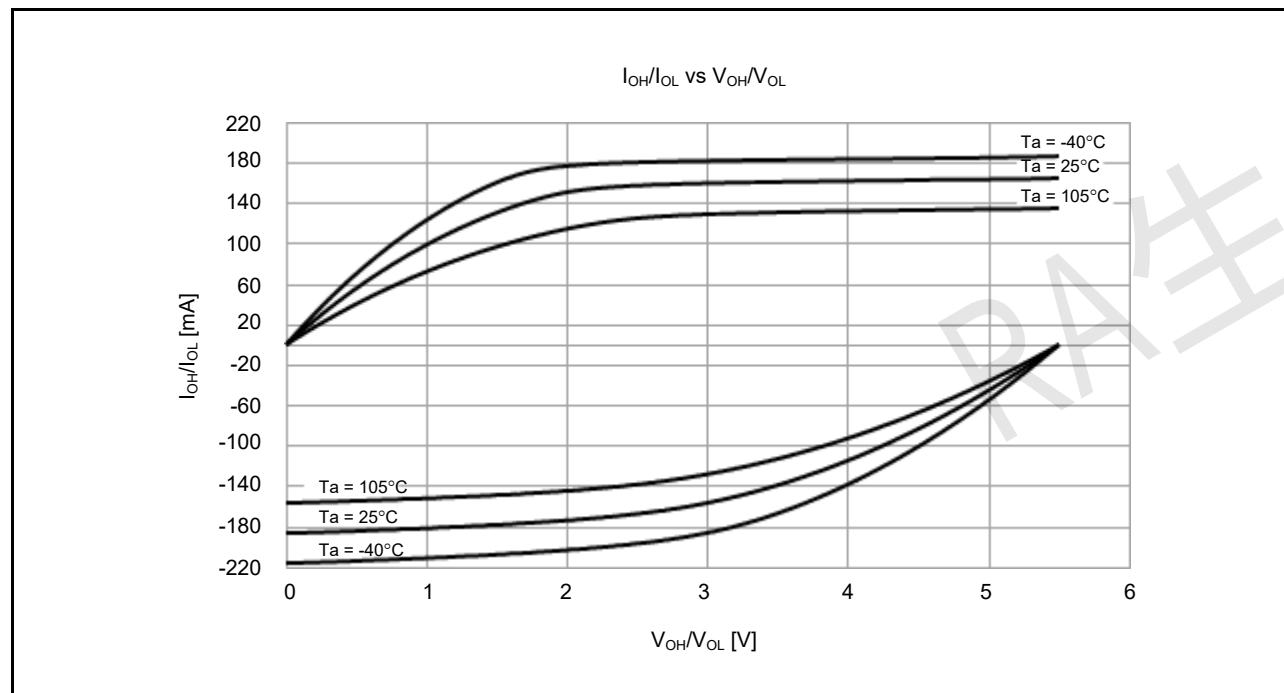


Figure 2.15  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 5.5\text{ V}$  when middle drive output is selected (reference data)

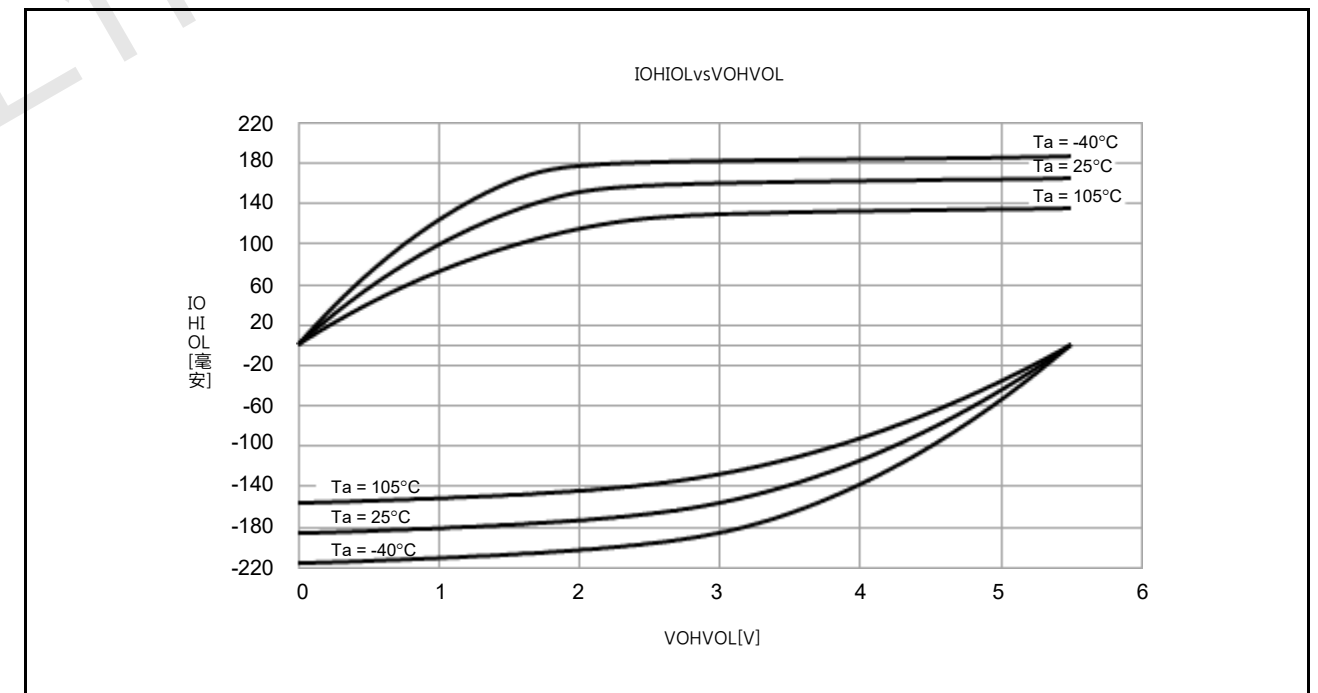


Figure 2.15 选择中间驱动输出时,  $V_{CC}=5.5\text{V}$ 时的 $V_{OHVOL}$ 和 $I_{OHVOL}$ 温度特性 (参考数据)



2.2.8 Output Characteristics for IIC I/O Pins

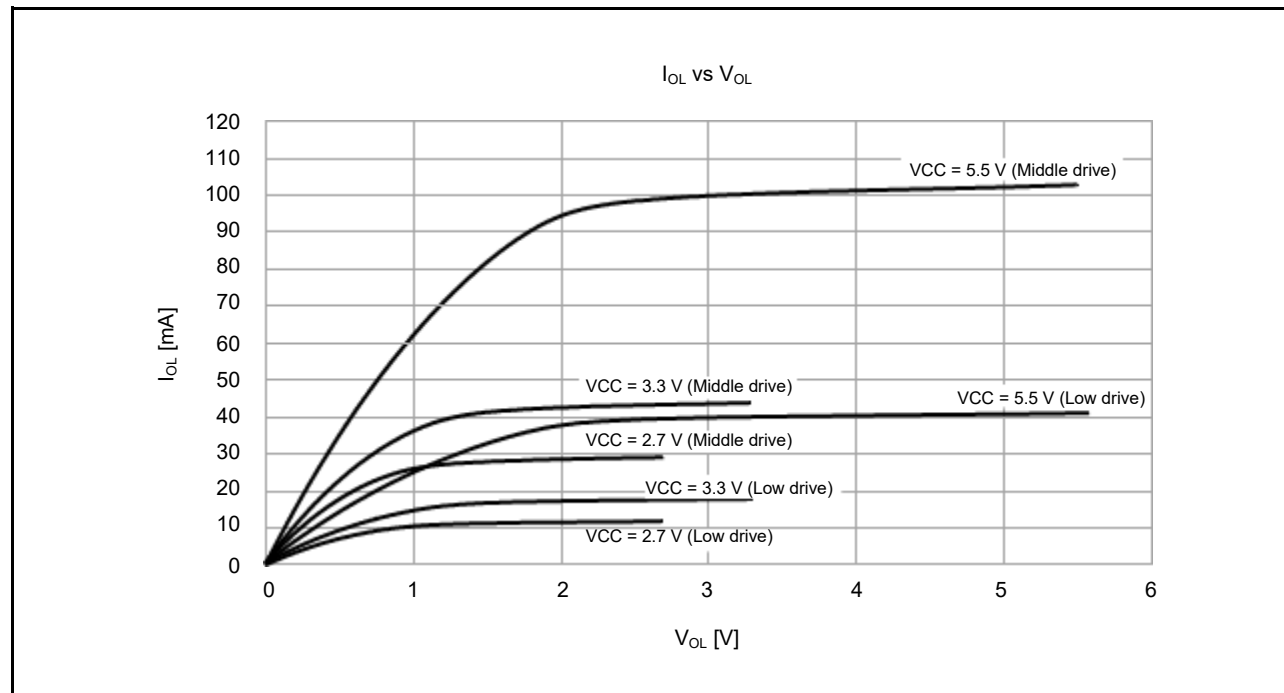


Figure 2.16  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$

2.2.8 IIC I/O引脚的输出特性

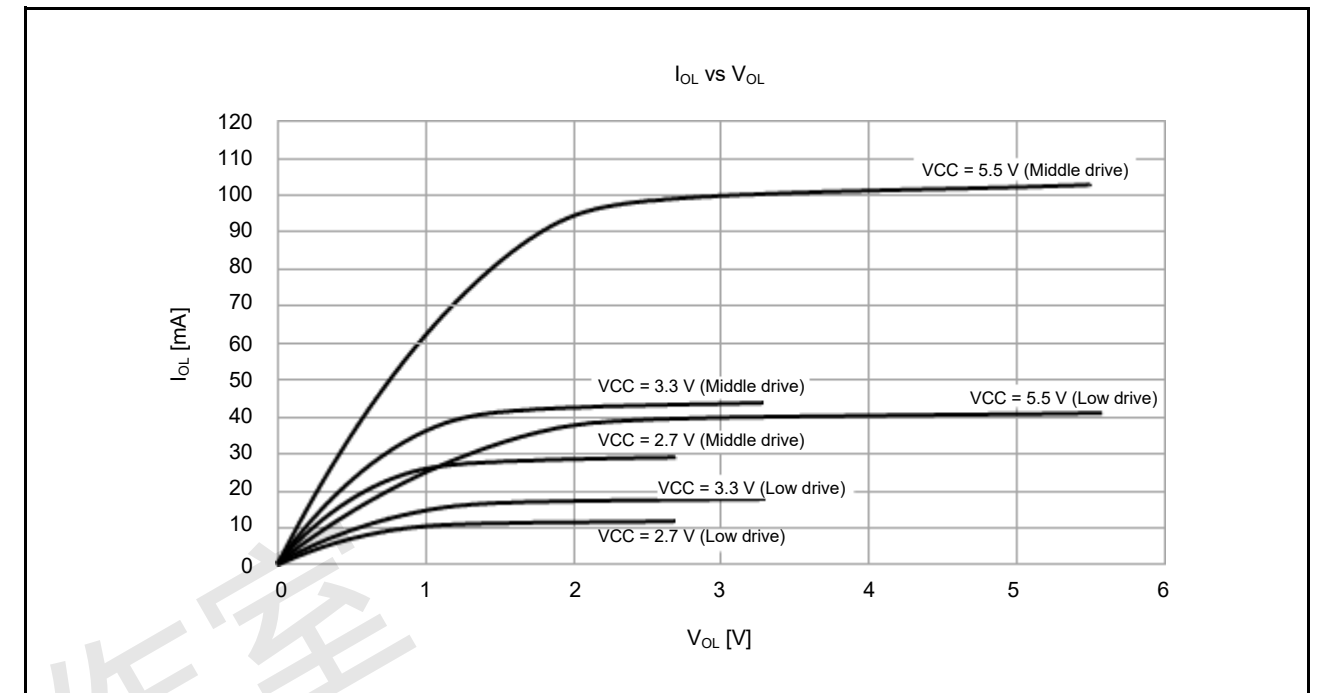


Figure 2.16  $T_a=25^\circ\text{C}$ 时的 $V_{OH}/V_{OL}$ 和 $I_{OH}/I_{OL}$ 电压特性

RA生态工作室

2.2.9 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Typ*10	Max	Unit	Test Conditions			
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 48 MHz	5.2	-	mA	*7, *11			
				ICLK = 32 MHz	3.8	-					
				ICLK = 16 MHz	2.3	-					
				ICLK = 8 MHz	1.6	-					
			All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz	12.1	-					
				ICLK = 32 MHz	8.3	-					
				ICLK = 16 MHz	4.6	-					
				ICLK = 8 MHz	2.8	-					
		All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 48 MHz	12.6	-	*9, *11					
			ICLK = 32 MHz	10.9	-	*8, *11					
			ICLK = 16 MHz	5.9	-						
			ICLK = 8 MHz	3.4	-						
		All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz	-	28.5	*9, *11					
			Sleep mode		All peripheral clocks disabled*5	ICLK = 48 MHz			2.7	-	*7
						ICLK = 32 MHz			2.1	-	
						ICLK = 16 MHz			1.5	-	
			ICLK = 8 MHz	1.1		-					
			All peripheral clocks enabled*5	ICLK = 48 MHz	9.8	-	*9				
				ICLK = 32 MHz	8.9	-	*8				
				ICLK = 16 MHz	5.0	-					
		ICLK = 8 MHz		2.9	-						
Increase during BGO operation*6					2.5	-	-				
Middle-speed mode*2	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 12 MHz	1.6	-	mA	*7, *11				
			ICLK = 8 MHz	1.3	-						
		All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 12 MHz	3.4	-						
			ICLK = 8 MHz	2.6	-						
		All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 12 MHz	4.3	-			*8, *11			
			ICLK = 8 MHz	3.1	-						
		All peripheral clocks enabled, code executing from flash*5	ICLK = 12 MHz	-	12.6						
			Sleep mode		All peripheral clocks disabled*5			ICLK = 12 MHz	1.0	-	*7
			ICLK = 8 MHz	0.9				-			
			All peripheral clocks enabled*5	ICLK = 12 MHz	3.6			-	*8		
				ICLK = 8 MHz	2.7			-			
	Increase during BGO operation*6							2.5	-	-	

2.2.9 工作和待机电流

Table 2.10 工作和待机电流(1)(1of2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Typ*10	Max	Unit	Test Conditions			
Supply current*1	High-speed mode*2	正常模式	禁用所有外设时钟, 同时(1)代码从闪存执行*5	ICLK = 48 MHz	5.2	-	mA	*7, *11			
				ICLK = 32 MHz	3.8	-					
				ICLK = 16 MHz	2.3	-					
				ICLK = 8 MHz	1.6	-					
			禁用所有外设时钟, CoreMark代码从闪存执行*5	ICLK = 48 MHz	12.1	-					
				ICLK = 32 MHz	8.3	-					
				ICLK = 16 MHz	4.6	-					
				ICLK = 8 MHz	2.8	-					
		启用所有外设时钟, 同时(1)代码从闪存执行*5	ICLK = 48 MHz	12.6	-	*9, *11					
			ICLK = 32 MHz	10.9	-	*8, *11					
			ICLK = 16 MHz	5.9	-						
			ICLK = 8 MHz	3.4	-						
		启用所有外设时钟, 从闪存执行代码*5	ICLK = 48 MHz	-	28.5	*9, *11					
			睡眠模式		禁用所有外设时钟*5	ICLK = 48 MHz			2.7	-	*7
						ICLK = 32 MHz			2.1	-	
						ICLK = 16 MHz			1.5	-	
			ICLK = 8 MHz	1.1		-					
			启用所有外设时钟*5	ICLK = 48 MHz	9.8	-	*9				
				ICLK = 32 MHz	8.9	-	*8				
				ICLK = 16 MHz	5.0	-					
		ICLK = 8 MHz		2.9	-						
BGO运行时增加*6					2.5	-	-				
Middle-speed mode*2	正常模式	禁用所有外设时钟, 同时(1)代码从闪存执行*5	ICLK = 12 MHz	1.6	-	mA	*7, *11				
			ICLK = 8 MHz	1.3	-						
		禁用所有外设时钟, CoreMark代码从闪存执行*5	ICLK = 12 MHz	3.4	-						
			ICLK = 8 MHz	2.6	-						
		启用所有外设时钟, 同时(1)代码从闪存执行*5	ICLK = 12 MHz	4.3	-			*8, *11			
			ICLK = 8 MHz	3.1	-						
		启用所有外设时钟, 从闪存执行代码*5	ICLK = 12 MHz	-	12.6						
			睡眠模式		禁用所有外设时钟*5			ICLK = 12 MHz	1.0	-	*7
			ICLK = 8 MHz	0.9				-			
			启用所有外设时钟*5	ICLK = 12 MHz	3.6			-	*8		
				ICLK = 8 MHz	2.7			-			
	BGO运行时增加*6							2.5	-	-	

**Table 2.10 Operating and standby current (1) (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Typ*10	Max	Unit	Test Conditions	
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICC	0.3	-	mA	*7, *11	
			All peripheral clocks disabled, CoreMark code executing from flash*5		0.4	-			
			All peripheral clocks enabled, while (1) code executing from flash*5		0.5	-			
			All peripheral clocks enabled, code executing from flash*5		-	2.5			
		Sleep mode	All peripheral clocks disabled*5		0.2	-	*7		
			All peripheral clocks enabled*5		0.4	-	*8		
		Low-voltage mode*3	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICC	1.5	-	mA	*7, *11
				All peripheral clocks disabled, CoreMark code executing from flash*5		2.2	-		
	All peripheral clocks enabled, while (1) code executing from flash*5				2.5	-			
	All peripheral clocks enabled, code executing from flash*5				-	7.0			
Sleep mode	All peripheral clocks disabled*5			1.3	-	*7			
	All peripheral clocks enabled*5			2.3	-	*8			
Subosc-speed mode*4	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICC	6.5	-	μA	*8, *11		
		All peripheral clocks enabled, while (1) code executing from flash*5		12.1	-				
		All peripheral clocks enabled, code executing from flash*5		-	190.0				
		All peripheral clocks disabled*5		4.5	-			*8	
	Sleep mode	All peripheral clocks enabled*5		10.2	-	*8			

- Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
- Note 2. The clock source is HOCO.
- Note 3. The clock source is MOCO.
- Note 4. The clock source is the sub-clock oscillator.
- Note 5. This does not include BGO operation.
- Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
- Note 7. FCLK, PCLKB, and PCLKD are set to divided by 64.
- Note 8. FCLK, PCLKB, and PCLKD are the same frequency as that of ICLK.
- Note 9. FCLK and PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
- Note 10. VCC = 3.3 V.
- Note 11. The flash cache is operating.

**Table 2.10 工作和待机电流(1)(2of2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Typ*10	Max	Unit	Test Conditions	
Supply current*1	Low-speed mode*3	正常模式	禁用所有外设时钟, 同时(1)代码从闪存执行*5	ICC	0.3	-	mA	*7, *11	
			禁用所有外设时钟, CoreMark代码从闪存执行*5		0.4	-			
			启用所有外设时钟, 同时(1)代码从闪存执行*5		0.5	-			
			启用所有外设时钟, 从闪存执行代码*5		-	2.5			
		睡眠模式	禁用所有外设时钟*5		0.2	-	*7		
			启用所有外设时钟*5		0.4	-	*8		
		Low-voltage mode*3	正常模式	禁用所有外设时钟, 同时(1)代码从闪存执行*5	ICC	1.5	-	mA	*7, *11
				禁用所有外设时钟, CoreMark代码从闪存执行*5		2.2	-		
	启用所有外设时钟, 同时(1)代码从闪存执行*5				2.5	-			
	启用所有外设时钟, 从闪存执行代码*5				-	7.0			
睡眠模式	禁用所有外设时钟*5			1.3	-	*7			
	启用所有外设时钟*5			2.3	-	*8			
Subosc-speed mode*4	正常模式	禁用所有外设时钟, 同时(1)代码从闪存执行*5	ICC	6.5	-	μA	*8, *11		
		启用所有外设时钟, 同时(1)代码从闪存执行*5		12.1	-				
		启用所有外设时钟, 从闪存执行代码*5		-	190.0				
		禁用所有外设时钟*5		4.5	-			*8	
	睡眠模式	启用所有外设时钟*5		10.2	-	*8			

- Note 1. 电源电流值不包括所有引脚的输出充电放电电流。这些值适用于内部上拉时 MOS处于关闭状态。
- Note 2. 时钟源是HOCO。
- Note 3. 时钟源为MOCO。
- Note 4. 时钟源是子时钟振荡器。
- Note 5. 这包括BGO操作。
- Note 6. 这是在程序执行期间用于数据存储的闪存的编程或擦除的增加。
- Note 7. FCLK、PCLKB和PCLKD设置为64分频。
- Note 8. FCLK、PCLKB和PCLKD的频率与ICLK的频率相同。
- Note 9. FCLK和PCLKB设置为2分频, P CLKD与ICLK的频率相同。
- Note 10. VCC = 3.3 V.
- 注11. 闪存缓存正在运行。

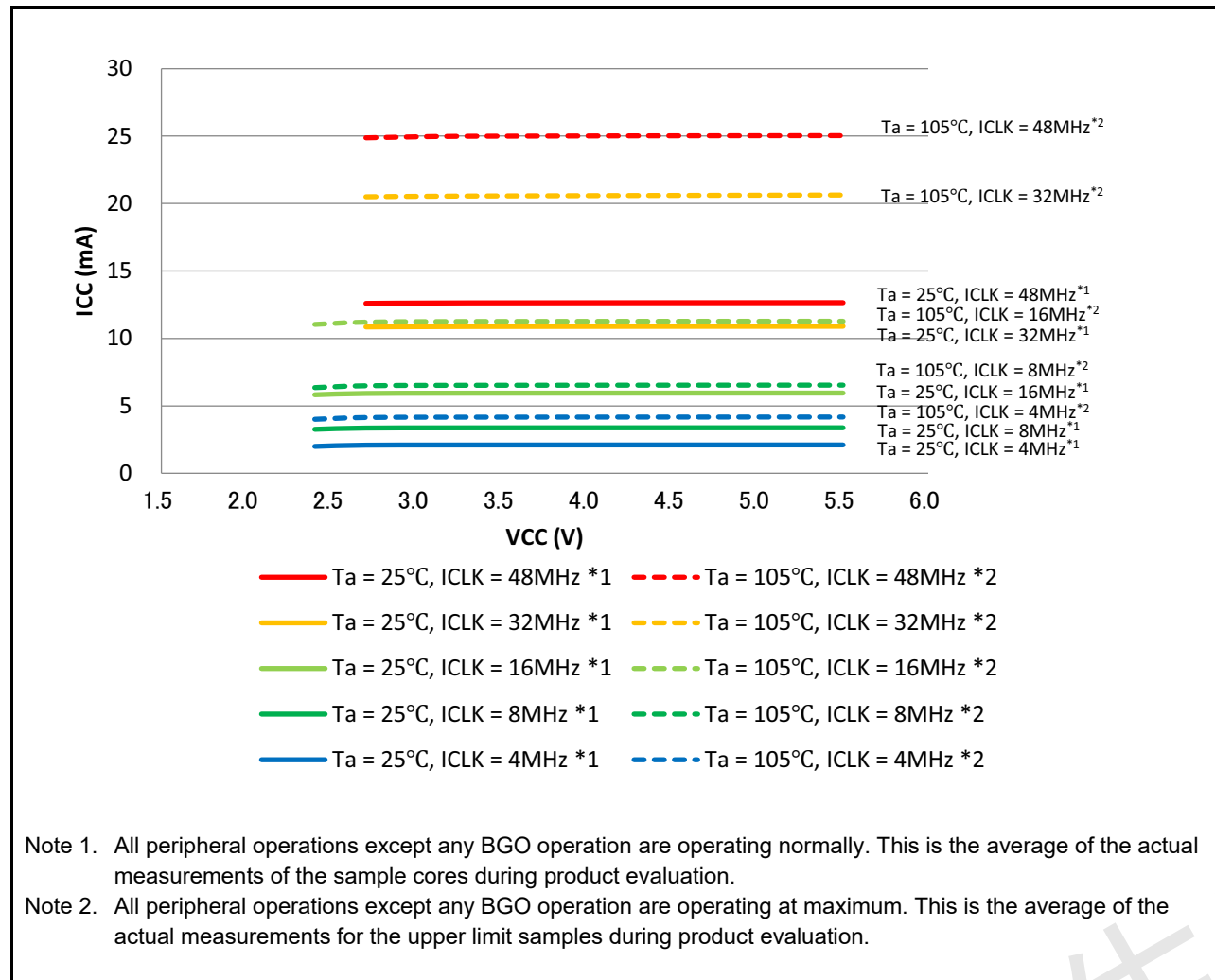


Figure 2.17 Voltage dependency in high-speed operating mode (reference data)

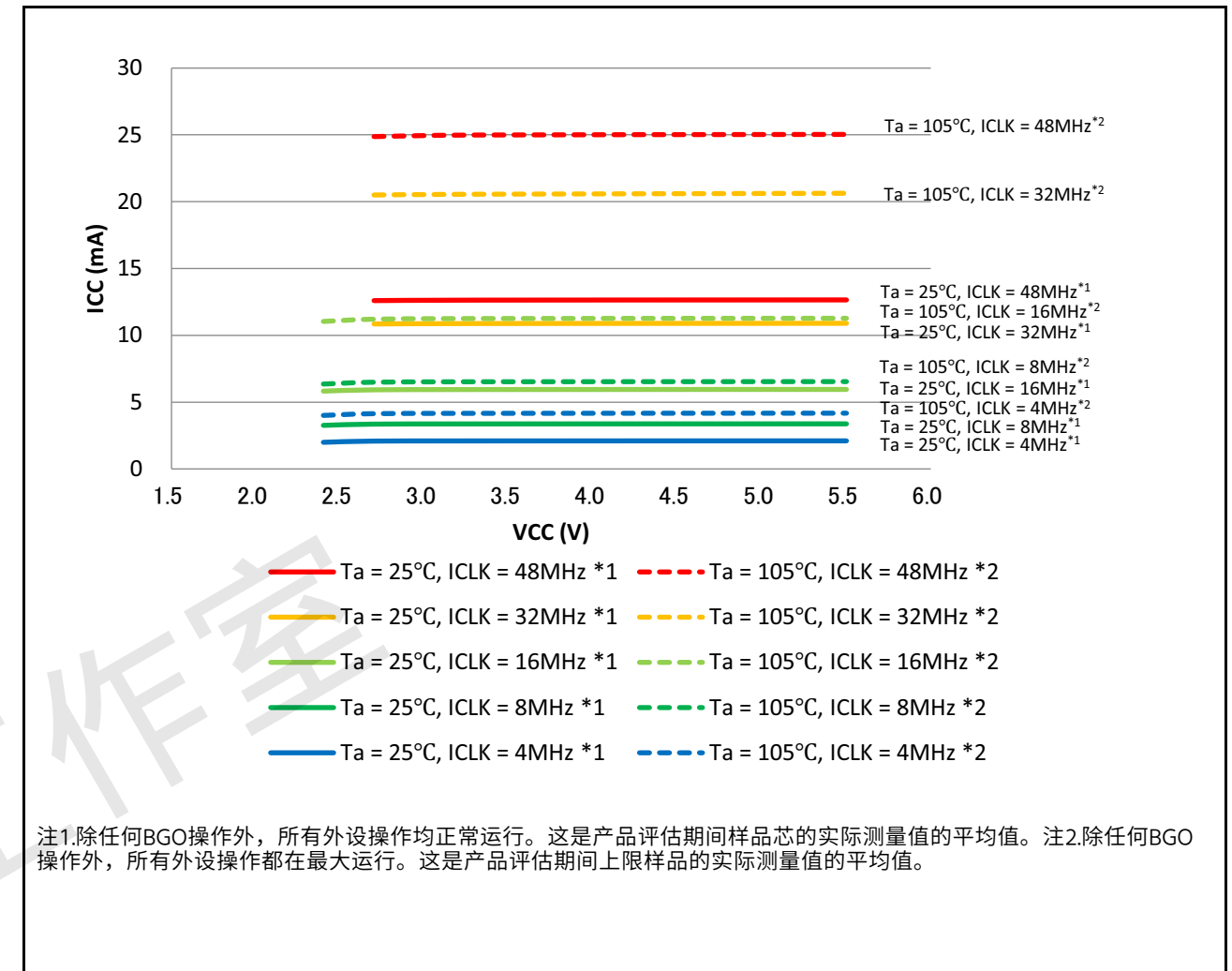


Figure 2.17 高速运行模式下的电压依赖性 (参考数据)

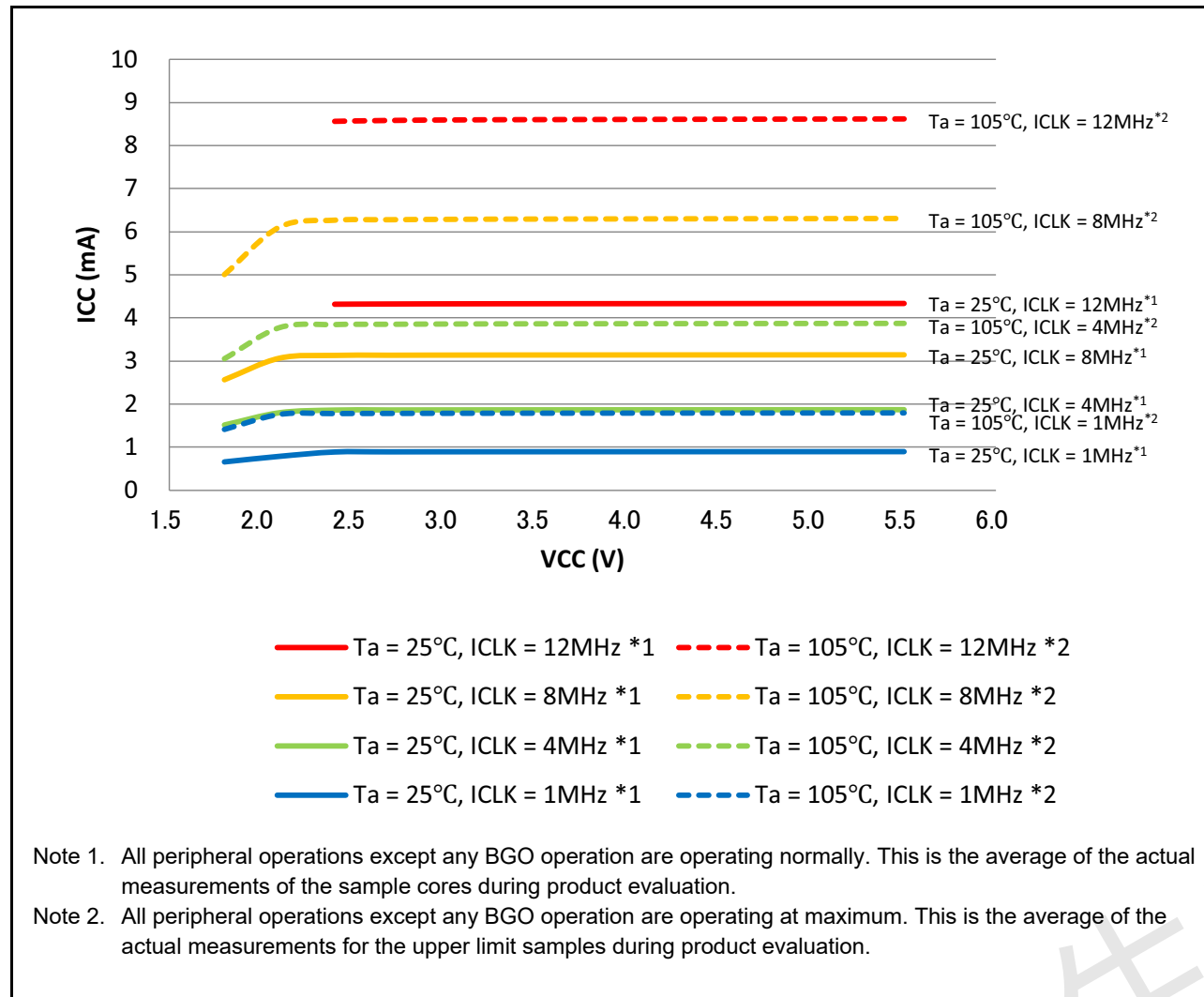


Figure 2.18 Voltage dependency in middle-speed operating mode (reference data)

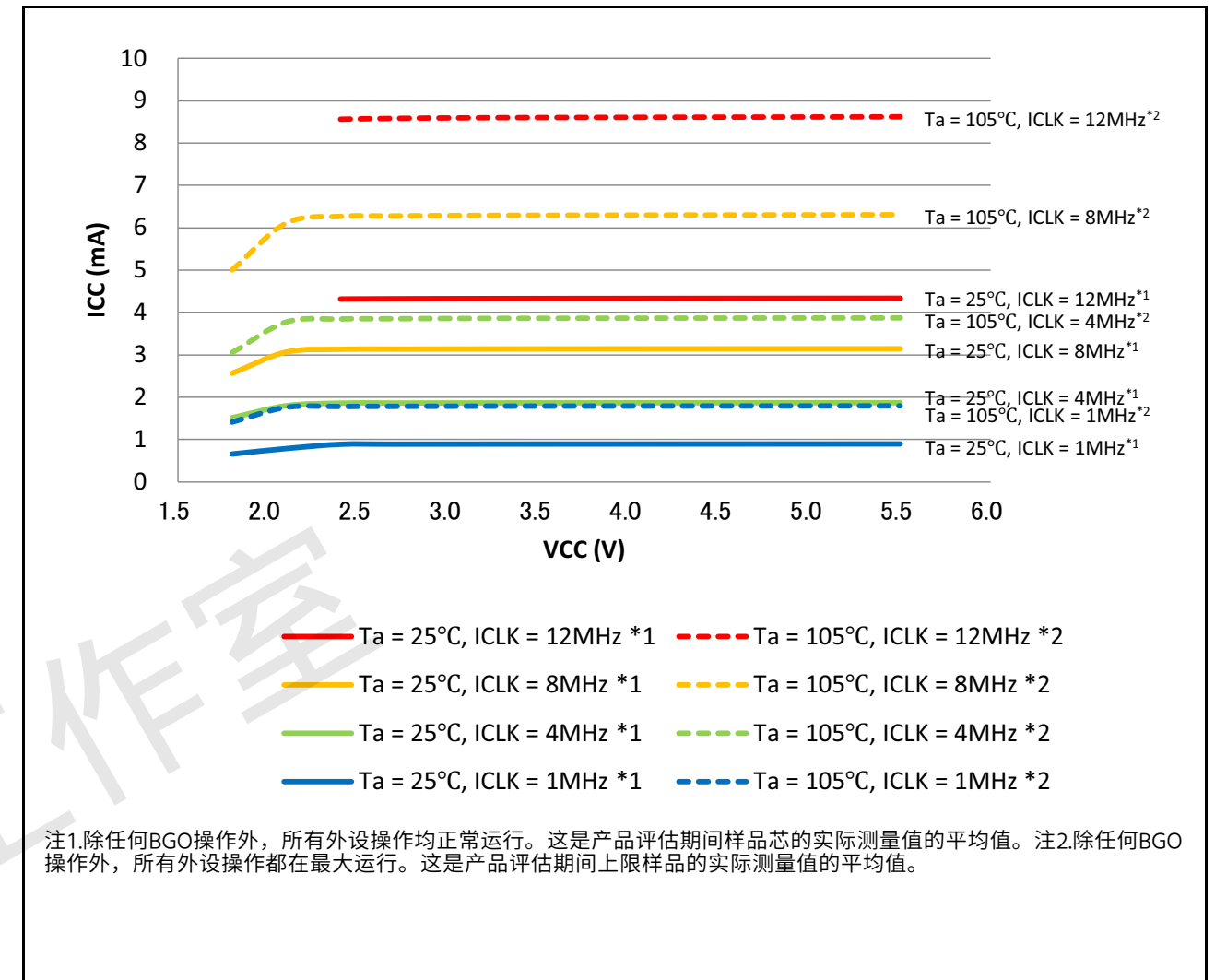


Figure 2.18 中速运行模式下的电压依赖性 (参考数据)



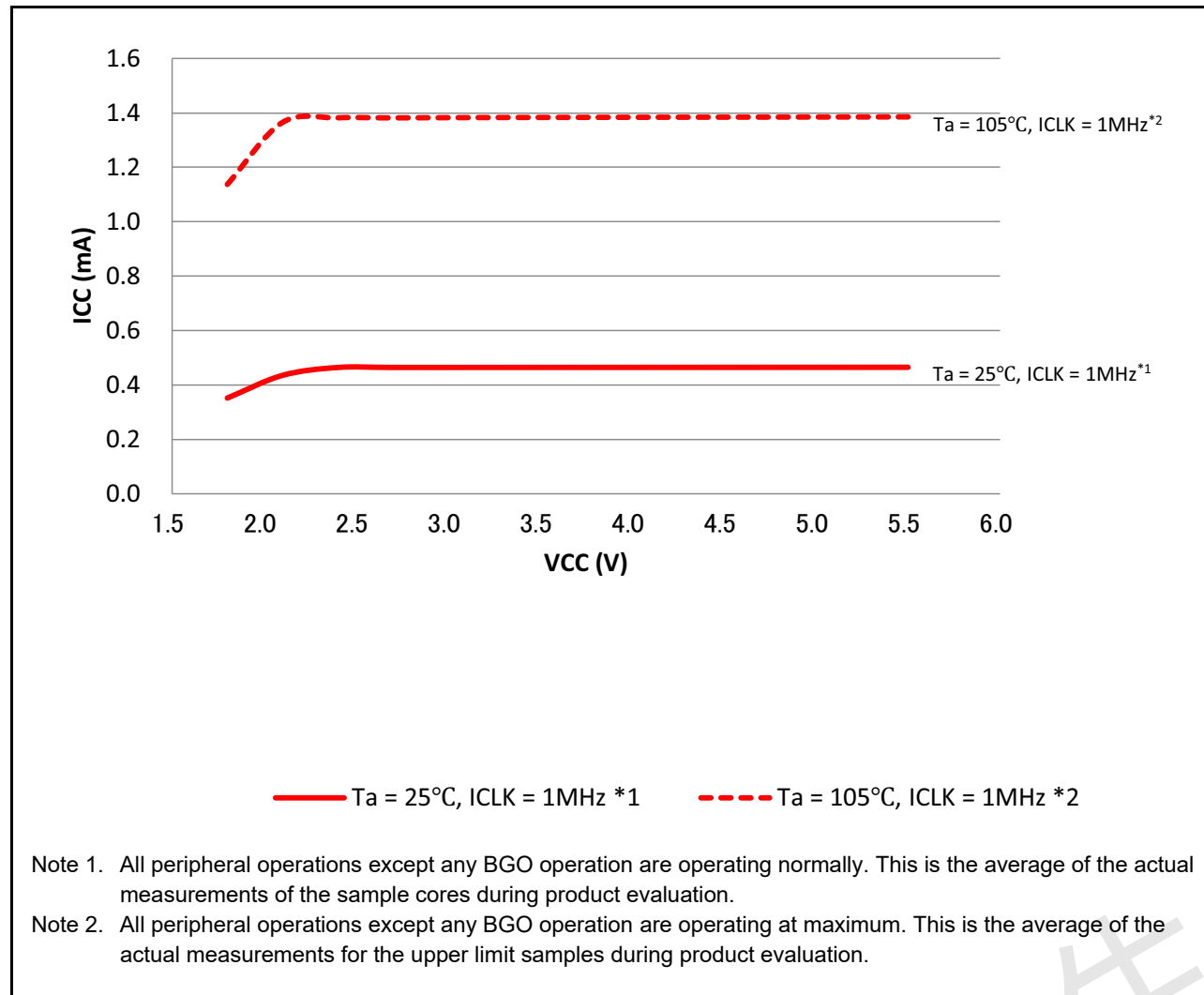


Figure 2.19 Voltage dependency in low-speed operating mode (reference data)

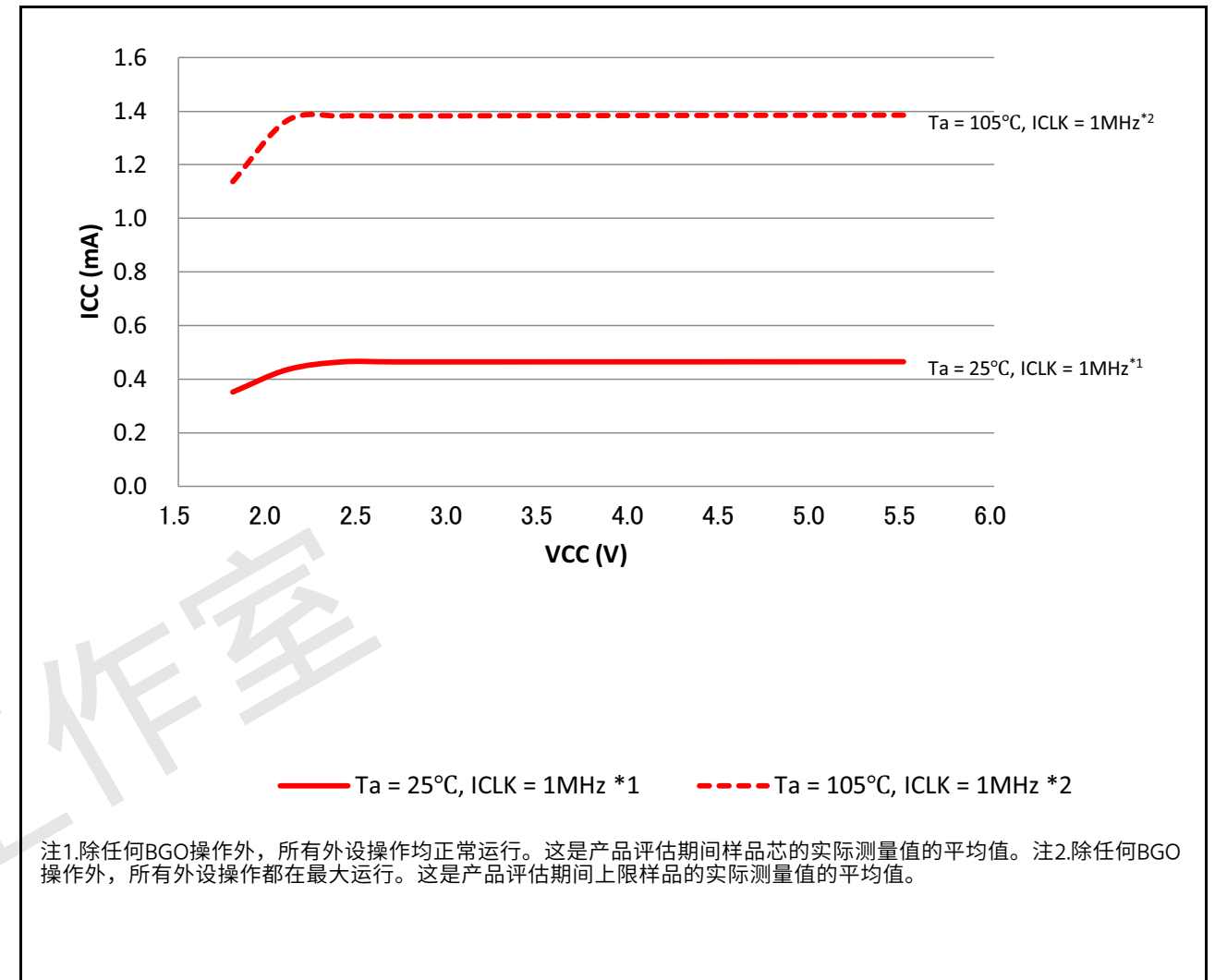


Figure 2.19 低速运行模式下的电压依赖性 (参考数据)

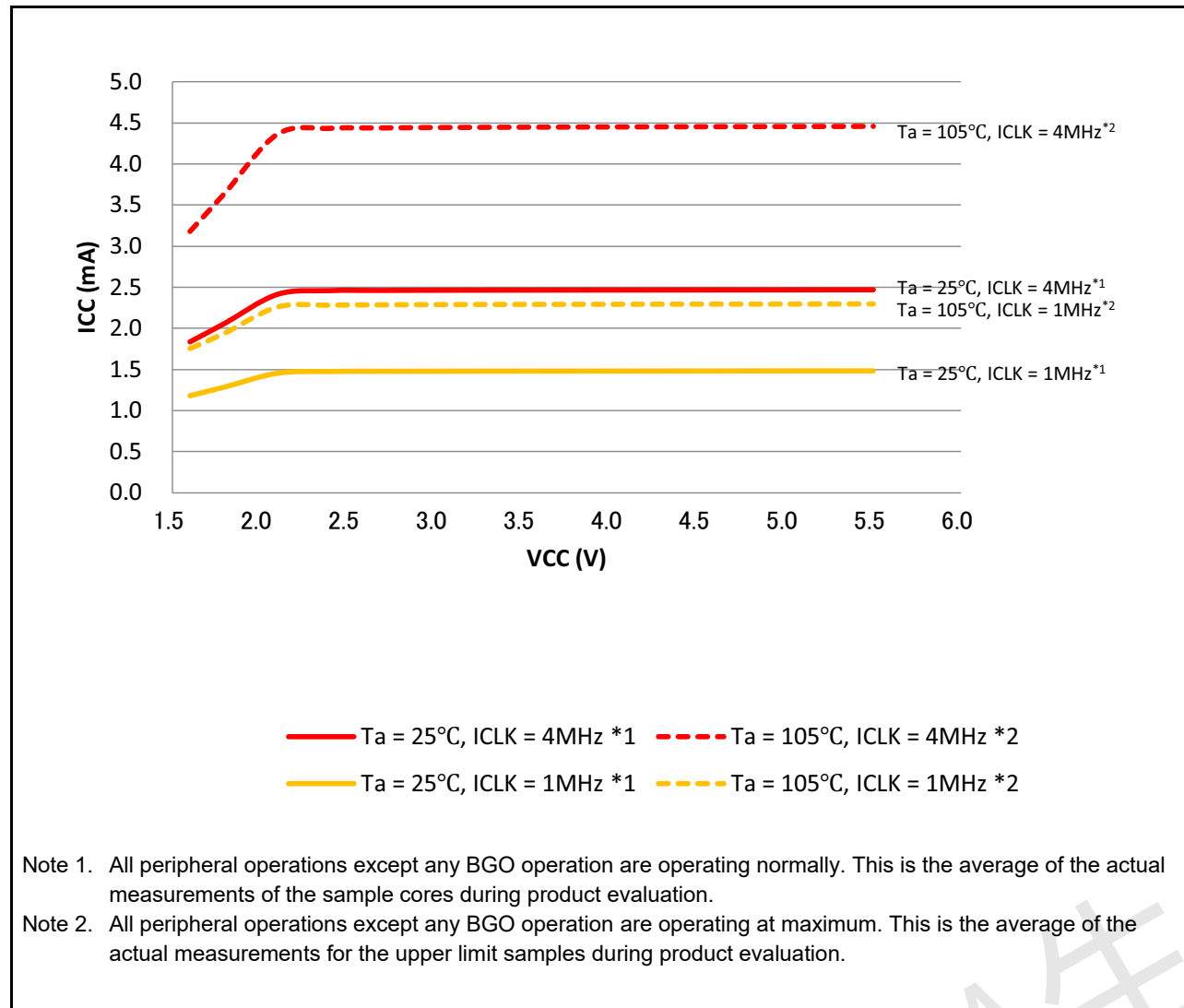


Figure 2.20 Voltage dependency in low-voltage operating mode (reference data)

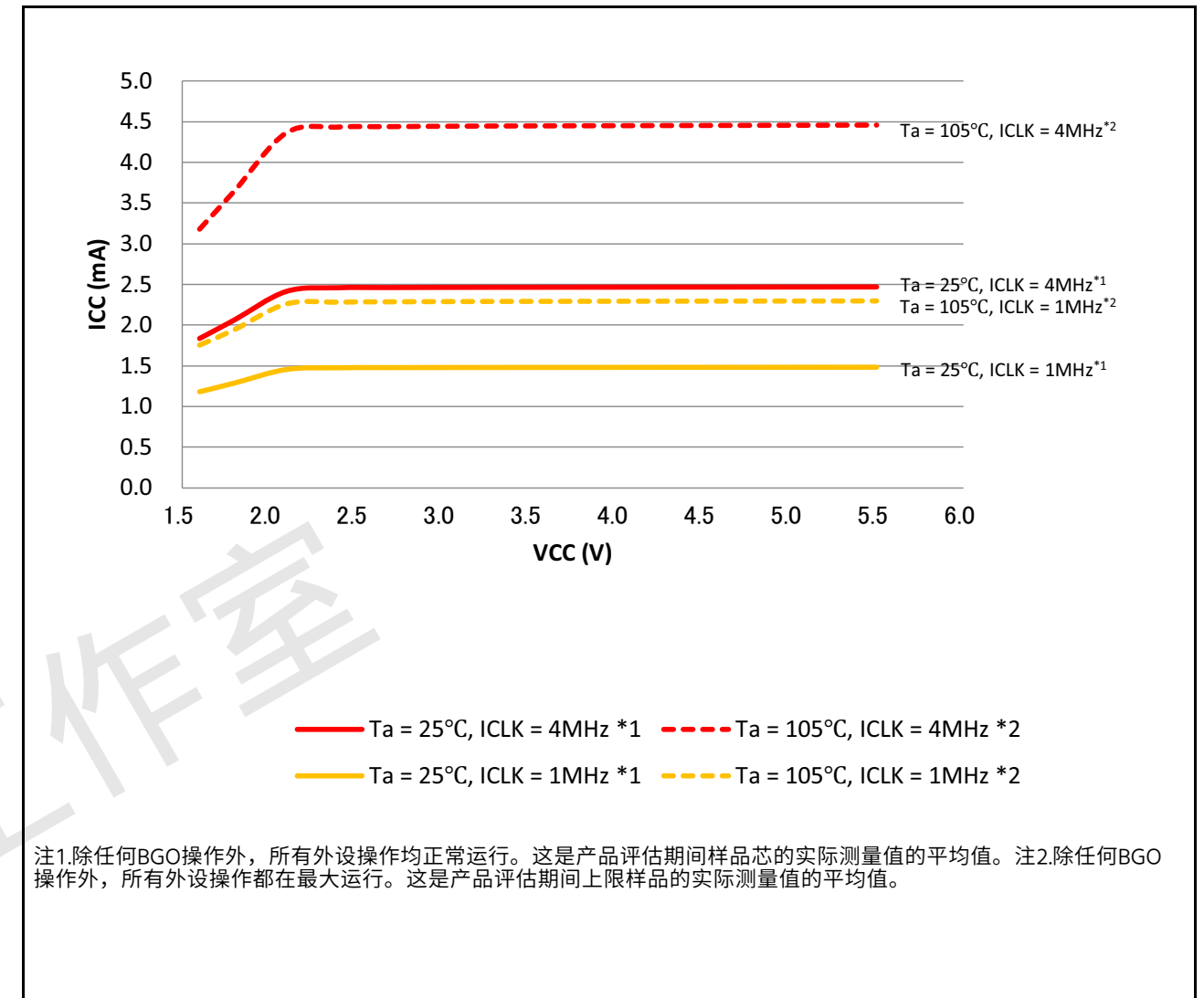


Figure 2.20 低压运行模式下的电压依赖性 (参考数据)

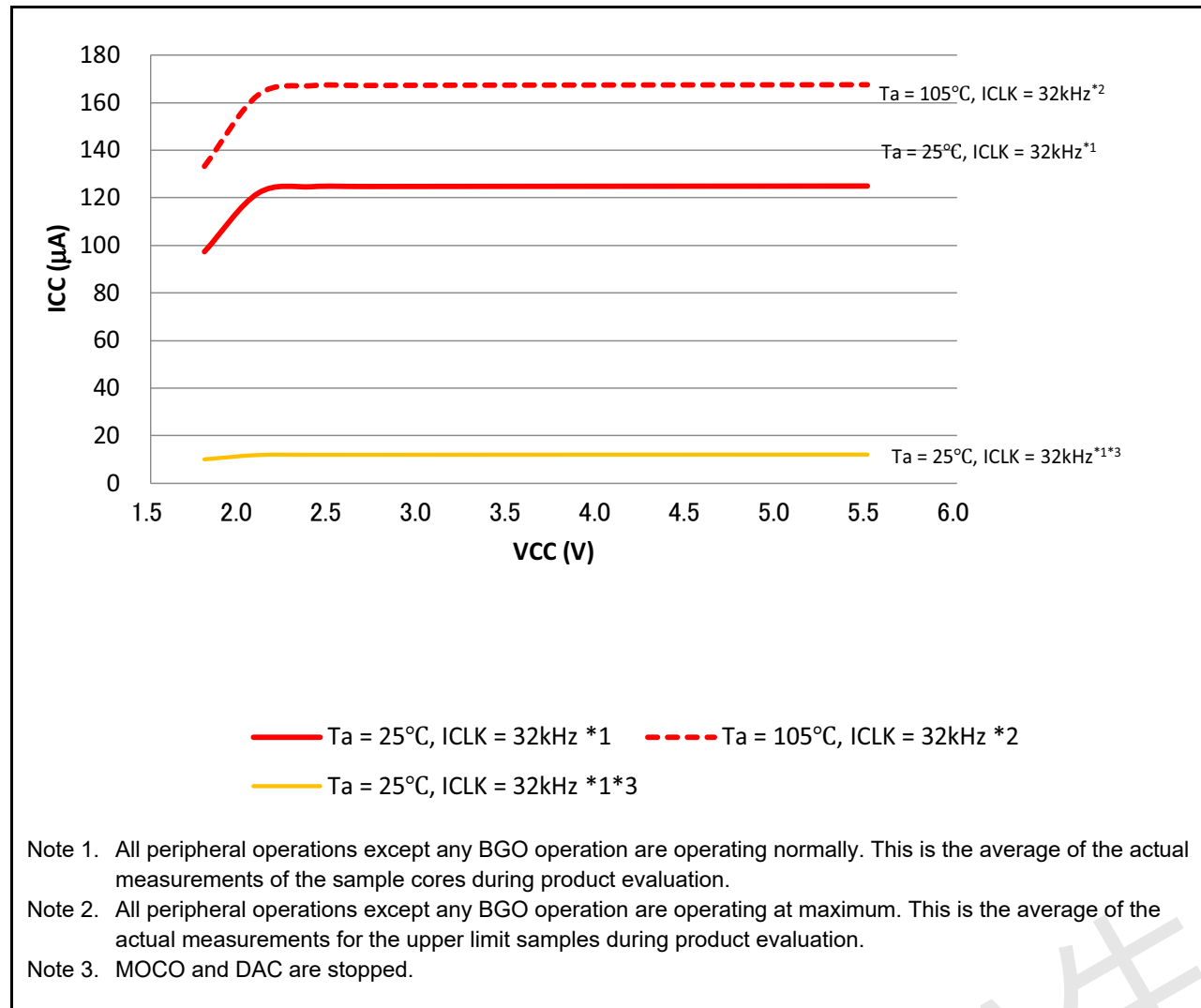


Figure 2.21 Voltage dependency in subosc-speed operating mode (reference data)

Table 2.11 Operating and standby current (2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Typ*3	Max	Unit	Test conditions	
Supply current*1	Software Standby mode*2	T <sub>a</sub> = 25°C	0.5	2.0	µA	-
		T <sub>a</sub> = 55°C	0.8	7.0		
		T <sub>a</sub> = 85°C	1.8	17.0		
		T <sub>a</sub> = 105°C	4.4	45.0		
	Increment for RTC operation with low-speed on-chip oscillator*4	0.4	-		-	
	Increment for RTC operation with sub-clock oscillator*4	0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)	
1.3		-		SOMCR.SODRV[1:0] are 00b (normal mode)		

- Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
- Note 2. The IWDT and LVD are not operating.
- Note 3. VCC = 3.3 V.
- Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

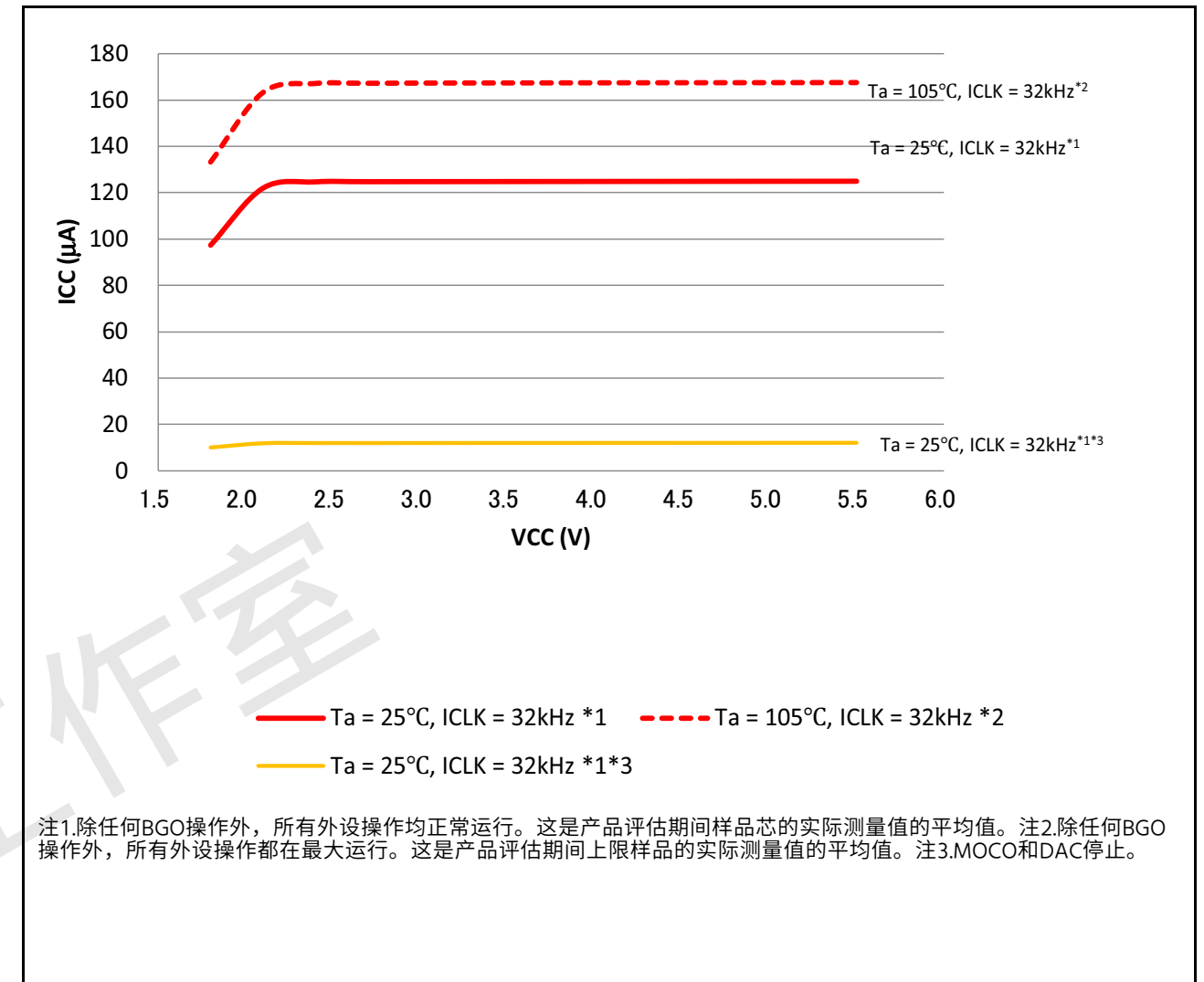


Figure 2.21 subosc速度操作模式下的电压依赖性 (参考数据)

Table 2.11 工作和待机电流(2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Typ*3	Max	Unit	测试条件	
Supply current*1	软件待机模式*2	T <sub>a</sub> = 25°C	0.5	2.0	µA	-
		T <sub>a</sub> = 55°C	0.8	7.0		
		T <sub>a</sub> = 85°C	1.8	17.0		
		T <sub>a</sub> = 105°C	4.4	45.0		
	使用低速片上振荡器*4的RTC操作增量	0.4	-		-	
	使用副时钟振荡器的RTC操作增量*4	0.5	-		SOMCR.SODRV[1:0]为11b (低功耗模式3)	
1.3		-		SOMCR.SODRV[1:0] are 00b (normal mode)		

- Note 1. 电源电流值不包括所有引脚的输出充放电电流。这些值适用于内部上拉时MOS晶体管处于关闭状态。
- Note 2. IWDT和LVD未运行。
- Note 3. VCC = 3.3 V.
- Note 4. 包括低速片上振荡器或子振荡电路电流。

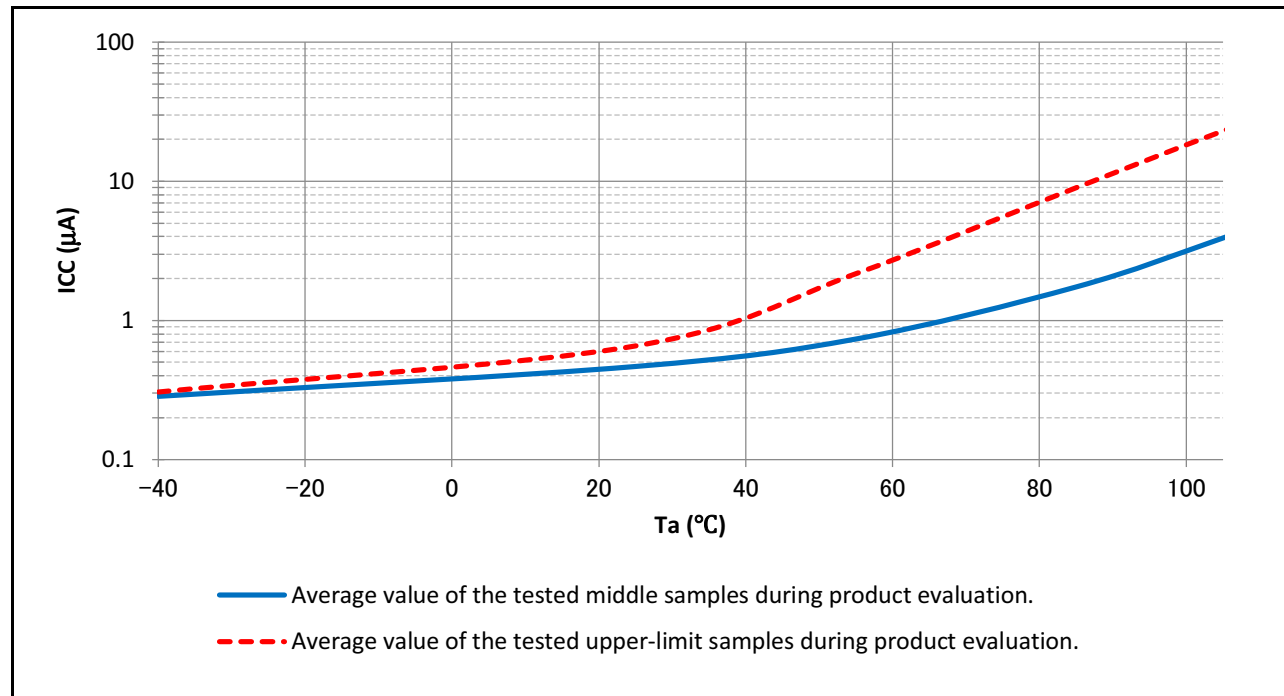


Figure 2.22 Temperature dependency in Software Standby mode (reference data)

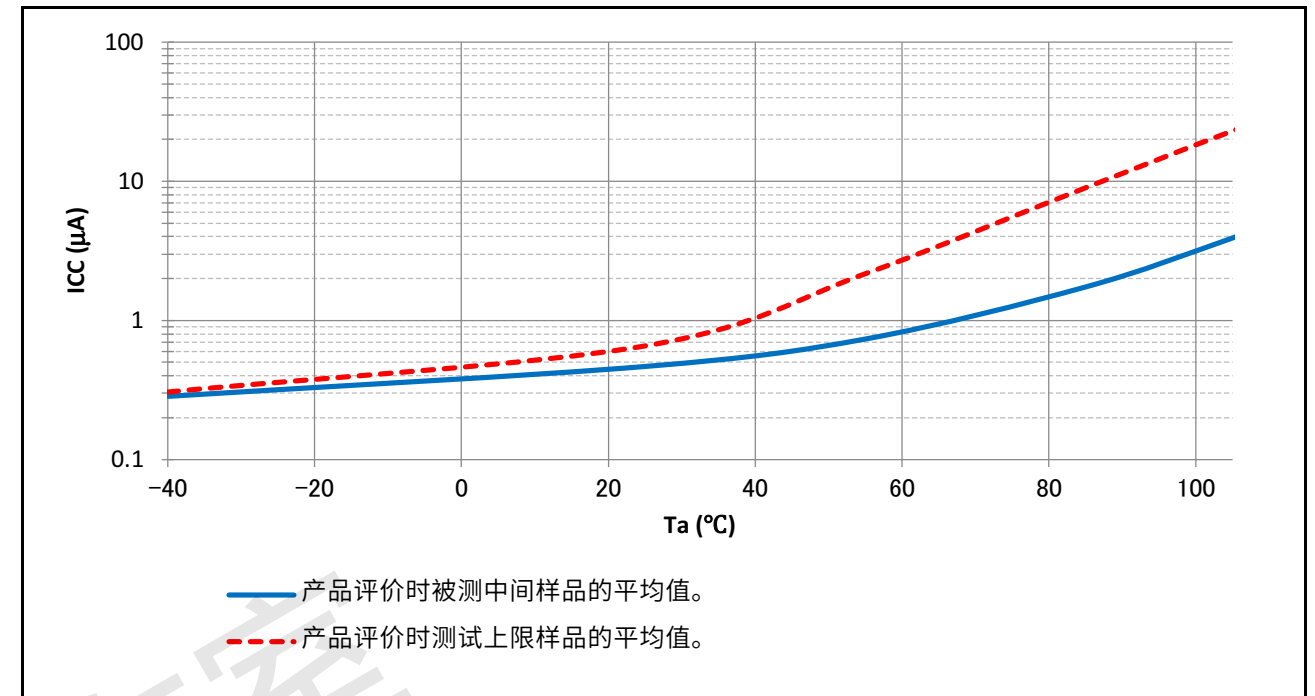


Figure 2.22 软件待机模式下的温度依赖性 (参考数据)

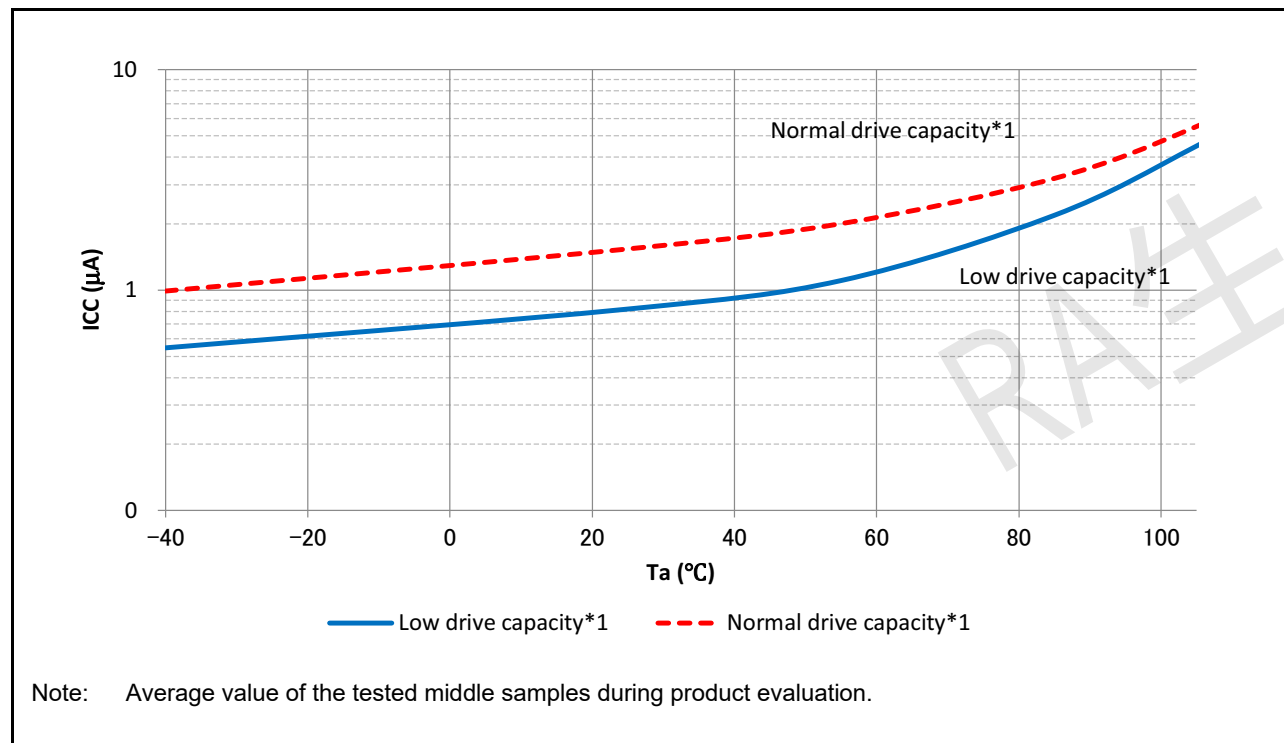


Figure 2.23 Temperature dependency of RTC operation (reference data)

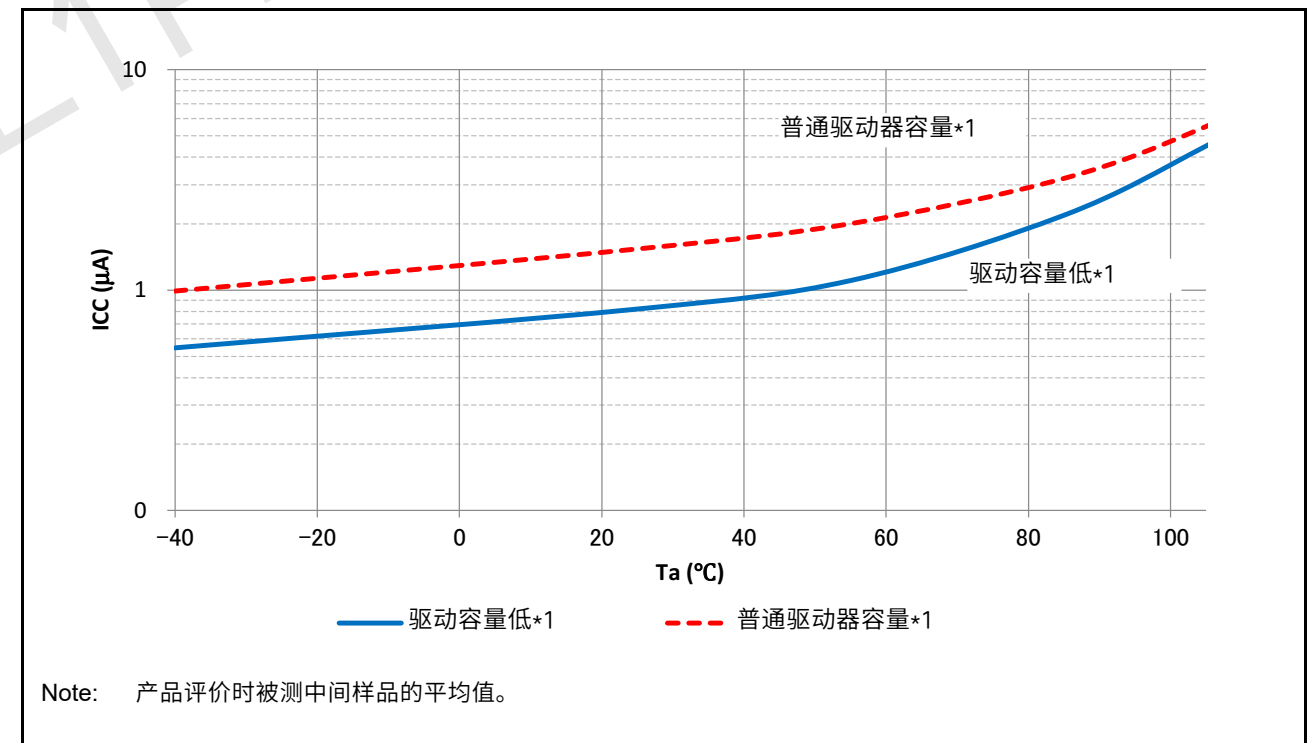


Figure 2.23 RTC操作的温度依赖性 (参考数据)

**Table 2.12 Operating and standby current (3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions					
Analog power supply current	During 16-bit A/D conversion	-	-	1.5	mA	-					
				1.6	mA	-					
				0.9	mA	-					
	During 8-bit D/A conversion (per channel) *1	-	-	-	-	-	-				
	During 12-bit D/A conversion (per channel) *1	-	-	-	-	-	-				
	Waiting for 16-bit A/D, 8-bit D/A and 12-bit D/A conversion (all units) *5	-	-	-	2.0	μA	-				
	Reference power supply current	During 24-bit sigma-delta A/D conversion (at normal mode)	-	-	1.29	mA	-				
1.06					mA	G <sub>SET1</sub> = 8, or G <sub>TOTAL</sub> = 24,32					
During 24-bit sigma-delta A/D conversion (at low-power conversion)		-	-	-	0.9	mA	G <sub>SET1</sub> , G <sub>TOTAL</sub> = the others				
Waiting for 24-bit sigma-delta A/D conversion*6		-	-	-	1.0	μA	-				
Reference power supply current	During 16-bit A/D conversion	-	-	80	μA	-					
	Waiting for 16-bit A/D conversion	-	-	60	nA	-					
	During 12-bit D/A conversion	-	-	650	μA	-					
	Waiting for 12-bit D/A conversion	-	-	100	nA	-					
	During 24-bit sigma-delta A/D conversion	-	-	30	μA	External VREF mode					
Temperature Sensor (TSN) operating current	I <sub>TNS</sub>	-	75	-	μA	-					
Low-power Analog Comparator (ACMPLP) operating current	Window comparator (high-speed mode)	-	15	-	μA	-					
				10	μA	-					
				2	μA	-					
High-speed analog comparator (ACMPHS) operating current	-	70	100	μA	AVCC0 ≥ 2.7 V	-					
				Operational Amplifier (OPAMP) operating current	Low power mode	1 unit operating	-	10	16	μA	-
						2 unit operating	-	19	30	μA	-
3 unit operating	-	28	44			μA	-				
Middle speed mode	1 unit operating	-	280		360	μA	-				
	2 unit operating	-	530		690	μA	-				
	3 unit operating	-	770		1020	μA	-				
High speed mode	1 unit operating	-	0.74	0.91	mA	-					
	2 unit operating	-	1.41	1.74	mA	-					
	3 unit operating	-	2.07	2.57	mA	-					
Internal reference voltage for ADC16 operating current	I <sub>VREFADC</sub>	-	65	130	μA	-					
USBFS operating current	During USB communication under the following settings and conditions: • Function controller is in Full-Speed mode and - Bulk OUT transfer is (64 bytes) × 1 - Bulk IN transfer is (64 bytes) × 1 • Host device is connected by a 1-meter USB cable from the USB port.	I <sub>USBF</sub> *2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-				
	During suspended state under the following setting and conditions: • Function controller is in Full-Speed mode (the USB_DP pin is pulled up) • Software Standby mode • Host device is connected through a 1-meter USB cable from the USB port.	I <sub>SUSP</sub> *3	-	0.35 (VCC) 170 (VCC_USB)*4	-	μA	-				

- Note 1. The reference power supply current is included in the power supply current value for D/A conversion.  
 Note 2. Current is consumed only by the USBFS.  
 Note 3. Includes the current supplied from the pull-up resistor of the USB\_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.  
 Note 4. When VCC = VCC\_USB = 3.3 V.  
 Note 5. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC160 module-stop bit) is in the module-stop

**Table 2.12 工作和待机电流(3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件					
模拟电源电流	在16位AD转换期间	-	-	1.5	mA	-					
				1.6	mA	-					
				0.9	mA	-					
	8位DA转换期间 (每个通道) *1	-	-	-	-	-	-				
	12位DA转换期间 (每个通道) *1	-	-	-	-	-	-				
	等待16位AD、8位DA和12位DA转换 (所有单元) *5	-	-	-	2.0	μA	-				
	参考电源电流	在24位sigma-deltaAD转换期间 (在正常模式下)	-	-	1.29	mA	-				
1.06					mA	G <sub>SET1</sub> = 8, or G <sub>TOTAL</sub> = 24,32					
24位sigma-deltaAD转换期间 (低功率转换时)		-	-	-	0.9	mA	G <sub>SET1</sub> G <sub>TOTAL</sub> =其他				
等待24位sigma-deltaAD转换*6		-	-	-	1.0	μA	-				
参考电源电流	在16位AD转换期间	-	-	80	μA	-					
	等待16位AD转换	-	-	60	nA	-					
	在12位DA转换期间	-	-	650	μA	-					
	等待12位DA转换	-	-	100	nA	-					
	在24位sigma-deltaAD转换期间	-	-	30	μA	外部VREF模式					
温度传感器(TSN)工作电流	I <sub>TNS</sub>	-	75	-	μA	-					
Low-power Analog Comparator (ACMPLP) 工作电流	窗口比较器 (高速模式)	-	15	-	μA	-					
				10	μA	-					
				2	μA	-					
高速模拟比较器(ACMPHS)工作电流	-	70	100	μA	AVCC0 ≥ 2.7 V	-					
				Operational 放大器(OPAMP)工作电流	低功耗模式	1个单位运营	-	10	16	μA	-
						2个单元操作	-	19	30	μA	-
3个单元操作	-	28	44			μA	-				
中速模式	1个单位运营	-	280		360	μA	-				
	2个单元操作	-	530		690	μA	-				
	3个单元操作	-	770		1020	μA	-				
高速模式	1个单位运营	-	0.74	0.91	mA	-					
	2个单元操作	-	1.41	1.74	mA	-					
	3个单元操作	-	2.07	2.57	mA	-					
ADC16工作电流的内部参考电压	I <sub>VREFADC</sub>	-	65	130	μA	-					
USBFS工作电流	在以下设置和条件下进行USB通信期间: 功能控制器处于全速模式并且BulkOUT传输为(64字节) × 1 Bulk IN传输为(64字节) × 1 主机设备通过1米连接来自USB端口的USB电缆。	I <sub>USBF</sub> *2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-				
	在以下设置和条件下处于挂起状态: 功能控制器处于全速模式 (USB_DP引脚上拉) 软件待机模式 主机设备通过1米长的USB电缆从USB端口连接。	I <sub>SUSP</sub> *3	-	0.35 (VCC) 170 (VCC_USB)*4	-	μA	-				

- Note 1. 基准电源电流包含在DA转换的电源电流值中。  
 Note 2. 电流仅由USBFS消耗。  
 Note 3. 包括从USB\_DP引脚的上拉电阻提供给主机设备下拉电阻的电流, 以及MCU在挂起状态下消耗的电流。  
 Note 4. When VCC = VCC\_USB = 3.3 V.  
 Note 5. 当MCU处于软件待机模式或MSTPCRD.MSTPD16 (ADC160模块停止位) 处于模块停止状态时



state.

Note 6. When the MCU is in the MSTPCRD.MSTPD17 (SDADC24 module-stop bit) is in the module-stop state.

### 2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.13 Rise and fall gradient characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1, *2				-		
	SCI/USB boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

**Table 2.14 Rising and falling gradient and ripple frequency characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency  $f_{r(VCC)}$  within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When the VCC change exceeds VCC  $\pm$  10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC $\pm$ 10%

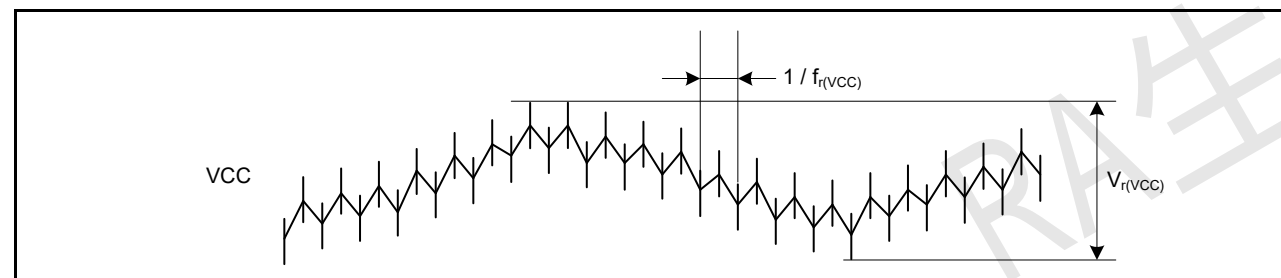


Figure 2.24 Ripple waveform

state.

Note 6. 当MCU处于MSTPRD.MSTPD17 (SDADC24模块停止位) 处于模块停止状态时。

### 2.2.10 VCC上升和下降梯度和纹波频率

**Table 2.13 上升和下降梯度特性**

Conditions: VCC = AVCC0 = AVCC1 = 0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
上电VCC上升梯度	SrVCC	0.02	-	2	ms/V	-	
				启动时禁用电压监视器0复位			-
				启动时启用电压监视器0复位*1 *2			2

Note 1. When OFS1.LVDAS = 0.

Note 2. 在引导模式下, 无论OFS1.LVDAS位的值如何, 电压监视器0的复位均被禁用。

**Table 2.14 上升下降梯度和纹波频率特性**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

纹波电压必须在VCC上限(5.5V)和下限(1.6V)之间的范围内满足允许的纹波频率 $f_{r(VCC)}$ 。当VCC变化超过VCC  $\pm$  10%时, 必须满足允许的电压变化上升和下降梯度dt/dVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	-	-	ms/V	当VCC变化超过VCC $\pm$ 10%

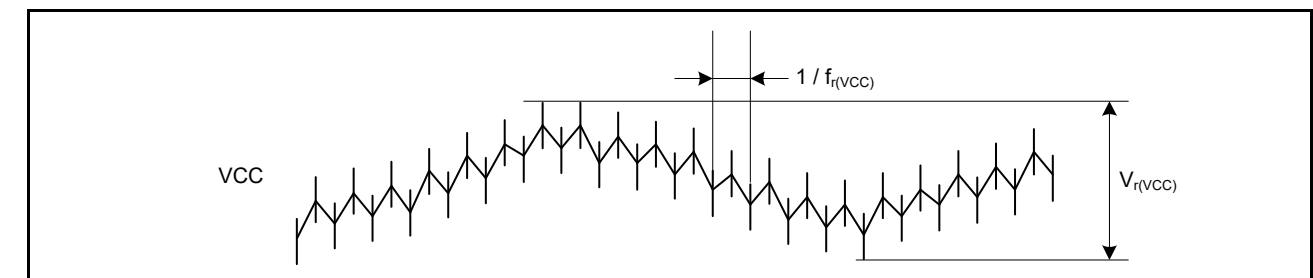


Figure 2.24 纹波波形

## 2.3 AC Characteristics

## 2.3.1 Frequency

**Table 2.15 Operation frequency in high-speed operating mode**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max*7	Unit		
Operation frequency	System clock (ICLK)*6	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
		2.7 to 5.5 V		0.032768	-	32	
	FlashIF clock (FCLK)*1,*2,*6	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
		2.7 to 5.5 V		-	-	32	
Peripheral module clock (PCLKB)*5,*6	2.7 to 5.5 V		-	-	32		
	2.4 to 2.7 V		-	-	16		
	2.7 to 5.5 V		-	-	64*4		
Peripheral module clock (PCLKD)*3,*6	2.7 to 5.5 V		-	-	64*4		
	2.4 to 2.7 V		-	-	16		

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.

Note 4. The upper-limit frequency of PCLKD is 32 MHz when the ADC16 is in use.

Note 5. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Note 6. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.

Note 7. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.20, Clock timing](#).

**Table 2.16 Operation frequency in middle-speed mode**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
Operation frequency	System clock (ICLK)*5	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1,*2,*5	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKB)*4,*5	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
Peripheral module clock (PCLKD)*3,*5	2.7 to 5.5 V		-	-	12		
	2.4 to 2.7 V		-	-	12		
	1.8 to 2.4 V		-	-	8		

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.

Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK,

## 2.3 交流特性

## 2.3.1 Frequency

**Table 2.15 高速运行模式下的运行频率**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max*7	Unit		
运行频率	系统时钟(ICLK)*6	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
		2.7 to 5.5 V		0.032768	-	32	
	FlashIF clock (FCLK)*1,*2,*6	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
		2.7 to 5.5 V		-	-	32	
外设模块时钟 (PCLKB) *5 *6	2.7 to 5.5 V		-	-	32		
	2.4 to 2.7 V		-	-	16		
外设模块时钟 (PCLKD) *3 *6	2.7 to 5.5 V		-	-	64*4		
	2.4 to 2.7 V		-	-	16		

注1.对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。注2.在对闪存进行编程或擦除时，FCLK的频率精度必须为 $\pm 3.5\%$ 。确认时钟源的频率精度。注3.使用ADC16时，PCLKD的下限频率为1MHz。

注4.使用ADC16时，PCLKD的上限频率为32MHz。

注5.使用SDADC24时，PCLKB的下限频率为1MHz。

注6.ICLK之间的频率关系见用户手册第9节，时钟生成电路，

PCLKB, PCLKD, and FCLK.

注7.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.20，时钟时序。

**Table 2.16 中速运行频率**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
运行频率	系统时钟(ICLK)*5	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1,*2,*5	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	外设模块时钟 (PCLKB) *4 *5	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
外设模块时钟 (PCLKD) *3 *5	2.7 to 5.5 V		-	-	12		
	2.4 to 2.7 V		-	-	12		
	1.8 to 2.4 V		-	-	8		

注1.对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

注2.在对闪存进行编程或擦除时，FCLK的频率精度必须为 $\pm 3.5\%$ 。确认时钟源的频率精度。注3.使用ADC16时，PCLKD的下限频率为1MHz。

注4.使用SDADC24时，PCLKB的下限频率为1MHz。

注5.ICLK之间的频率关系见用户手册第9节，时钟生成电路，

PCLKB, PCLKD, and FCLK.

Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.20, Clock timing](#).

**Table 2.17 Operation frequency in low-speed mode**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
Operation frequency	System clock (ICLK)*5	1.8 to 5.5 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK) *1,*2,*5	1.8 to 5.5 V		0.032768	-	1	
	Peripheral module clock (PCLKB)*4,*5	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3,*5	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.

Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.

Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.

Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.20, Clock timing](#).

**Table 2.18 Operation frequency in low-voltage mode**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
Operation frequency	System clock (ICLK)*5	1.6 to 5.5 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1,*2,*5	1.6 to 5.5 V		0.032768	-	4	
	Peripheral module clock (PCLKB)*4,*5	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3,*5	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.

Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.

Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.20, Clock timing](#).

**Table 2.19 Operation frequency in Subosc-speed mode**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit		
Operation frequency	System clock (ICLK)*4	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1,*4	1.8 to 5.5 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKB)*3,*4	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2,*4	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.

Note 2. The ADC16 cannot be used.

Note 3. The SDADC24 cannot be used.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.

PCLKB, PCLKD, and FCLK.

注6.工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.20，时钟时序。

**Table 2.17 低速运行频率**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
运行频率	系统时钟(ICLK)*5	1.8 to 5.5 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK) *1,*2,*5	1.8 to 5.5 V		0.032768	-	1	
	外设模块时钟 (PCLKB) *4 *5	1.8 to 5.5 V		-	-	1	
	外设模块时钟 (PCLKD) *3 *5	1.8 to 5.5 V		-	-	1	

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。

Note 2. 在对闪存进行编程或擦除时，FCLK的频率精度必须为 $\pm 3.5\%$ 。确认时钟源的频率精度。

Note 3. 使用ADC16时，PCLKD的下限频率为1MHz。

Note 4. 使用SDADC24时，PCLKB的下限频率为1MHz。

Note 5. 关于ICLK、PCLKB、PCLKD和FCLK之间的频率关系，请参见用户手册中的第9节“时钟生成电路”。

Note 6. 工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.20，时钟时序。

**Table 2.18 低压模式下的工作频率**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max*6	Unit		
运行频率	系统时钟(ICLK)*5	1.6 to 5.5 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1,*2,*5	1.6 to 5.5 V		0.032768	-	4	
	外设模块时钟 (PCLKB) *4 *5	1.6 to 5.5 V		-	-	4	
	外设模块时钟 (PCLKD) *3 *5	1.6 to 5.5 V		-	-	4	

Note 1. 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用FCLK在4MHz以下对闪存进行编程或擦除时，频率可以设置为1 MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。

Note 2. 在对闪存进行编程或擦除时，FCLK的频率精度必须为 $\pm 3.5\%$ 。确认时钟源的频率精度。

Note 3. 使用ADC16时，PCLKD的下限频率为1MHz。

Note 4. 使用SDADC24时，PCLKB的下限频率为1MHz。

Note 5. 关于ICLK、PCLKB、PCLKD和FCLK之间的频率关系，请参见用户手册中的第9节“时钟生成电路”。

Note 6. 工作频率的最大值不包括内部振荡器误差。有关保证操作范围的详细信息，请参见表2.20，时钟时序。

**Table 2.19 Subosc速度模式下的运行频率**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit		
运行频率	系统时钟(ICLK)*4	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1,*4	1.8 to 5.5 V		27.8528	32.768	37.6832	
	外设模块时钟 (PCLKB) *3 *4	1.8 to 5.5 V		-	-	37.6832	
	外设模块时钟 (PCLKD) *2 *4	1.8 to 5.5 V		-	-	37.6832	

Note 1. 无法对闪存进行编程和擦除。

Note 2. ADC16不能使用。

Note 3. SDADC24不能使用。

Note 4. 关于ICLK、PCLKB、PCLKD和FCLK之间的频率关系，请参见用户手册中的第9节“时钟生成电路”。

## 2.3.2 Clock Timing

Table 2.20 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t <sub>XCYC</sub>	50	-	-	ns	Figure 2.25
EXTAL external clock input high pulse width	t <sub>XH</sub>	20	-	-	ns	
EXTAL external clock input low pulse width	t <sub>XL</sub>	20	-	-	ns	
EXTAL external clock rising time	t <sub>Xr</sub>	-	-	5	ns	
EXTAL external clock falling time	t <sub>Xf</sub>	-	-	5	ns	
EXTAL external clock input wait time*1	t <sub>EXWT</sub>	0.3	-	-	μs	-
EXTAL external clock input frequency	f <sub>EXTAL</sub>	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		-	-	8		1.8 ≤ VCC < 2.4
		-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f <sub>MAIN</sub>	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		1	-	8		1.8 ≤ VCC < 2.4
		1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f <sub>LOCO</sub>	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time	t <sub>LOCO</sub>	-	-	100	μs	Figure 2.26
IWDT-dedicated clock oscillation frequency	f <sub>ILOCO</sub>	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency	f <sub>MOCO</sub>	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time	t <sub>MOCO</sub>	-	-	1	μs	-
HOCO clock oscillation frequency	f <sub>HOCO24</sub>	23.64	24	24.36	MHz	Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
		22.68	24	25.32		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
		23.76	24	24.24		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
		23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO32</sub>	31.52	32	32.48		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
		30.24	32	33.76		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
		31.68	32	32.32		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
		31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO48</sub> *3	47.28	48	48.72		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
		47.52	48	48.48		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
		47.04	48	48.96		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO64</sub> *4	63.04	64	64.96		Ta = -40 to -20°C 2.4 ≤ VCC ≤ 5.5
63.36		64	64.64	Ta = -20 to 85°C 2.4 ≤ VCC ≤ 5.5		
62.72		64	65.28	Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5		
HOCO clock oscillation stabilization time*5, *6	Except low-voltage mode	t <sub>HOCO24</sub>	-	-	μs	Figure 2.27
		t <sub>HOCO32</sub>	-	-		
		t <sub>HOCO48</sub>	-	-		
		t <sub>HOCO64</sub>	-	-		
	Low-voltage mode	t <sub>HOCO24</sub>	-	-		
Sub-clock oscillator oscillation frequency	f <sub>SUB</sub>	-	32.768	-	kHz	-

## 2.3.2 时钟时序

Table 2.20 时钟计时(1of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间	t <sub>XCYC</sub>	50	-	-	ns	Figure 2.25
EXTAL外部时钟输入高脉冲宽度	t <sub>XH</sub>	20	-	-	ns	
EXTAL外部时钟输入低脉冲宽度	t <sub>XL</sub>	20	-	-	ns	
EXTAL外部时钟上升时间	t <sub>Xr</sub>	-	-	5	ns	
EXTAL外部时钟下降时间	t <sub>Xf</sub>	-	-	5	ns	
EXTAL外部时钟输入等待时间*1	t <sub>EXWT</sub>	0.3	-	-	μs	-
EXTAL外部时钟输入频率	f <sub>EXTAL</sub>	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		-	-	8		1.8 ≤ VCC < 2.4
		-	-	1		1.6 ≤ VCC < 1.8
主时钟振荡器振荡频率	f <sub>MAIN</sub>	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		1	-	8		1.8 ≤ VCC < 2.4
		1	-	4		1.6 ≤ VCC < 1.8
LOCO时钟振荡频率	f <sub>LOCO</sub>	27.8528	32.768	37.6832	kHz	-
LOCO时钟振荡稳定时间	t <sub>LOCO</sub>	-	-	100	μs	Figure 2.26
IWDT专用时钟振荡频率	f <sub>ILOCO</sub>	12.75	15	17.25	kHz	-
MOCO时钟振荡频率	f <sub>MOCO</sub>	6.8	8	9.2	MHz	-
MOCO时钟振荡稳定时间	t <sub>MOCO</sub>	-	-	1	μs	-
HOCO时钟振荡频率	f <sub>HOCO24</sub>	23.64	24	24.36	MHz	Ta = -40至-20°C 1.8 ≤ VCC ≤ 5.5
		22.68	24	25.32		Ta = -40至85°C 1.6 ≤ VCC < 1.8
		23.76	24	24.24		Ta = -20至85°C 1.8 ≤ VCC ≤ 5.5
		23.52	24	24.48		Ta = 85至105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO32</sub>	31.52	32	32.48		Ta = -40至-20°C 1.8 ≤ VCC ≤ 5.5
		30.24	32	33.76		Ta = -40至85°C 1.6 ≤ VCC < 1.8
		31.68	32	32.32		Ta = -20至85°C 1.8 ≤ VCC ≤ 5.5
		31.36	32	32.64		Ta = 85至105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO48</sub> *3	47.28	48	48.72		Ta = -40至-20°C 1.8 ≤ VCC ≤ 5.5
		47.52	48	48.48		Ta = -20至85°C 1.8 ≤ VCC ≤ 5.5
		47.04	48	48.96		Ta = 85至105°C 2.4 ≤ VCC ≤ 5.5
	f <sub>HOCO64</sub> *4	63.04	64	64.96		Ta = -40至-20°C 2.4 ≤ VCC ≤ 5.5
63.36		64	64.64	Ta = -20至85°C 2.4 ≤ VCC ≤ 5.5		
62.72		64	65.28	Ta = 85至105°C 2.4 ≤ VCC ≤ 5.5		
HOCO时钟振荡稳定时间*5 *6	低压模式除外	t <sub>HOCO24</sub>	-	-	μs	Figure 2.27
		t <sub>HOCO32</sub>	-	-		
		t <sub>HOCO48</sub>	-	-		
		t <sub>HOCO64</sub>	-	-		
	Low-voltage mode	t <sub>HOCO24</sub>	-	-		
副时钟振荡器振荡频率	f <sub>SUB</sub>	-	32.768	-	kHz	-



Table 2.20 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation stabilization time*2	$t_{SUBOSC}$	-	0.5	-	s	Figure 2.28

- Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
- Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
- Note 3. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.
- Note 4. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.
- Note 5. This is a characteristic when the HOCOCR.HCSTP bit is cleared to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1  $\mu$ s.
- Note 6. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

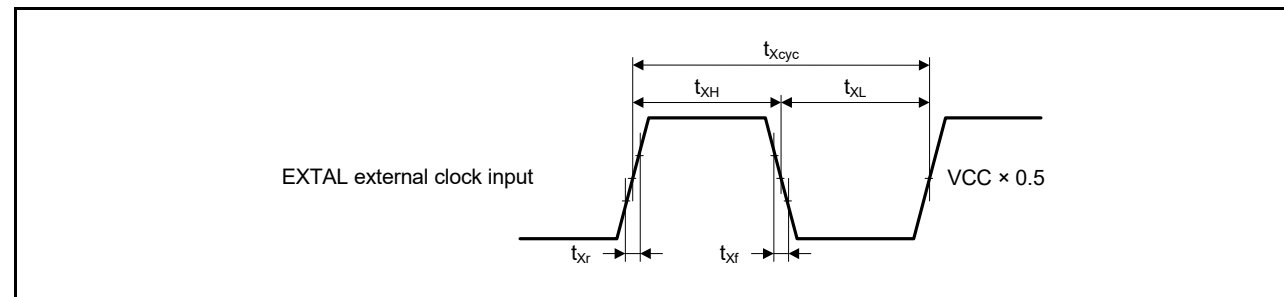


Figure 2.25 EXTAL external clock input timing

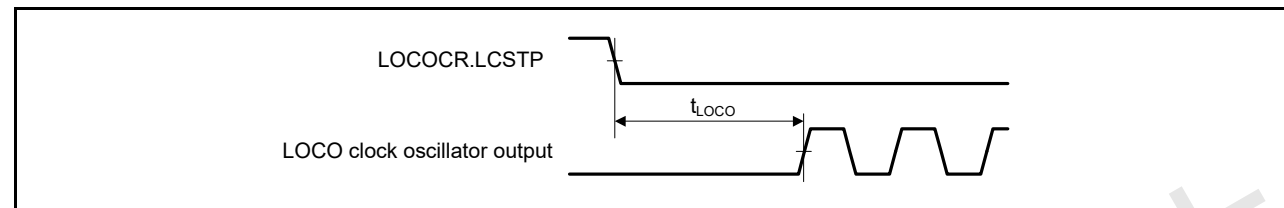


Figure 2.26 LOCO clock oscillator start timing

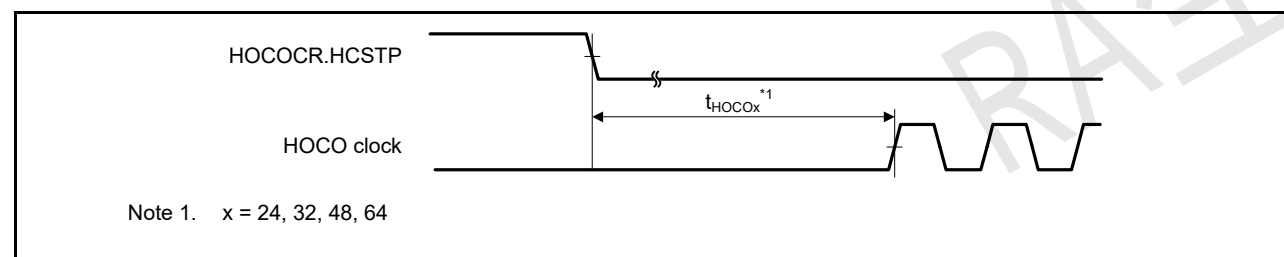


Figure 2.27 HOCO clock oscillator start timing (started by setting the HOCOCR.HCSTP bit)

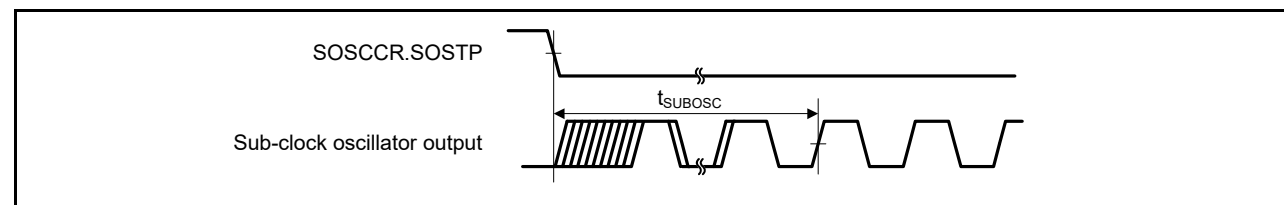


Figure 2.28 Sub-clock oscillator start timing

Table 2.20 时钟计时 (2个中的2个)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
副时钟振荡稳定时间*2	$t_{SUBOSC}$	-	0.5	-	s	Figure 2.28

- Note 1. 当外部时钟稳定时，主时钟振荡器停止位(MOSCCR.MOSTP)设置为0 (运行) 后，时钟可以使用的时。
- Note 2. 更改SOSCCR.SOSTP位的设置以启动副时钟振荡器操作后，仅在经过副时钟振荡器稳定等待时间后才开始使用副时钟振荡器。使用振荡器制造商推荐的振荡器等待时间值。
- Note 3. 48MHzHOCO可在1.8V至5.5V的VCC范围内使用。
- Note 4. 64MHzHOCO可在2.4V至5.5V的VCC范围内使用。
- Note 5. 这是在MOCO停止状态下HOCOCR.HCSTP位被清除为0 (振荡) 时的特性。在MOCO振荡期间将HOCOCR.HCSTP位设置为0 (振荡) 时，该规范将缩短1 $\mu$ s。
- Note 6. 检查OSCSF.HOCOSF以确认稳定时间是否已过。

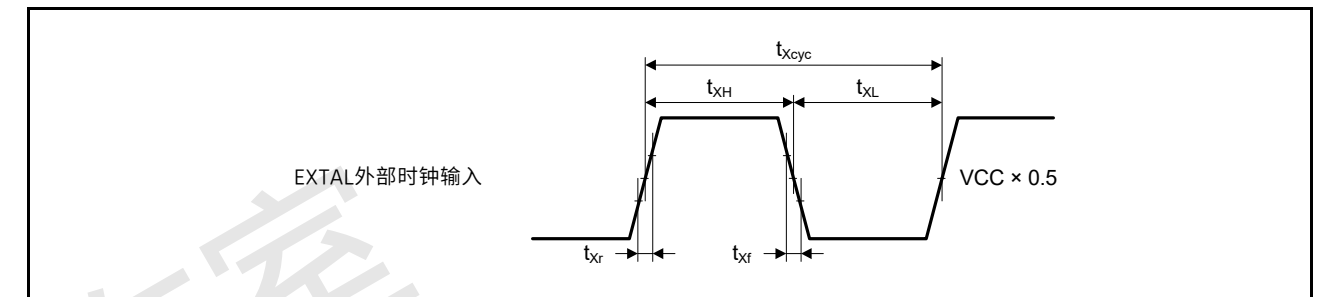


Figure 2.25 EXTAL外部时钟输入时序

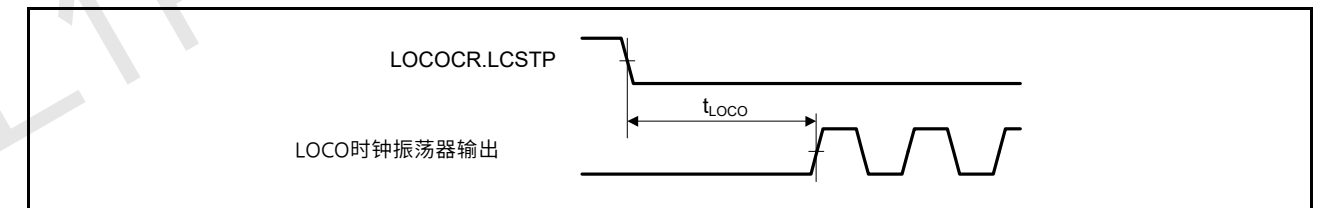


Figure 2.26 LOCO时钟振荡开始时序

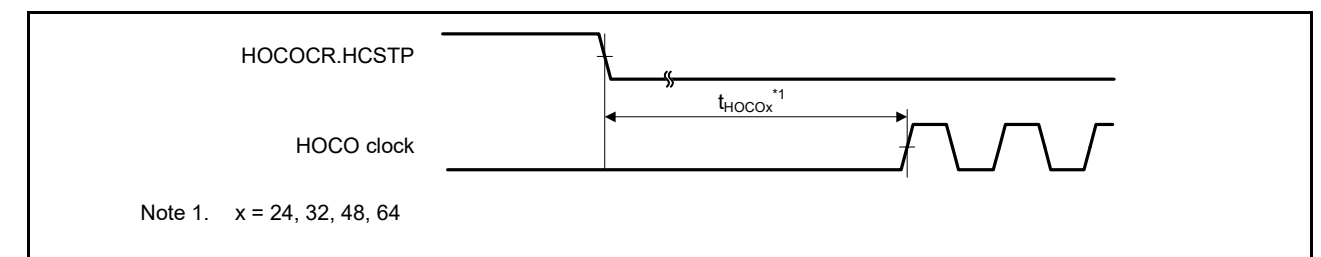


Figure 2.27 HOCO时钟振荡开始时序 (通过设置HOCOCR.HCSTP位开始)

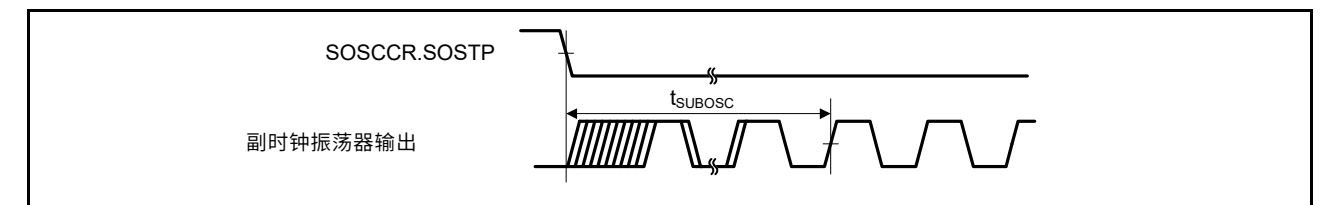


Figure 2.28 副时钟振荡开始时序



2.3.3 Reset Timing

Table 2.21 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	$t_{RESWP}$	3	-	-	ms	Figure 2.29
	Not at power-on	$t_{RESW}$	30	-	-	$\mu$ s	Figure 2.30
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	$t_{RESWT}$	-	0.7	-	ms	Figure 2.29
	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	$t_{RESWT2}$	-	0.5	-	ms	Figure 2.30
	LVD0 disabled*2		-	0.1	-		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	$t_{RESWT3}$	-	0.6	-	ms	Figure 2.31
	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

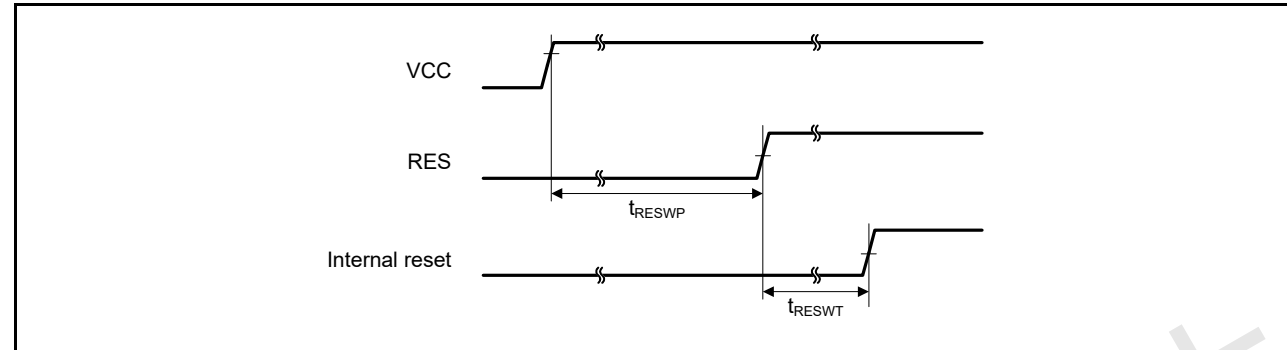


Figure 2.29 Reset input timing at power-on

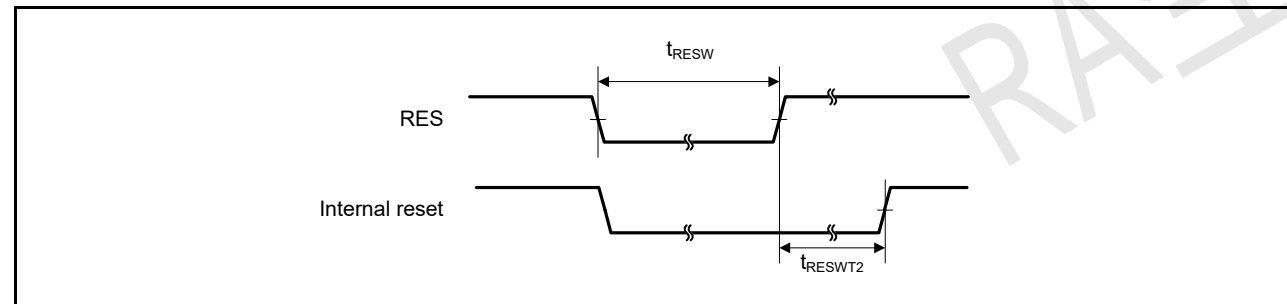


Figure 2.30 Reset input timing (1)

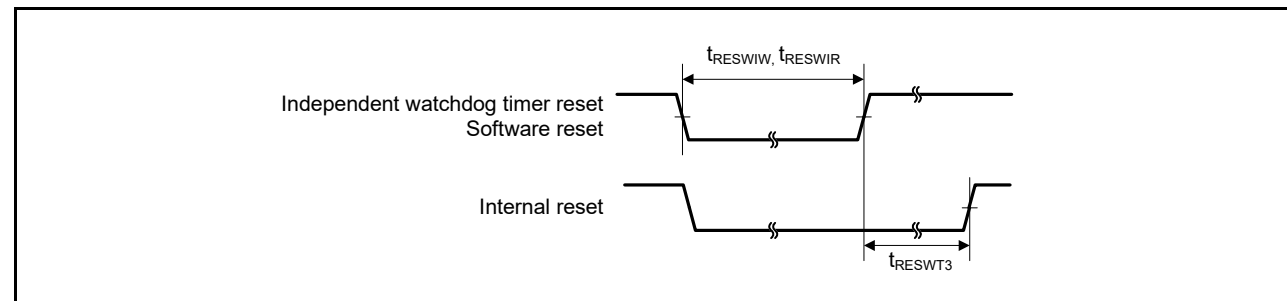


Figure 2.31 Reset input timing (2)

2.3.3 重置时间

Table 2.21 重置时间

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	At power-on	$t_{RESWP}$	3	-	-	ms	Figure 2.29
	不开机	$t_{RESW}$	30	-	-	$\mu$ s	Figure 2.30
RES取消后的等待时间（上电时）	LVD0 enabled*1	$t_{RESWT}$	-	0.7	-	ms	Figure 2.29
	LVD0 disabled*2		-	0.3	-		
RES取消后的等待时间（开机状态下）	LVD0 enabled*1	$t_{RESWT2}$	-	0.5	-	ms	Figure 2.30
	LVD0 disabled*2		-	0.1	-		
内部复位取消后的等待时间（看门狗定时器复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主控MPU错误复位、总线从属MPU错误复位、堆栈指针错误复位、软件复位）	LVD0 enabled*1	$t_{RESWT3}$	-	0.6	-	ms	Figure 2.31
	LVD0 disabled*2		-	0.15	-		

注1.当OFS1.LVDAS=0时。注2.当OFS1.LVDAS=1时。

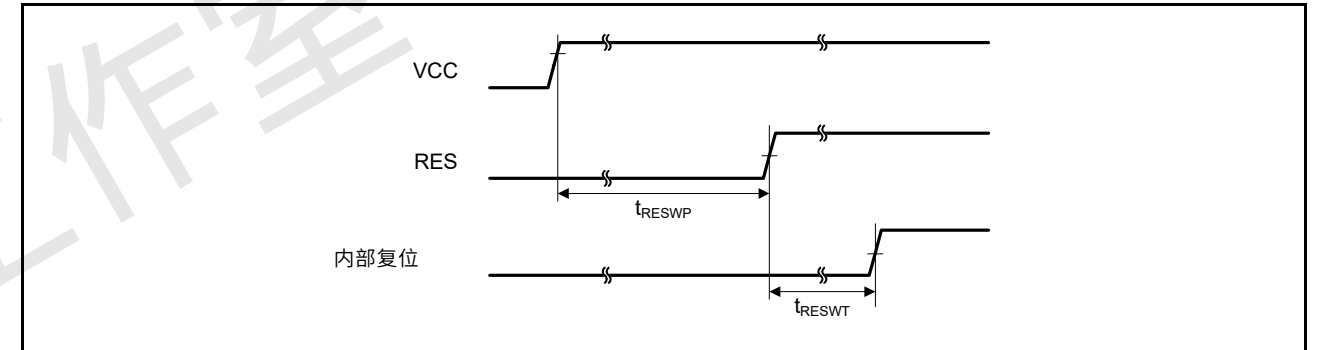


Figure 2.29 上电时复位输入时序

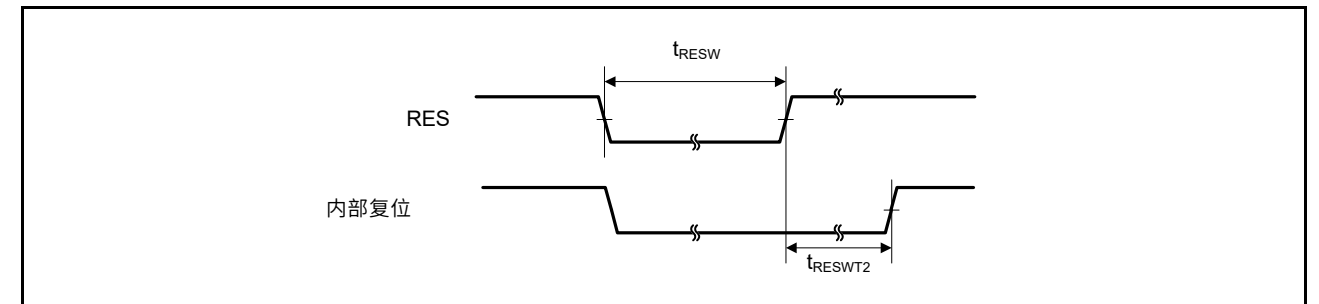


Figure 2.30 复位输入时序(1)

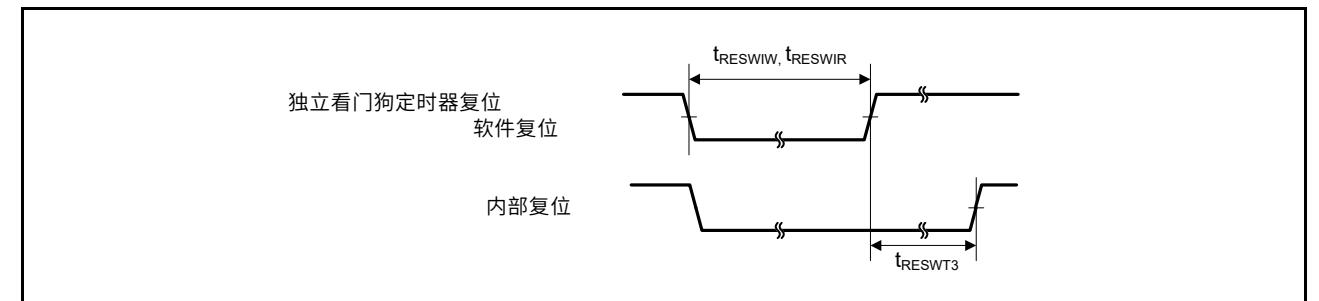


Figure 2.31 复位输入时序(2)

## 2.3.4 Wakeup Time

Table 2.22 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t <sub>SBYEX</sub>	-	14	25	μs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t <sub>SBYHO</sub>	-	43	52	μs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t <sub>SBYHO</sub>	-	44	52	μs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t <sub>SBYHO</sub>	-	82	110	μs	
		System clock source is MOCO		t <sub>SBYMO</sub>	-	16	25	μs	

- Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
- Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
- Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
- Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.
- Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

Table 2.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t <sub>SBYEX</sub>	-	2.9	10	μs	
		System clock source is HOCO*4		t <sub>SBYHO</sub>	-	38	50	μs	
		System clock source is MOCO (8 MHz)		t <sub>SBYMO</sub>	-	3.5	5.5	μs	

- Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
- Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
- Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
- Note 4. The system clock is 12 MHz.

## 2.3.4 唤醒时间

Table 2.22 从低功耗模式恢复的时间(1)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	High-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器 (20MHz) *2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器 (20MHz) *3	t <sub>SBYEX</sub>	-	14	25	μs	
		系统时钟源为HOCO*4 (HOCO时钟为32MHz)		t <sub>SBYHO</sub>	-	43	52	μs	
		系统时钟源为HOCO*4 (HOCO时钟为48MHz)		t <sub>SBYHO</sub>	-	44	52	μs	
		系统时钟源为HOCO*5 (HOCO时钟为64MHz)		t <sub>SBYHO</sub>	-	82	110	μs	
		系统时钟源为MOCO		t <sub>SBYMO</sub>	-	16	25	μs	

- Note 1. ICK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。
- Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
- Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。
- Note 4. HOCO时钟等待控制寄存器(HOCOWTCR)设置为05h。
- Note 5. HOCO时钟等待控制寄存器(HOCOWTCR)设置为06h。

Table 2.23 从低功耗模式恢复的时间(2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Middle-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器(12MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器(12MHz)*3	t <sub>SBYEX</sub>	-	2.9	10	μs	
		系统时钟源为HOCO*4		t <sub>SBYHO</sub>	-	38	50	μs	
		系统时钟源为MOCO(8MHz)		t <sub>SBYMO</sub>	-	3.5	5.5	μs	

- Note 1. ICK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。
- Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。
- Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。
- Note 4. 系统时钟为12MHz。

Table 2.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t <sub>SBYEX</sub>	-	28	50	μs	
		System clock source is MOCO (1 MHz)		t <sub>SBYMO</sub>	-	25	35	μs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.25 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t <sub>SBYEX</sub>	-	108	130	μs	
		System clock source is HOCO (4 MHz)		t <sub>SBYHO</sub>	-	108	130	μs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t <sub>SBYSC</sub>	-	0.85	1	ms	Figure 2.32
		System clock source is LOCO (32.768 kHz)	t <sub>SBYLO</sub>	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

Table 2.24 从低功耗模式恢复的时间(3)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-speed mode	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器(1MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器(1MHz)*3	t <sub>SBYEX</sub>	-	28	50	μs	
		系统时钟源为MOCO(1MHz)		t <sub>SBYMO</sub>	-	25	35	μs	

Note 1. ICK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。

Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。

Table 2.25 从低功耗模式恢复的时间(4)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Low-voltage mode	连接到主时钟振荡器的晶体谐振器	系统时钟源是主时钟振荡器(4MHz)*2	t <sub>SBYMC</sub>	-	2	3	ms	Figure 2.32
		主时钟振荡器的外部时钟输入	系统时钟源是主时钟振荡器(4MHz)*3	t <sub>SBYEX</sub>	-	108	130	μs	
		系统时钟源是HOCO(4MHz)		t <sub>SBYHO</sub>	-	108	130	μs	

Note 1. ICK、FCK、PCKx的分频比是允许频率范围内的最小分频比。恢复时间由系统时钟源决定。

Note 2. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为05h。

Note 3. 主时钟振荡器等待控制寄存器(MOSCWTCR)设置为00h。

Table 2.26 从低功耗模式恢复的时间(5)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	Subosc-speed mode	系统时钟源为副时钟振荡器(32.768kHz)	t <sub>SBYSC</sub>	-	0.85	1	ms	Figure 2.32
		系统时钟源为LOCO(32.768kHz)	t <sub>SBYLO</sub>	-	0.85	1.2	ms	

Note 1. 在Subosc速度模式期间,副时钟振荡器或LOCO本身在软件待机模式下继续振荡。

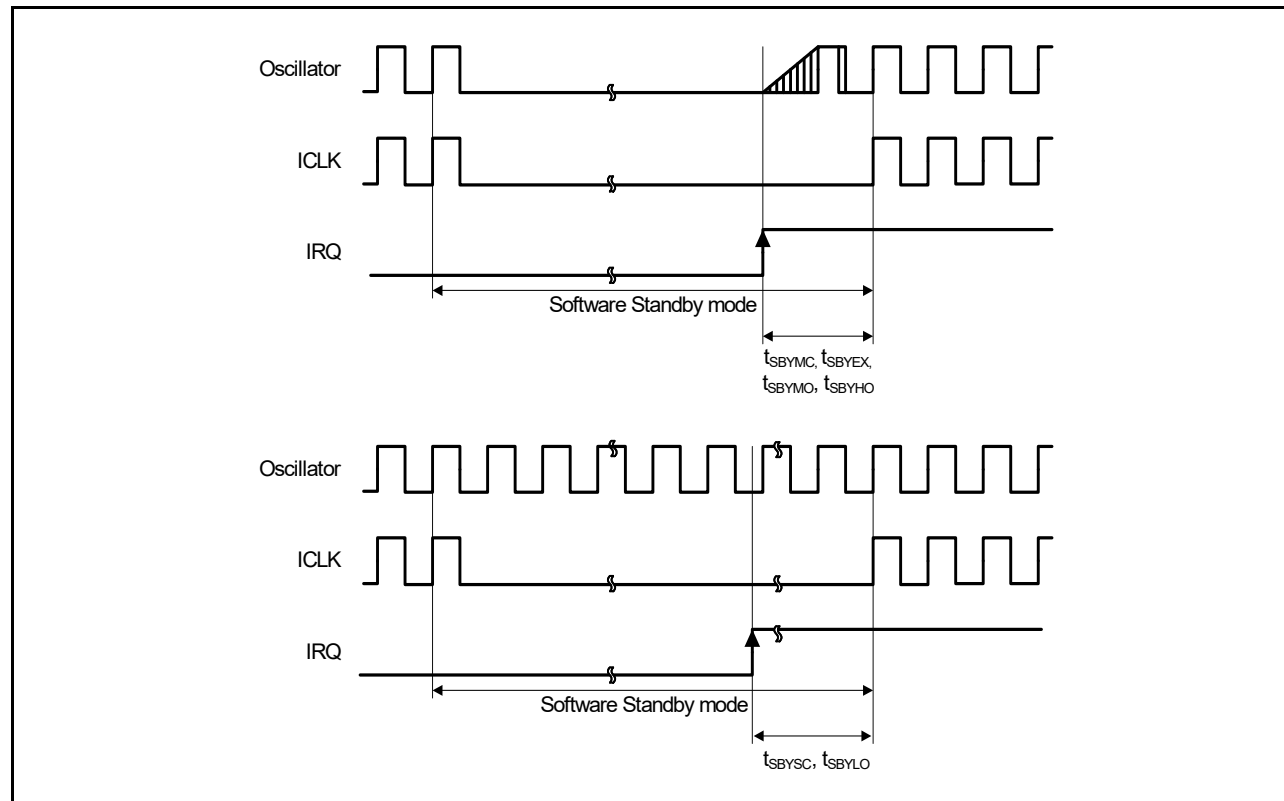


Figure 2.32 Software Standby mode cancellation timing

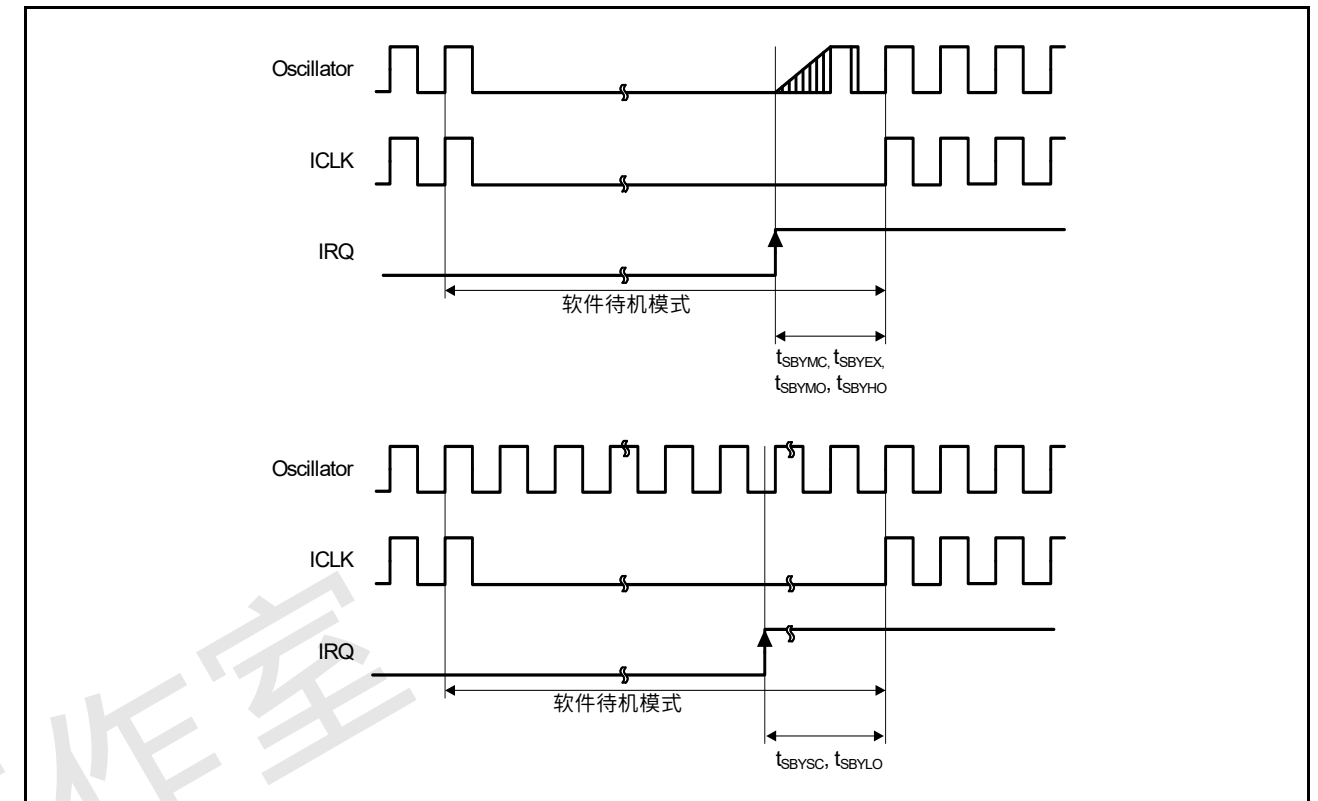


Figure 2.32 软件待机模式取消时序

Table 2.27 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	$t_{SNZ}$	-	36	45	$\mu s$	Figure 2.33
	Middle-speed mode System clock source is MOCO (8 MHz)	$t_{SNZ}$	-	1.3	3.6	$\mu s$	
	Low-speed mode System clock source is MOCO (1 MHz)	$t_{SNZ}$	-	10	13	$\mu s$	
	Low-voltage mode System clock source is HOCO (4 MHz)	$t_{SNZ}$	-	87	110	$\mu s$	

Table 2.27 从低功耗模式恢复的时间(6)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
软件恢复时间 待机模式到贪睡模式	High-speed mode 系统时钟源为HOCO	$t_{SNZ}$	-	36	45	$\mu s$	Figure 2.33
	Middle-speed mode 系统时钟源为MOCO(8MHz)	$t_{SNZ}$	-	1.3	3.6	$\mu s$	
	Low-speed mode 系统时钟源为MOCO(1MHz)	$t_{SNZ}$	-	10	13	$\mu s$	
	Low-voltage mode 系统时钟源是HOCO(4MHz)	$t_{SNZ}$	-	87	110	$\mu s$	

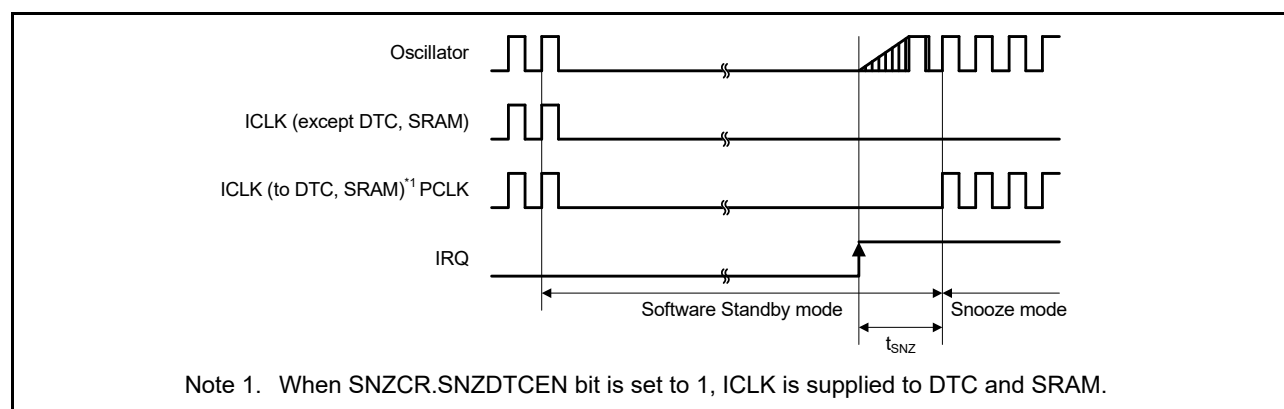


Figure 2.33 Recovery timing from Software Standby mode to Snooze mode

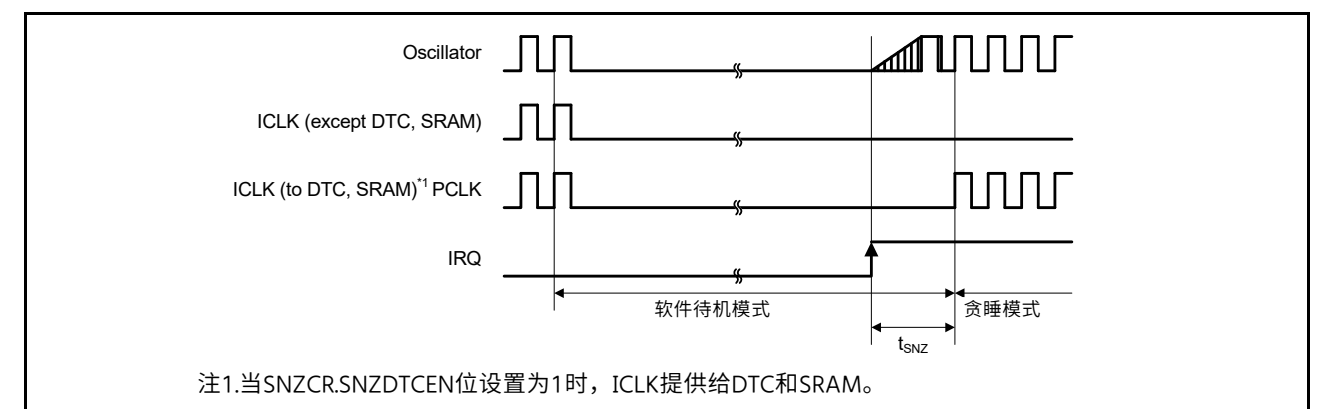


Figure 2.33 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI and IRQ Noise Filter

Table 2.28 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	$t_{NMIW}$	200	-	-	ns	NMI digital filter disabled	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	$t_{IRQW}$	200	-	-	ns	IRQ digital filter disabled	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.  
 Note: If the clock source is switched, add 4 clock cycles of the switched source.  
 Note 1.  $t_{Pcyc}$  indicates the PCLKB cycle.  
 Note 2.  $t_{NMICK}$  indicates the cycle of the NMI digital filter sampling clock.  
 Note 3.  $t_{IRQCK}$  indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

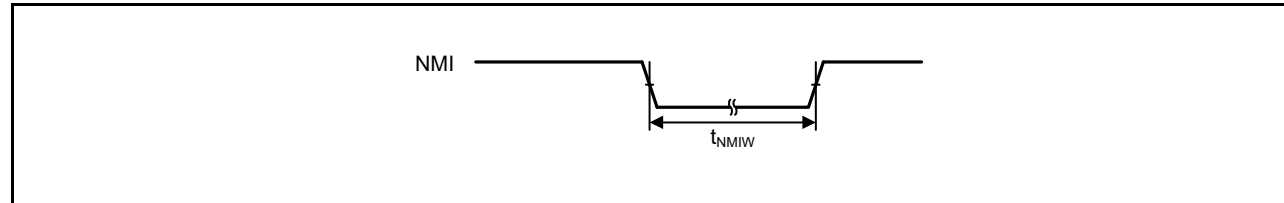


Figure 2.34 NMI interrupt input timing

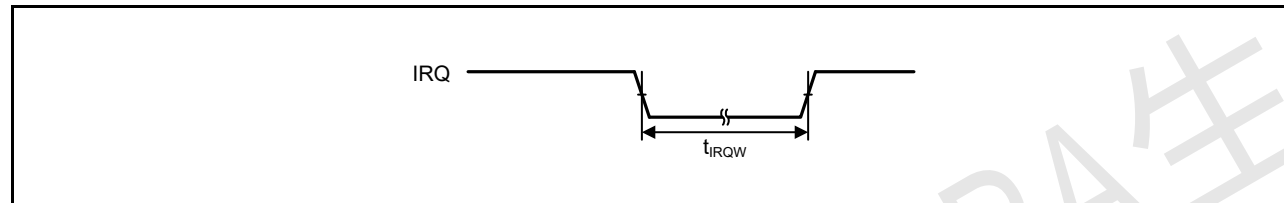


Figure 2.35 IRQ interrupt input timing

2.3.5 NMI和IRQ噪声滤波器

Table 2.28 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	$t_{NMIW}$	200	-	-	ns	NMI数字滤波器禁用	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	$t_{IRQW}$	200	-	-	ns	IRQ数字滤波器禁用	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。  
 Note: 如果时钟源切换，则增加切换源的4个时钟周期。  
 Note 1.  $t_{Pcyc}$ 表示PCLKB周期。  
 Note 2.  $t_{NMICK}$ 表示NMI数字滤波器采样时钟的周期。  
 Note 3.  $t_{IRQCK}$ 表示IRQi数字滤波器采样时钟的周期 (i=0到7)。

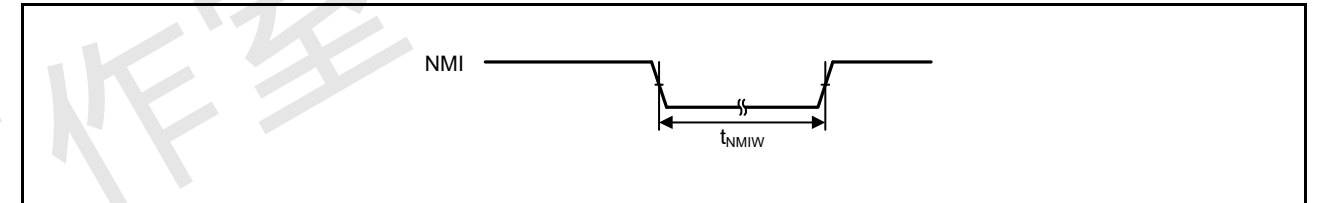


Figure 2.34 NMI中断输入时序

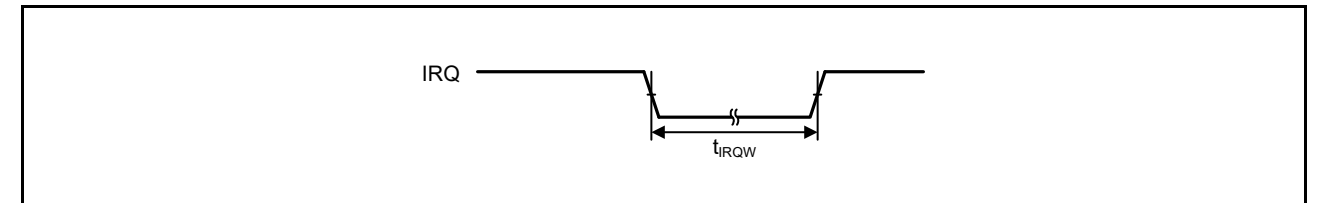


Figure 2.35 IRQ中断输入时序



2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC16 Trigger Timing

Note:

Table 2.29 I/O Ports, POEG, GPT, AGT, KINT, and ADC16 trigger timing

Parameter		Symbol	Min	Max	Unit	Test conditions	
I/O Ports	Input data pulse width	$t_{PRW}$	1.5	-	$t_{Pcyc}$	Figure 2.36	
POEG	POEG input trigger pulse width	$t_{POEW}$	3	-	$t_{Pcyc}$	Figure 2.37	
GPT	Input capture pulse width	$t_{GTICW}$	Single edge	1.5	-	$t_{PDcyc}$	Figure 2.38
			Dual edge	2.5	-		
AGT	AGTIO, AGTEE input cycle	$t_{ACYC}^{*1}$	$2.7 V \leq VCC \leq 5.5 V$	250	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	500	-		
			$1.8 V \leq VCC < 2.4 V$	1000	-		
			$1.6 V \leq VCC < 1.8 V$	2000	-		
	AGTIO, AGTEE input high-level width, low-level width	$t_{ACKWH}$ , $t_{ACKWL}$	$2.7 V \leq VCC \leq 5.5 V$	100	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	200	-		
			$1.8 V \leq VCC < 2.4 V$	400	-		
			$1.6 V \leq VCC < 1.8 V$	800	-		
	AGTIO, AGTO, AGTOA, AGTOB output cycle	$t_{ACYC2}$	$2.7 V \leq VCC \leq 5.5 V$	62.5	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	125	-		
			$1.8 V \leq VCC < 2.4 V$	250	-		
			$1.6 V \leq VCC < 1.8 V$	500	-		
ADC16	16-bit A/D converter trigger input pulse width	$t_{TRGW}$	1.5	-	$t_{Pcyc}$	Figure 2.40	
KINT	KRn (n = 00 to 07) pulse width	$t_{KR}$	250	-	ns	Figure 2.41	

Note:  $t_{Pcyc}$ : PCLKB cycle,  $t_{PDcyc}$ : PCLKD cycle.

Note 1. Constraints on input cycle:

When not switching the source clock:  $t_{Pcyc} \times 2 < t_{ACYC}$  should be satisfied.

When switching the source clock:  $t_{Pcyc} \times 6 < t_{ACYC}$  should be satisfied.

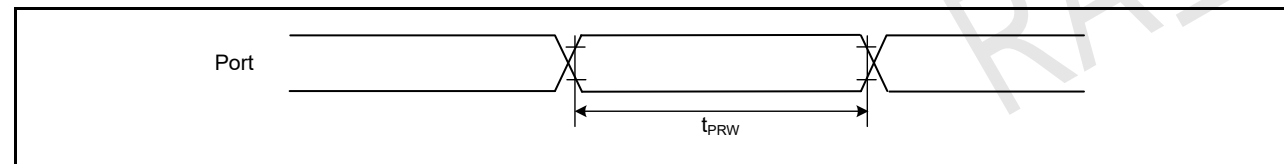


Figure 2.36 I/O ports input timing

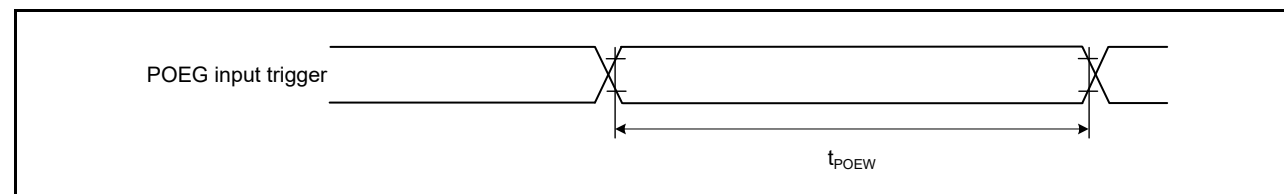


Figure 2.37 POEG input trigger timing

2.3.6 IO端口、POEG、GPT、AGT、KINT和ADC16触发时序

Note:

Table 2.29 IO端口、POEG、GPT、AGT、KINT和ADC16触发时序

Parameter		Symbol	Min	Max	Unit	测试条件	
I/O Ports	输入数据脉冲宽度	$t_{PRW}$	1.5	-	$t_{Pcyc}$	Figure 2.36	
POEG	POEG输入触发脉冲宽度	$t_{POEW}$	3	-	$t_{Pcyc}$	Figure 2.37	
GPT	输入捕捉脉冲宽度	$t_{GTICW}$	单边	1.5	-	$t_{PDcyc}$	Figure 2.38
			双刃	2.5	-		
AGT	AGTIO、AGTEE输入周期	$t_{ACYC}^{*1}$	$2.7 V \leq VCC \leq 5.5 V$	250	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	500	-		
			$1.8 V \leq VCC < 2.4 V$	1000	-		
			$1.6 V \leq VCC < 1.8 V$	2000	-		
	AGTIO、AGTEE输入高电平宽度、低电平宽度	$t_{ACKWH}$ , $t_{ACKWL}$	$2.7 V \leq VCC \leq 5.5 V$	100	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	200	-		
			$1.8 V \leq VCC < 2.4 V$	400	-		
			$1.6 V \leq VCC < 1.8 V$	800	-		
	AGTIO、AGTO、AGTOA、AGTOB输出周期	$t_{ACYC2}$	$2.7 V \leq VCC \leq 5.5 V$	62.5	-	ns	Figure 2.39
			$2.4 V \leq VCC < 2.7 V$	125	-		
			$1.8 V \leq VCC < 2.4 V$	250	-		
			$1.6 V \leq VCC < 1.8 V$	500	-		
ADC16	16位模数转换器触发输入脉冲宽度	$t_{TRGW}$	1.5	-	$t_{Pcyc}$	Figure 2.40	
KINT	KRn(n=00to07)脉冲宽度	$t_{KR}$	250	-	ns	Figure 2.41	

注:  $t_{Pcyc}$ : PCLKB周期,  $t_{PDcyc}$ : PCLKD周期。注

1.输入周期约束:

不切换源时钟时:  $t_{Pcyc} \times 2 < t_{ACYC}$ 应满足。

切换源时钟时:  $t_{Pcyc} \times 6 < t_{ACYC}$ 应满足。

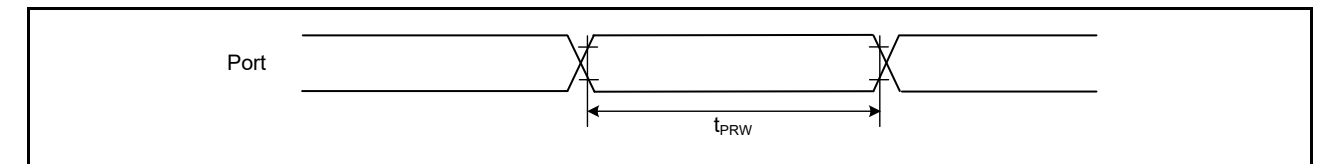


Figure 2.36 IO端口输入时序

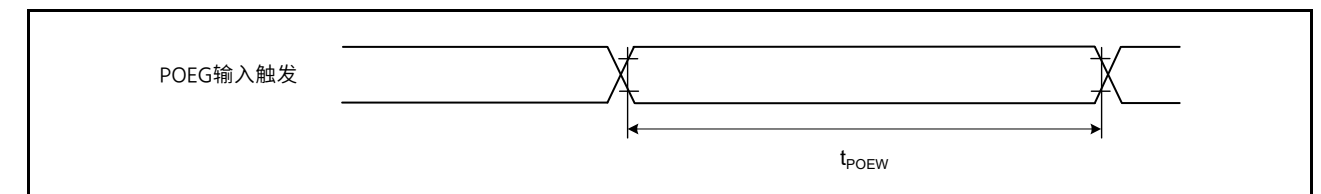


Figure 2.37 POEG输入触发时序

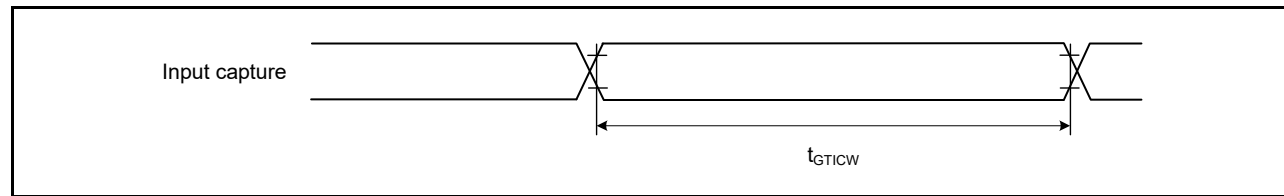


Figure 2.38 GPT input capture timing

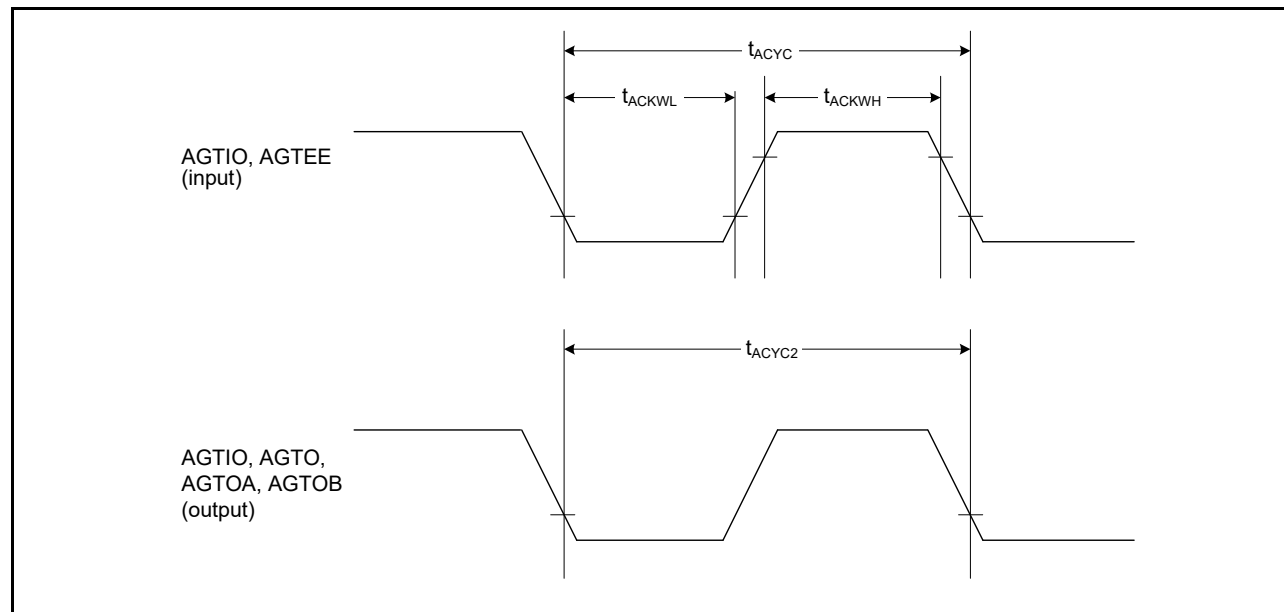


Figure 2.39 AGT I/O timing

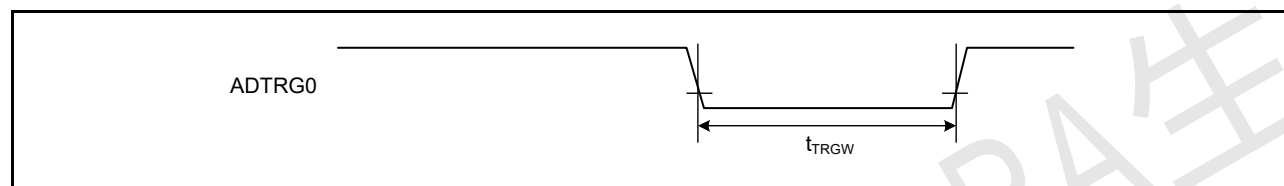


Figure 2.40 ADC16 trigger input timing

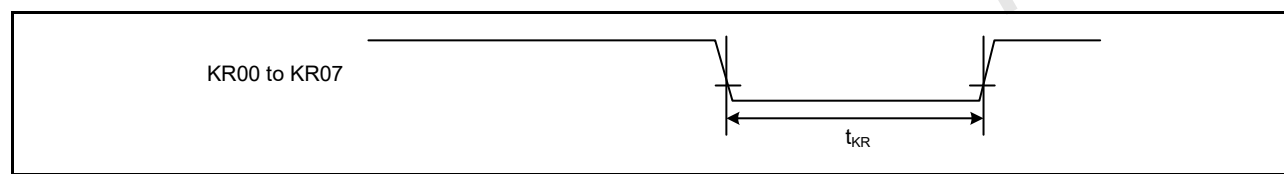


Figure 2.41 Key interrupt input timing

2.3.7 CAC Timing

Table 2.30 CAC timing  
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
CAC CACREF input pulse width	$t_{CACREF}$	$t_{Pcyc}^{*1} \leq t_{cac}^{*2}$	$4.5 \times t_{cac} + 3 \times t_{Pcyc}$	-	-	ns
		$t_{Pcyc}^{*1} > t_{cac}^{*2}$	$5 \times t_{cac} + 6.5 \times t_{Pcyc}$	-	-	ns

Note 1.  $t_{Pcyc}$ : PCLKB cycle.

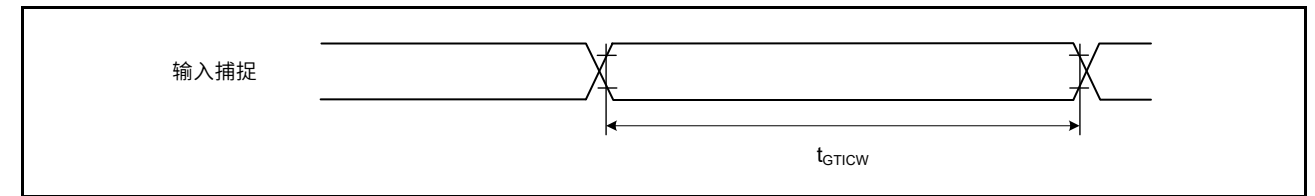


Figure 2.38 GPT输入捕捉时序

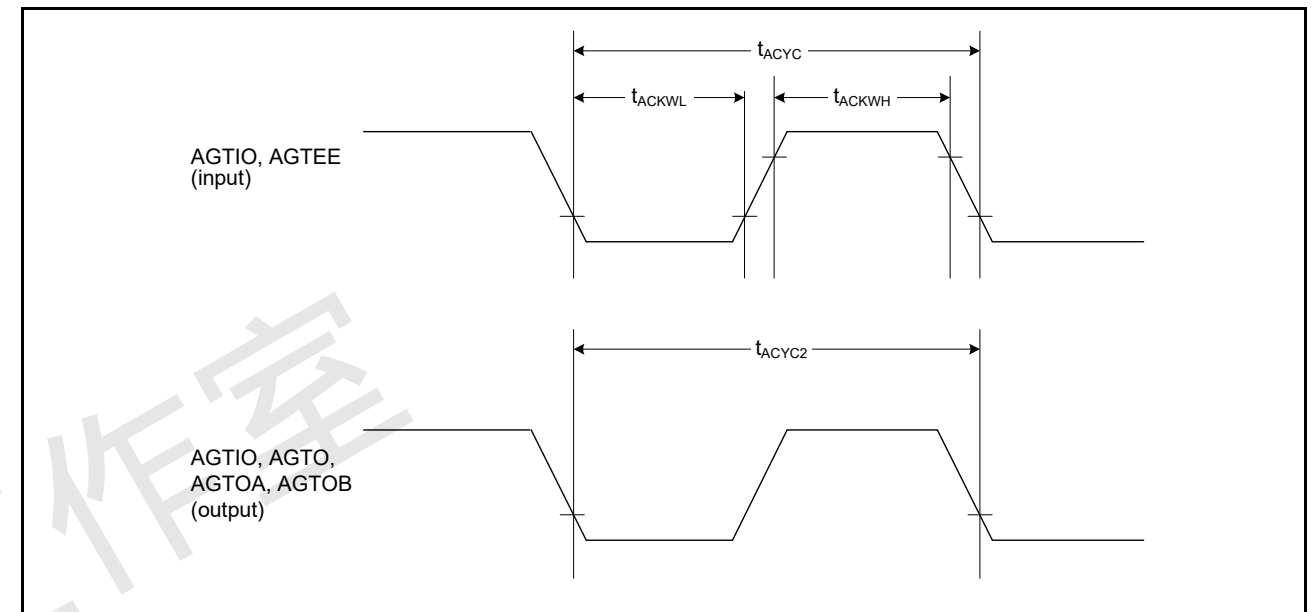


Figure 2.39 AGT I/O timing

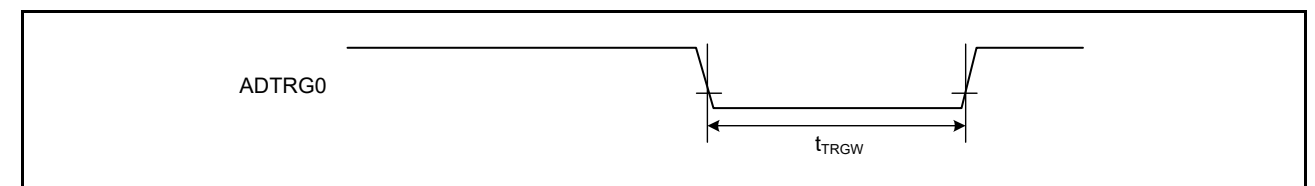


Figure 2.40 ADC16触发输入时序

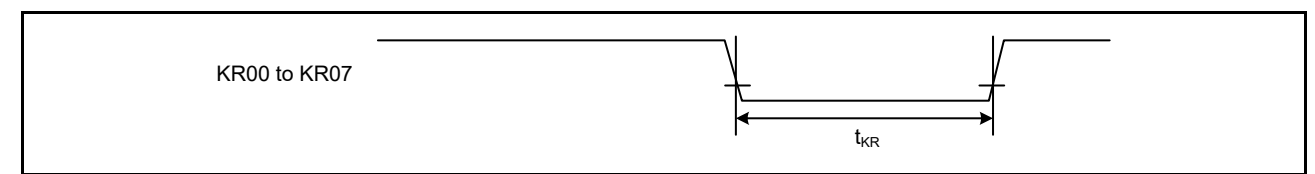


Figure 2.41 按键中断输入时序

2.3.7 CAC时序

Table 2.30 CAC计时  
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
CAC CACREF输入脉冲宽度	$t_{CACREF}$	$t_{Pcyc}^{*1} \leq t_{cac}^{*2}$	$4.5 \times t_{cac} + 3 \times t_{Pcyc}$	-	-	ns
		$t_{Pcyc}^{*1} > t_{cac}^{*2}$	$5 \times t_{cac} + 6.5 \times t_{Pcyc}$	-	-	ns

Note 1.  $t_{Pcyc}$ : PCLKB cycle.

Note 2.  $t_{cac}$ : CAC count clock source cycle.

### 2.3.8 SCI Timing

**Table 2.31 SCI timing (1)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Max	Unit*1	Test conditions	
SCI	Input clock cycle	Asynchronous	4	-	$t_{Pcyc}$	Figure 2.42
		Clock synchronous	6	-		
Input clock pulse width	$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
Input clock rise time	$t_{SCKr}$	-	20	ns		
Input clock fall time	$t_{SCKf}$	-	20	ns		
Output clock cycle	Asynchronous	6	-	$t_{Pcyc}$		
	Clock synchronous	4	-			
Output clock pulse width	$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
Output clock rise time	$t_{SCKr}$	$1.8 V \leq VCC \leq 5.5 V$	-	20	ns	
		$1.6 V \leq VCC < 1.8 V$	-	30		
Output clock fall time	$t_{SCKf}$	$1.8 V \leq VCC \leq 5.5 V$	-	20	ns	
		$1.6 V \leq VCC < 1.8 V$	-	30		
Transmit data delay (master)	Clock synchronous	$1.8 V \leq VCC \leq 5.5 V$	-	40	ns	Figure 2.43
		$1.6 V \leq VCC < 1.8 V$	-	45		
Transmit data delay (slave)	Clock synchronous	$2.7 V \leq VCC \leq 5.5 V$	-	55	ns	
		$2.4 V \leq VCC < 2.7 V$	-	60		
		$1.8 V \leq VCC < 2.4 V$	-	100		
		$1.6 V \leq VCC < 1.8 V$	-	125		
Receive data setup time (master)	Clock synchronous	$2.7 V \leq VCC \leq 5.5 V$	45	-	ns	
		$2.4 V \leq VCC < 2.7 V$	55	-		
		$1.8 V \leq VCC < 2.4 V$	90	-		
		$1.6 V \leq VCC < 1.8 V$	110	-		
Receive data setup time (slave)	Clock synchronous	$2.7 V \leq VCC \leq 5.5 V$	40	-	ns	
		$1.6 V \leq VCC < 2.7 V$	45	-		
Receive data hold time (master)	Clock synchronous	$t_{RXH}$	5	-	ns	
Receive data hold time (slave)	Clock synchronous	$t_{RXH}$	40	-	ns	

Note 1.  $t_{Pcyc}$ : PCLKB cycle.

Note 2.  $t_{cac}$ : CAC计数时钟源周期。

### 2.3.8 SCI时序

**Table 2.31 SCI时序 (1)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Max	Unit*1	测试条件	
SCI	输入时钟周期	Asynchronous	4	-	$t_{Pcyc}$	Figure 2.42
		时钟同步	6	-		
输入时钟脉冲宽度	$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
输入时钟上升时间	$t_{SCKr}$	-	20	ns		
输入时钟下降时间	$t_{SCKf}$	-	20	ns		
输出时钟周期	Asynchronous	6	-	$t_{Pcyc}$		
	时钟同步	4	-			
输出时钟脉冲宽度	$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
输出时钟上升时间	$t_{SCKr}$	$1.8 V \leq VCC \leq 5.5 V$	-	20	ns	
		$1.6 V \leq VCC < 1.8 V$	-	30		
输出时钟下降时间	$t_{SCKf}$	$1.8 V \leq VCC \leq 5.5 V$	-	20	ns	
		$1.6 V \leq VCC < 1.8 V$	-	30		
传输数据延迟 (主)	时钟同步	$1.8 V \leq VCC \leq 5.5 V$	-	40	ns	Figure 2.43
		$1.6 V \leq VCC < 1.8 V$	-	45		
传输数据延迟 (从)	时钟同步	$2.7 V \leq VCC \leq 5.5 V$	-	55	ns	
		$2.4 V \leq VCC < 2.7 V$	-	60		
		$1.8 V \leq VCC < 2.4 V$	-	100		
		$1.6 V \leq VCC < 1.8 V$	-	125		
接收数据建立时间 (主)	时钟同步	$2.7 V \leq VCC \leq 5.5 V$	45	-	ns	
		$2.4 V \leq VCC < 2.7 V$	55	-		
		$1.8 V \leq VCC < 2.4 V$	90	-		
		$1.6 V \leq VCC < 1.8 V$	110	-		
接收数据建立时间 (从机)	时钟同步	$2.7 V \leq VCC \leq 5.5 V$	40	-	ns	
		$1.6 V \leq VCC < 2.7 V$	45	-		
接收数据保持时间 (主机)	时钟同步	$t_{RXH}$	5	-	ns	
接收数据保持时间 (从机)	时钟同步	$t_{RXH}$	40	-	ns	

Note 1.  $t_{Pcyc}$ : PCLKB cycle.

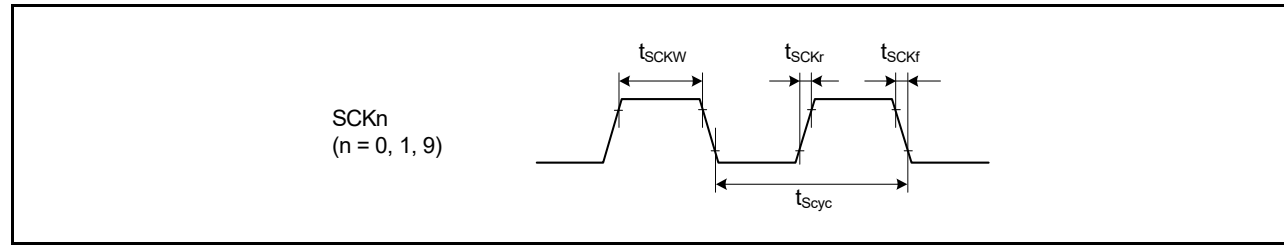


Figure 2.42 SCK clock input timing

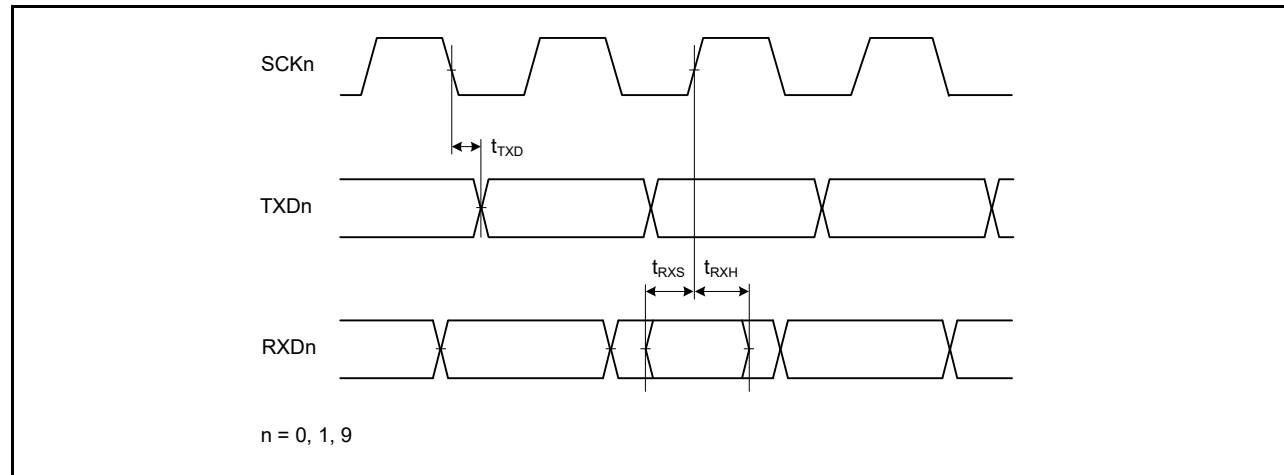


Figure 2.43 SCI input/output timing in clock synchronous mode

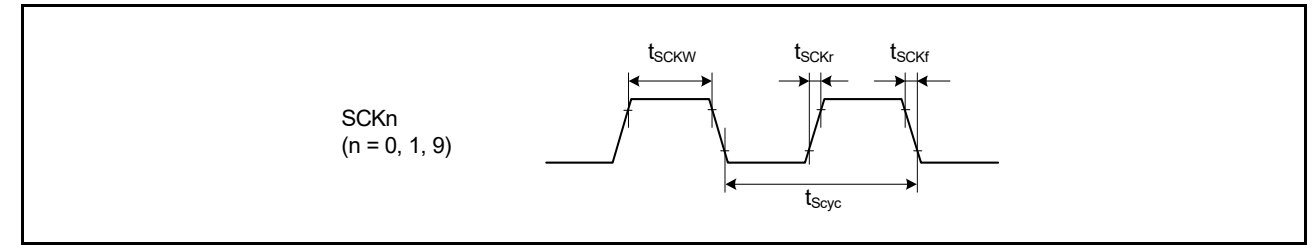


Figure 2.42 SCK时钟输入时序

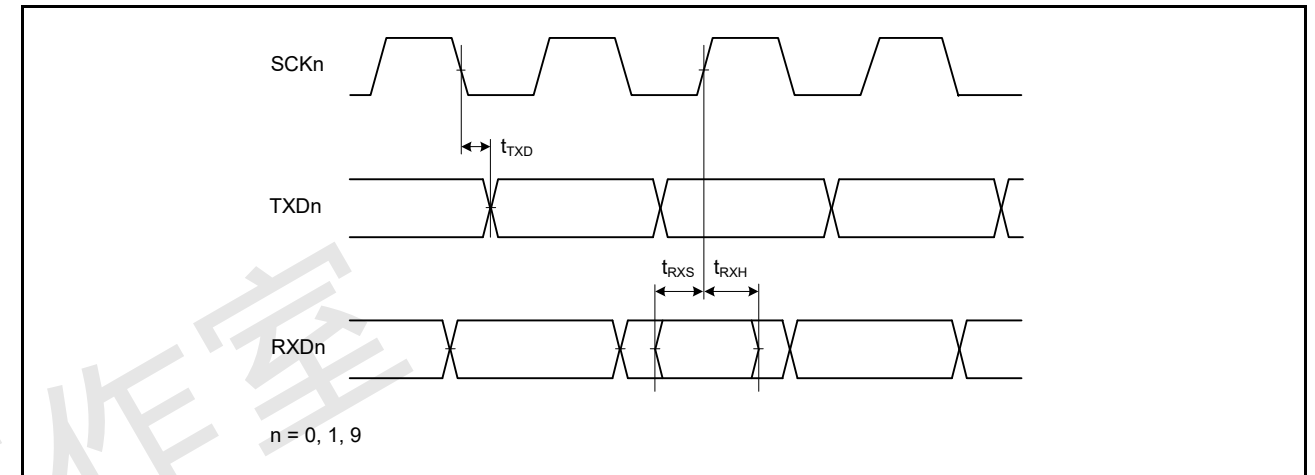


Figure 2.43 时钟同步模式下的SCI输入输出时序

Table 2.32 SCI timing (2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Max	Unit*1	Test conditions		
Simple SPI	SCK clock cycle output (master)	$t_{SPcyc}$	4	65536	$t_{Pcyc}$	Figure 2.44	
	SCK clock cycle input (slave)		6	65536			
	SCK clock high pulse width	$t_{SPCKWH}$	0.4	0.6	$t_{SPcyc}$		
	SCK clock low pulse width	$t_{SPCKWL}$	0.4	0.6	$t_{SPcyc}$		
	SCK clock rise and fall time	$t_{SPCKr}, t_{SPCKf}$	$1.8 V \leq VCC \leq 5.5 V$	-	20		ns
			$1.6 V \leq VCC < 1.8 V$	-	30		
	Data input setup time	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{SU}$	45	ns	Figure 2.45 to Figure 2.48
			$2.4 V \leq VCC < 2.7 V$		55		
			$1.8 V \leq VCC < 2.4 V$		80		
			$1.6 V \leq VCC < 1.8 V$		110		
Slave		$2.7 V \leq VCC \leq 5.5 V$		40			
		$1.6 V \leq VCC < 2.7 V$		45			
Data input hold time	Master	$t_H$	33.3	-	ns		
	Slave		40	-			
SS input setup time	$t_{LEAD}$	1	-	$t_{SPcyc}$			
SS input hold time	$t_{LAG}$	1	-	$t_{SPcyc}$			
Data output delay	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{OD}$	-	ns		
		$1.6 V \leq VCC < 1.8 V$		-		40	
	Slave	$2.4 V \leq VCC \leq 5.5 V$		-		50	
		$1.8 V \leq VCC < 2.4 V$		-		65	
		$1.6 V \leq VCC < 1.8 V$		-		100	
Data output hold time	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{OH}$	-10	ns		
		$2.4 V \leq VCC < 2.7 V$		-20			
		$1.8 V \leq VCC < 2.4 V$		-30			
		$1.6 V \leq VCC < 1.8 V$		-40			
	Slave			-10		-	
Data rise and fall time	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{Dr}, t_{Df}$	-	ns		
		$1.6 V \leq VCC < 1.8 V$		-		20	
	Slave	$1.8 V \leq VCC \leq 5.5 V$		-		30	
		$1.6 V \leq VCC < 1.8 V$		-		20	
Simple SPI	Slave access time	$t_{SA}$	-	6	$t_{Pcyc}$	Figure 2.48	
	Slave output release time	$t_{REL}$	-	6	$t_{Pcyc}$		

Note 1.  $t_{Pcyc}$ : PCLKB cycle.

Table 2.32 SCI时序 (2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter	Symbol	Min	Max	Unit*1	测试条件		
Simple SPI	SCK时钟周期输出 (主机)	$t_{SPcyc}$	4	65536	$t_{Pcyc}$	Figure 2.44	
	SCK时钟周期输入 (从机)		6	65536			
	SCK时钟高脉冲宽度	$t_{SPCKWH}$	0.4	0.6	$t_{SPcyc}$		
	SCK时钟低脉冲宽度	$t_{SPCKWL}$	0.4	0.6	$t_{SPcyc}$		
	SCK时钟上升和下降时间	$t_{SPCKr}, t_{SPCKf}$	$1.8 V \leq VCC \leq 5.5 V$	-	20		ns
			$1.6 V \leq VCC < 1.8 V$	-	30		
	数据输入建立时间	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{SU}$	45	ns	图2.45至 Figure 2.48
			$2.4 V \leq VCC < 2.7 V$		55		
			$1.8 V \leq VCC < 2.4 V$		80		
			$1.6 V \leq VCC < 1.8 V$		110		
Slave		$2.7 V \leq VCC \leq 5.5 V$	40				
		$1.6 V \leq VCC < 2.7 V$	45				
数据输入保持时间	Master	$t_H$	33.3	-	ns		
	Slave		40	-			
SS输入建立时间	$t_{LEAD}$	1	-	$t_{SPcyc}$			
SS输入保持时间	$t_{LAG}$	1	-	$t_{SPcyc}$			
数据输出延迟	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{OD}$	-	ns		
		$1.6 V \leq VCC < 1.8 V$		-		40	
	Slave	$2.4 V \leq VCC \leq 5.5 V$		-		50	
		$1.8 V \leq VCC < 2.4 V$		-		65	
		$1.6 V \leq VCC < 1.8 V$		-		100	
数据输出保持时间	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{OH}$	-10	ns		
		$2.4 V \leq VCC < 2.7 V$		-20			
		$1.8 V \leq VCC < 2.4 V$		-30			
		$1.6 V \leq VCC < 1.8 V$		-40			
	Slave			-10		-	
数据上升和下降时间	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{Dr}, t_{Df}$	-	ns		
		$1.6 V \leq VCC < 1.8 V$		-		20	
	Slave	$1.8 V \leq VCC \leq 5.5 V$		-		30	
		$1.6 V \leq VCC < 1.8 V$		-		20	
Simple SPI	从站访问时间	$t_{SA}$	-	6	$t_{Pcyc}$	Figure 2.48	
	从机输出释放时间	$t_{REL}$	-	6	$t_{Pcyc}$		

注1.  $t_{Pcyc}$ : PCLKB周期。



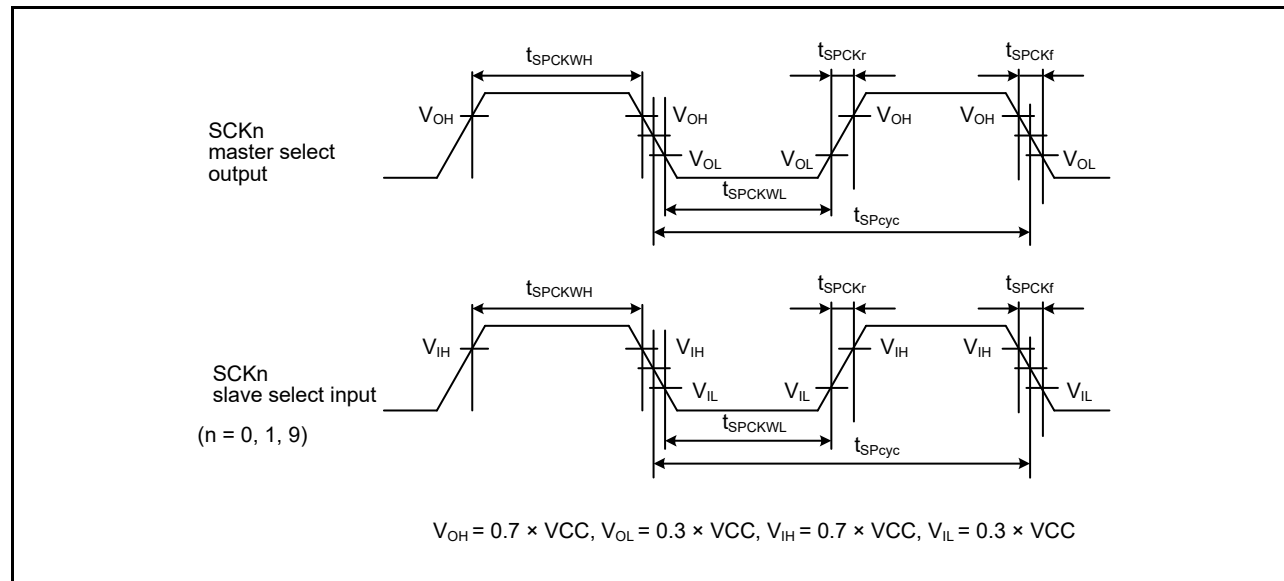


Figure 2.44 SCI simple SPI mode clock timing

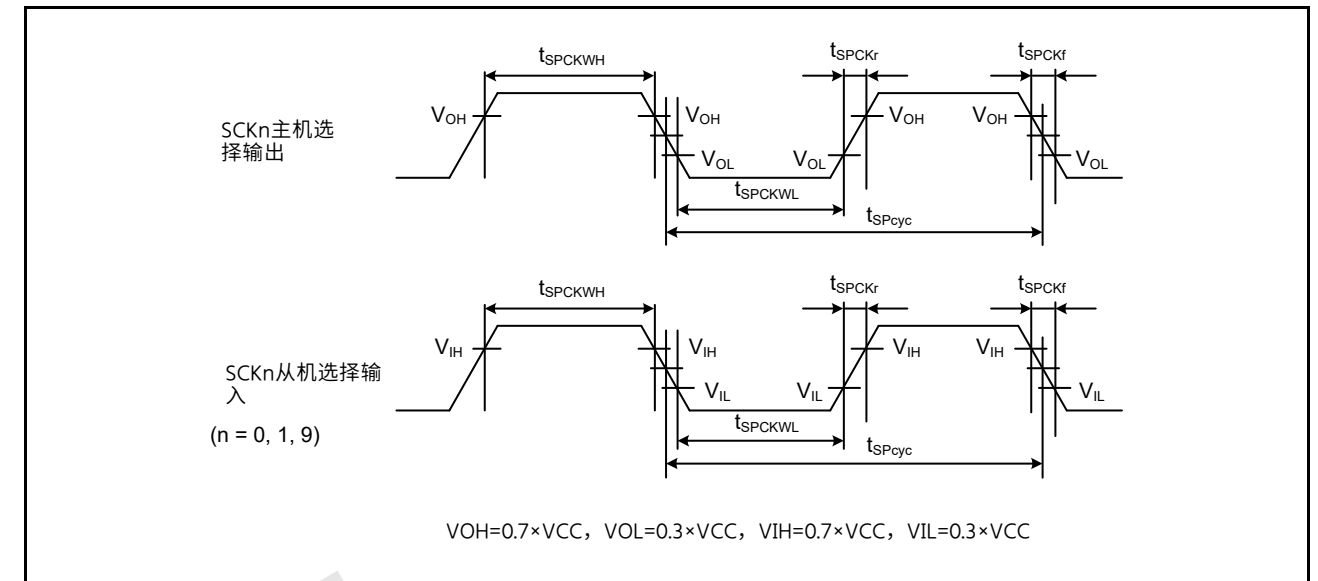


Figure 2.44 SCI简单SPI模式时钟时序

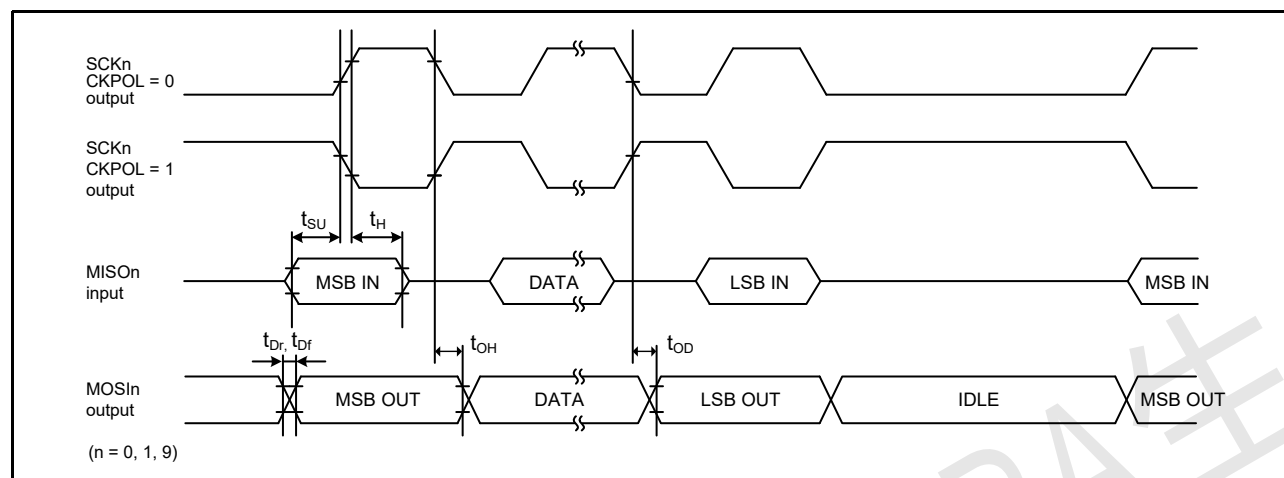


Figure 2.45 SCI simple SPI mode timing (master, CKPH = 1)

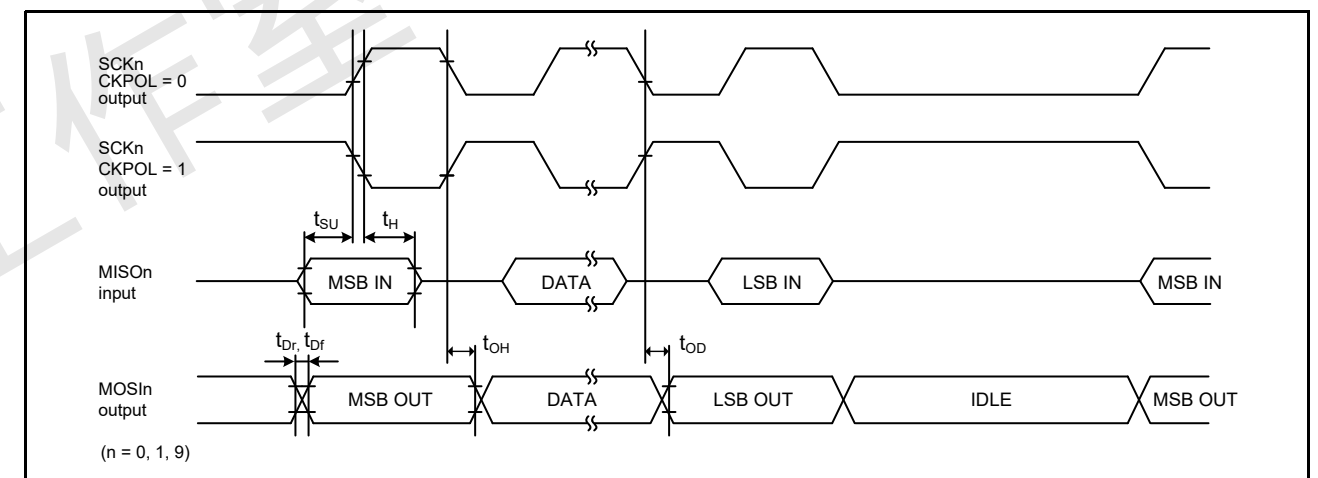


Figure 2.45 SCI简单SPI模式时序 (主机, CKPH=1)

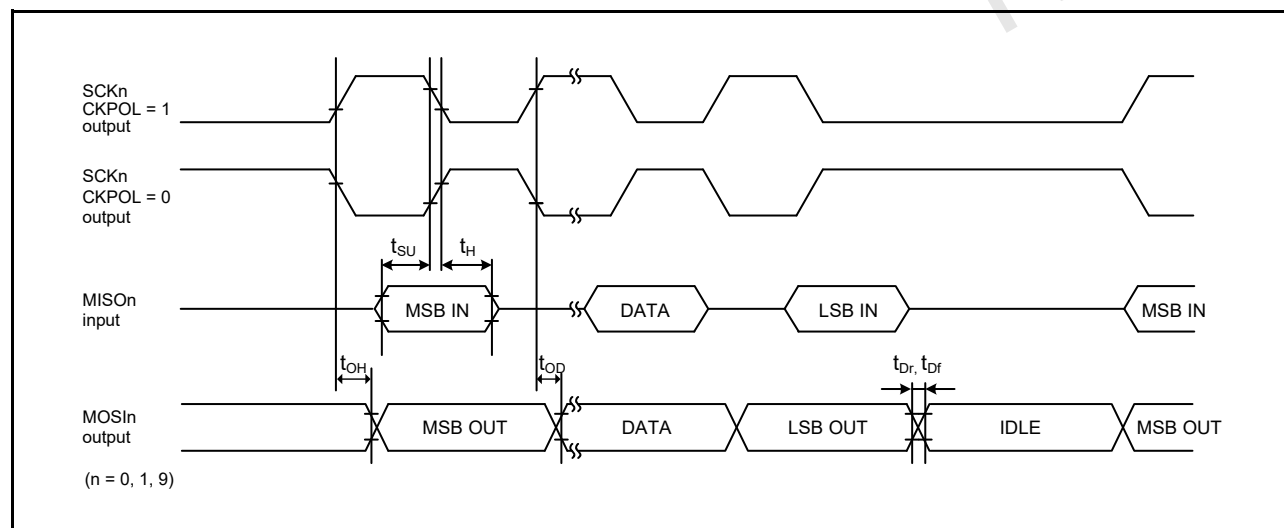


Figure 2.46 SCI simple SPI mode timing (master, CKPH = 0)

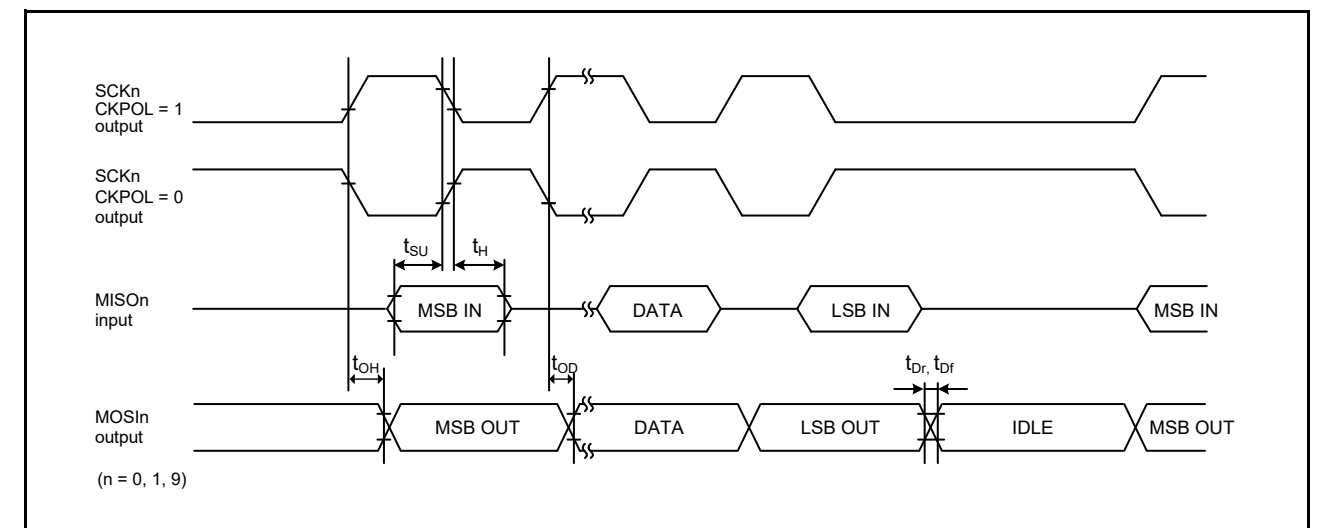


Figure 2.46 SCI简单SPI模式时序 (主机, CKPH=0)

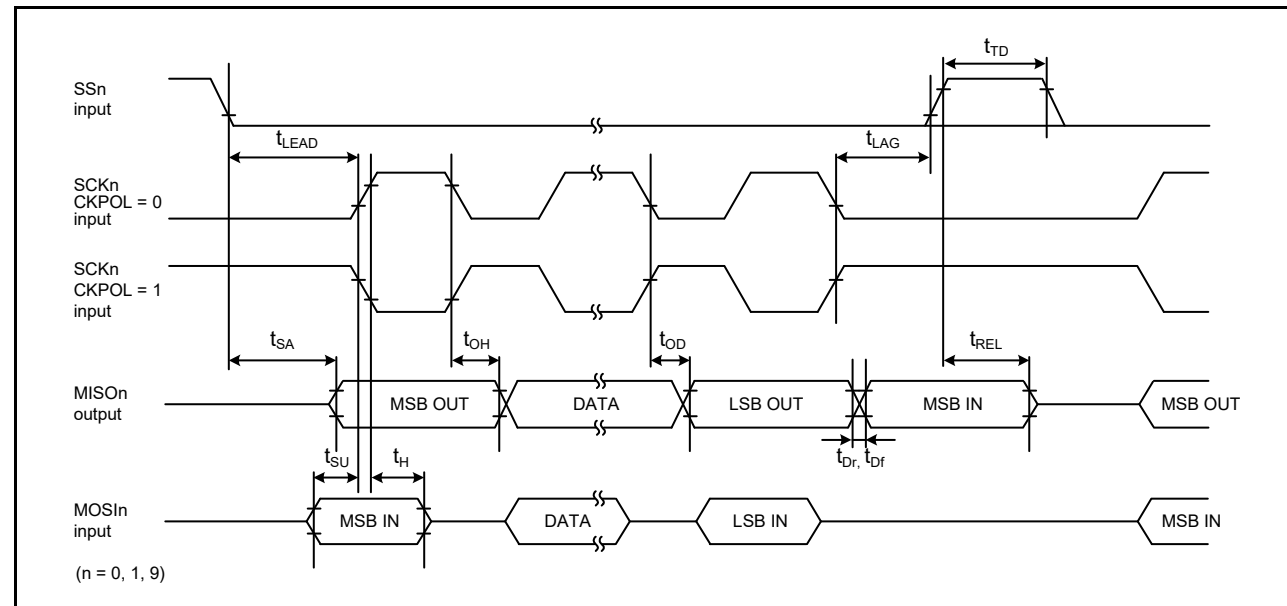


Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 1)

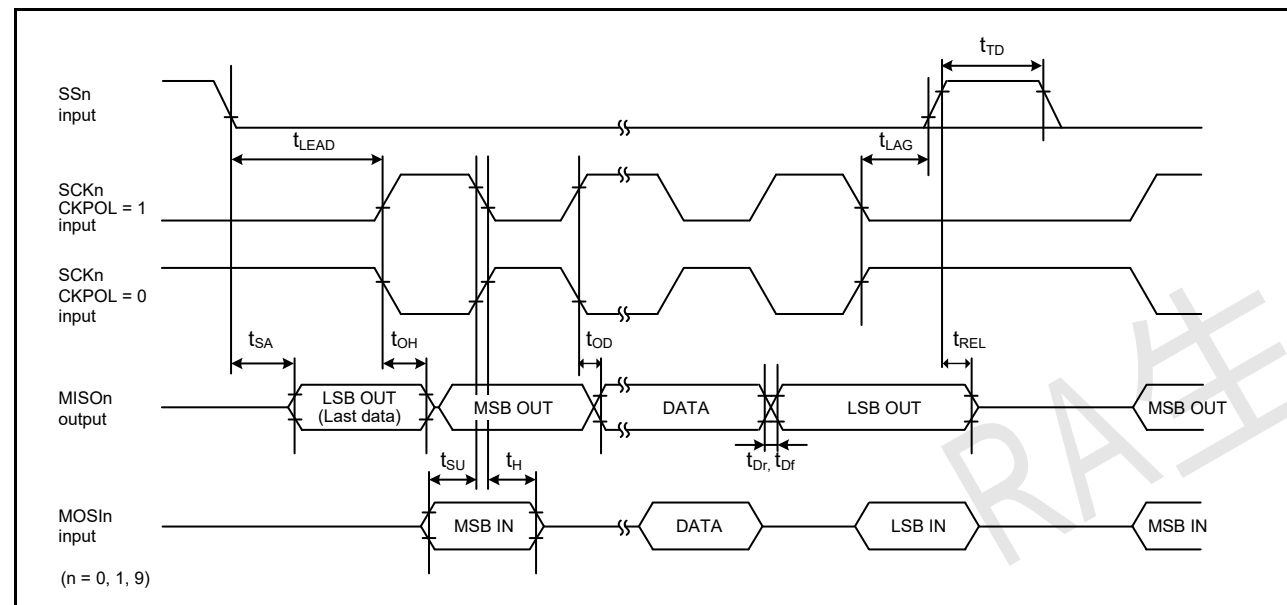


Figure 2.48 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.33 SCI timing (3)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Standard mode)	SDA input rise time	t <sub>Sr</sub>	-	1000	ns	Figure 2.49
	SDA input fall time	t <sub>Sf</sub>	-	300	ns	
	SDA input spike pulse removal time	t <sub>SP</sub>	0	4 × t <sub>IICyc</sub> *1	ns	
	Data input setup time	t <sub>SDAS</sub>	250	-	ns	
	Data input hold time	t <sub>SDAH</sub>	0	-	ns	
SCL, SDA capacitive load	C <sub>b</sub> *2	-	400	pF		

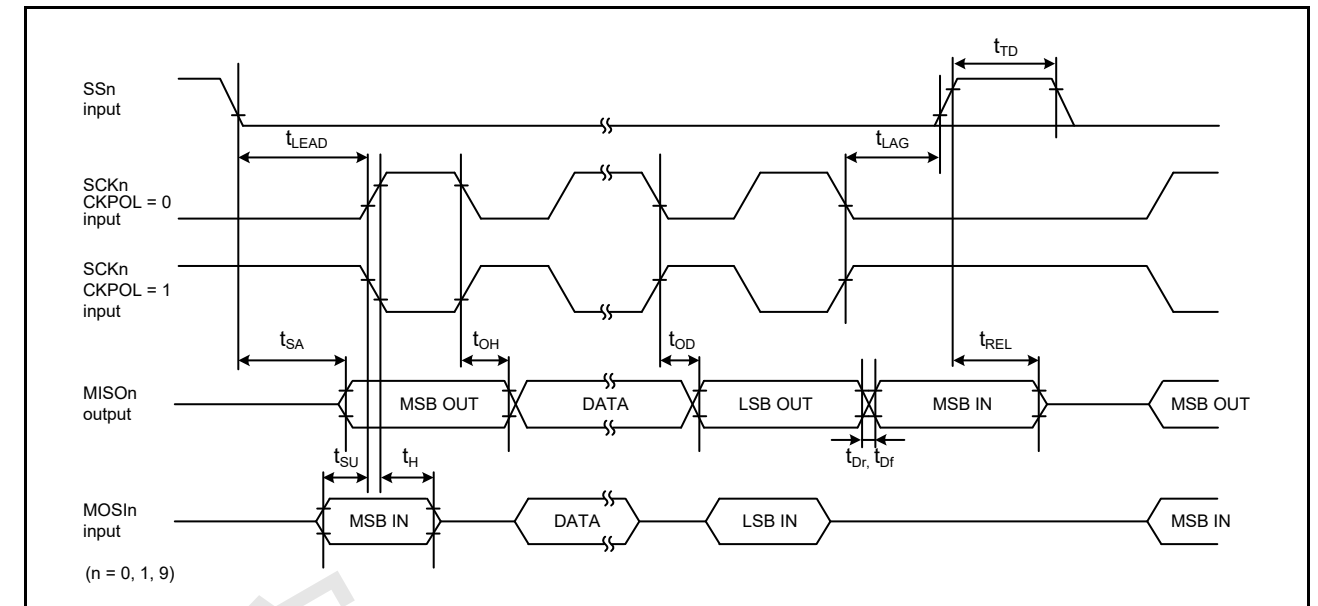


Figure 2.47 SCI简单SPI模式时序 (从机, CKPH=1)

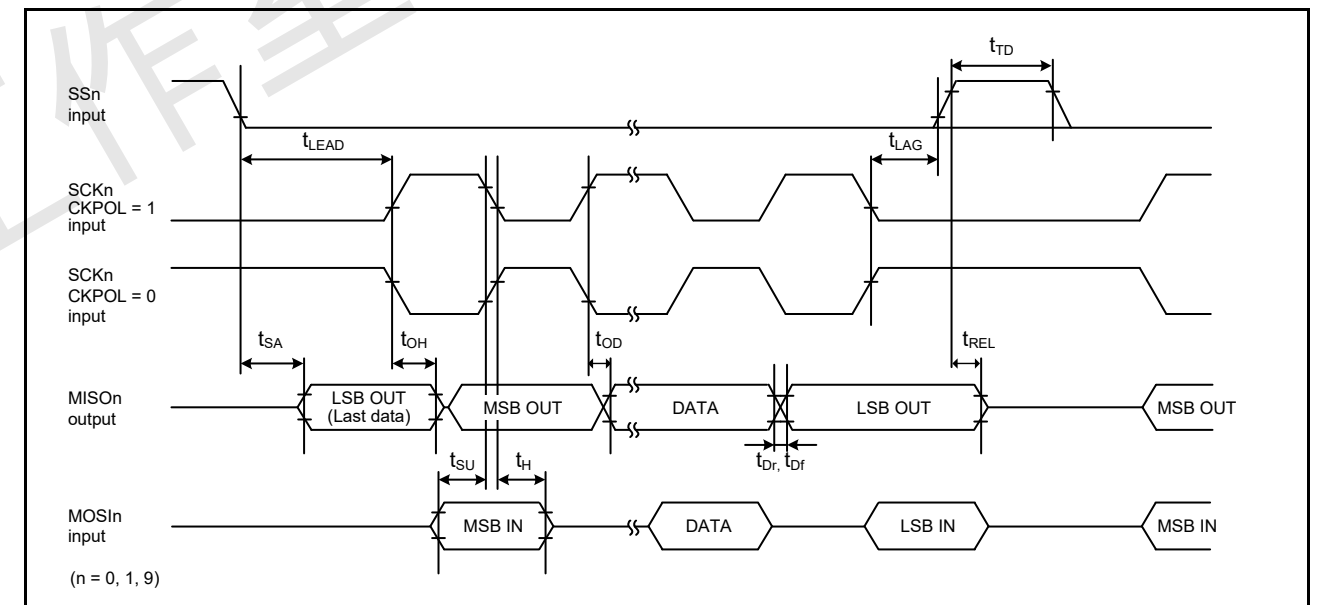


Figure 2.48 SCI简单SPI模式时序 (从机, CKPH=0)

Table 2.33 SCI时序 (3)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	测试条件	
Simple IIC (Standard mode)	SDA输入上升时间	t <sub>Sr</sub>	-	1000	ns	Figure 2.49
	SDA输入下降时间	t <sub>Sf</sub>	-	300	ns	
	SDA输入尖峰脉冲去除时间	t <sub>SP</sub>	0	4 × t <sub>IICyc</sub> *1	ns	
	数据输入建立时间	t <sub>SDAS</sub>	250	-	ns	
	数据输入保持时间	t <sub>SDAH</sub>	0	-	ns	
SCL, SDA capacitive load	C <sub>b</sub> *2	-	400	pF		

**Table 2.33 SCI timing (3)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Fast mode)	SDA input rise time	$t_{Sr}$	-	300	ns	Figure 2.49
	SDA input fall time	$t_{Sf}$	-	300	ns	
	SDA input spike pulse removal time	$t_{SP}$	0	$4 \times t_{IICcyc}^{*1}$	ns	
	Data input setup time	$t_{SDAS}$	100	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b^{*2}$	-	400	pF	

Note 1.  $t_{IICcyc}$ : Clock cycle selected by the SMR.CKS[1:0] bits.

Note 2.  $C_b$  indicates the total capacity of the bus line.

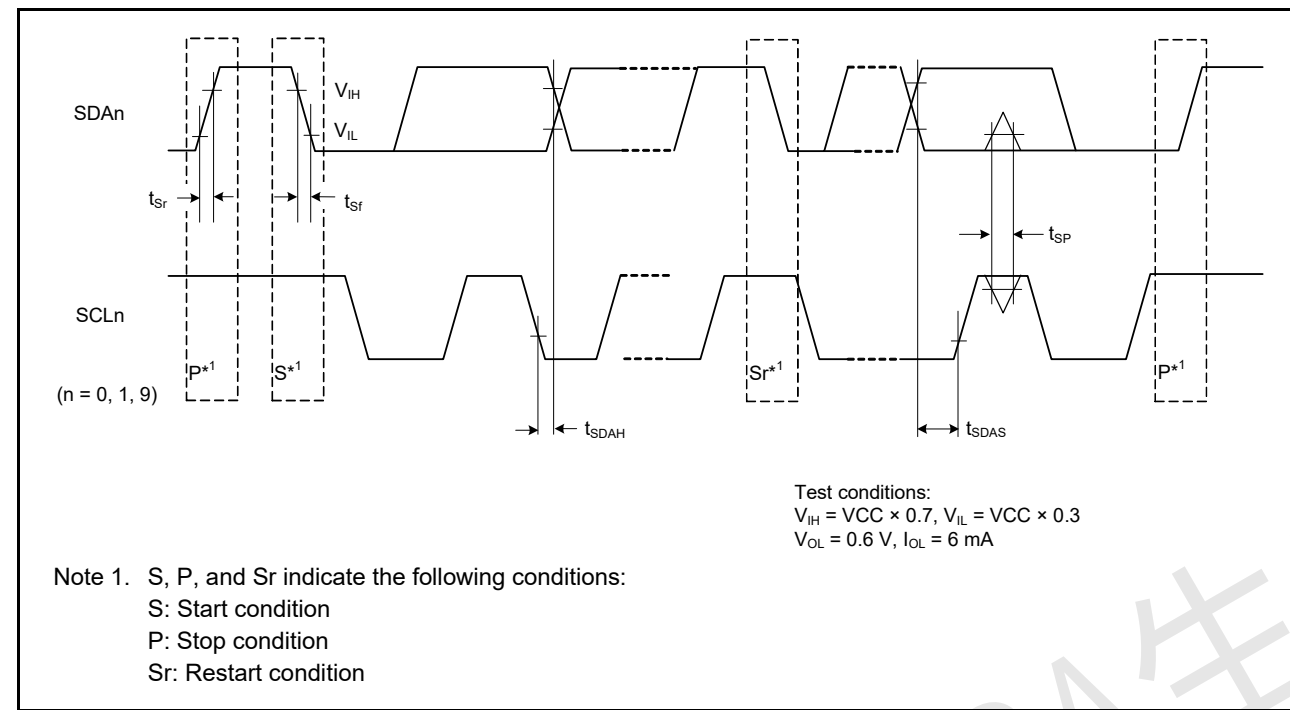


Figure 2.49 SCI simple IIC mode timing

**Table 2.33 SCI时序 (3)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	测试条件	
Simple IIC (Fast mode)	SDA输入上升时间	$t_{Sr}$	-	300	ns	Figure 2.49
	SDA输入下降时间	$t_{Sf}$	-	300	ns	
	SDA输入尖峰脉冲去除时间	$t_{SP}$	0	$4 \times t_{IICcyc}^{*1}$	ns	
	数据输入建立时间	$t_{SDAS}$	100	-	ns	
	数据输入保持时间	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b^{*2}$	-	400	pF	

Note 1.  $t_{IICcyc}$ : 由SMR.CKS[1:0]位选择的时钟周期。

Note 2.  $C_b$ 表示公交线路的总容量。

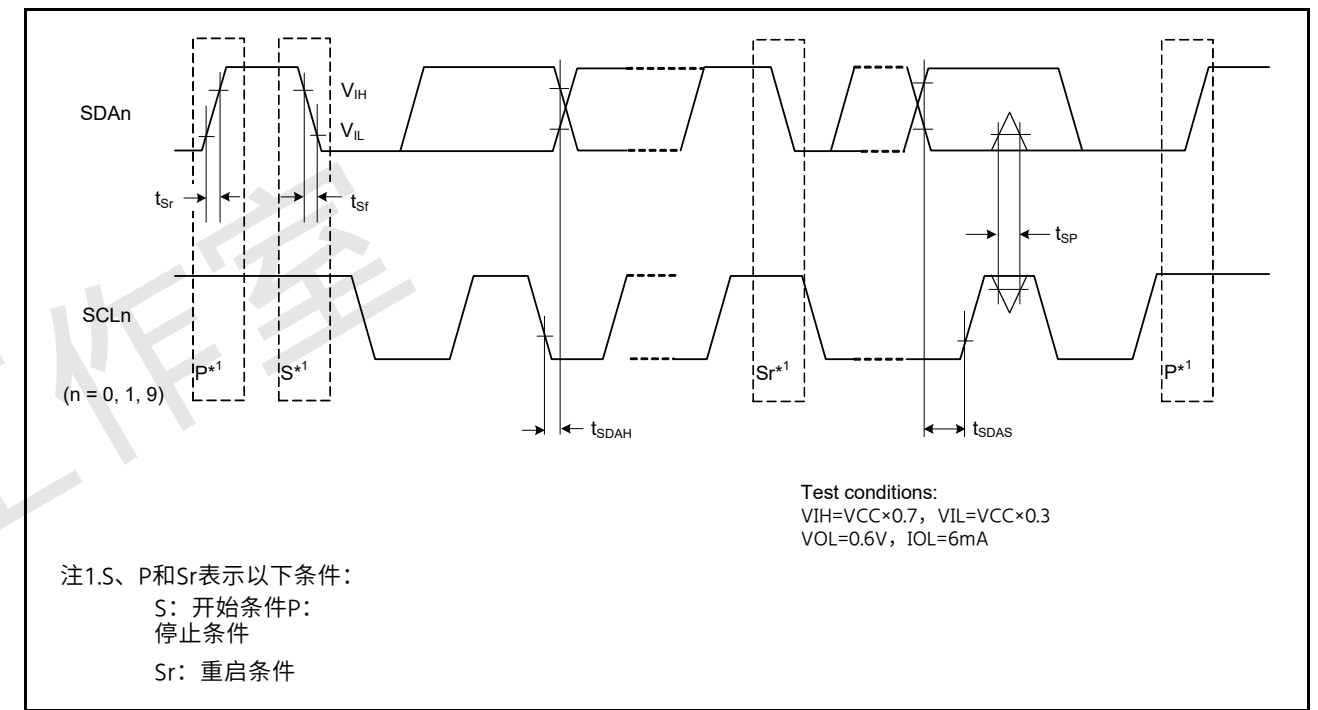


Figure 2.49 SCI简单IIC模式时序

2.3.9 SPI Timing

Table 2.34 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit*1	Test conditions	
SPI RSPCK clock cycle	Master	$t_{SPCyc}$	2	4096	$t_{Pcyc}$	Figure 2.50 C = 30 pF
	Slave		6	4096		
RSPCK clock high pulse width	Master	$t_{SPCKWH}$	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
	Slave		$3 \times t_{Pcyc}$	-		
RSPCK clock low pulse width	Master	$t_{SPCKWL}$	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
	Slave		$3 \times t_{Pcyc}$	-		
RSPCK clock rise and fall time	Output	$2.7 V \leq VCC \leq 5.5 V$	$t_{SPCKr}$	-	ns	
		$2.4 V \leq VCC < 2.7 V$	$t_{SPCKf}$	-		
		$1.8 V \leq VCC \leq 2.4 V$		-		
		$1.6 V \leq VCC < 1.8 V$		-		
	Input			-	$1$	$\mu s$
Data input setup time	Master		$t_{SU}$	10	ns	Figure 2.51 to Figure 2.56 C = 30 pF
	Slave	$2.4 V \leq VCC \leq 5.5 V$		10		
		$1.8 V \leq VCC < 2.4 V$		15		
		$1.6 V \leq VCC < 1.8 V$		20		
Data input hold time	Master (RSPCK is PCLKB/2)		$t_{HF}$	0	ns	
	Master (RSPCK is not PCLKB/2)		$t_H$	$t_{Pcyc}$		
	Slave		$t_H$	20		
SSL setup time	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{LEAD}$	$-30 + N \times t_{SPcyc}^2$	ns	
		$1.6 V \leq VCC < 1.8 V$		$-50 + N \times t_{SPcyc}^2$		
	Slave			$6 \times t_{Pcyc}$		
SSL hold time	Master		$t_{LAG}$	$-30 + N \times t_{SPcyc}^3$	ns	
	Slave			$6 \times t_{Pcyc}$	ns	
Data output delay	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{OD}$	-	ns	
		$2.4 V \leq VCC < 2.7 V$		-		
		$1.8 V \leq VCC < 2.4 V$		-		
		$1.6 V \leq VCC < 1.8 V$		-		
	Slave	$2.7 V \leq VCC \leq 5.5 V$			-	
		$2.4 V \leq VCC < 2.7 V$			-	
		$1.8 V \leq VCC < 2.4 V$			-	
		$1.6 V \leq VCC < 1.8 V$			-	
Data output hold time	Master		$t_{OH}$	0	ns	
	Slave			0		
Successive transmission delay	Master		$t_{TD}$	$t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			$6 \times t_{Pcyc}$		

2.3.9 SPI时序

Table 2.34 SPI时序 (1of2)

条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter	Symbol	Min	Max	Unit*1	测试条件	
SPI RSPCK时钟周期	Master	$t_{SPcyc}$	2	4096	$t_{Pcyc}$	Figure 2.50 C = 30 pF
	Slave		6	4096		
RSPCK时钟高脉冲宽度	Master	$t_{SPCKWH}$	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
	Slave		$3 \times t_{Pcyc}$	-		
RSPCK时钟低脉冲宽度	Master	$t_{SPCKWL}$	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
	Slave		$3 \times t_{Pcyc}$	-		
RSPCK时钟上升和下降时间	Output	$2.7 V \leq VCC \leq 5.5 V$	$t_{SPCKr}$	-	ns	
		$2.4 V \leq VCC < 2.7 V$	$t_{SPCKf}$	-		
		$1.8 V \leq VCC \leq 2.4 V$		-		
		$1.6 V \leq VCC < 1.8 V$		-		
	Input			-	$1$	$\mu s$
数据输入建立时间	Master		$t_{SU}$	10	ns	图2.51至 Figure 2.56 C = 30 pF
	Slave	$2.4 V \leq VCC \leq 5.5 V$		10		
		$1.8 V \leq VCC < 2.4 V$		15		
		$1.6 V \leq VCC < 1.8 V$		20		
数据输入保持时间	主机 (RSPCK为PCLK B2)		$t_{HF}$	0	ns	
	主控 (RSPCK不是PCLK B2)		$t_H$	$t_{Pcyc}$		
	Slave		$t_H$	20		
SSL设置时间	Master	$1.8 V \leq VCC \leq 5.5 V$	$t_{LEAD}$	$-30 + N \times t_{SPcyc}^2$	ns	
		$1.6 V \leq VCC < 1.8 V$		$-50 + N \times t_{SPcyc}^2$		
	Slave			$6 \times t_{Pcyc}$		
SSL保持时间	Master		$t_{LAG}$	$-30 + N \times t_{SPcyc}^3$	ns	
	Slave			$6 \times t_{Pcyc}$	ns	
数据输出延迟	Master	$2.7 V \leq VCC \leq 5.5 V$	$t_{OD}$	-	ns	
		$2.4 V \leq VCC < 2.7 V$		-		
		$1.8 V \leq VCC < 2.4 V$		-		
		$1.6 V \leq VCC < 1.8 V$		-		
	Slave	$2.7 V \leq VCC \leq 5.5 V$			-	
		$2.4 V \leq VCC < 2.7 V$			-	
		$1.8 V \leq VCC < 2.4 V$			-	
		$1.6 V \leq VCC < 1.8 V$			-	
数据输出保持时间	Master		$t_{OH}$	0	ns	
	Slave			0		
连续传输延迟	Master		$t_{TD}$	$t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			$6 \times t_{Pcyc}$		

**Table 2.34 SPI timing (2 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit*1	Test conditions	
SPI MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	-	10	ns	Figure 2.51 to Figure 2.56 C = 30 pF
		2.4 V ≤ VCC < 2.7 V	-	15		
		1.8 V ≤ VCC < 2.4 V	-	20		
		1.6 V ≤ VCC < 1.8 V	-	30		
Input		-	1	μs		
SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	-	10	ns	
		2.4 V ≤ VCC < 2.7 V	-	15		
		1.8 V ≤ VCC < 2.4 V	-	20		
		1.6 V ≤ VCC < 1.8 V	-	30		
Input		-	1	μs		
Slave access time	2.4 V ≤ VCC ≤ 5.5 V	-	2 × t <sub>PCYC</sub> + 100	ns	Figure 2.55 and Figure 2.56 C = 30 pF	
		1.8 V ≤ VCC < 2.4 V	-			2 × t <sub>PCYC</sub> + 140
		1.6 V ≤ VCC < 1.8 V	-			2 × t <sub>PCYC</sub> + 180
Slave output release time	2.4 V ≤ VCC ≤ 5.5 V	-	2 × t <sub>PCYC</sub> + 100	ns		
		1.8 V ≤ VCC < 2.4 V	-			2 × t <sub>PCYC</sub> + 140
		1.6 V ≤ VCC < 1.8 V	-			2 × t <sub>PCYC</sub> + 180

- Note 1. t<sub>PCYC</sub>: PCLKB cycle.
- Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
- Note 3. N is set as an integer from 1 to 8 by the SSLND register.

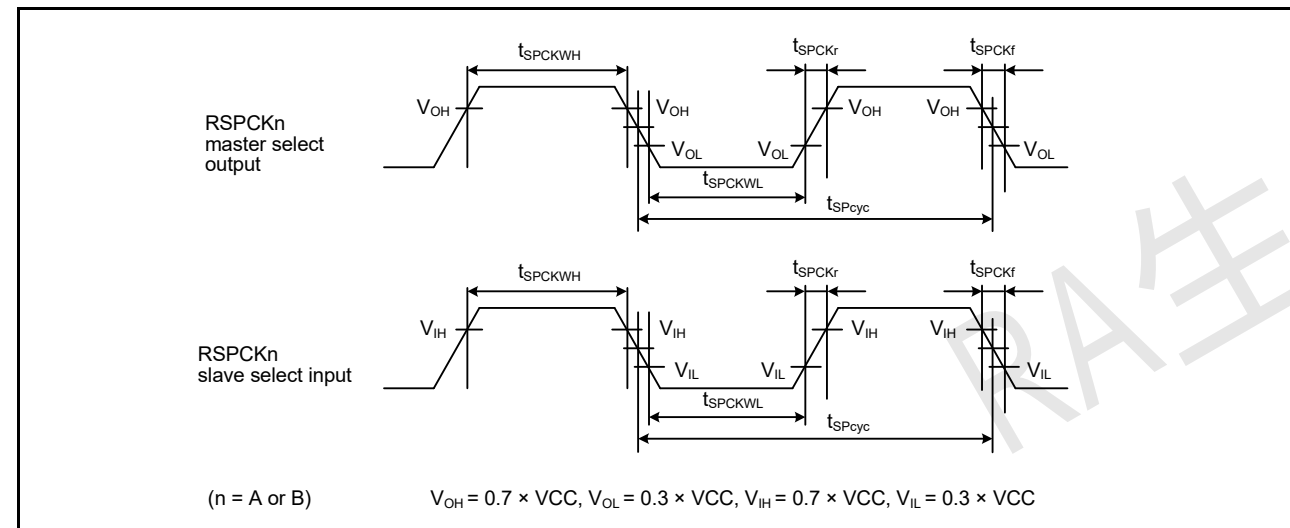


Figure 2.50 SPI clock timing

**Table 2.34 SPI时序 (2之2)**

条件: 在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter	Symbol	Min	Max	Unit*1	测试条件	
SPI MOSI和MISO上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	-	10	ns	图2.51至图2.56 C = 30 pF
		2.4 V ≤ VCC < 2.7 V	-	15		
		1.8 V ≤ VCC < 2.4 V	-	20		
		1.6 V ≤ VCC < 1.8 V	-	30		
Input		-	1	μs		
SSL上升和下降时间	Output	2.7 V ≤ VCC ≤ 5.5 V	-	10	ns	
		2.4 V ≤ VCC < 2.7 V	-	15		
		1.8 V ≤ VCC < 2.4 V	-	20		
		1.6 V ≤ VCC < 1.8 V	-	30		
Input		-	1	μs		
从站访问时间	2.4 V ≤ VCC ≤ 5.5 V	-	2 × t <sub>PCYC</sub> + 100	ns	图2.55和图2.56 C = 30 pF	
		1.8 V ≤ VCC < 2.4 V	-			2 × t <sub>PCYC</sub> + 140
		1.6 V ≤ VCC < 1.8 V	-			2 × t <sub>PCYC</sub> + 180
从机输出释放时间	2.4 V ≤ VCC ≤ 5.5 V	-	2 × t <sub>PCYC</sub> + 100	ns		
		1.8 V ≤ VCC < 2.4 V	-			2 × t <sub>PCYC</sub> + 140
		1.6 V ≤ VCC < 1.8 V	-			2 × t <sub>PCYC</sub> + 180

- Note 1. t<sub>PCYC</sub>: PCLKB cycle.
- Note 2. N由SPCKD寄存器设置为从1到8的整数。
- Note 3. N由SSLND寄存器设置为1到8的整数。

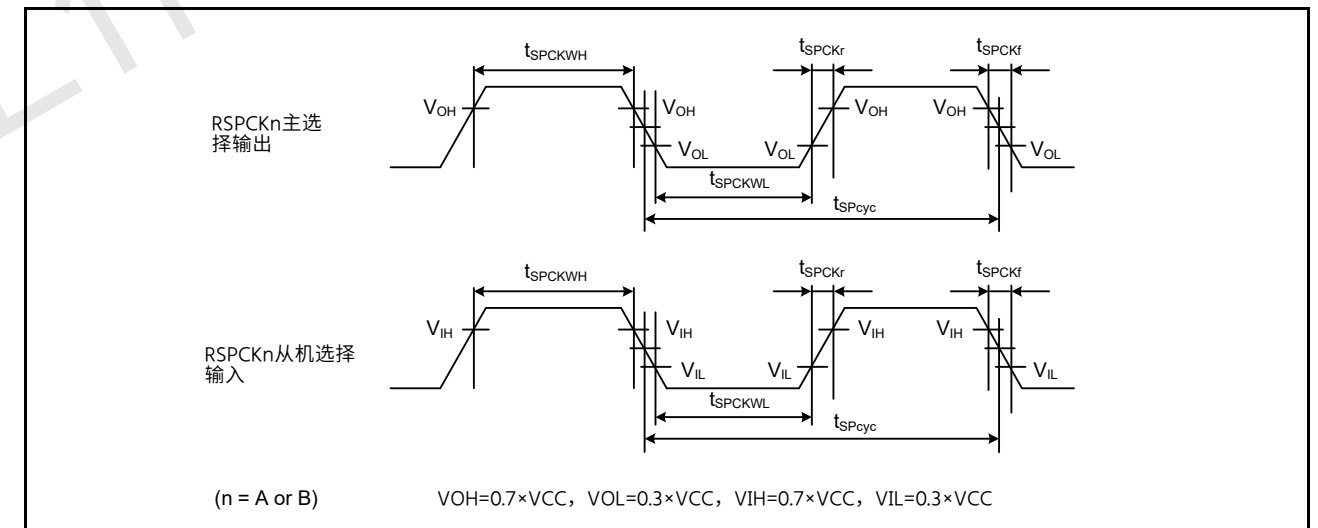


Figure 2.50 SPI时钟时序



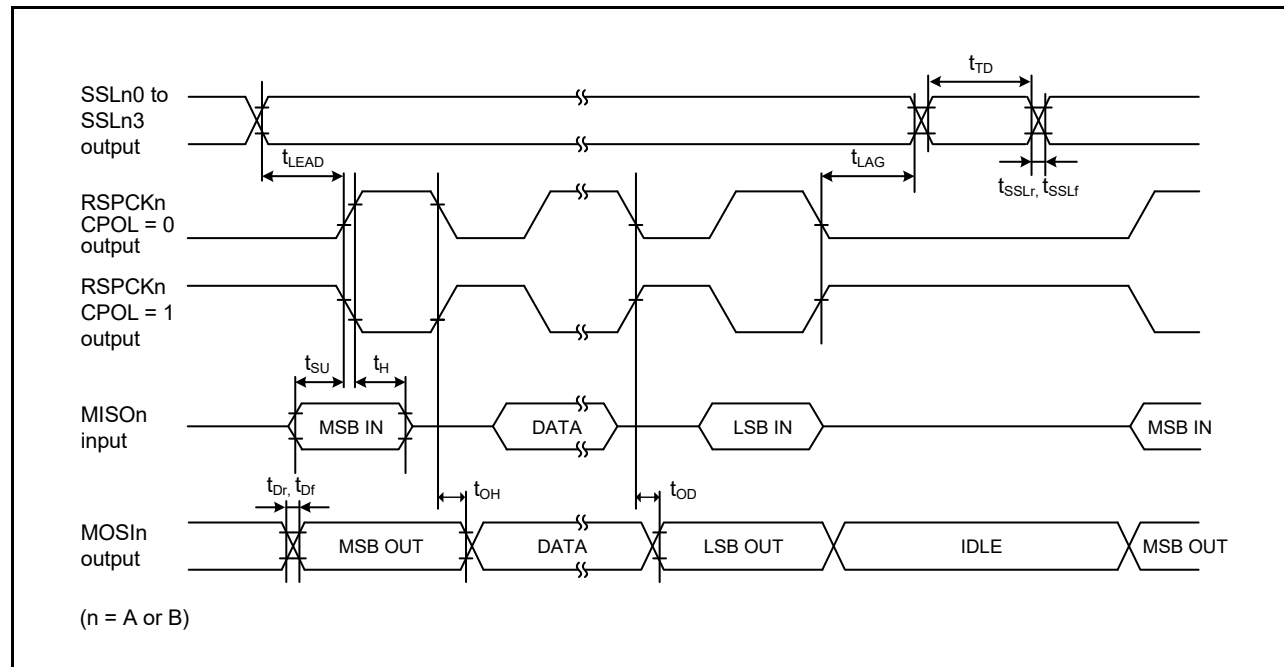


Figure 2.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

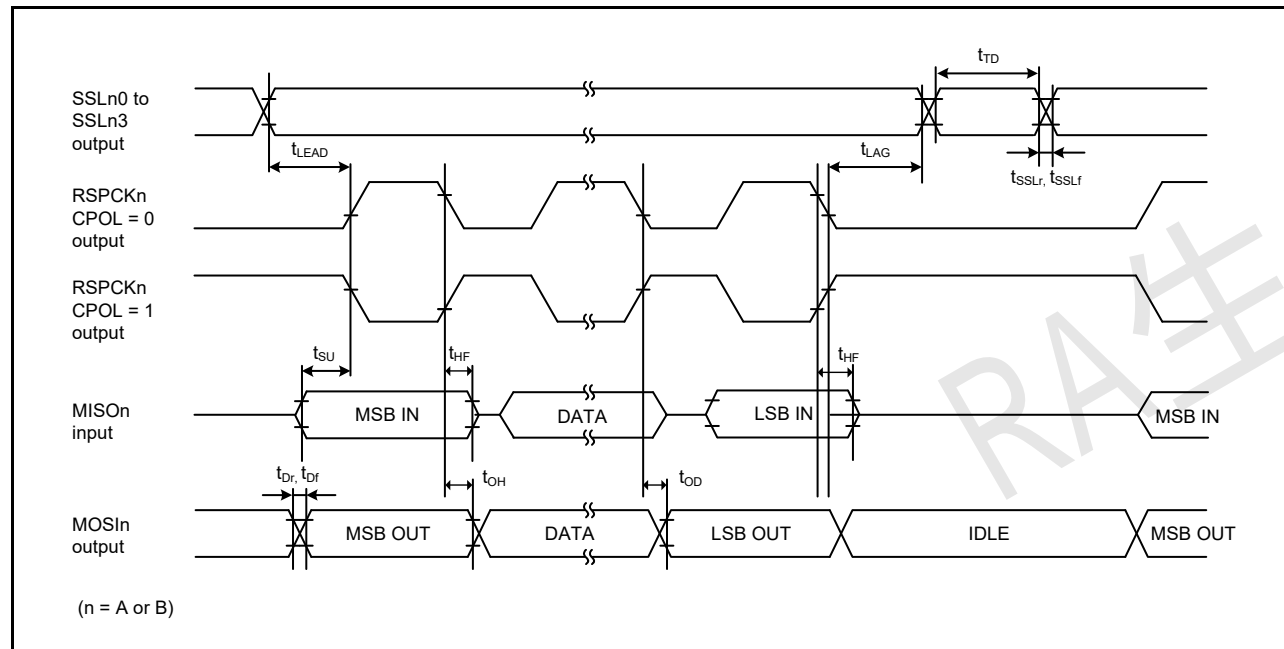


Figure 2.52 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

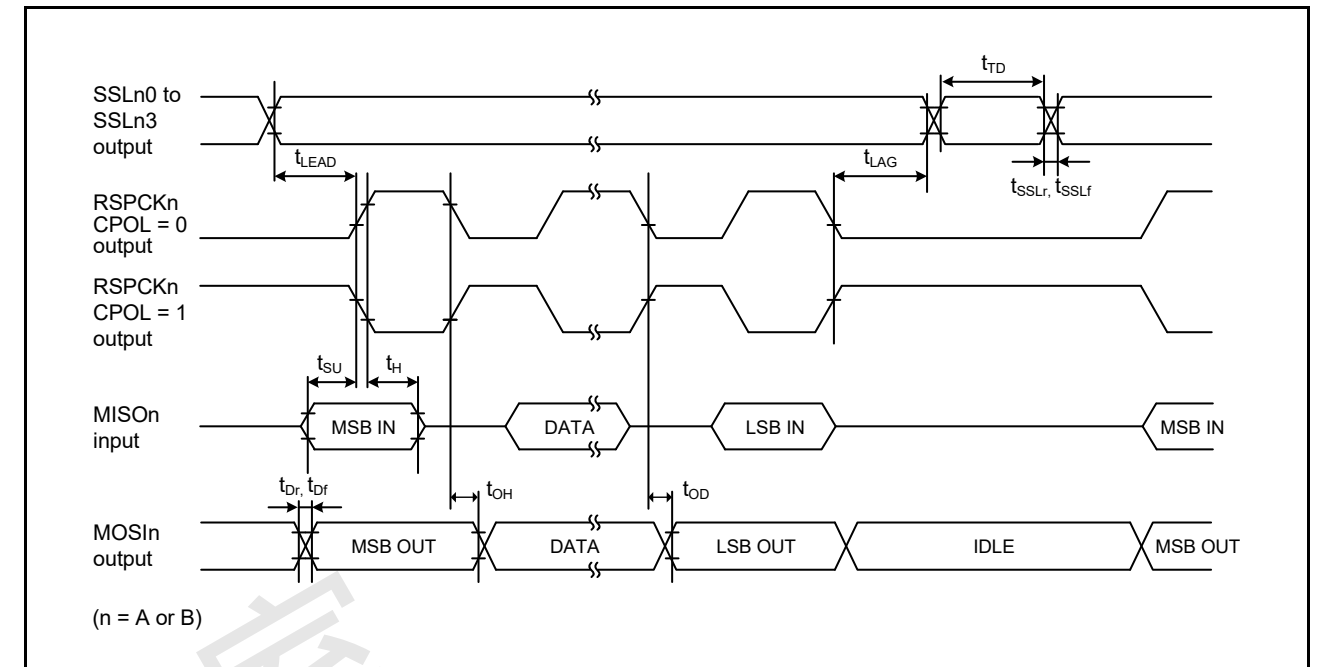


Figure 2.51 SPI时序 (主机, CPHA=0) (比特率: PCLKB分频比设置为12以外的任何值)

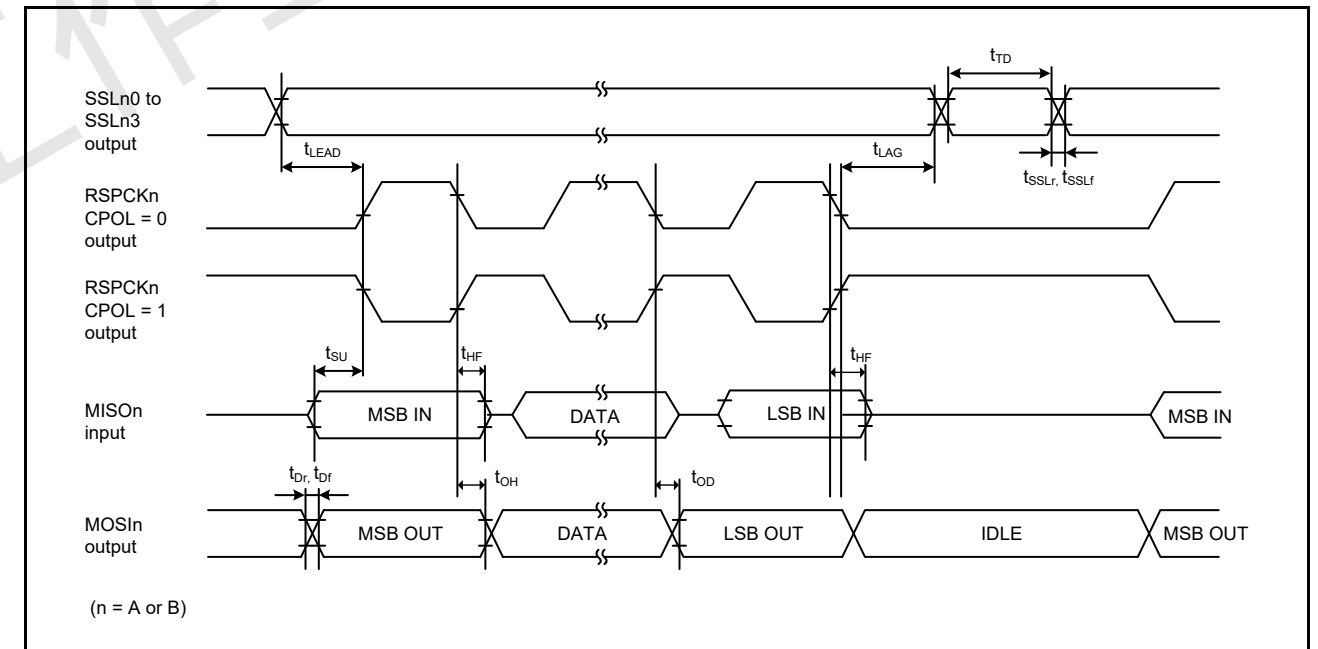


Figure 2.52 SPI时序 (主控, CPHA=0) (比特率: PCLKB分频比设置为1/2)

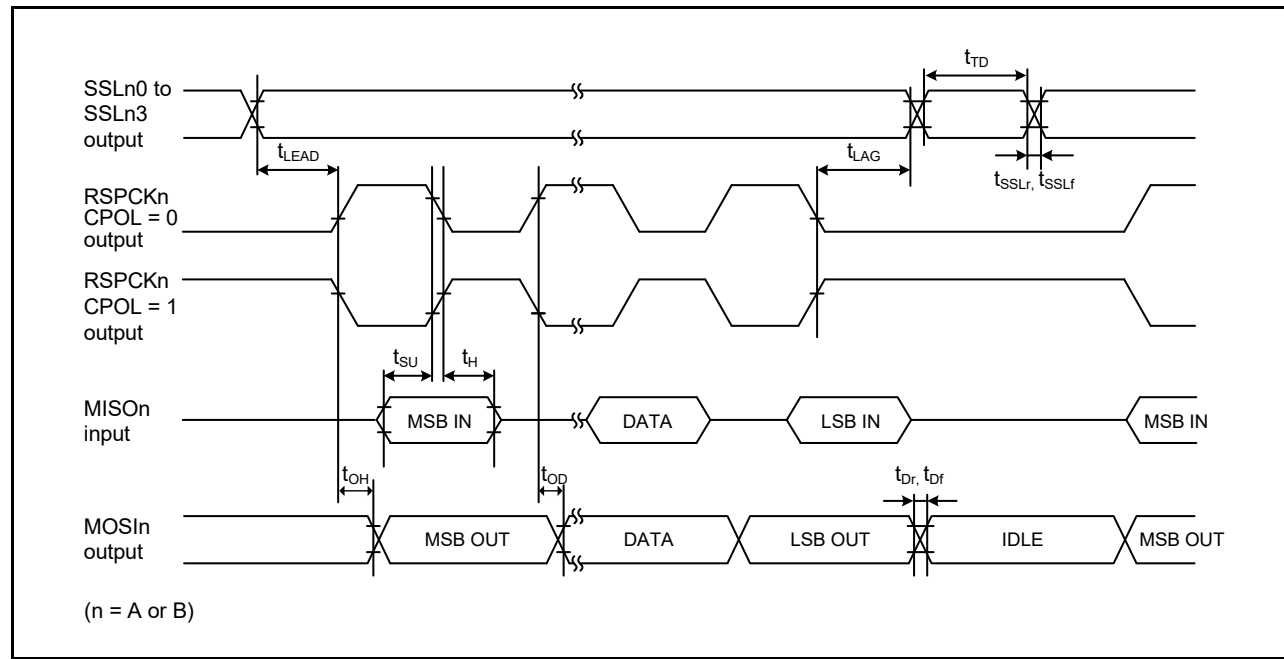


Figure 2.53 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

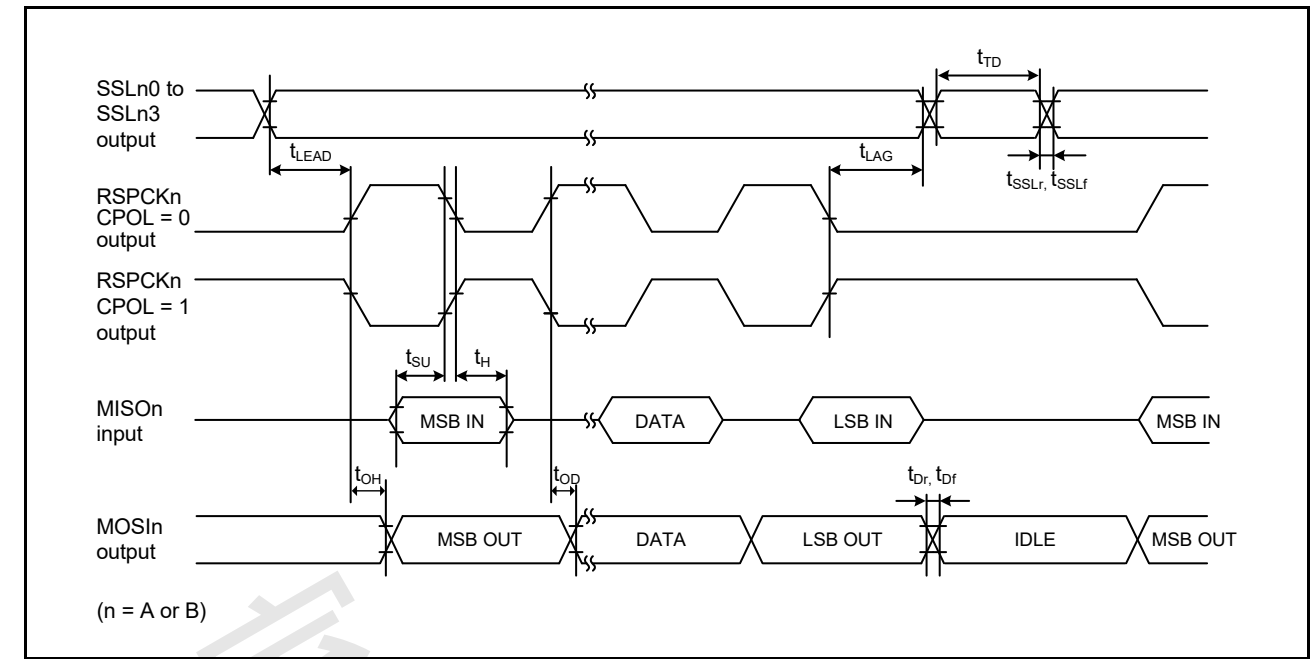


Figure 2.53 SPI时序 (主机, CPHA=1) (比特率: PCLKB分频比设置为12以外的任何值)

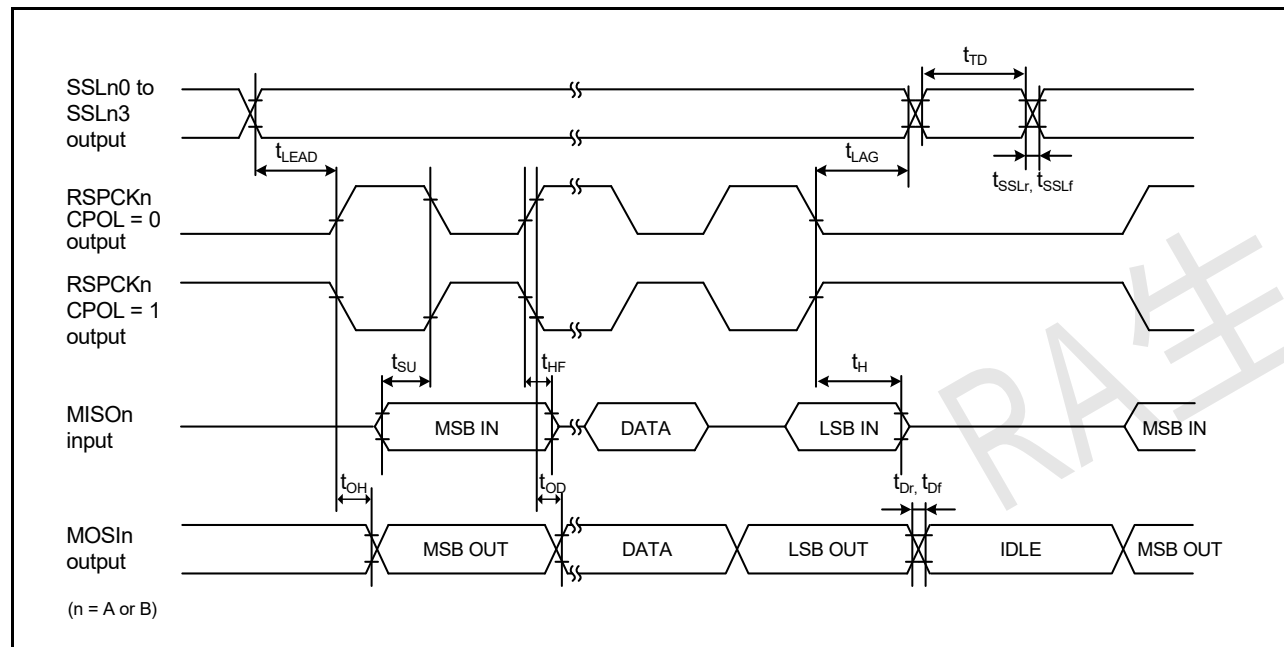


Figure 2.54 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

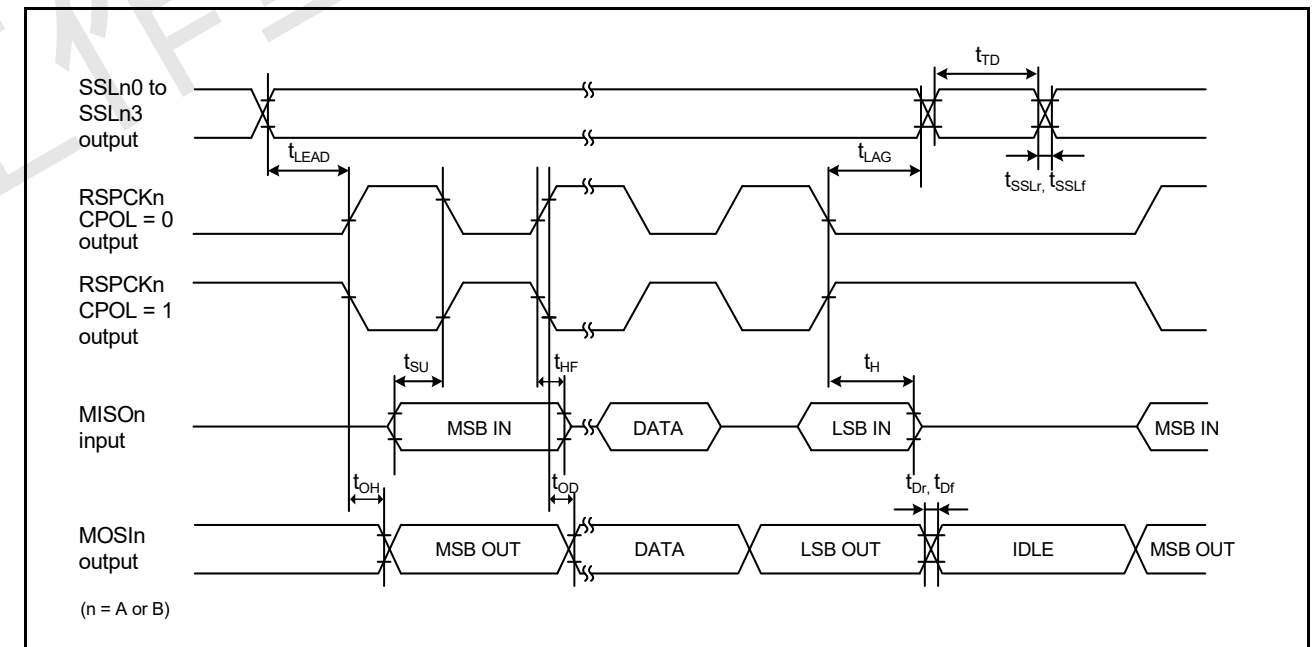


Figure 2.54 SPI时序 (主控, CPHA=1) (比特率: PCLKB分频比设置为1/2)

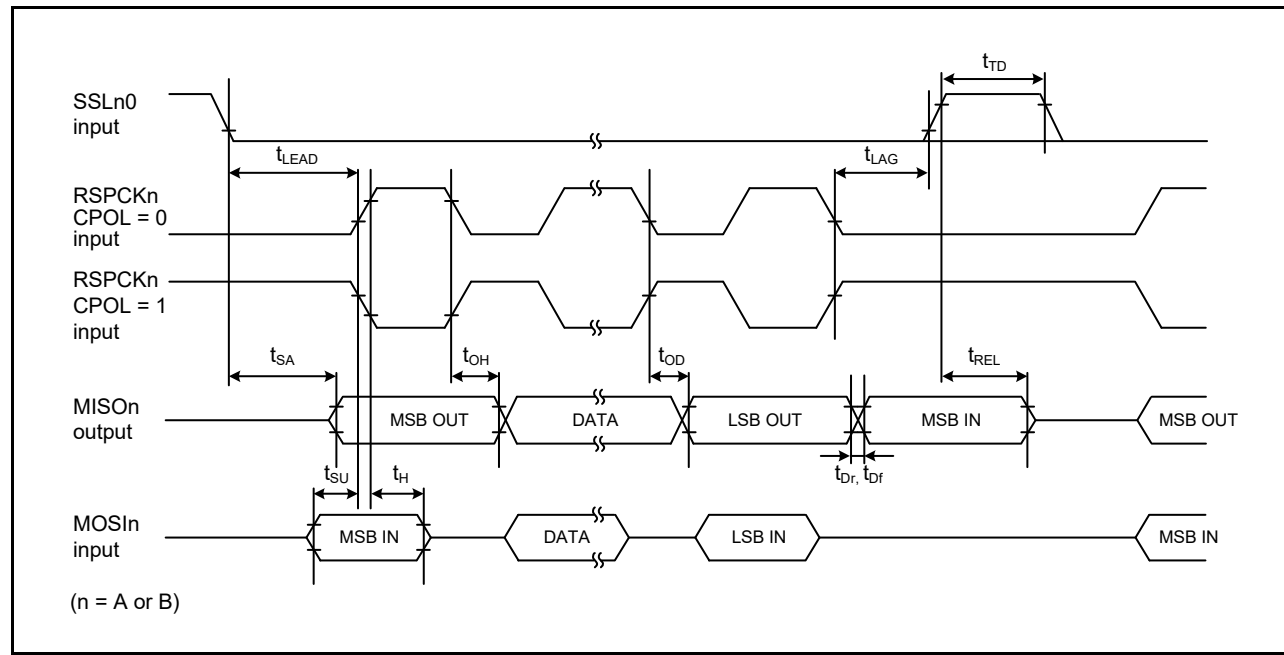


Figure 2.55 SPI timing (slave, CPHA = 0)

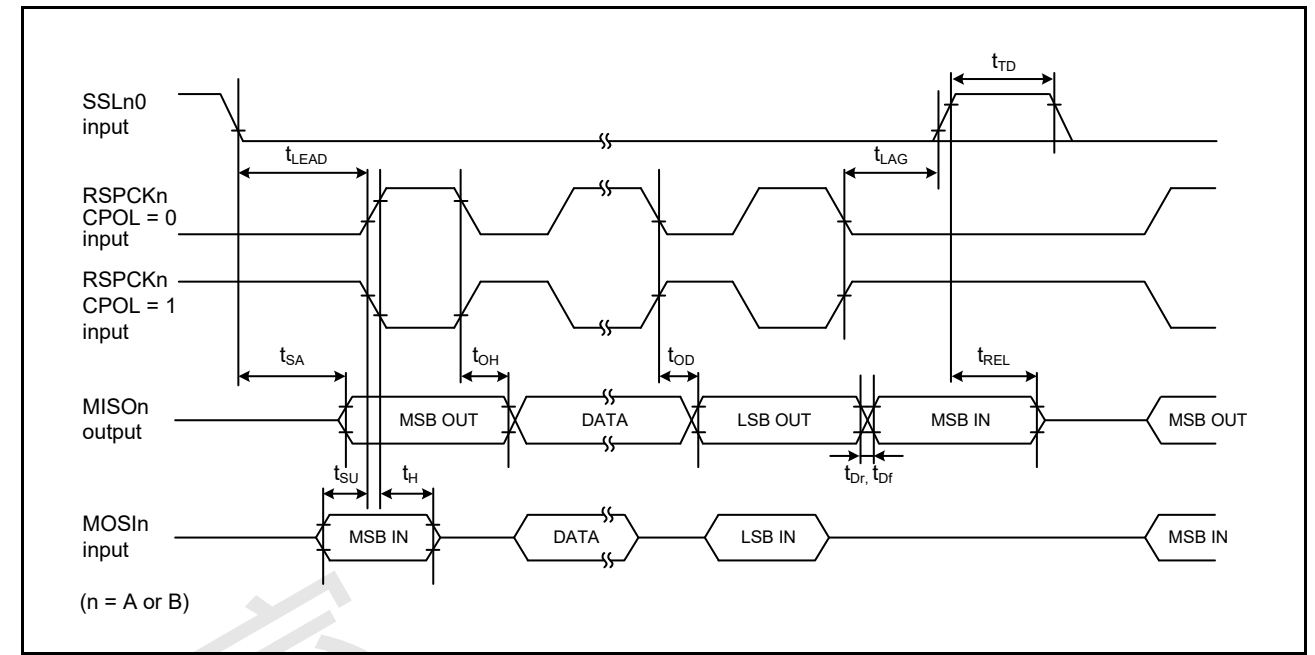


Figure 2.55 SPI时序 (从机, CPHA=0)

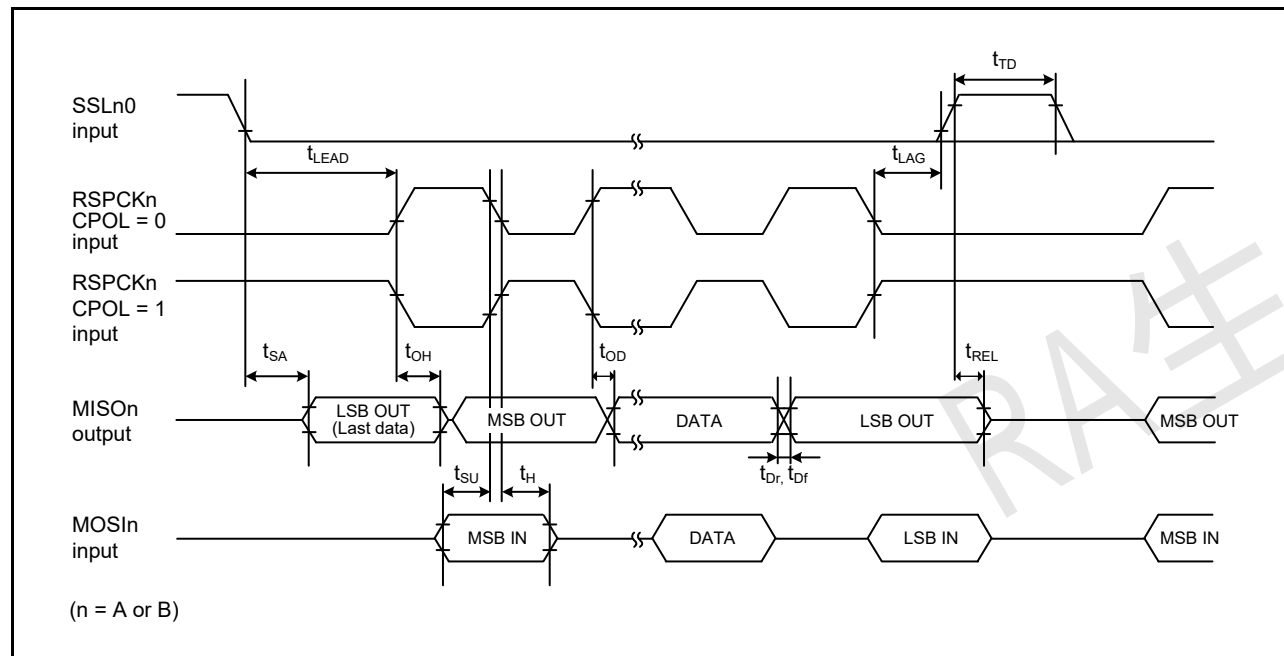


Figure 2.56 SPI timing (slave, CPHA = 1)

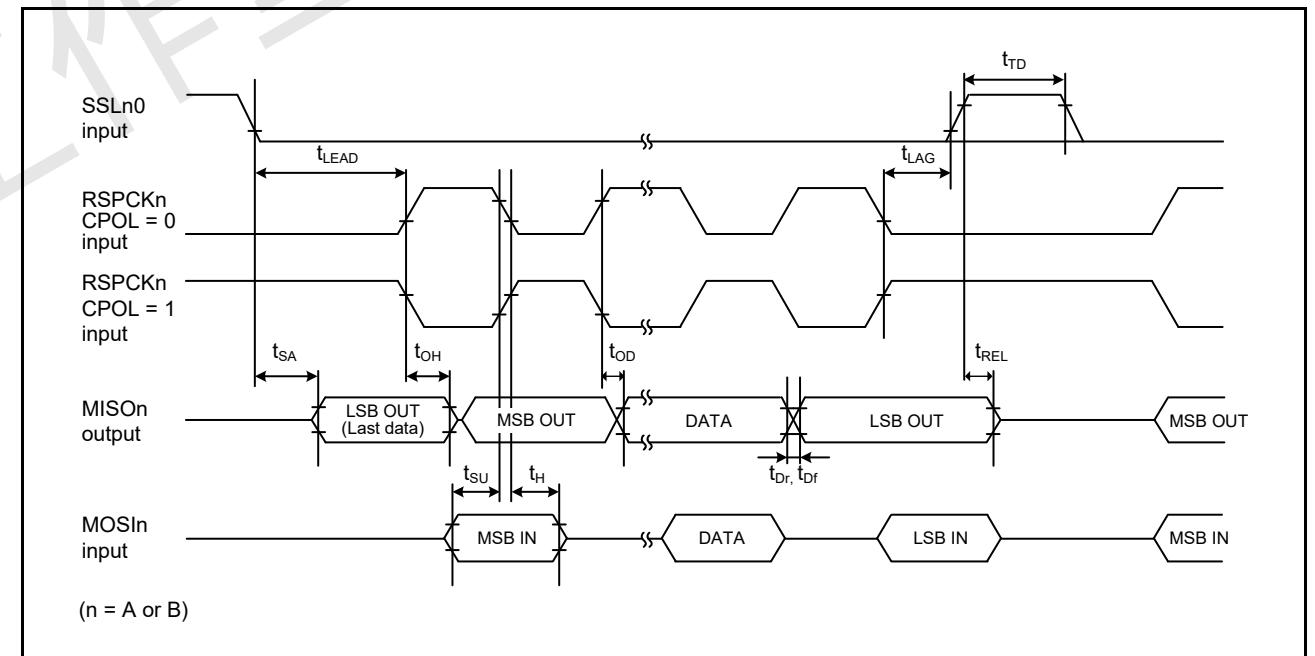


Figure 2.56 SPI时序 (从机, CPHA=1)

## 2.3.10 IIC Timing

Table 2.35 IIC timing

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min*1	Max	Unit	Test conditions	
IIC (Standard mode, SMBus)	SCL input cycle time	$t_{SCL}$	$6(12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.57
	SCL input high pulse width	$t_{SCLH}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	$t_{SCLL}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	$t_{Sr}$	-	1000	ns	
	SCL, SDA input fall time	$t_{Sf}$	-	300	ns	
	SCL, SDA input spike pulse removal time	$t_{SP}$	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time (when wakeup function is disabled)	$t_{BUF}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (when wakeup function is enabled)	$t_{BUF}$	$3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (when wakeup function is disabled)	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (when wakeup function is enabled)	$t_{STAH}$	$1(5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	$t_{STAS}$	1000	-	ns	
	STOP condition input setup time	$t_{STOS}$	1000	-	ns	
	Data input setup time	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	400	pF	
IIC (Fast mode)	SCL input cycle time	$t_{SCL}$	$6(12) \times t_{IICcyc} + 600$	-	ns	Figure 2.57
	SCL input high pulse width	$t_{SCLH}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	$t_{SCLL}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	$t_{Sr}$	-	300	ns	
	SCL, SDA input fall time	$t_{Sf}$	-	300	ns	
	SCL, SDA input spike pulse removal time	$t_{SP}$	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time (When wakeup function is disabled)	$t_{BUF}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (When wakeup function is enabled)	$t_{BUF}$	$3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is disabled)	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is enabled)	$t_{STAH}$	$1(5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	$t_{STAS}$	300	-	ns	
	STOP condition input setup time	$t_{STOS}$	300	-	ns	
	Data input setup time	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	400	pF	

Note:  $t_{IICcyc}$ : IIC internal reference clock (IICφ) cycle,  $t_{Pcyc}$ : PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

## 2.3.10 IIC Timing

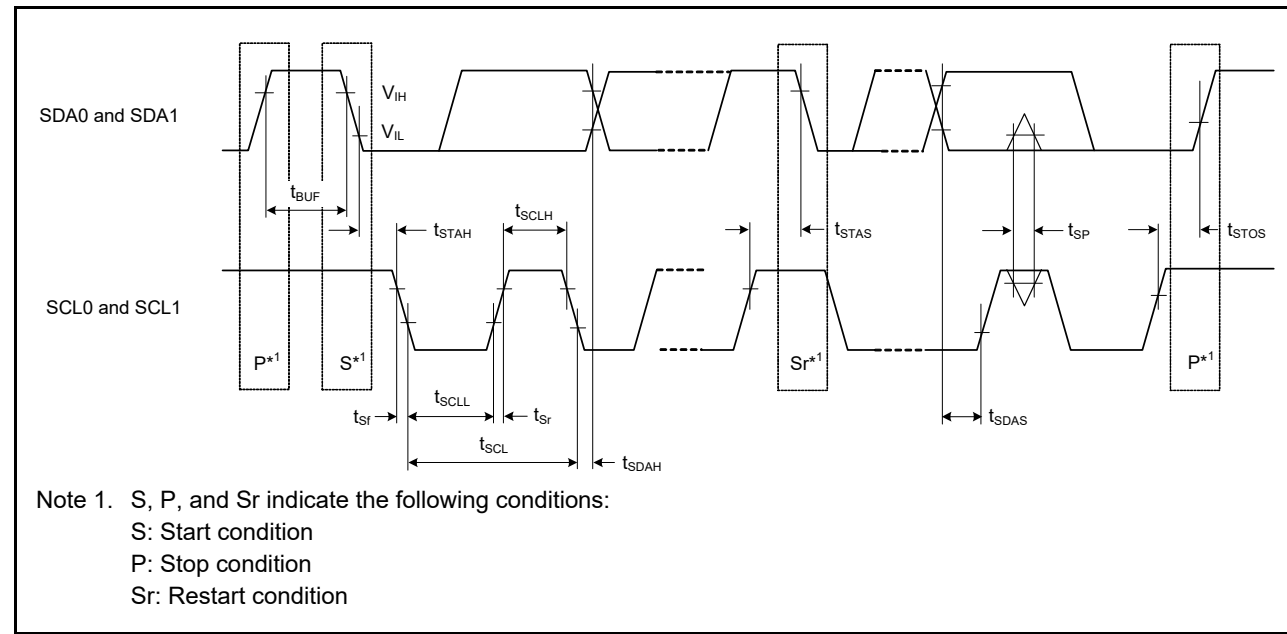
Table 2.35 IIC timing

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	Min*1	Max	Unit	测试条件	
IIC (Standard mode, SMBus)	SCL输入周期时间	$t_{SCL}$	$6(12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.57
	SCL输入高脉冲宽度	$t_{SCLH}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL输入低脉冲宽度	$t_{SCLL}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL、SDA输入上升时间	$t_{Sr}$	-	1000	ns	
	SCL、SDA输入下降时间	$t_{Sf}$	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	$t_{SP}$	0	$1(4) \times t_{IICcyc}$	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	$t_{BUF}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	$t_{BUF}$	$3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START条件输入保持时间（禁用唤醒功能时）	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START条件输入保持时间（启用唤醒功能时）	$t_{STAH}$	$1(5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	重复启动条件输入建立时间	$t_{STAS}$	1000	-	ns	
	STOP条件输入建立时间	$t_{STOS}$	1000	-	ns	
	数据输入建立时间	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	数据输入保持时间	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	400	pF	
IIC (Fast mode)	SCL输入周期时间	$t_{SCL}$	$6(12) \times t_{IICcyc} + 600$	-	ns	Figure 2.57
	SCL输入高脉冲宽度	$t_{SCLH}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL输入低脉冲宽度	$t_{SCLL}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SCL、SDA输入上升时间	$t_{Sr}$	-	300	ns	
	SCL、SDA输入下降时间	$t_{Sf}$	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	$t_{SP}$	0	$1(4) \times t_{IICcyc}$	ns	
	SDA输入总线空闲时间（禁用唤醒功能时）	$t_{BUF}$	$3(6) \times t_{IICcyc} + 300$	-	ns	
	SDA输入总线空闲时间（启用唤醒功能时）	$t_{BUF}$	$3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START条件输入保持时间（禁用唤醒功能时）	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START条件输入保持时间（启用唤醒功能时）	$t_{STAH}$	$1(5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	重复启动条件输入建立时间	$t_{STAS}$	300	-	ns	
	STOP条件输入建立时间	$t_{STOS}$	300	-	ns	
	数据输入建立时间	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	数据输入保持时间	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	400	pF	

Note:  $t_{IICcyc}$ : IIC内部参考时钟(IICφ)周期,  $t_{Pcyc}$ : PCLKB周期

Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时, 括号中的值适用。



Note 1. S, P, and Sr indicate the following conditions:  
 S: Start condition  
 P: Stop condition  
 Sr: Restart condition

Figure 2.57 I<sup>2</sup>C bus interface input/output timing

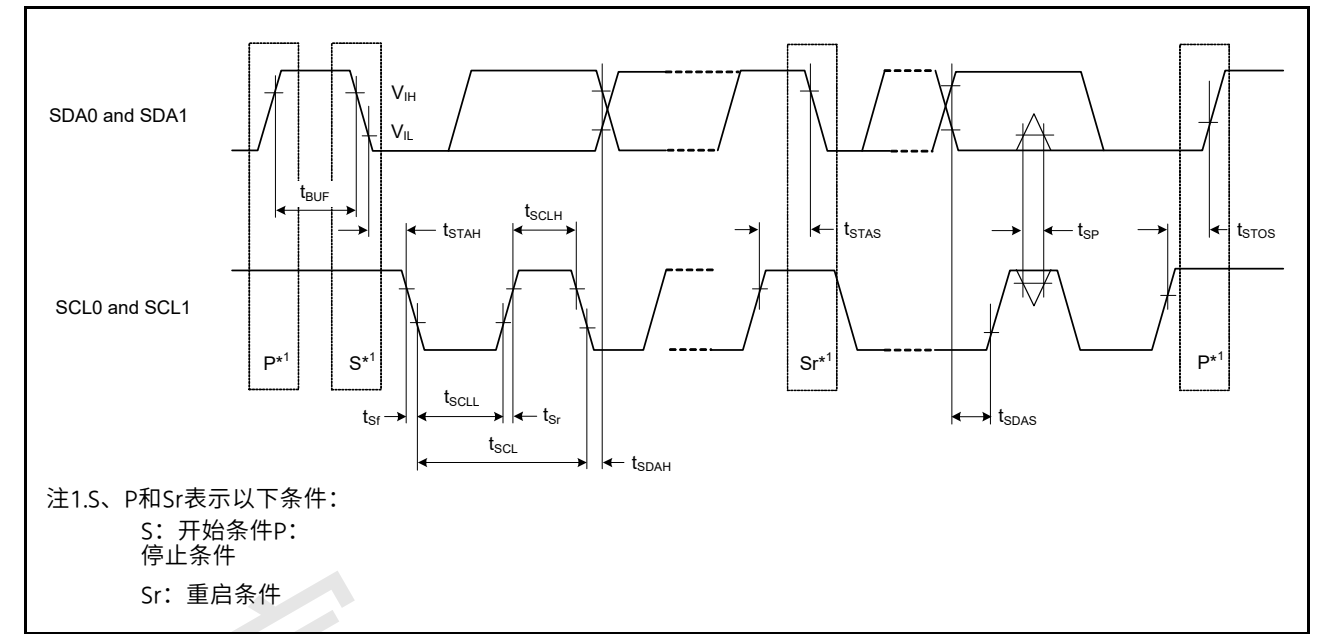
2.3.11 CLKOUT Timing

Table 2.36 CLKOUT timing

Parameter	Symbol	Min	Max	Unit	Test conditions	
CLKOUT pin output cycle*1	t <sub>Cyc</sub>	2.7 V ≤ VCC ≤ 5.5 V	62.5	-	ns	Figure 2.58
		1.8 V ≤ VCC < 2.7 V	125	-		
		1.6 V ≤ VCC < 1.8 V	250	-		
CLKOUT pin high pulse width*2	t <sub>CH</sub>	2.7 V ≤ VCC ≤ 5.5 V	15	-	ns	
		1.8 V ≤ VCC < 2.7 V	30	-		
		1.6 V ≤ VCC < 1.8 V	150	-		
CLKOUT pin low pulse width*2	t <sub>CL</sub>	2.7 V ≤ VCC ≤ 5.5 V	15	-	ns	
		1.8 V ≤ VCC < 2.7 V	30	-		
		1.6 V ≤ VCC < 1.8 V	150	-		
CLKOUT pin output rise time	t <sub>Cr</sub>	2.7 V ≤ VCC ≤ 5.5 V	-	12	ns	
		1.8 V ≤ VCC < 2.7 V	-	25		
		1.6 V ≤ VCC < 1.8 V	-	50		
CLKOUT pin output fall time	t <sub>Cf</sub>	2.7 V ≤ VCC ≤ 5.5 V	-	12	ns	
		1.8 V ≤ VCC < 2.7 V	-	25		
		1.6 V ≤ VCC < 1.8 V	-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.36 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



注1.S、P和Sr表示以下条件：  
 S：开始条件P：  
 停止条件  
 Sr：重启条件

Figure 2.57 I<sup>2</sup>C总线接口输入输出时序

2.3.11 CLKOUT Timing

Table 2.36 CLKOUT timing

Parameter	Symbol	Min	Max	Unit	测试条件	
CLKOUT 引脚输出周期*1	t <sub>Cyc</sub>	2.7 V ≤ VCC ≤ 5.5 V	62.5	-	ns	Figure 2.58
		1.8 V ≤ VCC < 2.7 V	125	-		
		1.6 V ≤ VCC < 1.8 V	250	-		
CLKOUT 引脚高脉冲宽度*2	t <sub>CH</sub>	2.7 V ≤ VCC ≤ 5.5 V	15	-	ns	
		1.8 V ≤ VCC < 2.7 V	30	-		
		1.6 V ≤ VCC < 1.8 V	150	-		
CLKOUT 引脚低脉冲宽度*2	t <sub>CL</sub>	2.7 V ≤ VCC ≤ 5.5 V	15	-	ns	
		1.8 V ≤ VCC < 2.7 V	30	-		
		1.6 V ≤ VCC < 1.8 V	150	-		
CLKOUT 引脚输出上升时间	t <sub>Cr</sub>	2.7 V ≤ VCC ≤ 5.5 V	-	12	ns	
		1.8 V ≤ VCC < 2.7 V	-	25		
		1.6 V ≤ VCC < 1.8 V	-	50		
CLKOUT 引脚输出下降时间	t <sub>Cf</sub>	2.7 V ≤ VCC ≤ 5.5 V	-	12	ns	
		1.8 V ≤ VCC < 2.7 V	-	25		
		1.6 V ≤ VCC < 1.8 V	-	50		

Note 1. 当使用EXTAL外部时钟输入或振荡器除以1 (CKOCR.CKOSSEL[2:0]位为011b, CKOCR.CKODIV[2:0]位为000b) 从CLKOUT输出时, 表中的规格2.36应满足45%至55%的输入占空比。

Note 2. 当MOCO被选为时钟输出源(CKOCR.CKOSSEL[2:0]位为001b) 设时钟输出分频比到被除以2(CKOCR.CKODIV[2:0]位为001b)。



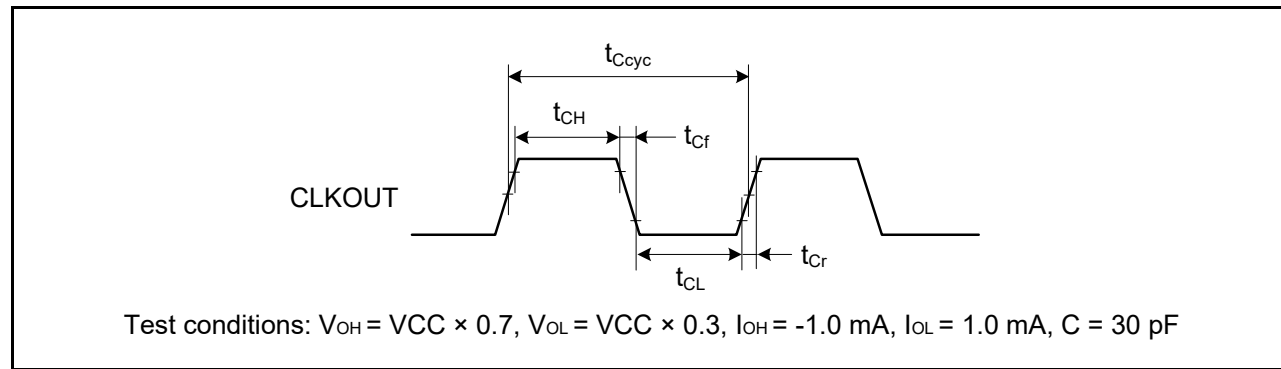


Figure 2.58 CLKOUT output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.37 USB characteristics

Conditions:  $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC\_USB} = 3.0 \text{ to } 3.6 \text{ V}$ ,  $T_a = -20 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	Min	Max	Unit	Test conditions		
Input characteristics	Input high level voltage	$V_{IH}$	2.0	-	V	-	
	Input low level voltage	$V_{IL}$	-	0.8	V	-	
	Differential input sensitivity	$V_{DI}$	0.2	-	V	USB_DP - USB_DM	
	Differential common mode range	$V_{CM}$	0.8	2.5	V	-	
Output characteristics	Output high level voltage	$V_{OH}$	2.8	$V_{CC\_USB}$	V	$I_{OH} = -200 \mu\text{A}$	
	Output low level voltage	$V_{OL}$	0.0	0.3	V	$I_{OL} = 2 \text{ mA}$	
	Cross-over voltage	$V_{CRS}$	1.3	2.0	V	Figure 2.59, Figure 2.60, Figure 2.61	
	Rise time	FS	$t_r$	4	20	ns	(Adjusting the resistance of external elements is not required.)
		LS		75	300		
	Fall time	FS	$t_f$	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	$t_r/t_f$	90	111.11	%	
LS			80	125			
Output resistance	$Z_{DRV}$	28	44	$\Omega$			
VBUS characteristics	VBUS input voltage	$V_{IH}$	$V_{CC} \times 0.8$	-	V	-	
		$V_{IL}$	-	$V_{CC} \times 0.2$	V	-	
Pull-up, pull-down	Pull-down resistor	$R_{PD}$	14.25	24.80	$k\Omega$	-	
	Pull-up resistor	$R_{PUI}$	0.9	1.575	$k\Omega$	During idle state	
		$R_{PUA}$	1.425	3.09	$k\Omega$	During reception	
Battery charging specification version 1.2	D+ sink current	$I_{DP\_SINK}$	25	175	$\mu\text{A}$	-	
	D- sink current	$I_{DM\_SINK}$	25	175	$\mu\text{A}$	-	
	DCD source current	$I_{DP\_SRC}$	7	13	$\mu\text{A}$	-	
	Data detection voltage	$V_{DAT\_REF}$	0.25	0.4	V	-	
	D+ source voltage	$V_{DP\_SRC}$	0.5	0.7	V	Output current = 250 $\mu\text{A}$	
	D- source voltage	$V_{DM\_SRC}$	0.5	0.7	V	Output current = 250 $\mu\text{A}$	

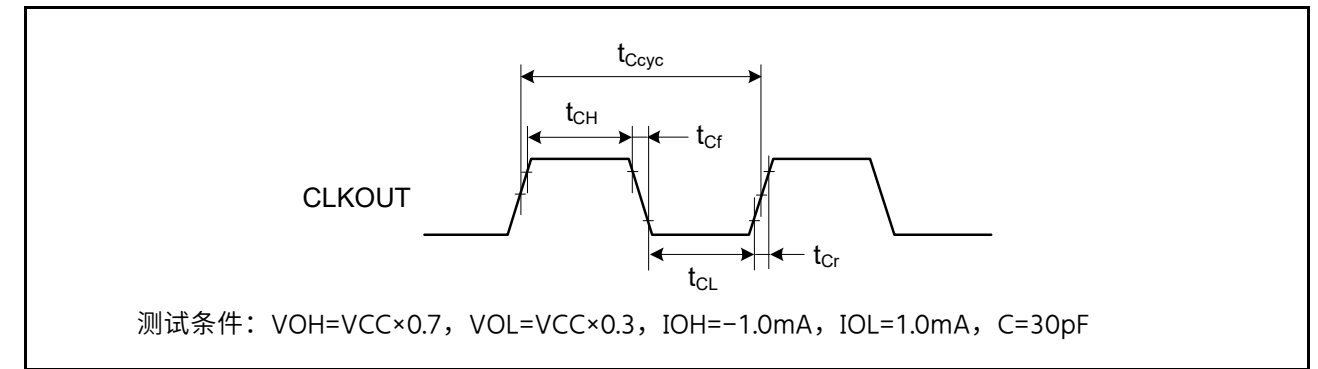


Figure 2.58 CLKOUT输出时序

2.4 USB特性

2.4.1 USBFS Timing

Table 2.37 USB特性

条件:  $V_{CC}=AV_{CC0}=AV_{CC1}=V_{CC\_USB}=3.0\text{至}3.6\text{V}$ ,  $T_a=-20\text{至}+85^\circ\text{C}$

Parameter	Symbol	Min	Max	Unit	测试条件		
输入特性	输入高电平电压	$V_{IH}$	2.0	-	V	-	
	输入低电平电压	$V_{IL}$	-	0.8	V	-	
	差分输入灵敏度	$V_{DI}$	0.2	-	V	USB_DP - USB_DM	
	差分共模范围	$V_{CM}$	0.8	2.5	V	-	
输出特性	输出高电平电压	$V_{OH}$	2.8	$V_{CC\_USB}$	V	$I_{OH} = -200 \mu\text{A}$	
	输出低电平电压	$V_{OL}$	0.0	0.3	V	我OL=2毫安	
	Cross-over voltage	$V_{CRS}$	1.3	2.0	V	Figure 2.59, Figure 2.60, Figure 2.61	
	上升时间	FS	$t_r$	4	20	ns	(不需要调整外部元件的电阻。)
		LS		75	300		
	秋季时间	FS	$t_f$	4	20	ns	
		LS		75	300		
	上升下降时间比	FS	$t_r/t_f$	90	111.11	%	
LS			80	125			
输出电阻	$Z_{DRV}$	28	44	$\Omega$			
VBUS characteristics	VBUS输入电压	$V_{IH}$	$V_{CC} \times 0.8$	-	V	-	
		$V_{IL}$	-	$V_{CC} \times 0.2$	V	-	
Pull-up, pull-down	Pull-down resistor	$R_{PD}$	14.25	24.80	$k\Omega$	-	
	Pull-up resistor	$R_{PUI}$	0.9	1.575	$k\Omega$	空闲状态期间	
		$R_{PUA}$	1.425	3.09	$k\Omega$	接待期间	
电池充电规范1.2版	D+灌电流	$I_{DP\_SINK}$	25	175	$\mu\text{A}$	-	
	D- sink current	$I_{DM\_SINK}$	25	175	$\mu\text{A}$	-	
	DCD源电流	$I_{DP\_SRC}$	7	13	$\mu\text{A}$	-	
	数据检测电压	$V_{DAT\_REF}$	0.25	0.4	V	-	
	D+源电压	$V_{DP\_SRC}$	0.5	0.7	V	输出电流=250 $\mu\text{A}$	
	D- source voltage	$V_{DM\_SRC}$	0.5	0.7	V	输出电流=250 $\mu\text{A}$	

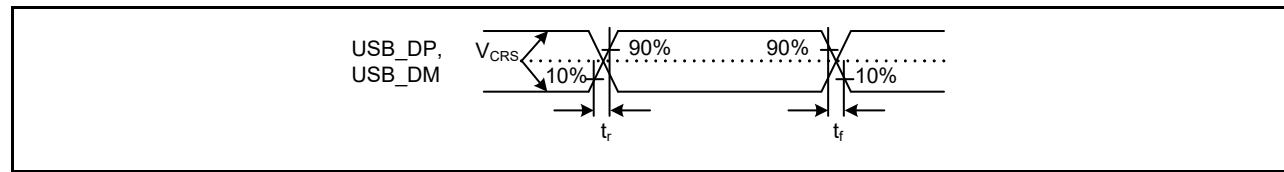


Figure 2.59 USB\_DP and USB\_DM output timing

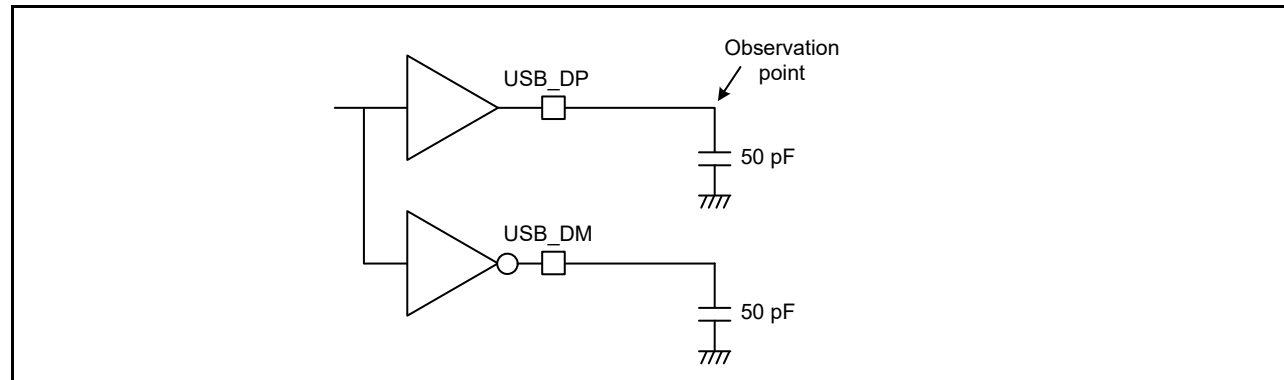


Figure 2.60 Test circuit for Full-Speed (FS) connection

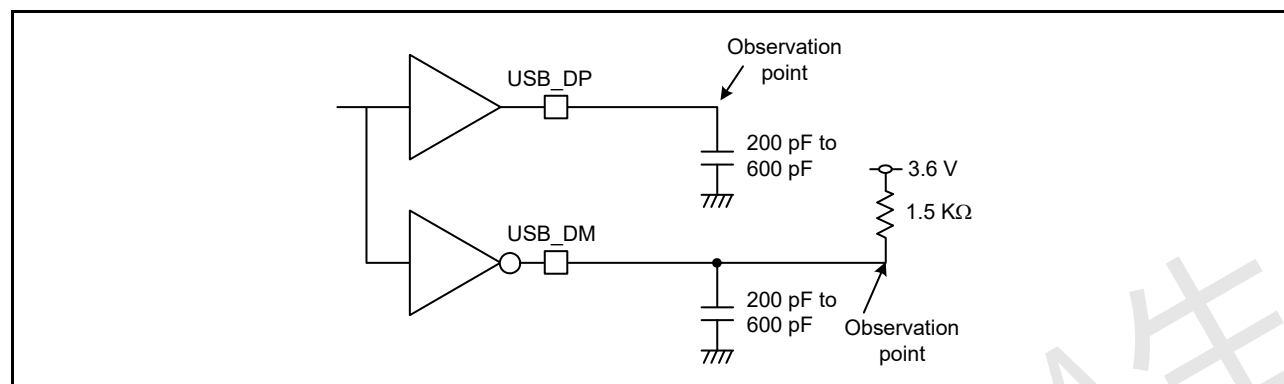


Figure 2.61 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.38 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	$3.8\text{ V} \leq \text{VCC\_USB\_LDO} < 4.5\text{ V}$	-	-	50	mA	-
	$4.5\text{ V} \leq \text{VCC\_USB\_LDO} \leq 5.5\text{ V}$	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

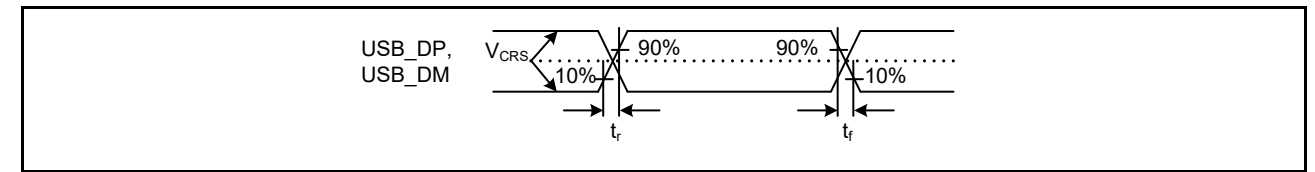


Figure 2.59 USB\_DP和USB\_DM输出时序

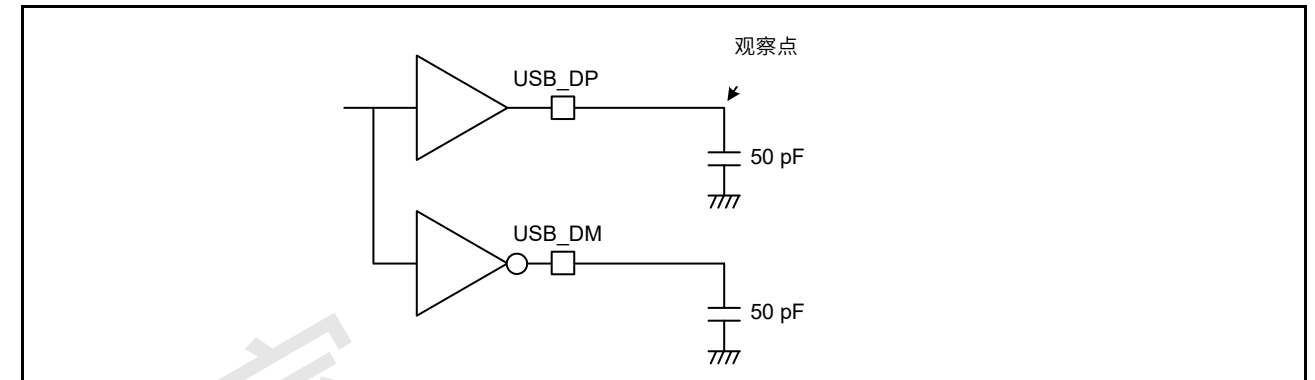


Figure 2.60 全速(FS)连接测试电路

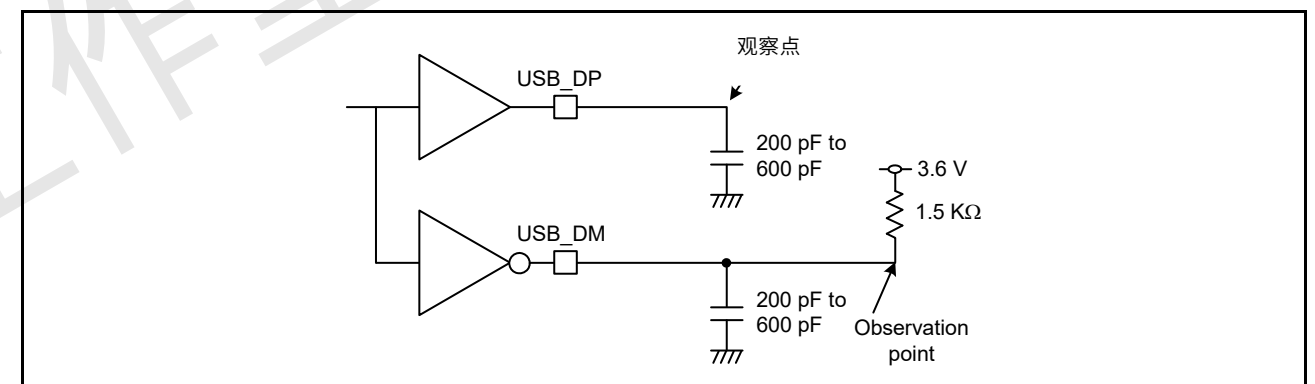


Figure 2.61 低速(LS)连接测试电路

2.4.2 USB外部电源

Table 2.38 USB稳压器

Parameter		Min	Typ	Max	Unit	测试条件
VCC_USB供电电流	$3.8\text{ V} \leq \text{VCC\_USB\_LDO} < 4.5\text{ V}$	-	-	50	mA	-
	$4.5\text{ V} \leq \text{VCC\_USB\_LDO} \leq 5.5\text{ V}$	-	-	100	mA	-
VCC_USB电源电压		3.0	-	3.6	V	-

2.5 ADC16 Characteristics

**Table 2.39 16-bit A/D conversion, power supply, and input range conditions**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions	
High-potential reference voltage	1.5	3.3	AVCC0	V	-	
Low-potential reference voltage	-	AVSS0	-	V	-	
Analog input voltage range	0	-	VREFH0	V	-	
Input common-mode range	Acm	0	VREFH0/2	V	Differential analog input	
Analog input capacitance*2	Cs	-	-	4.3	pF	
Analog input resistance*1	Rs	-	-	0.7	kΩ	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	1.5		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
		-	-	2.5		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.8		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V

Note 1. These values are based on simulation. They are not production tested.  
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.

Figure 2.62 shows the equivalent circuit for analog input.

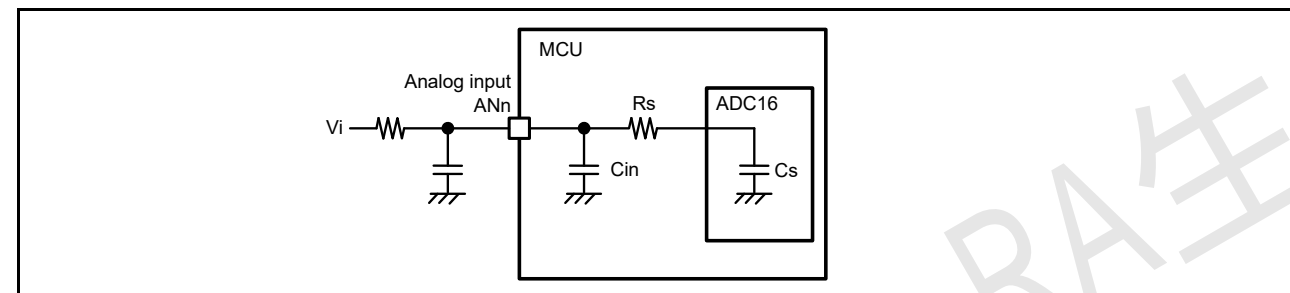


Figure 2.62 Equivalent circuit for analog input

**Table 2.40 16-bit A/D conversion, timing parameters (1 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Frequency	ADCLK	1	-	32	MHz	3.0 V ≤ AVCC0 ≤ 5.5 V, 3.0 V ≤ VREFH0
		1	-	24		2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		1	-	16		2.4 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	8		1.8 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	4		1.7 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
Conversion rate	Fs	-	-	1 / (tsPL + 18 / ADCLK)	S/s	-

2.5 ADC16 Characteristics

**表2.39 16位AD转换、电源和输入范围条件条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5 V, VSS=AVSS0=AVSS1=VREFL0=0V**

应用于VREFH0和VREFL0的参考电压范围。

Parameter	Min	Typ	Max	Unit	测试条件	
高电位参考电压	1.5	3.3	AVCC0	V	-	
低电位参考电压	-	AVSS0	-	V	-	
模拟输入电压范围	0	-	VREFH0	V	-	
输入共模范围	Acm	0	VREFH0/2	V	差分模拟输入	
模拟输入电容*2	Cs	-	-	4.3	pF	
模拟输入电阻*1	Rs	-	-	0.7	kΩ	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	1.5		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
		-	-	2.5		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.8		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V

Note 1. 这些值基于模拟。它们未经生产测试。  
Note 2. 除IO输入电容(Cin)外, 请参阅第2.2.4节, IOVOH、VOL和其他特性。

图2.62显示了模拟输入的等效电路。

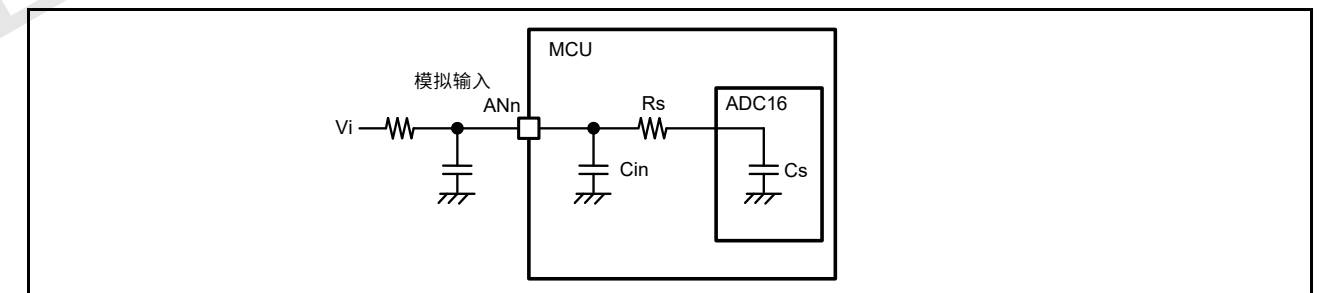


Figure 2.62 模拟输入等效电路

**表2.40 16位AD转换, 时序参数 (1of2) 条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

应用于VREFH0和VREFL0的参考电压范围。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Frequency	ADCLK	1	-	32	MHz	3.0 V ≤ AVCC0 ≤ 5.5 V, 3.0 V ≤ VREFH0
		1	-	24		2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		1	-	16		2.4 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	8		1.8 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	4		1.7 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
兑换率	Fs	-	-	1 / (tsPL + 18 / ADCLK)	S/s	-

**Table 2.40 16-bit A/D conversion, timing parameters (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sampling time*1 Permissible signal source impedance Max = 0.5 kΩ	tsPL	0.25	-	-	μs	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		3	-	-		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
		3	-	-		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		10	-	-		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V
Settling time*1	tSTART	-	-	1	μs	2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.2		1.8 V ≤ AVCC0 < 2.7 V
		-	-	8.9		1.7 V ≤ AVCC0 < 1.8 V

Note 1. These values are based on simulation. They are not production tested.

**Table 2.41 16-bit A/D conversion, linearity parameters**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
External clock input used. Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	16	-	Bit	-
Integral non-linearity *1	INL	-	± 4	± 8	LSB	2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		-	-	± 16		1.7 V ≤ AVCC0 < 2.7 V
Differential non-linearity*1	DNL	-	-1 to +2	-	LSB	-
Offset error*1	Ofst	-	± 4	-	LSB	-
Gain error*1	Gerr	-	-	±0.1	%	2.7 V ≤ VREFH0

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. These values are based on simulation. They are not production tested.

**Table 2.42 16-bit A/D conversion, dynamic parameters (1) (1 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
External clock input used. Reference voltage range applied to VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Signal-to-noise and distortion*2	SINAD	67	81	-	dB	Differential input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		78	81	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	92	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		61	75	-		Single input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		72	75	-		Single input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V

**表2.40 16位AD转换, 时序参数(2of2)条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

应用于VREFH0和VREFL0的参考电压范围。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sampling time*1 允许的的信号源阻抗 Max=0.5kΩ	tsPL	0.25	-	-	μs	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		3	-	-		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
		3	-	-		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		10	-	-		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V
Settling time*1	tSTART	-	-	1	μs	2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.2		1.8 V ≤ AVCC0 < 2.7 V
		-	-	8.9		1.7 V ≤ AVCC0 < 1.8 V

Note 1. 这些值基于模拟。它们未经生产测试。

**表2.41 16位AD转换, 线性参数条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

使用外部时钟输入。应用于VREFH0和VREFL0的参考电压范围。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Resolution	-	-	16	-	Bit	-
Integral non-linearity *1	INL	-	± 4	± 8	LSB	2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		-	-	± 16		1.7 V ≤ AVCC0 < 2.7 V
Differential non-linearity*1	DNL	-	-1 to +2	-	LSB	-
Offset error*1	Ofst	-	± 4	-	LSB	-
Gain error*1	Gerr	-	-	±0.1	%	2.7 V ≤ VREFH0

Note: 该特性适用于不使用除16位AD转换器输入以外的引脚功能时。偏移误差, 满量程误差, DNL微分非线性误差和INL积分非线性误差不包括量化误差。

Note 1. 这些值基于模拟。它们未经生产测试。

**表2.42 16位AD转换, 动态参数(1)(1of2)条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

使用外部时钟输入。应用于VREFH0和VREFL0的参考电压范围。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Signal-to-noise and distortion*2	SINAD	67	81	-	dB	差分输入, Fin=1kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		78	81	-		差分输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	92	-		差分输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		61	75	-		单输入, Fin=1kHz, VRE FH0=1.7V至5.5V, AVCC0 = 1.7 V to 5.5 V
		72	75	-		单输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V

**Table 2.42 16-bit A/D conversion, dynamic parameters (1) (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
External clock input used. Reference voltage range applied to VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Effective number of bits*2	ENOB	11	13.2	-	bit	Differential input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		12.7	13.2	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	15	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		10	12.2	-		Single input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		11.7	12.2	-		Single input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
Total harmonic distortion*1, *2	THD	-	-100	-	dB	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V
		-	-90	-		Single input, Fin = 1 kHz, AVCC0 = 3.3 V
Common mode rejection ratio*2	CMRR	-	100	-	dB	Differential input, Acm = 0 to VREFH0 at 1 kHz, AVCC0 = 3.3 V

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used.

Note 1. THD = HD2 + HD3 + HD4 + HD5.

Note 2. These values are based on simulation. They are not production tested.

**Table 2.43 16-bit A/D conversion, dynamic parameters (2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V  
External clock input used.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Signal-to-noise and distortion*1	SINAD	-	78.6	-	dB	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	76.6	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	74.2	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V
Effective number of bits*1	ENOB	-	12.8	-	bit	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	12.4	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	12.0	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used.

Note 1. These values are based on simulation. They are not production tested.

**表2.42 16位AD转换, 动态参数(1)(2of2)条件: VCC=AVCC0=AVCC1=1.7至5.5V, VREFH0=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

使用外部时钟输入。应用于VREFH0和VREFL0的参考电压范围。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
有效位数*2	ENOB	11	13.2	-	bit	差分输入, Fin=1kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		12.7	13.2	-		差分输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	15	-		差分输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		10	12.2	-		单输入, Fin=1kHz, VREFH0=1.7V至5.5V, AVCC0 = 1.7 V to 5.5 V
		11.7	12.2	-		单输入, Fin=1kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
总谐波失真*1 *2	THD	-	-100	-	dB	差分输入, Fin=1kHz, AVCC0 = 3.3 V
		-	-90	-		单输入, Fin=1kHz, AVCC0 = 3.3 V
共模抑制比*2	CMRR	-	100	-	dB	差分输入, Acm=0至VREFH0, 频率为1kHz, AVCC0 = 3.3 V

Note: 该特性适用于不使用除16位AD转换器输入以外的引脚功能时。

Note 1. THD = HD2 + HD3 + HD4 + HD5.

Note 2. 这些值基于模拟。它们未经生产测试。

**表2.43 16位AD转换, 动态参数(2)条件: VCC=AVCC0=AVCC1=1.7至5.5V, VSS=AVSS0=AVSS1=VREFL0=0V**

使用外部时钟输入。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Signal-to-noise and distortion*1	SINAD	-	78.6	-	dB	差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	76.6	-		差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	74.2	-		差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V
有效位数*1	ENOB	-	12.8	-	bit	差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	12.4	-		差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	12.0	-		差分输入, Fin=1kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V

Note: 该特性适用于不使用除16位AD转换器输入以外的引脚功能时。

Note 1. 这些值基于模拟。它们未经生产测试。



Table 2.44 16-bit A/D converter channel classification

Classification	Channel	Conditions
High-precision channel	AN000 to AN008	AVCC0 = 1.7 to 5.5 V
Normal-precision channel	AN016 to AN023	
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V

Table 2.45 Internal reference voltage for 16-bit ADC (VREFADC) characteristics

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Output voltage range	1.41	1.5	1.59	V	VREFAMPCNT.VREFADCG[1:0] = 00b AVCC0 ≥ 1.7 V
	1.88	2	2.12		VREFAMPCNT.VREFADCG[1:0] = 10b AVCC0 ≥ 2.2 V
	2.35	2.5	2.65		VREFAMPCNT.VREFADCG[1:0] = 11b AVCC0 ≥ 2.7 V
BGR stabilization time*2 (after BGR is enabled)	-	-	150	μs	VREFAMPCNT.BGREN = 1
VREF AMP stabilization time*2 (after VREFAMP is enabled)	-	-	1500	μs	VREFAMPCNT.VREFADCEN = 1
Detect over current*2	-	20	40	mA	-
Load capacitance*1	0.75	1	1.25	μF	-

Note 1. Connect capacitors as stabilization capacitance between the VREFH0 and VREFL0 pins when VREFADC is used.

Note 2. These values are based on simulation. They are not production tested.

Table 2.46 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 2.0 to 5.5 V\*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Sampling time*3	5.0	-	-	μs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 &lt; 2.0 V.

Note 2. The 16-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 16-bit A/D converter.

Note 3. This is a parameter for ADC16 when the internal reference voltage is selected for an analog input channel in ADC16.

## 2.6 SDADC24 Characteristics

Table 2.47 Analog inputs characteristics (1 of 2)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Full-scale range	F <sub>SR</sub>	-	± 0.8 / G <sub>TOTAL</sub>	-	V	-
Analog input in differential input mode	Differential input voltage range	V <sub>ID</sub>	-0.8 / G <sub>TOTAL</sub>	0.8 / G <sub>TOTAL</sub>	V	V <sub>ID</sub> = ANSDnP - ANSDnN, or AMP00 - AMP10 (n = 0 to 3), d <sub>OFR</sub> = 0 mV
	Input voltage range	V <sub>I</sub>	0.2	1.8	V	V <sub>I</sub> = ANSDnP, ANSDnN, AMP00, or AMP10 (n = 0 to 3)
	Common mode Input voltage range	V <sub>COM</sub>	0.2 + ( V <sub>ID</sub>   × G <sub>SET1</sub> ) / 2	1.0	1.8 - ( V <sub>ID</sub>   × G <sub>SET1</sub> ) / 2	V

Table 2.44 16位模数转换器通道分类

Classification	Channel	Conditions
High-precision channel	AN000 to AN008	AVCC0 = 1.7 to 5.5 V
Normal-precision channel	AN016 to AN023	
内部参考电压输入通道	内部参考电压	AVCC0 = 2.0 to 5.5 V
温度传感器输入通道	温度传感器输出	AVCC0 = 2.0 to 5.5 V

Table 2.45 16位ADC(VREFADC)特性的内部参考电压

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V

Parameter	Min	Typ	Max	Unit	测试条件
输出电压范围	1.41	1.5	1.59	V	VREFAMPCNT.VREFADCG[1:0] = 00b AVCC0 ≥ 1.7 V
	1.88	2	2.12		VREFAMPCNT.VREFADCG[1:0] = 10b AVCC0 ≥ 2.2 V
	2.35	2.5	2.65		VREFAMPCNT.VREFADCG[1:0] = 11b AVCC0 ≥ 2.7 V
BGR稳定时间*2 (启用BGR后)	-	-	150	μs	VREFAMPCNT.BGREN = 1
VREFAMP稳定时间*2 (启用VREFAMP后)	-	-	1500	μs	VREFAMPCNT.VREFADCEN = 1
检测过电流*2	-	20	40	mA	-
Load capacitance*1	0.75	1	1.25	μF	-

Note 1. 使用VREFADC时，在VREFH0和VREFL0引脚之间连接电容器作为稳定电容。

Note 2. 这些值基于模拟。它们未经生产测试。

Table 2.46 AD内部参考电压特性

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 2.0 to 5.5 V\*1

Parameter	Min	Typ	Max	Unit	测试条件
内部参考电压输入通道*2	1.36	1.43	1.50	V	-
Sampling time*3	5.0	-	-	μs	-

Note 1. 当AVCC0 &lt; 2.0V时，不能为输入通道选择内部参考电压。

Note 2. 16位AD内部参考电压是指内部参考电压输入到16位AD转换器时的电压。

Note 3. 当为ADC16中的模拟输入通道选择内部参考电压时，这是ADC16的参数。

## 2.6 SDADC24 Characteristics

Table 2.47 模拟输入特性(1of2)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Full-scale range	F <sub>SR</sub>	-	± 0.8 / G <sub>TOTAL</sub>	-	V	-
差分输入模式下的模拟输入	差分输入电压范围	V <sub>ID</sub>	-0.8 / G <sub>TOTAL</sub>	0.8 / G <sub>TOTAL</sub>	V	V <sub>ID</sub> = ANSDnPANSDnN, 或 AMP00AMP10 (n=0至3), d <sub>OFR</sub> =0mV
	输入电压范围	V <sub>I</sub>	0.2	1.8	V	V <sub>I</sub> = ANSDnP, ANSDnN, AMP00或AMP10 (n=0至3)
	共模输入电压范围	V <sub>COM</sub>	0.2 + ( V <sub>ID</sub>   × G <sub>SET1</sub> ) / 2	1.0	1.8 - ( V <sub>ID</sub>   × G <sub>SET1</sub> ) / 2	V

**Table 2.47 Analog inputs characteristics (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Analog Input in single-ended input mode	Input voltage range*1 V <sub>I</sub>	0.2	-	1.8	V	V <sub>I</sub> = ANSDnP, ANSDnN, AMP00, or AMP10 (n = 0 to 3), V <sub>COM</sub> = 1.0 V, d <sub>OFR</sub> = 0 mV, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256

Note 1. The single-ended input mode supports only d<sub>OFR</sub> = 0 mV, G<sub>SET1</sub> = 1, G<sub>SET2</sub> = 1 and OSR = 256.**Table 2.48 Programmable gain instrumentation amplifier and sigma-delta A/D converter (1)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	RES	-	24	-	bits	-
Over sampling frequency	Normal A/D conversion mode	F <sub>OS</sub>	-	1	MHz	-
	Low-power A/D conversion mode	-	0.125	-	-	-
Output data rate	f <sub>DATA1</sub>	0.48828	-	15.625	ksp	Normal A/D conversion mode
	f <sub>DATA2</sub>	61.03615	-	1953.125	sps	Low-power A/D conversion mode
Gain Setting range	G <sub>TOTAL</sub>	1	-	32	V/V	G <sub>TOTAL</sub> = G <sub>SET1</sub> × G <sub>SET2</sub>
1st Gain Setting range	G <sub>SET1</sub>	-	1, 2, 3, 4, 8	-	V/V	-
2nd Gain Setting range	G <sub>SET2</sub>	-	1, 2, 4, 8	-	V/V	-
Offset adjust bit range	d <sub>OFB</sub>	-	5	-	bits	-
Offset adjust range	d <sub>OFR</sub>	-164.06 / G <sub>SET1</sub>	-	+164.06 / G <sub>SET1</sub>	mV	Referred to input
Offset adjust step	d <sub>OFS</sub>	-	350 / 32 / G <sub>SET1</sub>	-	mV	Referred to input

**Table 2.49 Programmable gain instrumentation amplifier and sigma-delta A/D converter (2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

The electrical specifications are applied at differential input mode, external clock input used, F<sub>OS</sub> = 1 MHz, d<sub>OFR</sub> = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Signal to Noise Ratio*1,*3 V <sub>ID</sub> = 0 V	SNR	83	86	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256
		81	84	-	dB	G <sub>SET1</sub> = 8, G <sub>SET2</sub> = 4, OSR = 1024
Signal to Noise and Distortion Ratio*1,*2,*3 f <sub>in</sub> = 50 Hz	SINAD	82	85	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256
		79	82	-	dB	G <sub>SET1</sub> = 8, G <sub>SET2</sub> = 4, OSR = 1024
		74	80	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256, Single-ended input mode

Note: The characteristics apply when no pin functions other than 24-bit sigma-delta A/D converter input are used.

Note 1. SNR and SINAD are the ratio to Full-Scale Range (FSR) of analog inputs. These do not include the noise of analog inputs.

Note 2. When V<sub>ID</sub> is equal to ±0.8 / G<sub>TOTAL</sub> actually, the digital output may overflow due to Gain Error (E<sub>G</sub>), Offset Error (E<sub>OS</sub>), and so forth. As a result, SINAD is degraded. See Table 33.7 of 24-Bit Sigma-Delta A/D Converter (SDADC24) in User's Manual for the relation between analog input and digital output.

Note 3. Not production tested but is guaranteed by the design and characterization.

**Table 2.47 模拟输入特性 (2个中的2个)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
单端输入模式下的模拟输入	输入电压范围*1 V <sub>I</sub>	0.2	-	1.8	V	V <sub>I</sub> = ANSDnP, ANSDnN, AMP00或AMP10 (n = 0至3), V <sub>COM</sub> = 1.0 V, d <sub>OFR</sub> = 0mV, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256

Note 1. 单端输入模式仅支持d<sub>OFR</sub>=0mV、G<sub>SET1</sub>=1、G<sub>SET2</sub>=1和OSR=256。**Table 2.48 可编程增益仪表放大器和sigma-delta AD转换器(1)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Resolution	RES	-	24	-	bits	-
过采样频率	普通模数转换模式	F <sub>OS</sub>	-	1	MHz	-
	低功耗模数转换模式	-	0.125	-	-	-
输出数据速率	f <sub>DATA1</sub>	0.48828	-	15.625	ksp	普通模数转换模式
	f <sub>DATA2</sub>	61.03615	-	1953.125	sps	低功耗模数转换模式
增益设定范围	G <sub>TOTAL</sub>	1	-	32	V/V	G <sub>TOTAL</sub> = G <sub>SET1</sub> × G <sub>SET2</sub>
第一增益设定范围	G <sub>SET1</sub>	-	1, 2, 3, 4, 8	-	V/V	-
第二增益设定范围	G <sub>SET2</sub>	-	1, 2, 4, 8	-	V/V	-
偏移调整位范围	d <sub>OFB</sub>	-	5	-	bits	-
偏移调整范围	d <sub>OFR</sub>	-164.06 / G <sub>SET1</sub>	-	+164.06 / G <sub>SET1</sub>	mV	参考输入
偏移调整步骤	d <sub>OFS</sub>	-	350 / 32 / G <sub>SET1</sub>	-	mV	参考输入

**Table 2.49 可编程增益仪表放大器和sigma-delta AD转换器(2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

除非另有说明, 否则电气规范适用于差分输入模式、使用外部时钟输入、F<sub>OS</sub>=1MHz、d<sub>OFR</sub>=0mV。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
信噪比*1*3 V <sub>ID</sub> = 0 V	SNR	83	86	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256
		81	84	-	dB	G <sub>SET1</sub> = 8, G <sub>SET2</sub> = 4, OSR = 1024
信噪比和失真率*1*2*3 f <sub>in</sub> = 50 Hz	SINAD	82	85	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256
		79	82	-	dB	G <sub>SET1</sub> = 8, G <sub>SET2</sub> = 4, OSR = 1024
		74	80	-	dB	G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, OSR = 256, 单端输入方式

Note: 这些特性适用于除24位sigma-delta AD转换器输入之外没有引脚功能的情况。

Note 1. SNR和SINAD是模拟输入与满量程范围(FSR)的比值。这些不包括模拟输入的噪声。

Note 2. 当V<sub>ID</sub>实际上等于±0.8/G<sub>TOTAL</sub>时, 数字输出可能会因增益误差(EG)、偏移量而溢出错误(EOS)等等。结果, SINAD被降级。请参见表33.7中的24位Sigma-Delta AD转换器(SDADC24)模拟输入和数字输出之间关系的用户手册。

Note 3. 未经生产测试, 但由设计和特性保证。

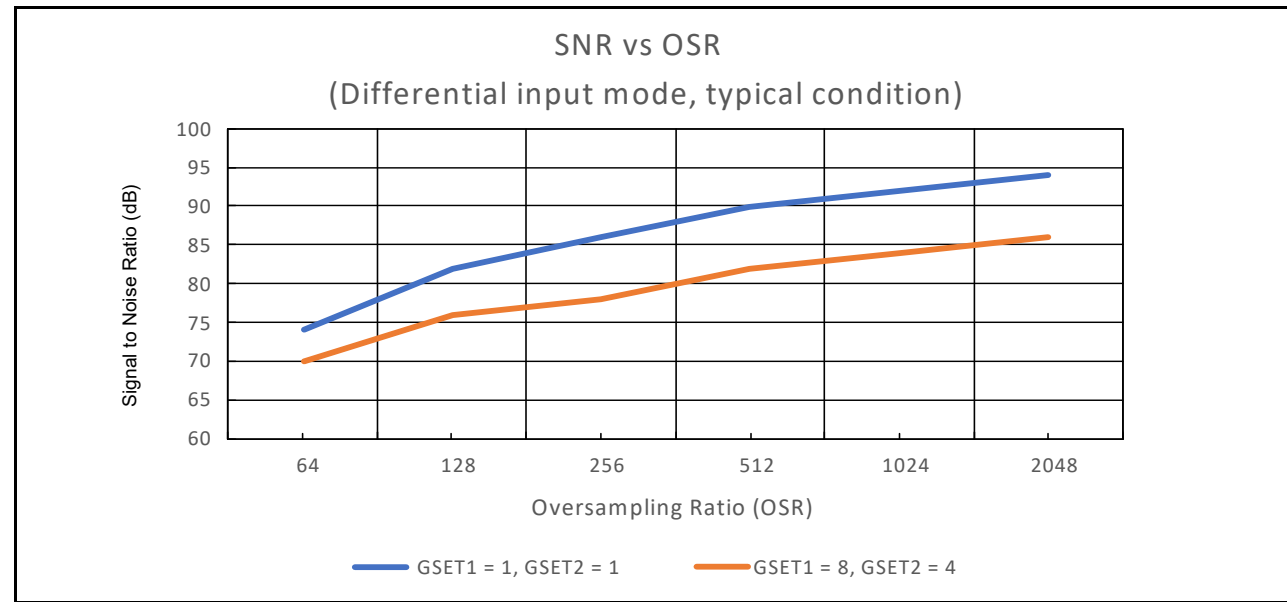


Figure 2.63 SNR vs. OSR (reference data)

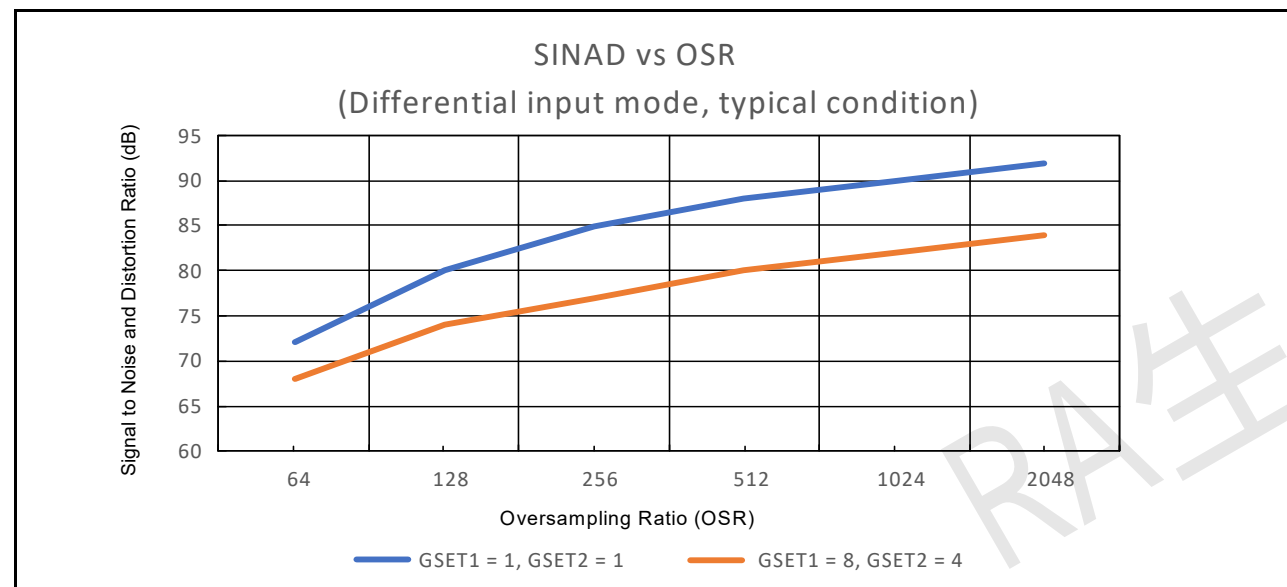


Figure 2.64 SINAD vs. OSR (reference data)

Table 2.50 Programmable gain instrumentation amplifier and sigma-delta A/D converter (3) (1 of 2)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

The electrical specifications are applied at the differential input mode, with external clock input used, Fos = 1 MHz, OSR = 256, and d<sub>OFR</sub> = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain error*2 (excluding SINC3 frequency response characteristic)	E <sub>G</sub>	-0.5	-	0.5	%	After internal calibration, excluding SBIAS error or VREFI error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1
		-3	-	3		Single-ended input mode, excluding SBIAS error or VREFI error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1

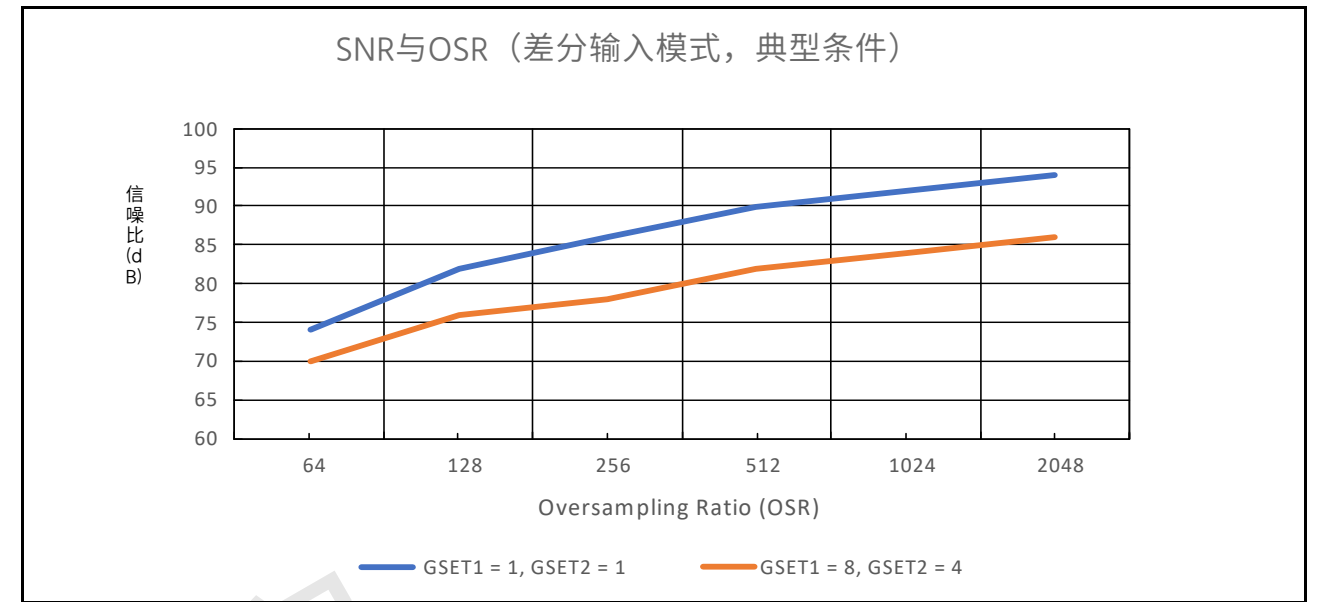


Figure 2.63 SNR vs. OSR (reference data)

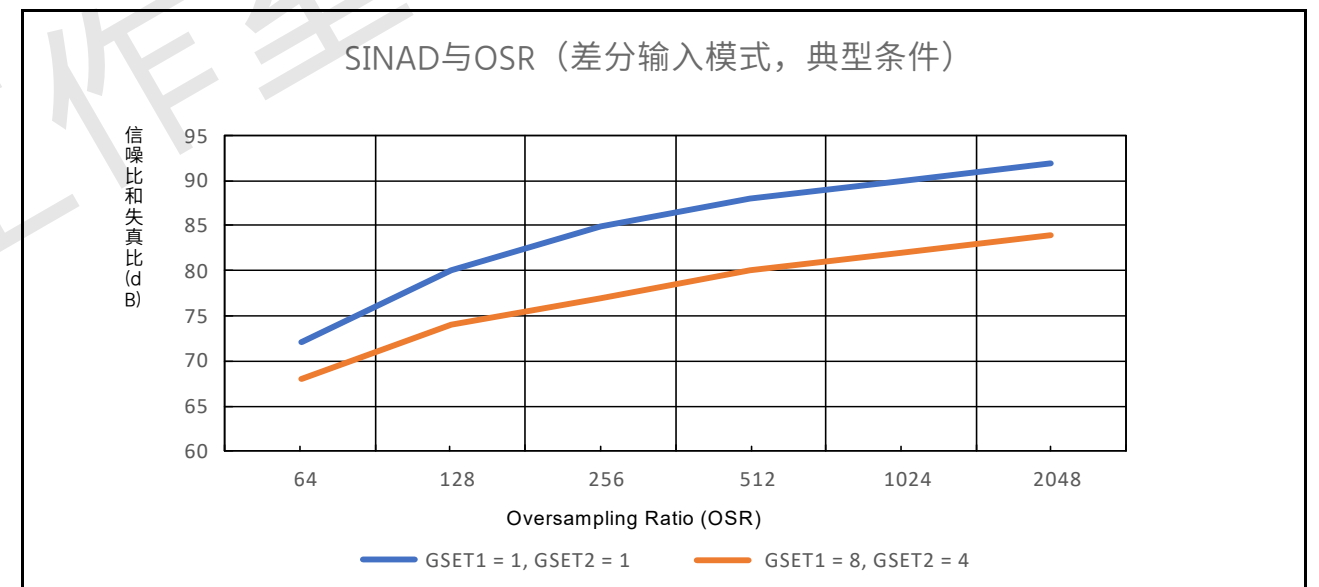


Figure 2.64 SINAD vs. OSR (reference data)

Table 2.50 可编程增益仪表放大器和sigma-delta AD转换器(3)(1of2)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

电气规格适用于差分输入模式, 使用外部时钟输入, Fos=1MHz, 除非另有说明, 否则OSR=256, d<sub>OFR</sub>=0mV。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
增益误差*2 (不包括SINC3频率响应特性)	E <sub>G</sub>	-0.5	-	0.5	%	内部校准后, 排除SBIAS误差或VREFI误差, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1
		-3	-	3		单端输入模式, 不包括SBIAS错误或VREFI错误, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1

**Table 2.50 Programmable gain instrumentation amplifier and sigma-delta A/D converter (3) (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

The electrical specifications are applied at the differential input mode, with external clock input used, Fos = 1 MHz, OSR = 256, and d<sub>OFR</sub> = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain drift*1, *2	dE <sub>G</sub>	-	6	22	ppm/°C	Excluding SBIAS error or VREFI error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1
Offset error*2	E <sub>OS</sub>	-1	-	1	mV	After internal calibration, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, referred to input
		-50	-	50		Single-ended input mode, including SBIAS error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, referred to input
Offset drift*1, *2	dE <sub>OS</sub>	-	2	6	μV/°C	Referred to input
		-	-	120		Single-ended input mode, including SBIAS error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1
Integral non-linearity*2	INL	-	15	-	ppm of FSR	Input = DC, OSR = 2048
Common mode Rejection ratio*2	CMRR	-	80	-	dB	V <sub>COM</sub> = 1.0 ± 0.8 V, f <sub>in</sub> = 50 Hz, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1
Power supply Rejection ratio*2	PSRR	-	70	-	dB	AVCC1 = 5.0 V + 0.1 V <sub>pp_ripple</sub> , f <sub>in</sub> = 50 Hz, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1, excluding SBIAS error or VREFI error
Input absolute current*2	I <sub>IN</sub>	-	2	-	nA	V <sub>I</sub> = 1 V
Input offset current*2	I <sub>INOFFR</sub>	-	1	-	nA	V <sub>ID</sub> = 0 V, V <sub>COM</sub> = 1 V
Input impedance*2	Z <sub>IN</sub>	-	500	-	Mohm	V <sub>ID</sub> = 1 V, V <sub>COM</sub> = 1 V
Offset adjust gain error*2	d <sub>OFGE</sub>	-5	-	5	%	Including SBIAS error, d <sub>OFR</sub> ≠ 0 mV
Offset adjust integral non-linearity*2	d <sub>OFINL</sub>	-0.5	-	0.5	LSB	d <sub>OFR</sub> ≠ 0 mV

Note: The characteristics apply when no pin functions other than 24-bit sigma-delta A/D converter input are used.

Note 1. Gain drift is calculated by (Max (EG (T (-40°C) to T (125°C)))) - Min (EG (T (-40°C) to T (125°C)))) / (125°C - (-40°C)). Offset drift is calculated by (Max (EOS (T (-40°C) to T (125°C)))) - Min (EOS (T (-40°C) to T (125°C)))) / (125°C - (-40°C)).

Note 2. Not production tested but is guaranteed by the design and characterization.

**Table 2.51 2.1 V LDO linear regulator for ADC (ADREG) characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Connect the ADREG pin to a AVSS1 pin by a 0.47 μF (-50% to +20%) capacitor.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
ADREG output voltage	V <sub>ADREG</sub>	-	2.1	-	V	-

**Table 2.52 ADC external reference voltage (VREFI) characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External reference voltage range*1	VREFI	0.8	-	2.4	V	SDADCSTC1.VREFSEL = 1
External reference voltage step	VR <sub>STEP</sub>	-	0.2	-	V	SDADCSTC1.VREFSEL = 1
External reference voltage accuracy	VR <sub>A</sub>	-3	-	3	%	SDADCSTC1.VREFSEL = 1

Note 1. Select the reference voltage input value with STC1.VSBIAS[3:0].

**Table 2.50 可编程增益仪表放大器和sigma-delta AD转换器(3)(2of2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

电气规格适用于差分输入模式, 使用外部时钟输入, Fos=1MHz, 除非另有说明, 否则OSR=256, d<sub>OFR</sub>=0mV。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Gain drift*1, *2	dE <sub>G</sub>	-	6	22	ppm/°C	排除SBIAS错误或VREFI error, G <sub>SET1</sub> = 1, G <sub>SET2</sub> = 1
Offset error*2	E <sub>OS</sub>	-1	-	1	mV	内部校准后, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1, 参考输入
		-50	-	50		单端输入模式, 包括SBIAS误差, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1, 参考输入
Offset drift*1, *2	dE <sub>OS</sub>	-	2	6	μV/°C	参考输入
		-	-	120		单端输入模式, 包括SBIAS误差, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1
Integral non-linearity*2	INL	-	15	-	ppm of FSR	Input = DC, OSR = 2048
共模抑制比*2	CMRR	-	80	-	dB	V <sub>COM</sub> =1.0±0.8V, f <sub>i</sub> n=50Hz, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1
电源 Rejection ratio*2	PSRR	-	70	-	dB	AVCC1=5.0V+0.1V <sub>pp_ripple</sub> , f <sub>i</sub> n=50Hz, G <sub>SET1</sub> =1, G <sub>SET2</sub> =1, 不包括 SBIAS错误或VREFI错误
输入绝对电流*2	I <sub>IN</sub>	-	2	-	nA	V <sub>I</sub> = 1 V
输入失调电流*2	I <sub>INOFFR</sub>	-	1	-	nA	V <sub>ID</sub> =0V, V <sub>COM</sub> =1V
Input impedance*2	Z <sub>IN</sub>	-	500	-	Mohm	V <sub>ID</sub> =1V, V <sub>COM</sub> =1V
偏移调整增益误差*2	d <sub>OFGE</sub>	-5	-	5	%	包括SBIAS误差, d <sub>OFR</sub> ≠0mV
偏移调整积分非线性*2	d <sub>OFINL</sub>	-0.5	-	0.5	LSB	d <sub>OFR</sub> ≠0mV

Note: 这些特性适用于除24位sigma-delta AD转换器输入之外没有引脚功能的情况。

Note 1. 增益漂移计算公式为(Max(EG(T(-40°C)toT(125°C)))Min(EG(T(-40°C)toT(125°C))))/(125°C-(-40°C))。偏移漂移的计算公式为(Max(EOS(T(-40°C)toT(125°C)))Min(EOS(T(-40°C)toT(125°C))))/(125°C-(-40°C))。

Note 2. 未经生产测试, 但由设计和特性保证。

**表2.51用于ADC(ADREG)特性的2.1VLDO线性稳压器条件: VCC=AVCC0=AVCC1=2.7至5.5V, VSS=AVSS0=AVSS1=0V**

通过一个0.47μF (-50%至+20%) 电容将ADREG引脚连接到AVSS1引脚。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
ADREG输出电压	V <sub>ADREG</sub>	-	2.1	-	V	-

**Table 2.52 ADC外部参考电压(VREFI)特性**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
外部参考电压范围*1	VREFI	0.8	-	2.4	V	SDADCSTC1.VREFSEL = 1
外部参考电压阶跃	VR <sub>STEP</sub>	-	0.2	-	V	SDADCSTC1.VREFSEL = 1
外部参考电压精度	VR <sub>A</sub>	-3	-	3	%	SDADCSTC1.VREFSEL = 1

Note 1. 使用STC1.VSBIAS[3:0]选择参考电压输入值。



**Table 2.53 Sensor bias (SBIAS) characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V  
Connect the SBIAS/VREF1 pin to a AVSS1 pin by a 0.22  $\mu$ F (-20% to +20%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage range*2	SBIAS	0.8	-	2.2	V	-
Output voltage step	SV <sub>STEP</sub>	-	0.2	-	V	-
Output voltage accuracy*1	SV <sub>A</sub>	-3	-	3	%	SI <sub>OUT</sub> = 1 mA
Output current*1	SI <sub>OUT</sub>	-	-	10	mA	-
Short current*1	SI <sub>SHORT</sub>	-	35	65	mA	SBIAS = 0 V
Load regulation*1	SL <sub>R</sub>	-	-	15	mV	1 mA $\leq$ SI <sub>OUT</sub> $\leq$ 5 mA
		-	-	20	mV	1 mA $\leq$ SI <sub>OUT</sub> $\leq$ 10 mA
Power supply rejection ratio*1	SPSRR	-	50	-	dB	AVCC1 = 5.0 V + 0.1 V <sub>pp_ripple</sub> , f = 100 Hz, SI <sub>OUT</sub> = 2.5 mA
Transition time of one step*1,*3	ST <sub>TS</sub>	-	-	80	$\mu$ s	SBIAS $\leq$ SV <sub>A</sub> $\pm$ 3%
		-	-	-	-	1 mA $\leq$ SI <sub>OUT</sub> $\leq$ SI <sub>OUT_MAX</sub>

Note 1. Not production tested but is guaranteed by the design and characterization.

Note 2. Select the reference voltage output value for the sensor with STC1.VSBIAS[3:0].

Note 3. The load current of more than 1 mA is required because the output stage of SBIAS is Pch open drain. When the original load current is small, additional external load resistance is required.

## 2.7 DAC12 Characteristics

**Table 2.54 12-bit D/A conversion characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VREFH = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions	
Resolution	-	-	12	bit	-	
Charge pump stabilization time*1	-	-	100	$\mu$ s	-	
SW stabilization time*1	-	-	50	$\mu$ s	-	
Conversion time*1	DAC Ref. = AVCC or VREFH $\geq$ 2.7 V	-	-	1.0	$\mu$ s	Cl <sub>oad</sub> = 38 pF, @ 1 LSB step Cl <sub>oad</sub> = 8 pF, @ full range
	DAC Ref. = AVCC or VREFH < 2.7 V	-	-	1.2	$\mu$ s	-
Wake-up time*1	-	-	1.0	$\mu$ s	-	
Absolute accuracy	-	-	$\pm$ 12	LSB	2-M $\Omega$ resistive load	
DNL differential non-linearity error	DAC Ref. = AVCC or VREFH $\geq$ 2.7 V	-	-	$\pm$ 1.0	LSB	-
	DAC Ref. = AVCC or VREFH < 2.7 V	-	-	$\pm$ 2.0	LSB	-
INL integral non-linearity error	-	-	$\pm$ 7.0	LSB	-	
RO output resistance	-	3.5	-	k $\Omega$	-	
Load resistance	2	2	-	M $\Omega$	-	
Load capacitance	1 LSB step	-	38	-	pF	-
	Full range	-	8	-	pF	-

Note 1. These values are based on simulation. They are not production tested.

## 2.8 DAC8 Characteristics

**Table 2.55 8-bit D/A conversion characteristics (1 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	8	bit	-
Charge pump stabilization time*1	-	-	100	$\mu$ s	-

**Table 2.53 传感器偏置(SBIAS)特性**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V  
通过0.22 $\mu$ F (-20%至+20%) 将SBIAS/VREF1引脚连接到AVSS1引脚

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
输出电压范围*2	SBIAS	0.8	-	2.2	V	-
输出电压阶跃	SV <sub>STEP</sub>	-	0.2	-	V	-
输出电压精度*1	SV <sub>A</sub>	-3	-	3	%	SI输出=1毫安
Output current*1	出局	-	-	10	mA	-
Short current*1	SI短	-	35	65	mA	SBIAS = 0 V
Load regulation*1	SL <sub>R</sub>	-	-	15	mV	1毫安 $\leq$ SI输出 $\leq$ 5毫安
		-	-	20	mV	1毫安 $\leq$ SI输出 $\leq$ 10毫安
电源抑制比*1	SPSRR	-	50	-	dB	AVCC1=5.0V+0.1V <sub>pp_ripple</sub> , f=100Hz, SIOUT=2.5mA
一步过渡时间*1 *3	ST <sub>TS</sub>	-	-	80	$\mu$ s	SBIAS < SV <sub>A</sub> $\pm$ 3%
		-	-	-	-	1mA $\leq$ SIOUT $\leq$ SIOUT_MAX

Note 1. 未经生产测试，但由设计和特性保证。

Note 2. 使用STC1.VSBIAS[3:0]为传感器选择参考电压输出值。

Note 3. 由于SBIAS的输出级为Pch开漏，因此需要1mA以上的负载电流。当原始负载电流较小时，需要额外的外部负载电阻。

## 2.7 DAC12 Characteristics

**表2.54 12位DA转换特性条件: VCC=AVCC0=AVCC1=1.7V至5.5V, VREFH=1.7V至5.5V, VSS=AVSS0=AVSS1=VREFL=0V**

Parameter	Min	Typ	Max	Unit	测试条件	
Resolution	-	-	12	bit	-	
电荷泵稳定时间*1	-	-	100	$\mu$ s	-	
SW stabilization time*1	-	-	50	$\mu$ s	-	
Conversion time*1	DAC参考。=AVCC或VREFH $\geq$ 2.7V	-	-	1.0	$\mu$ s	Cl <sub>oad</sub> = 38 pF, @ 1 LSB step Cl <sub>oad</sub> =8pF, @全范围
	DAC参考。=AVCC或VREFH<2.7V	-	-	1.2	$\mu$ s	-
Wake-up time*1	-	-	1.0	$\mu$ s	-	
绝对精度	-	-	$\pm$ 12	LSB	2M $\Omega$ 电阻负载	
DNL微分非线性误差	DAC参考。=AVCC或VREFH $\geq$ 2.7V	-	-	$\pm$ 1.0	LSB	-
	DAC参考。=AVCC或VREFH<2.7V	-	-	$\pm$ 2.0	LSB	-
INL积分非线性误差	-	-	$\pm$ 7.0	LSB	-	
RO输出电阻	-	3.5	-	k $\Omega$	-	
负载电阻	2	2	-	M $\Omega$	-	
负载电容	1 LSB step	-	38	-	pF	-
	全系列	-	8	-	pF	-

Note 1. 这些值基于模拟。它们未经生产测试。

## 2.8 DAC8 Characteristics

**表2.55 8位DA转换特性(1 of 2)条件: VCC=AVCC0=AVCC1=1.7V至5.5V, VSS=AVSS0=AVSS1=0V**

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	8	bit	-
电荷泵稳定时间*1	-	-	100	$\mu$ s	-



**Table 2.55 8-bit D/A conversion characteristics (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Switch stabilization time*1	-	-	50	μs	-
Conversion time*1	AVCC0 = 2.7 to 5.5 V	-	3.0	μs	35-pF capacitive load
	AVCC0 = 1.7 to 2.7 V	-	6.0	μs	
Absolute accuracy	AVCC0 = 2.7 to 5.5 V	-	± 3.0	LSB	2-MΩ resistive load
	AVCC0 = 1.7 to 2.7 V	-	± 3.5		
	AVCC0 = 2.7 to 5.5 V	-	± 2.0	LSB	4-MΩ resistive load
	AVCC0 = 1.7 to 2.7 V	-	± 2.5		
RO output resistance	-	7.4	-	kΩ	-

Note 1. These values are based on simulation. They are not production tested.

## 2.9 TSN Characteristics

**Table 2.56 TSN characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy		-	± 1.5	-	°C	2.4 V or above
		-	± 2.0	-	°C	Below 2.4 V
Temperature slope	-	-	-3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t <sub>START</sub>	-	-	5	μs	-
Sampling time	-	5	-	-	μs	-

## 2.10 OSC Stop Detect Characteristics

**Table 2.57 Oscillation stop detection circuit characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t <sub>dr</sub>	-	-	1	ms	Figure 2.65

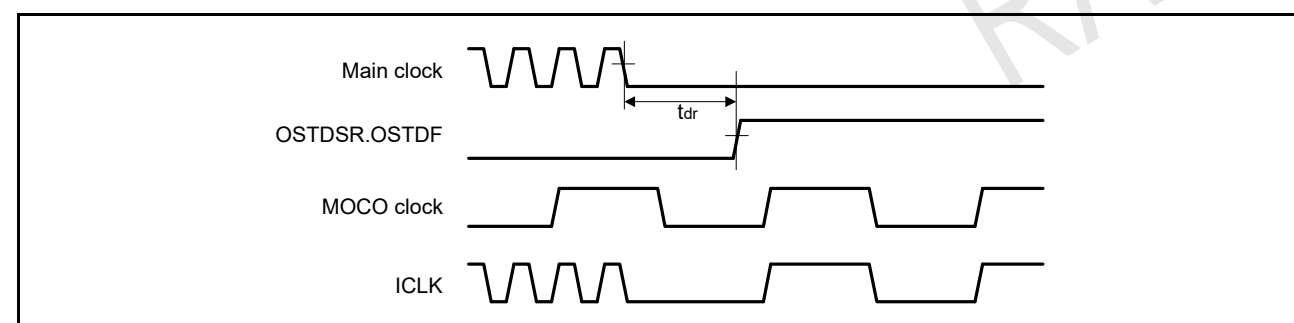


Figure 2.65 Oscillation stop detection timing

**表2.558位DA转换特性(2of2)条件: VCC=AVCC0=AVCC1=1.7V至5.5V, VSS=AVSS0=AVSS1=0V**

Parameter	Min	Typ	Max	Unit	测试条件
开关稳定时间*1	-	-	50	μs	-
Conversion time*1	AVCC0 = 2.7 to 5.5 V	-	3.0	μs	35-pF capacitive load
	AVCC0 = 1.7 to 2.7 V	-	6.0	μs	
绝对精度	AVCC0 = 2.7 to 5.5 V	-	± 3.0	LSB	2MΩ电阻负载
	AVCC0 = 1.7 to 2.7 V	-	± 3.5		
	AVCC0 = 2.7 to 5.5 V	-	± 2.0	LSB	4MΩ电阻负载
	AVCC0 = 1.7 to 2.7 V	-	± 2.5		
RO输出电阻	-	7.4	-	kΩ	-

Note 1. 这些值基于模拟。它们未经生产测试。

## 2.9 TSN Characteristics

**Table 2.56 TSN characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度		-	± 1.5	-	°C	2.4V或以上
		-	± 2.0	-	°C	Below 2.4 V
温度斜率	-	-	-3.65	-	mV/°C	-
输出电压 (25°C时)	-	-	1.05	-	V	VCC = 3.3 V
温度传感器启动时间	t <sub>START</sub>	-	-	5	μs	-
采样时间	-	5	-	-	μs	-

## 2.10 OSC停止检测特性

**Table 2.57 振荡停止检测电路特性**

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t <sub>dr</sub>	-	-	1	ms	Figure 2.65

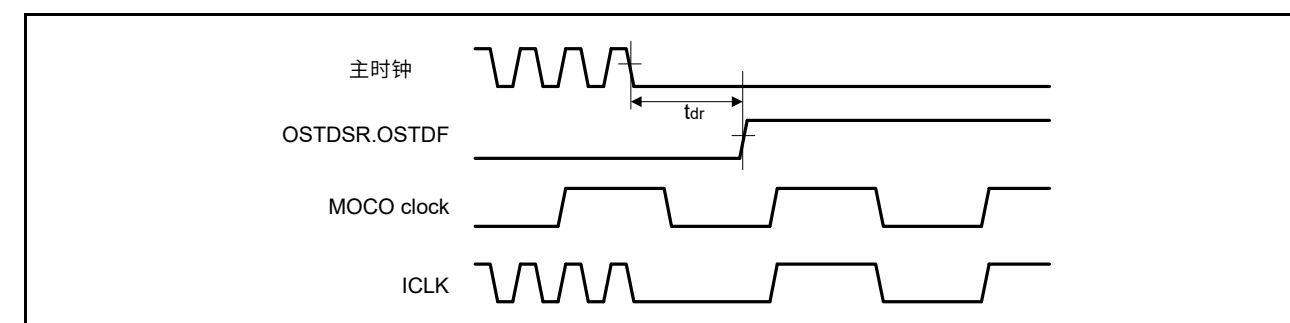


Figure 2.65 振荡停止检测时机

## 2.11 POR and LVD Characteristics

Table 2.58 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	V <sub>POR</sub>	1.27	1.42	1.57	V	Figure 2.66, Figure 2.67
	Voltage detection circuit (LVD0)*2	V <sub>det0_0</sub>	3.68	3.85	4.00	V	Figure 2.68 At falling edge VCC
		V <sub>det0_1</sub>	2.68	2.85	2.96		
		V <sub>det0_2</sub>	2.38	2.53	2.64		
		V <sub>det0_3</sub>	1.78	1.90	2.02		
		V <sub>det0_4</sub>	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V <sub>det1_0</sub>	4.13	4.29	4.45	V	Figure 2.69 At falling edge VCC
		V <sub>det1_1</sub>	3.98	4.16	4.30		
		V <sub>det1_2</sub>	3.86	4.03	4.18		
		V <sub>det1_3</sub>	3.68	3.86	4.00		
		V <sub>det1_4</sub>	2.98	3.10	3.22		
		V <sub>det1_5</sub>	2.89	3.00	3.11		
		V <sub>det1_6</sub>	2.79	2.90	3.01		
		V <sub>det1_7</sub>	2.68	2.79	2.90		
		V <sub>det1_8</sub>	2.58	2.68	2.78		
V <sub>det1_9</sub>		2.48	2.58	2.68			
V <sub>det1_A</sub>		2.38	2.48	2.58			
V <sub>det1_B</sub>		2.10	2.20	2.30			
V <sub>det1_C</sub>		1.84	1.96	2.05			
V <sub>det1_D</sub>		1.74	1.86	1.95			
V <sub>det1_E</sub>	1.63	1.75	1.84				
V <sub>det1_F</sub>	1.60	1.65	1.73				
Voltage detection circuit (LVD2)*4	V <sub>det2_0</sub>	4.11	4.31	4.48	V	Figure 2.70 At falling edge VCC	
	V <sub>det2_1</sub>	3.97	4.17	4.34			
	V <sub>det2_2</sub>	3.83	4.03	4.20			
	V <sub>det2_3</sub>	3.64	3.84	4.01			

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol V<sub>det0\_#</sub> denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol V<sub>det1\_#</sub> denotes the value of the LVDLVL.R.LVD1LVL[4:0] bits.

Note 4. # in the symbol V<sub>det2\_#</sub> denotes the value of the LVDLVL.R.LVD2LVL[2:0] bits.

## 2.11 POR和LVD特性

Table 2.58 上电复位电路及电压检测电路特性 (一)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平*1	Power-on reset (POR)	V <sub>POR</sub>	1.27	1.42	1.57	V	Figure 2.66, Figure 2.67
	电压检测电路 (LVD0) *2	V <sub>det0_0</sub>	3.68	3.85	4.00	V	Figure 2.68 在下降沿 VCC
		V <sub>det0_1</sub>	2.68	2.85	2.96		
		V <sub>det0_2</sub>	2.38	2.53	2.64		
		V <sub>det0_3</sub>	1.78	1.90	2.02		
		V <sub>det0_4</sub>	1.60	1.69	1.82		
	电压检测电路 (LVD1) *3	V <sub>det1_0</sub>	4.13	4.29	4.45	V	Figure 2.69 在下降沿 VCC
		V <sub>det1_1</sub>	3.98	4.16	4.30		
		V <sub>det1_2</sub>	3.86	4.03	4.18		
		V <sub>det1_3</sub>	3.68	3.86	4.00		
		V <sub>det1_4</sub>	2.98	3.10	3.22		
		V <sub>det1_5</sub>	2.89	3.00	3.11		
		V <sub>det1_6</sub>	2.79	2.90	3.01		
		V <sub>det1_7</sub>	2.68	2.79	2.90		
		V <sub>det1_8</sub>	2.58	2.68	2.78		
V <sub>det1_9</sub>		2.48	2.58	2.68			
V <sub>det1_A</sub>		2.38	2.48	2.58			
V <sub>det1_B</sub>		2.10	2.20	2.30			
V <sub>det1_C</sub>		1.84	1.96	2.05			
V <sub>det1_D</sub>		1.74	1.86	1.95			
V <sub>det1_E</sub>	1.63	1.75	1.84				
V <sub>det1_F</sub>	1.60	1.65	1.73				
电压检测电路 (LVD2) *4	V <sub>det2_0</sub>	4.11	4.31	4.48	V	Figure 2.70 在下降沿 VCC	
	V <sub>det2_1</sub>	3.97	4.17	4.34			
	V <sub>det2_2</sub>	3.83	4.03	4.20			
	V <sub>det2_3</sub>	3.64	3.84	4.01			

Note 1. 这些特性适用于电源上没有叠加噪声的情况。当设置导致该电压检测电平与电压检测电路的电平重叠时，无法指定是LVD1还是LVD2用于电压检测。

Note 2. 符号V<sub>det0\_#</sub>中的#表示OFS1.VDSEL1[2:0]位的值。

Note 3. 符号V<sub>det1\_#</sub>中的#表示LVDLVL.R.LVD1LVL[4:0]位的值。

Note 4. 符号V<sub>det2\_#</sub>中的#表示LVDLVL.R.LVD2LVL[2:0]位的值。

Table 2.59 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	$t_{POR}$	-	1.7	-	ms	-
	LVD0: disable	$t_{POR}$	-	1.3	-	ms	-
Wait time after voltage monitor 0,1,2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0: disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		$t_{det}$	-	-	350	$\mu$ s	Figure 2.66, Figure 2.67
Minimum VCC down time		$t_{VOFF}$	450	-	-	$\mu$ s	Figure 2.66, VCC = 1.0 V or above
Power-on reset enable time		$t_W$ (POR)	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$T_d$ (E-A)	-	-	300	$\mu$ s	Figure 2.69, Figure 2.70
Hysteresis width (POR)		$V_{PORH}$	-	110	-	mV	-
Hysteresis width (LVD0, LVD1 and LVD2)		$V_{LVH}$	-	60	-	mV	LVD0 selected
			-	100	-		$V_{det1\_0}$ to $V_{det1\_2}$ selected
			-	60	-		$V_{det1\_3}$ to $V_{det1\_9}$ selected
			-	50	-		$V_{det1\_A}$ to $V_{det1\_B}$ selected
			-	40	-		$V_{det1\_C}$ to $V_{det1\_F}$ selected
			-	60	-		LVD2 selected
			-	60	-		

Note 1. When OFS1.LVDAS = 0.  
 Note 2. When OFS1.LVDAS = 1.  
 Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels  $V_{POR}$ ,  $V_{det0}$ ,  $V_{det1}$ , and  $V_{det2}$  for the POR/LVD.

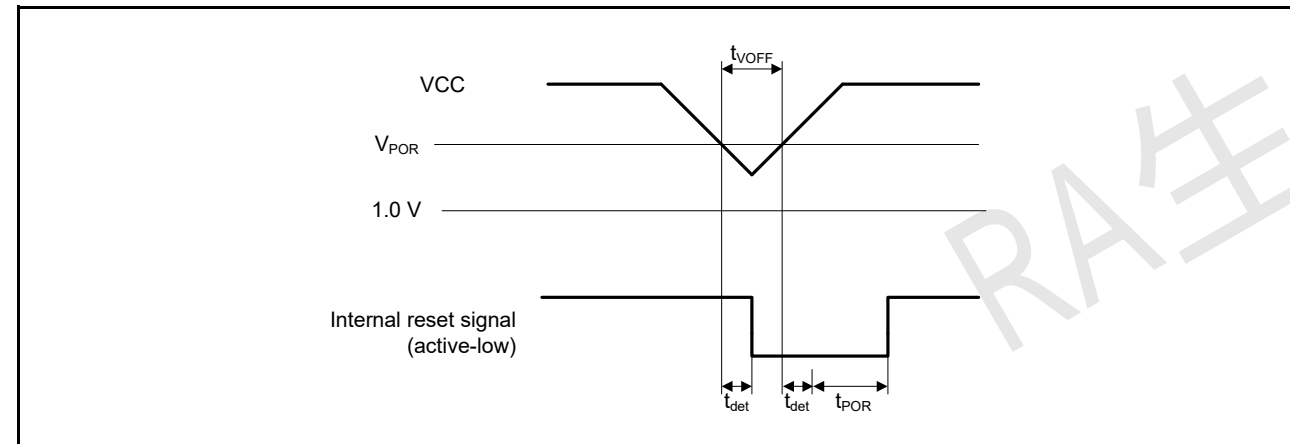


Figure 2.66 Voltage detection reset timing

Table 2.59 上电复位电路及电压检测电路特性 (二)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上电复位取消后的等待时间	LVD0: enable	$t_{POR}$	-	1.7	-	ms	-
	LVD0: disable	$t_{POR}$	-	1.3	-	ms	-
电压监视器0,1,2复位取消后的等待时间	LVD0: enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0: disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		$t_{det}$	-	-	350	$\mu$ s	Figure 2.66, Figure 2.67
最小VCC停机时间		$t_{VOFF}$	450	-	-	$\mu$ s	Figure 2.66, VCC=1.0V或以上
上电复位使能时间		$t_W$ (POR)	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD操作稳定时间 (启用LVD后)		$T_d$ (E-A)	-	-	300	$\mu$ s	Figure 2.69, Figure 2.70
迟滞宽度(POR)		$V_{PORH}$	-	110	-	mV	-
迟滞宽度 (LVD0、LVD1和LVD2)		$V_{LVH}$	-	60	-	mV	LVD0 selected
			-	100	-		选择 $V_{det1\_0}$ 至 $V_{det1\_2}$
			-	60	-		选择 $V_{det1\_3}$ 至 $V_{det1\_9}$
			-	50	-		选择 $V_{det1\_A}$ 至 $V_{det1\_B}$
			-	40	-		选择 $V_{det1\_C}$ 至 $V_{det1\_F}$
			-	60	-		LVD2 selected
			-	60	-		

Note 1. When OFS1.LVDAS = 0.  
 Note 2. When OFS1.LVDAS = 1.  
 Note 3. 最小VCC停机时间表示VCC低于电压检测电平 $V_{POR}$ 的最小值的时间，POR/LVD的 $V_{det0}$ 、 $V_{det1}$ 和 $V_{det2}$ 。

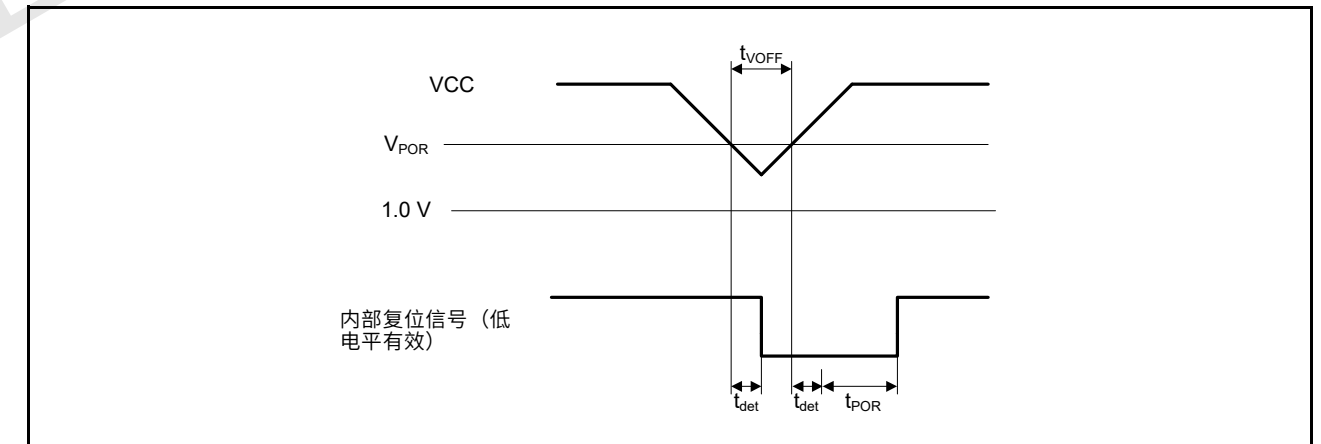


Figure 2.66 电压检测复位时序

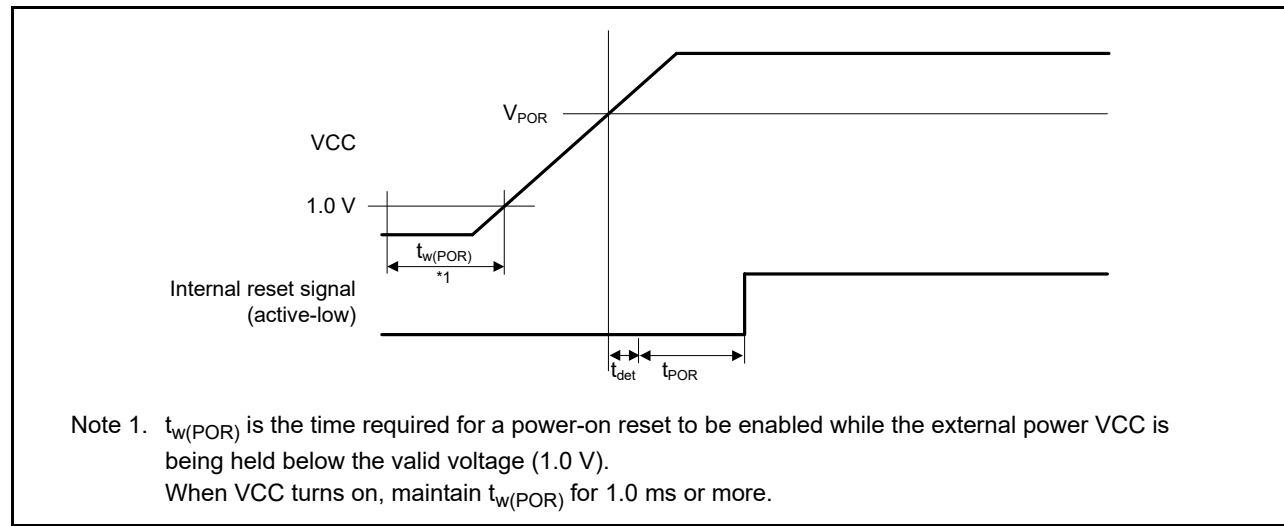


Figure 2.67 Power-on reset timing

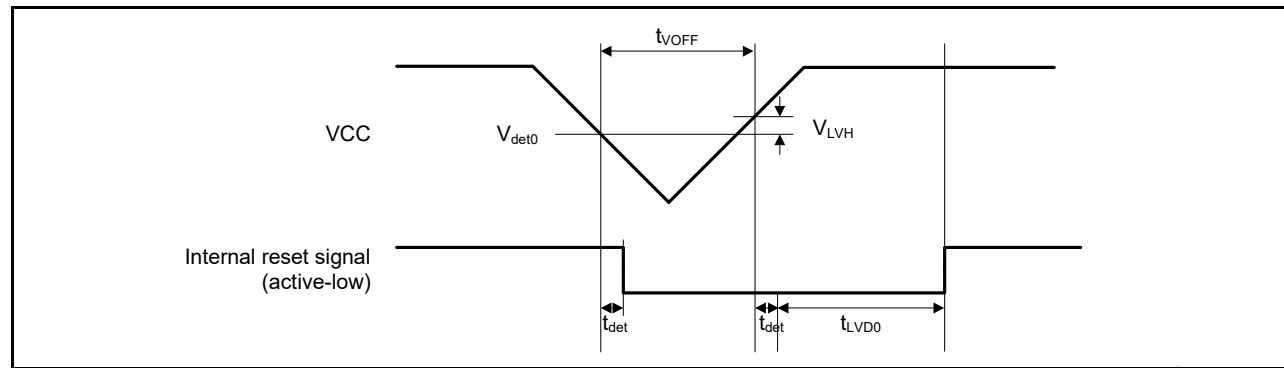


Figure 2.68 Voltage detection circuit timing (V<sub>det0</sub>)

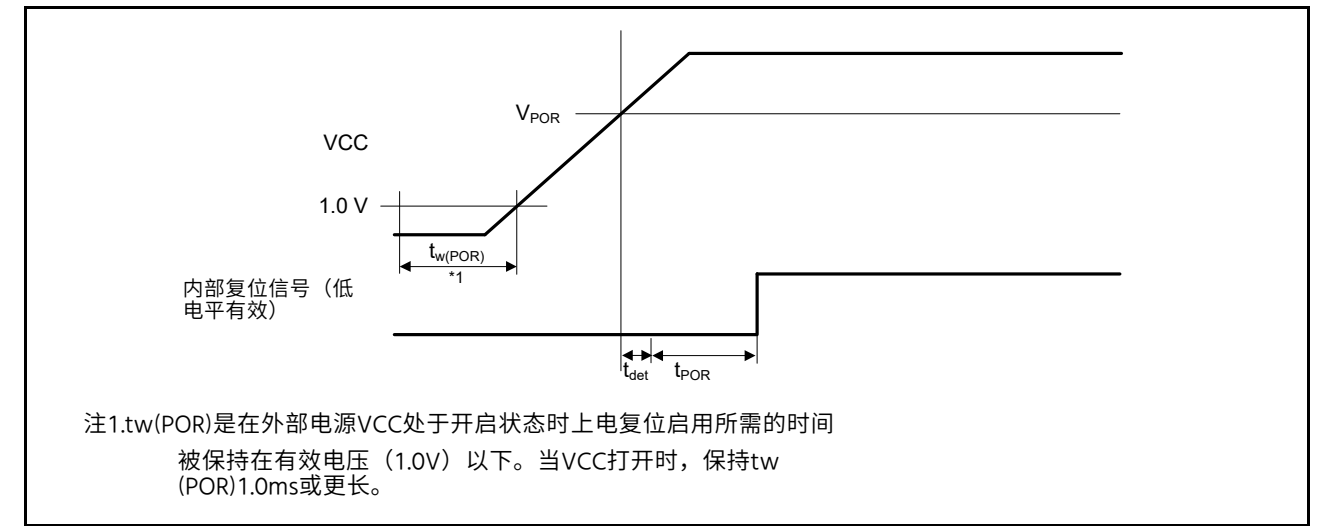


Figure 2.67 上电复位时序

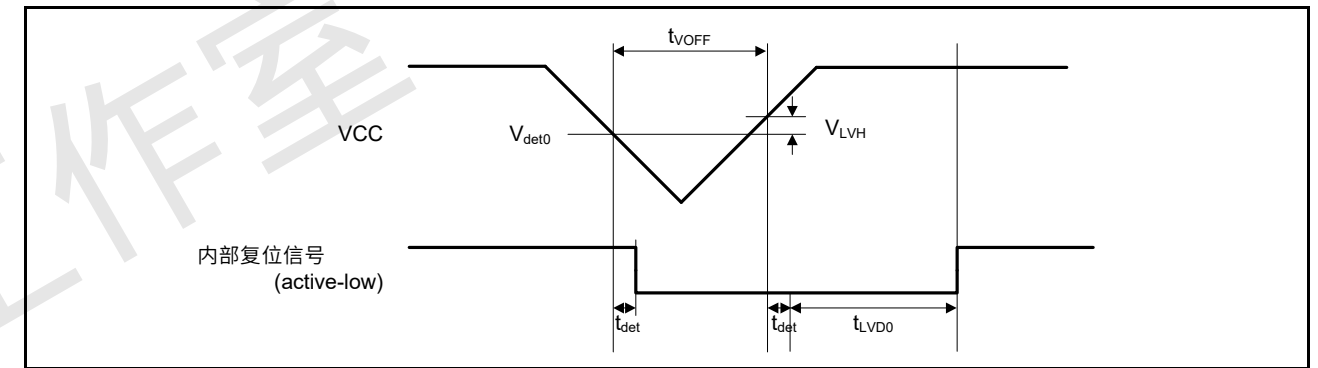


Figure 2.68 电压检测电路时序 (V<sub>det0</sub>)

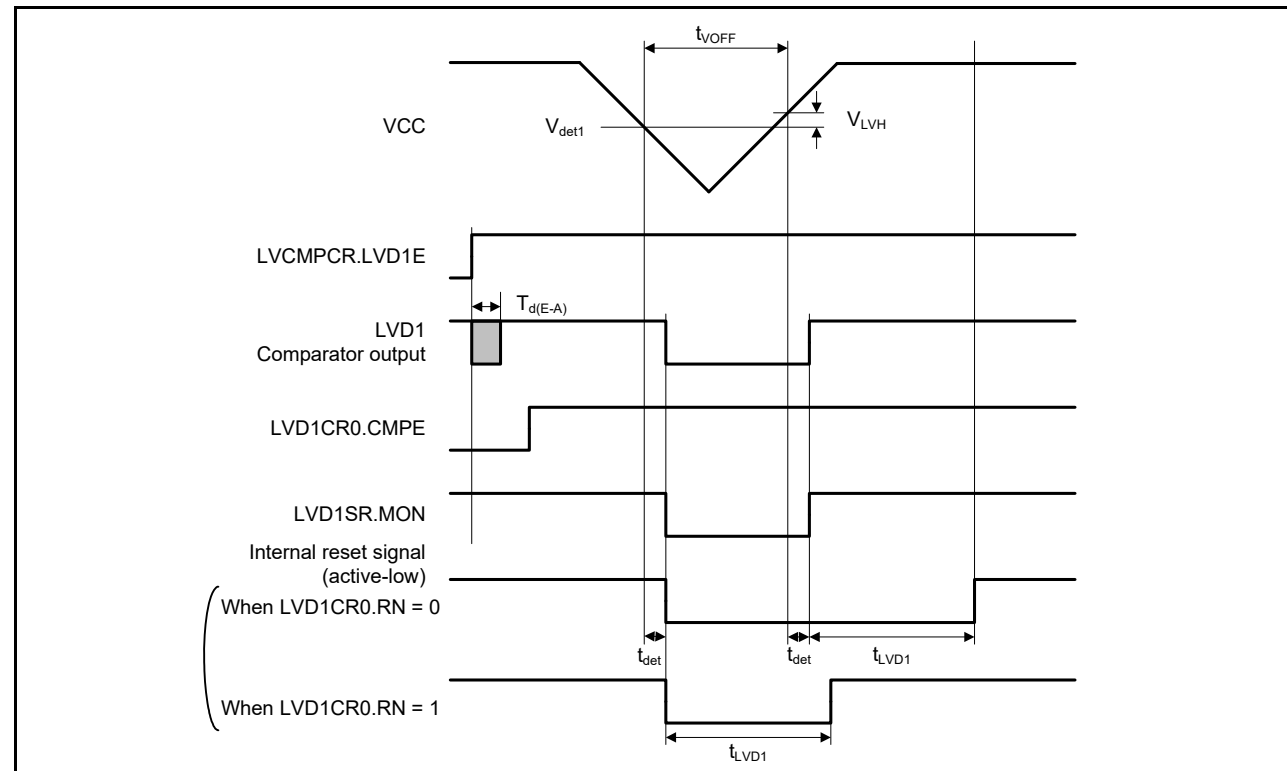


Figure 2.69 Voltage detection circuit timing (V<sub>det1</sub>)

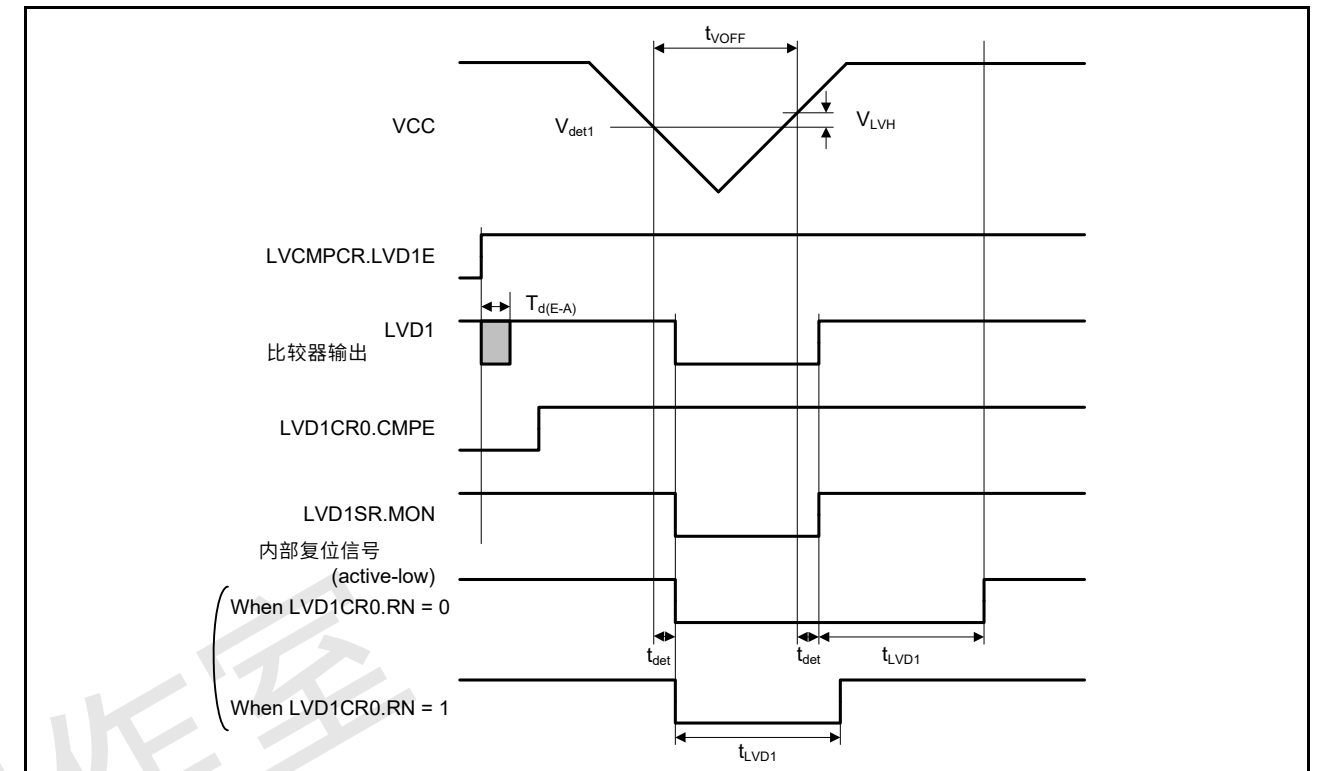


Figure 2.69 电压检测电路时序 (V<sub>det1</sub>)

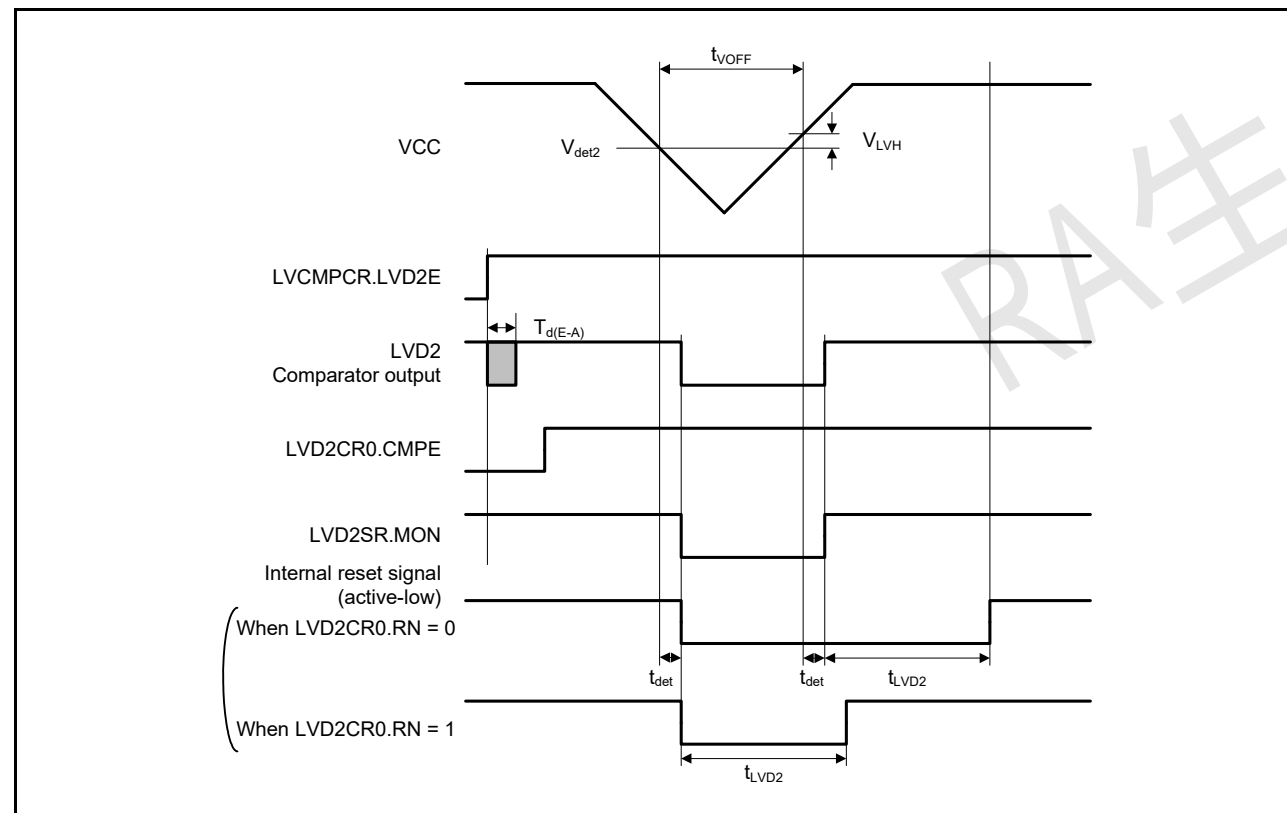


Figure 2.70 Voltage detection circuit timing (V<sub>det2</sub>)

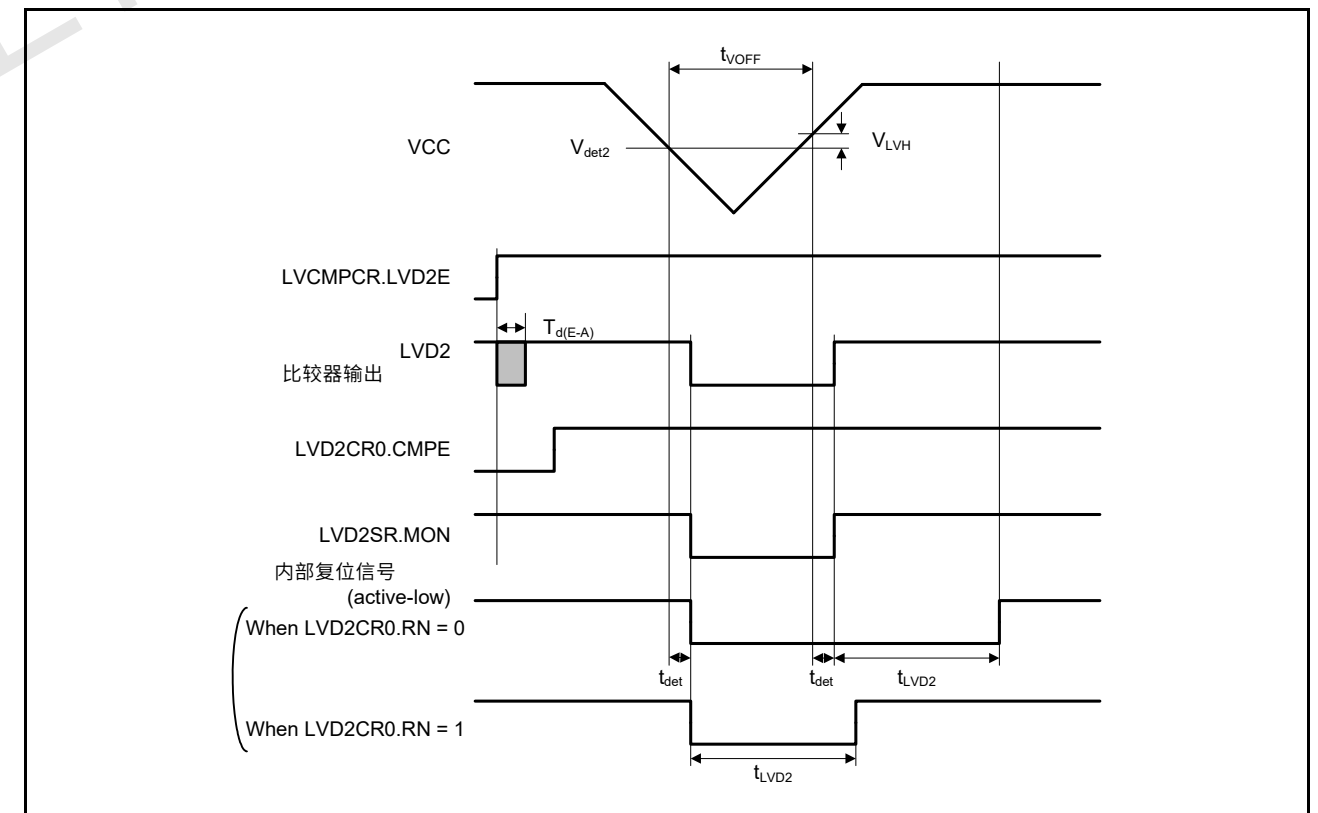


Figure 2.70 电压检测电路时序 (V<sub>det2</sub>)

## 2.12 CTSU Characteristics

**Table 2.60 CTSU characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C <sub>tscap</sub>	9	10	11	nF	-
TS pin capacitive load	C <sub>base</sub>	-	-	50	pF	-
Permissible output high current	ΣI <sub>OH</sub>	-	-	-24	mA	When the mutual capacitance method is applied and TS07 to TS14 are not used for transmit channel
		-	-	-14		When the mutual capacitance method is applied and TS07 to TS14 are used for transmit channel

## 2.13 Comparator Characteristics

**Table 2.61 ACMPHS characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V <sub>IOCOMP</sub>	-	± 5	± 40	mV	-
Input voltage range	V <sub>ICPM</sub>	0	-	AVCC0	V	-
Internal reference voltage input*3	V <sub>ref</sub>	1.36	1.43	1.50	V	AVCC0 ≥ 2.0 V
Input signal cycle	t <sub>PCMP</sub>	10	-	-	μs	-
Output delay time	T <sub>d</sub>	-	50	100	ns	Input amplitude ± 100 mV
Stabilization wait time during input channel switching*1	T <sub>WAIT</sub>	300	-	-	ns	Input amplitude ± 100 mV
Operation stabilization wait time*2	T <sub>cmp</sub>	1	-	-	μs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	μs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period from when the comparator input channel is switched until the switched result reflects in its output.

Note 2. Period from when comparator operation is enabled (CPMCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.

Note 3. The internal reference voltage cannot be selected for input channels when AVCC0 &lt; 2.0 V.

**Table 2.62 ACMPPLP characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Input voltage range	IVREF0	V <sub>REF</sub>	0	-	VCC - 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC - 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1		V <sub>I</sub>	0	-	VCC	
Internal reference voltage*2	-	1.36	1.43	1.50	V	VCC ≥ 2.0 V	
Output delay	Comparator high-speed mode (Standard mode)	T <sub>d</sub>	-	-	1.2	μs	VCC = 3.0 V Slew rate of input signal > 50 mV/μs
	Comparator high-speed mode (Window mode)		-	-	2.0	μs	
	Comparator low-speed mode (Standard mode)		-	-	5.0	μs	

## 2.12 CTSU Characteristics

**Table 2.60 CTSU characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C <sub>tscap</sub>	9	10	11	nF	-
TS引脚容性负载	C <sub>base</sub>	-	-	50	pF	-
允许输出大电流	ΣI <sub>OH</sub>	-	-	-24	mA	当应用互电容方法且TS07到TS14不用于传输通道时
		-	-	-14		当应用互电容方法并且TS07到TS14用于传输通道时

## 2.13 比较器特性

**Table 2.61 ACMPHS characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
输入失调电压	V <sub>IOCOMP</sub>	-	± 5	± 40	mV	-
输入电压范围	V <sub>ICPM</sub>	0	-	AVCC0	V	-
内部参考电压输入*3	V <sub>ref</sub>	1.36	1.43	1.50	V	AVCC0 ≥ 2.0 V
输入信号周期	t <sub>PCMP</sub>	10	-	-	μs	-
输出延迟时间	T <sub>d</sub>	-	50	100	ns	输入幅度±100mV
输入通道切换期间的稳定等待时间*1	T <sub>WAIT</sub>	300	-	-	ns	输入幅度±100mV
运行稳定等待时间*2	T <sub>cmp</sub>	1	-	-	μs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	μs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. 从比较器输入通道切换到切换结果反映在其输出中的时间段。

Note 2. 从比较器操作启用(CPMCTL.HCMPON=1)到比较器满足DC/AC特性的时间段。

Note 3. 当AVCC0&lt;2.0V时, 不能为输入通道选择内部参考电压。

**Table 2.62 ACMPPLP characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
输入电压范围	IVREF0	V <sub>REF</sub>	0	-	VCC - 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC - 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1		V <sub>I</sub>	0	-	VCC	
内部参考电压*2	-	1.36	1.43	1.50	V	VCC ≥ 2.0 V	
输出延迟	比较器高速模式 (标准模式)	T <sub>d</sub>	-	-	1.2	μs	VCC = 3.0 V 输入信号的压摆率>50mV/μs
	比较器高速模式 (窗口模式)		-	-	2.0	μs	
	比较器低速模式 (标准模式)		-	-	5.0	μs	



**Table 2.62 ACMPLP characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Offset voltage	Comparator high-speed mode (Standard mode)	-	-	50	mV	-
	Comparator high-speed mode (Window mode)	-	-	60	mV	
	Comparator low-speed mode (Standard mode)	-	-	40	mV	
Operation stabilization wait time	T <sub>cmp</sub>	100	-	-	μs	-

Note 1. In window mode, be sure to satisfy the following condition: V<sub>IVREF1</sub> - V<sub>IVREF0</sub> ≥ 0.2 V.

Note 2. The internal reference voltage cannot be selected for input channels when VCC &lt; 2.0 V.

## 2.14 OPAMP Characteristics

**Table 2.63 OPAMP characteristics (1 of 3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage range	AVCC0	Low power mode	1.7	-	5.5	V
		Middle-speed mode	2.1	-	5.5	V
		High-speed mode	2.4	-	5.5	V
Charge pump stabilization time*1	-	-	-	-	100	μs
SW stabilization time*1	-	-	-	-	50	μs
Input voltage range	V <sub>icm1</sub>	Low power mode	AVSS0	-	AVCC0	V
	V <sub>icm2</sub>	Middle-speed mode				
	V <sub>icm3</sub>	High-speed mode				
Output voltage range	V <sub>olh1</sub>	Low power mode, I <sub>load</sub> = 100 μA	AVSS0	-	AVCC0	V
	V <sub>olh2</sub>	Middle-speed mode, I <sub>load</sub> = 100 μA				
	V <sub>olh3</sub>	High-speed mode, I <sub>load</sub> = 100 μA				
Input offset trimming range*1	V <sub>offadj2l</sub>	Middle-speed mode, V <sub>in</sub> = 0.1 V, T <sub>j</sub> = 25°C	-3	-	3	mV
	V <sub>offadj2h</sub>	Middle-speed mode, V <sub>in</sub> = AVCC0 - 0.1 V, T <sub>j</sub> = 25°C				
	V <sub>offadj3l</sub>	High-speed mode, V <sub>in</sub> = 0.1 V, T <sub>j</sub> = 25°C				
	V <sub>offadj3h</sub>	High-speed mode, V <sub>in</sub> = AVCC0 - 0.1 V, T <sub>j</sub> = 25°C				

**Table 2.62 ACMPLP characteristics**

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
偏移电压	比较器高速模式 (标准模式)	-	-	50	mV	-
	比较器高速模式 (窗口模式)	-	-	60	mV	
	比较器低速模式 (标准模式)	-	-	40	mV	
运行稳定等待时间	T <sub>cmp</sub>	100	-	-	μs	-

Note 1. 在窗口模式下, 请务必满足以下条件: V<sub>IVREF1</sub> - V<sub>IVREF0</sub> ≥ 0.2V.

Note 2. 当VCC&lt;2.0V时, 不能为输入通道选择内部参考电压。

## 2.14 OPAMP Characteristics

**Table 2.63 运算放大器特性(1of3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
电源电压范围	AVCC0	低功耗模式	1.7	-	5.5	V
		Middle-speed mode	2.1	-	5.5	V
		High-speed mode	2.4	-	5.5	V
电荷泵稳定时间*1	-	-	-	-	100	μs
SW stabilization time*1	-	-	-	-	50	μs
输入电压范围	V <sub>icm1</sub>	低功耗模式	AVSS0	-	AVCC0	V
	V <sub>icm2</sub>	Middle-speed mode				
	V <sub>icm3</sub>	High-speed mode				
输出电压范围	V <sub>olh1</sub>	低功耗模式, I <sub>load</sub> = 100 μA	AVSS0	-	AVCC0	V
	V <sub>olh2</sub>	Middle-speed mode, I <sub>load</sub> = 100 μA				
	V <sub>olh3</sub>	High-speed mode, I <sub>load</sub> = 100 μA				
输入偏移微调范围*1	V <sub>offadj2l</sub>	Middle-speed mode, V <sub>in</sub> = 0.1 V, T <sub>j</sub> = 25°C	-3	-	3	mV
	V <sub>offadj2h</sub>	中速模式, V <sub>in</sub> =AVCC0-0.1V, T <sub>j</sub> = 25°C				
	V <sub>offadj3l</sub>	High-speed mode, V <sub>in</sub> = 0.1 V, T <sub>j</sub> = 25°C				
	V <sub>offadj3h</sub>	High-speed mode, V <sub>in</sub> = AVCC0 - 0.1 V, T <sub>j</sub> = 25°C				

**Table 2.63 OPAMP characteristics (2 of 3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input offset*1	V <sub>ioff1a</sub>	Low power mode, V <sub>in</sub> < AVCC0 - 1.0 V	-5.0	-	5.0	mV
	V <sub>ioff1b</sub>	Low power mode, V <sub>in</sub> ≥ AVCC0 - 1.0 V	-8.0	-	8.0	
	V <sub>ioff2a</sub>	Middle-speed mode, V <sub>in</sub> < AVCC0 - 1.2 V	-3.0	-	3.0	
	V <sub>ioff2b</sub>	Middle-speed mode, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-3.0	-	3.0	
	V <sub>ioff3a</sub>	High-speed mode, V <sub>in</sub> < AVCC0 - 1.2 V	-2.5	-	2.5	
	V <sub>ioff3b</sub>	High-speed mode, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-2.5	-	2.5	
Offset drift*1	Drift1a	Low power mode, V <sub>in</sub> < AVCC0 - 1.0 V	-70	-	70	μV/°C
	Drift1b	Low power mode, V <sub>in</sub> ≥ AVCC0 - 1.0 V	-70	-	70	
	Drift2a	Middle-speed mode, V <sub>in</sub> < AVCC0 - 1.2 V	-30	-	30	
	Drift2b	Middle-speed mode, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-30	-	30	
	Drift3a	High-speed mode, V <sub>in</sub> < AVCC0 - 1.2 V	-30	-	30	
	Drift3b	High-speed mode, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-30	-	30	
Open gain*1	Av1	Low power mode	70	130	-	dB
	Av2	Middle-speed mode	70	120	-	
	Av3	High-speed mode	60	130	-	
Gain bandwidth product*1	GBW1	Low power mode	-	90	-	kHz
	GBW2	Middle-speed mode	-	2	-	
	GBW3	High-speed mode	-	4.8	-	
Phase margin*1	PM1	Low power mode	35	-	-	deg
	PM2	Middle-speed mode	35	-	-	
	PM3	High-speed mode	35	-	-	
Gain margin*1	GM1	Low power mode	10	-	-	dB
	GM2	Middle-speed mode	10	-	-	
	GM3	High-speed mode	10	-	-	
Input noise density*1	V <sub>ind11</sub>	Low power mode, f = 10 Hz	-	860	-	nV/√Hz
	V <sub>ind12</sub>	Low power mode, f = 1 kHz	-	260	-	
	V <sub>ind21</sub>	Middle-speed mode, f = 1 kHz	-	50	-	
	V <sub>ind22</sub>	Middle-speed mode, f = 100 kHz	-	30	-	
	V <sub>ind31</sub>	High-speed mode, f = 1 kHz	-	40	-	
	V <sub>ind32</sub>	High-speed mode, f = 100 kHz	-	20	-	

**Table 2.63 运算放大器特性 (2个, 共3个)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input offset*1	V <sub>ioff1a</sub>	低功耗模式, V <sub>in</sub> < AVCC0 - 1.0 V	-5.0	-	5.0	mV
	V <sub>ioff1b</sub>	低功耗模式, V <sub>in</sub> ≥ AVCC0 - 1.0 V	-8.0	-	8.0	
	V <sub>ioff2a</sub>	中速模式, V <sub>in</sub> < AVCC0 - 1.2 V	-3.0	-	3.0	
	V <sub>ioff2b</sub>	中速模式, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-3.0	-	3.0	
	V <sub>ioff3a</sub>	高速模式, V <sub>in</sub> < AVCC0 - 1.2 V	-2.5	-	2.5	
	V <sub>ioff3b</sub>	高速模式, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-2.5	-	2.5	
Offset drift*1	Drift1a	低功耗模式, V <sub>in</sub> < AVCC0 - 1.0 V	-70	-	70	μV/°C
	Drift1b	低功耗模式, V <sub>in</sub> ≥ AVCC0 - 1.0 V	-70	-	70	
	Drift2a	中速模式, V <sub>in</sub> < AVCC0 - 1.2 V	-30	-	30	
	Drift2b	中速模式, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-30	-	30	
	Drift3a	高速模式, V <sub>in</sub> < AVCC0 - 1.2 V	-30	-	30	
	Drift3b	高速模式, V <sub>in</sub> ≥ AVCC0 - 1.2 V	-30	-	30	
Open gain*1	Av1	低功耗模式	70	130	-	dB
	Av2	Middle-speed mode	70	120	-	
	Av3	High-speed mode	60	130	-	
增益带宽积*1	GBW1	低功耗模式	-	90	-	kHz
	GBW2	Middle-speed mode	-	2	-	
	GBW3	High-speed mode	-	4.8	-	
Phase margin*1	PM1	低功耗模式	35	-	-	deg
	PM2	Middle-speed mode	35	-	-	
	PM3	High-speed mode	35	-	-	
Gain margin*1	GM1	低功耗模式	10	-	-	dB
	GM2	Middle-speed mode	10	-	-	
	GM3	High-speed mode	10	-	-	
输入噪声密度*1	V <sub>ind11</sub>	低功耗模式, f=10 Hz	-	860	-	nV/√Hz
	V <sub>ind12</sub>	低功耗模式, f=1 kHz	-	260	-	
	V <sub>ind21</sub>	中速模式, f=1 kHz	-	50	-	
	V <sub>ind22</sub>	中速模式, f=100 kHz	-	30	-	
	V <sub>ind31</sub>	高速模式, f=1 kHz	-	40	-	
	V <sub>ind32</sub>	高速模式, f=100 kHz	-	20	-	

**Table 2.63 OPAMP characteristics (3 of 3)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply rejection ratio*1	PSRR1	Low power mode	-	90	-	dB
	PSRR2	Middle-speed mode	-	90	-	
	PSRR3	High-speed mode	-	90	-	
Common mode rejection ratio*1	CMRR1	Low power mode	-	90	-	dB
	CMRR2	Middle-speed mode	-	90	-	
	CMRR3	High-speed mode	-	90	-	
Settling time*1	T <sub>set1</sub>	Low power mode	-	70	200	μS
	T <sub>set2</sub>	Middle-speed mode	-	2.8	8	
	T <sub>set3</sub>	High-speed mode	-	1.2	3.2	
Slew rate*1	SR1	Low power mode	0.02	0.05	-	V/μS
	SR2	Middle-speed mode	0.8	1.3	-	
	SR3	High-speed mode	1.8	3.0	-	
Turn on time*1	T <sub>turn1</sub>	Low power mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	80	220	μS
	T <sub>turn2</sub>	Middle-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	3	10	
	T <sub>turn3</sub>	High-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	1.3	4	
Input offset trimming step*1	V <sub>iofst2</sub>	Middle-speed mode, Vin < AVCC0 - 1.2 V	0.3	0.459	0.58	mV/code
		Middle-speed mode, Vin ≥ AVCC0 - 1.2 V	0.24	-	0.56	
	V <sub>iofst3</sub>	High-speed mode, Vin < AVCC0 - 1.2 V	0.35	0.52	0.65	
		High-speed mode, Vin ≥ AVCC0 - 1.2 V	0.28	-	0.61	
Wait time after trimming*1	T <sub>turn_tm2</sub>	Middle-speed mode	-	-	1.5	μS
	T <sub>turn_tm3</sub>	High-speed mode	-	-	1	
Load current	I <sub>load</sub>	-	-	-	100	μA
Load capacitance	C <sub>L</sub>	-	-	-	20	pF

Note 1. These values are based on simulation. They are not production tested.

## 2.15 Flash Memory Characteristics

### 2.15.1 Code Flash Memory Characteristics

**Table 2.64 Code flash characteristics (1)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1	N <sub>PEC</sub>	1000	-	-	Times	-
Data hold time	After 1000 times N <sub>PEC</sub>	t <sub>DRP</sub>	20*2, *3	-	Year	T <sub>a</sub> = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

**Table 2.63 运算放大器特性 (3个中的3个)**

Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
电源抑制比*1	PSRR1	低功耗模式	-	90	-	dB
	PSRR2	Middle-speed mode	-	90	-	
	PSRR3	High-speed mode	-	90	-	
共模抑制比*1	CMRR1	低功耗模式	-	90	-	dB
	CMRR2	Middle-speed mode	-	90	-	
	CMRR3	High-speed mode	-	90	-	
Settling time*1	T <sub>set1</sub>	低功耗模式	-	70	200	μS
	T <sub>set2</sub>	Middle-speed mode	-	2.8	8	
	T <sub>set3</sub>	High-speed mode	-	1.2	3.2	
Slew rate*1	SR1	低功耗模式	0.02	0.05	-	V/μS
	SR2	Middle-speed mode	0.8	1.3	-	
	SR3	High-speed mode	1.8	3.0	-	
开机时间*1	T <sub>turn1</sub>	低功耗模式, AMP ENx=0→1, IREFEN = 0 → 1	-	80	220	μS
	T <sub>turn2</sub>	Middle-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	3	10	
	T <sub>turn3</sub>	High-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	1.3	4	
输入偏移微调步骤*1	V <sub>iofst2</sub>	中速模式, Vin < AVCC0 - 1.2V	0.3	0.459	0.58	mV/code
		中速模式, Vin ≥ AVCC0 - 1.2V	0.24	-	0.56	
	V <sub>iofst3</sub>	High-speed mode, Vin < AVCC0 - 1.2 V	0.35	0.52	0.65	
		High-speed mode, Vin ≥ AVCC0 - 1.2 V	0.28	-	0.61	
修剪后的等待时间*1	T <sub>turn_tm2</sub>	Middle-speed mode	-	-	1.5	μS
	T <sub>turn_tm3</sub>	High-speed mode	-	-	1	
负载电流	I <sub>load</sub>	-	-	-	100	μA
负载电容	C <sub>L</sub>	-	-	-	20	pF

Note 1. 这些值基于模拟。它们未经生产测试。

## 2.15 闪存特性

### 2.15.1 代码闪存特性

**Table 2.64 码闪特性 (一)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1	N <sub>PEC</sub>	1000	-	-	Times	-
数据保持时间	1000次NPEC后	t <sub>DRP</sub>	20*2, *3	-	Year	T <sub>a</sub> = +85°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次 (n=1 000) 时, 可以对每个块执行n次擦除。例如, 当对1-KB块中的不同地址执行256次4字节编程, 然后擦除整个块时, 重新编程擦除周期计为1。但是, 不能将同一地址多次编程为一次擦除 (禁止覆盖)。

Note 2. 使用瑞萨电子提供的闪存编程器和自编程库时的特性。

Note 3. 这个结果是从可靠性测试中获得的。

**Table 2.65 Code flash characteristics (2)**

High-speed operating mode  
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte t <sub>P8</sub>	-	116	998	-	54	506	μs
Erase time	2-KB t <sub>E2K</sub>	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte t <sub>BC8</sub>	-	-	56.8	-	-	16.6	μs
	2-KB t <sub>BC2K</sub>	-	-	1899	-	-	140	μs
Erase suspended time	t <sub>SED</sub>	-	-	22.5	-	-	10.7	μs
Startup area switching setting time	t <sub>SAS</sub>	-	21.9	585	-	12.1	447	ms
Access window time	t <sub>AWS</sub>	-	21.9	585	-	12.1	447	ms
OCD/serial programmer ID setting time	t <sub>OSIS</sub>	-	21.9	585	-	12.1	447	ms
Flash memory mode transition wait time 1	t <sub>DIS</sub>	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2	t <sub>MS</sub>	5	-	-	5	-	-	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.  
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.  
Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

**Table 2.66 Code flash characteristics (3)**

Middle-speed operating mode  
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter	Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte t <sub>P8</sub>	-	157	1411	-	101	966	μs
Erase time	2-KB t <sub>E2K</sub>	-	9.10	289	-	6.10	228	ms
Blank check time	8-byte t <sub>BC8</sub>	-	-	87.7	-	-	52.5	μs
	2-KB t <sub>BC2K</sub>	-	-	1930	-	-	414	μs
Erase suspended time	t <sub>SED</sub>	-	-	32.7	-	-	21.6	μs
Startup area switching setting time	t <sub>SAS</sub>	-	22.8	592	-	14.2	465	ms
Access window time	t <sub>AWS</sub>	-	22.8	592	-	14.2	465	ms
OCD/serial programmer ID setting time	t <sub>OSIS</sub>	-	22.8	592	-	14.2	465	ms
Flash memory mode transition wait time 1	t <sub>DIS</sub>	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2	t <sub>MS</sub>	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.  
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.  
Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

## 2.15.2 Data Flash Memory Characteristics

**Table 2.67 Data flash characteristics (1)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1	N <sub>DPEC</sub>	100000	1000000	-	Times	-
Data hold time	After 10000 times of N <sub>DPEC</sub> t <sub>DDRP</sub>	20*2, *3	-	-	Year	Ta = +85°C
		5*2, *3	-	-	Year	
		-	1*2, *3	-	Year	Ta = +25°C

**Table 2.65 码闪特性 (二)**

高速运行模式  
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
编程时间	8-byte t <sub>P8</sub>	-	116	998	-	54	506	μs
擦除时间	2-KB t <sub>E2K</sub>	-	9.03	287	-	5.67	222	ms
空白检查时间	8-byte t <sub>BC8</sub>	-	-	56.8	-	-	16.6	μs
	2-KB t <sub>BC2K</sub>	-	-	1899	-	-	140	μs
擦除暂停时间	t <sub>SED</sub>	-	-	22.5	-	-	10.7	μs
启动区切换设置时间	t <sub>SAS</sub>	-	21.9	585	-	12.1	447	ms
访问窗口时间	t <sub>AWS</sub>	-	21.9	585	-	12.1	447	ms
OCD串口编程器ID设置时间	t <sub>OSIS</sub>	-	21.9	585	-	12.1	447	ms
闪存模式转换等待时间1	t <sub>DIS</sub>	2	-	-	2	-	-	μs
闪存模式转换等待时间2	t <sub>MS</sub>	5	-	-	5	-	-	μs

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。  
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。  
Note: 在对闪存进行编程或擦除时，FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

**Table 2.66 码闪特性 (三)**

中速运行模式  
条件: VCC=AVCC0=AVCC1=1.8至5.5V, Ta=-40至+85°C

Parameter	Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
编程时间	8-byte t <sub>P8</sub>	-	157	1411	-	101	966	μs
擦除时间	2-KB t <sub>E2K</sub>	-	9.10	289	-	6.10	228	ms
空白检查时间	8-byte t <sub>BC8</sub>	-	-	87.7	-	-	52.5	μs
	2-KB t <sub>BC2K</sub>	-	-	1930	-	-	414	μs
擦除暂停时间	t <sub>SED</sub>	-	-	32.7	-	-	21.6	μs
启动区切换设置时间	t <sub>SAS</sub>	-	22.8	592	-	14.2	465	ms
访问窗口时间	t <sub>AWS</sub>	-	22.8	592	-	14.2	465	ms
OCD串口编程器ID设置时间	t <sub>OSIS</sub>	-	22.8	592	-	14.2	465	ms
闪存模式转换等待时间1	t <sub>DIS</sub>	2	-	-	2	-	-	μs
闪存模式转换等待时间2	t <sub>MS</sub>	720	-	-	720	-	-	ns

Note: 不包括软件执行指令后到闪存的每次操作开始的时间。  
Note: 在对闪存进行编程或擦除时，FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时，频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率，例如1.5MHz。  
Note: 在对闪存进行编程或擦除时，FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

## 2.15.2 数据闪存特性

**Table 2.67 数据闪存特性 (一)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1	N <sub>DPEC</sub>	100000	1000000	-	Times	-
数据保持时间	NDPEC10000次后 t <sub>DDRP</sub>	20*2, *3	-	-	Year	Ta = +85°C
		5*2, *3	-	-	Year	
		-	1*2, *3	-	Year	Ta = +25°C



- Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
- Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
- Note 3. These results are obtained from reliability testing.

**Table 2.68 Data flash characteristics (2)**

High-speed operating mode  
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
Programming time	1-byte	t <sub>DP1</sub>	-	52.4	463	-	42.1	387	μs
Erasure time	1-KB	t <sub>DE1K</sub>	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t <sub>DBC1</sub>	-	-	24.3	-	-	16.6	μs
	1-KB	t <sub>DBC1K</sub>	-	-	1872	-	-	512	μs
Suspended time during erasing		t <sub>DSED</sub>	-	-	13.0	-	-	10.7	μs
Data flash STOP recovery time		t <sub>DSTOP</sub>	5	-	-	5	-	-	μs

- Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
- Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

**Table 2.69 Data flash characteristics (3)**

Middle-speed operating mode  
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter	Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
Programming time	1-byte	t <sub>DP1</sub>	-	94.7	886	-	89.3	849	μs
Erasure time	1-KB	t <sub>DE1K</sub>	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t <sub>DBC1</sub>	-	-	56.2	-	-	52.5	μs
	1-KB	t <sub>DBC1K</sub>	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t <sub>DSED</sub>	-	-	23.0	-	-	21.7	μs
Data flash STOP recovery time		t <sub>DSTOP</sub>	720	-	-	720	-	-	ns

- Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
- Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

### 2.15.3 Serial Wire Debug (SWD)

**Table 2.70 SWD characteristics (1) (1 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t <sub>SWCKcyc</sub>	80	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t <sub>SWCKH</sub>	35	-	-	ns	
SWCLK clock low pulse width	t <sub>SWCKL</sub>	35	-	-	ns	
SWCLK clock rise time	t <sub>SWCKr</sub>	-	-	5	ns	
SWCLK clock fall time	t <sub>SWCKf</sub>	-	-	5	ns	

- Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次 (n=100 000) 时, 可以对每个块执行n次擦除。例如, 当对1字节块中的不同地址执行1 000次1字节编程, 然后擦除整个块时, 重新编程擦除周期计为1。但是, 不能将同一地址多次编程为一次擦除。(禁止改写。)
- Note 2. 使用瑞萨电子提供的闪存编程器和自编程库时的特性。
- Note 3. 这些结果来自可靠性测试。

**Table 2.68 数据闪存特性 (2)**

高速运行模式  
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter	Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
编程时间	1-byte	t <sub>DP1</sub>	-	52.4	463	-	42.1	387	μs
擦除时间	1-KB	t <sub>DE1K</sub>	-	8.98	286	-	6.42	237	ms
空白检查时间	1-byte	t <sub>DBC1</sub>	-	-	24.3	-	-	16.6	μs
	1-KB	t <sub>DBC1K</sub>	-	-	1872	-	-	512	μs
擦除期间的暂停时间		t <sub>DSED</sub>	-	-	13.0	-	-	10.7	μs
数据闪存恢复时间		t <sub>DSTOP</sub>	5	-	-	5	-	-	μs

- Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
- Note: 在对闪存进行编程或擦除时, FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时, 频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率, 例如1.5MHz。
- Note: 在对闪存进行编程或擦除时, FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

**Table 2.69 数据闪存特性 (3)**

中速运行模式  
条件: VCC=AVCC0=AVCC1=1.8至5.5V, Ta=-40至+85°C

Parameter	Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
编程时间	1-byte	t <sub>DP1</sub>	-	94.7	886	-	89.3	849	μs
擦除时间	1-KB	t <sub>DE1K</sub>	-	9.59	299	-	8.29	273	ms
空白检查时间	1-byte	t <sub>DBC1</sub>	-	-	56.2	-	-	52.5	μs
	1-KB	t <sub>DBC1K</sub>	-	-	2.17	-	-	1.51	ms
擦除期间的暂停时间		t <sub>DSED</sub>	-	-	23.0	-	-	21.7	μs
数据闪存恢复时间		t <sub>DSTOP</sub>	720	-	-	720	-	-	ns

- Note: 不包括软件执行指令后到闪存的每次操作开始的时间。
- Note: 在对闪存进行编程或擦除时, FCLK的下限频率为1MHz。当使用低于4MHz的FCLK时, 频率可以设置为1MHz、2MHz或3MHz。不能设置非整数频率, 例如1.5MHz。
- Note: 在对闪存进行编程或擦除时, FCLK的频率精度必须为±3.5%。确认时钟源的频率精度。

### 2.15.3 串行线调试(SWD)

**Table 2.70 SWD特性(1)(1of2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	t <sub>SWCKcyc</sub>	80	-	-	ns	Figure 2.71
SWCLK时钟高脉冲宽度	t <sub>SWCKH</sub>	35	-	-	ns	
SWCLK时钟低脉冲宽度	t <sub>SWCKL</sub>	35	-	-	ns	
SWCLK时钟上升时间	t <sub>SWCKr</sub>	-	-	5	ns	
SWCLK时钟下降时间	t <sub>SWCKf</sub>	-	-	5	ns	

**Table 2.70 SWD characteristics (1) (2 of 2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWDIO setup time	$t_{SWDS}$	16	-	-	ns	Figure 2.72
SWDIO hold time	$t_{SWDH}$	16	-	-	ns	
SWDIO data delay time	$t_{SWDD}$	2	-	70	ns	

**Table 2.71 SWD characteristics (2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	-	-	ns	Figure 2.71
SWCLK clock high pulse width	$t_{SWCKH}$	120	-	-	ns	
SWCLK clock low pulse width	$t_{SWCKL}$	120	-	-	ns	
SWCLK clock rise time	$t_{SWCKr}$	-	-	5	ns	Figure 2.72
SWCLK clock fall time	$t_{SWCKf}$	-	-	5	ns	
SWDIO setup time	$t_{SWDS}$	50	-	-	ns	
SWDIO hold time	$t_{SWDH}$	50	-	-	ns	
SWDIO data delay time	$t_{SWDD}$	2	-	150	ns	

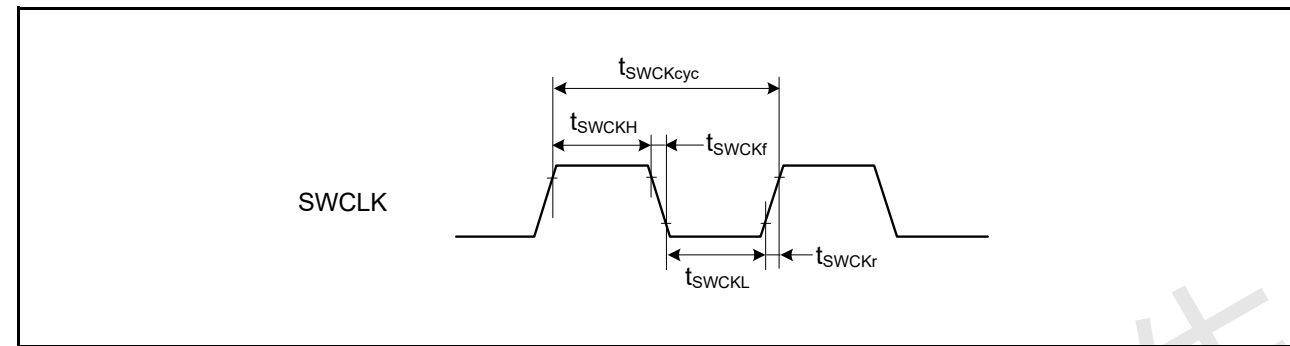


Figure 2.71 SWD SWCLK timing

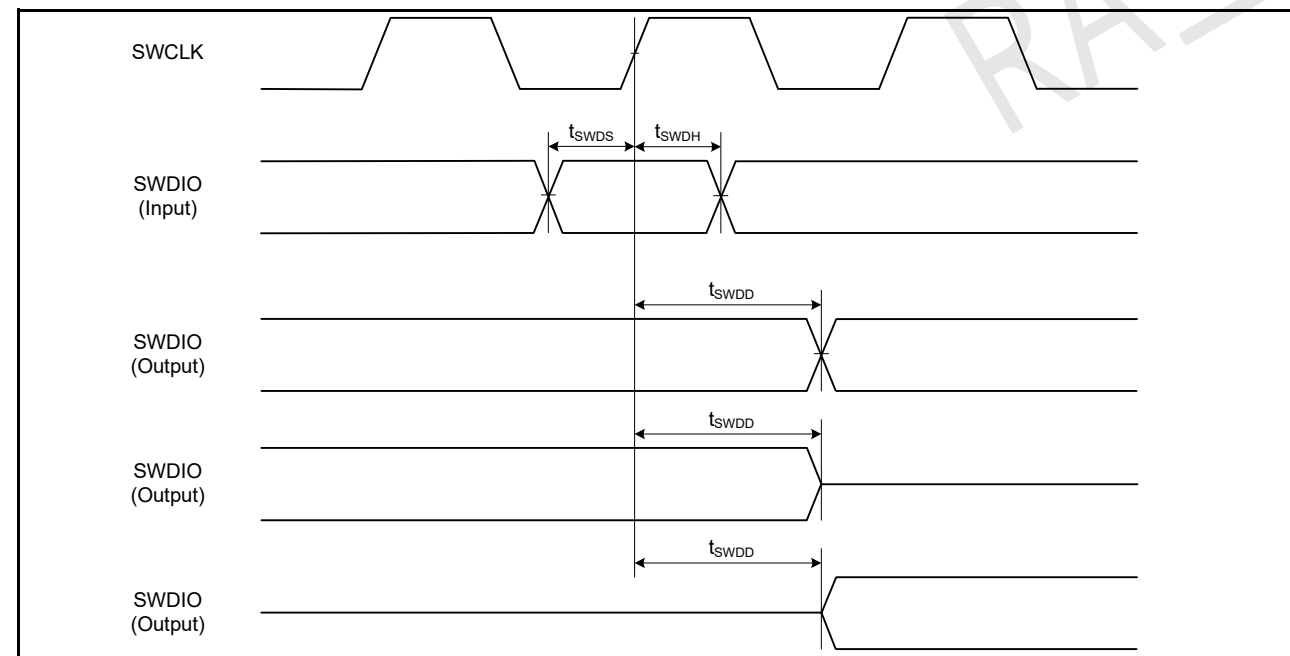


Figure 2.72 SWD input/output timing

**Table 2.70 SWD特征(1)(2of2)**

Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWDIO设置时间	$t_{SWDS}$	16	-	-	ns	Figure 2.72
SWDIO保持时间	$t_{SWDH}$	16	-	-	ns	
SWDIO数据延迟时间	$t_{SWDD}$	2	-	70	ns	

**Table 2.71 SWD characteristics (2)**

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	250	-	-	ns	Figure 2.71
SWCLK时钟高脉冲宽度	$t_{SWCKH}$	120	-	-	ns	
SWCLK时钟低脉冲宽度	$t_{SWCKL}$	120	-	-	ns	
SWCLK时钟上升时间	$t_{SWCKr}$	-	-	5	ns	Figure 2.72
SWCLK时钟下降时间	$t_{SWCKf}$	-	-	5	ns	
SWDIO设置时间	$t_{SWDS}$	50	-	-	ns	
SWDIO保持时间	$t_{SWDH}$	50	-	-	ns	
SWDIO数据延迟时间	$t_{SWDD}$	2	-	150	ns	

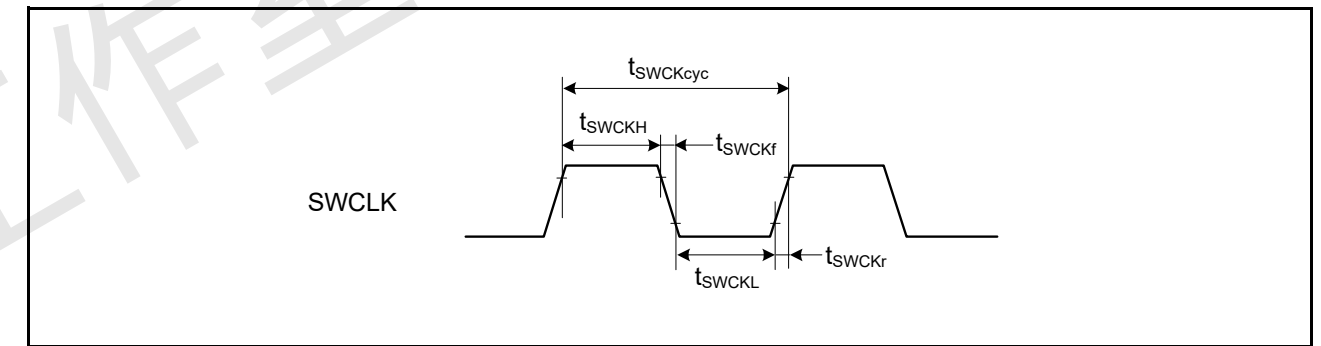


Figure 2.71 SWD SWCLK timing

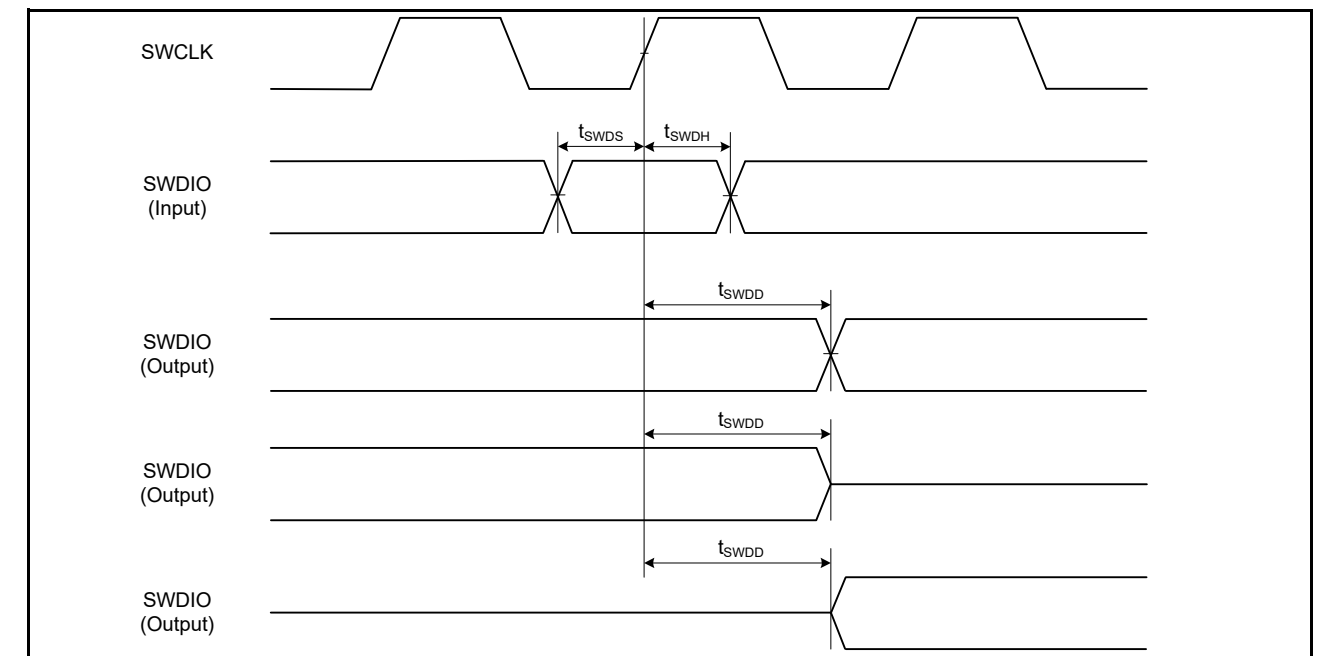


Figure 2.72 SWD input/output timing



### Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

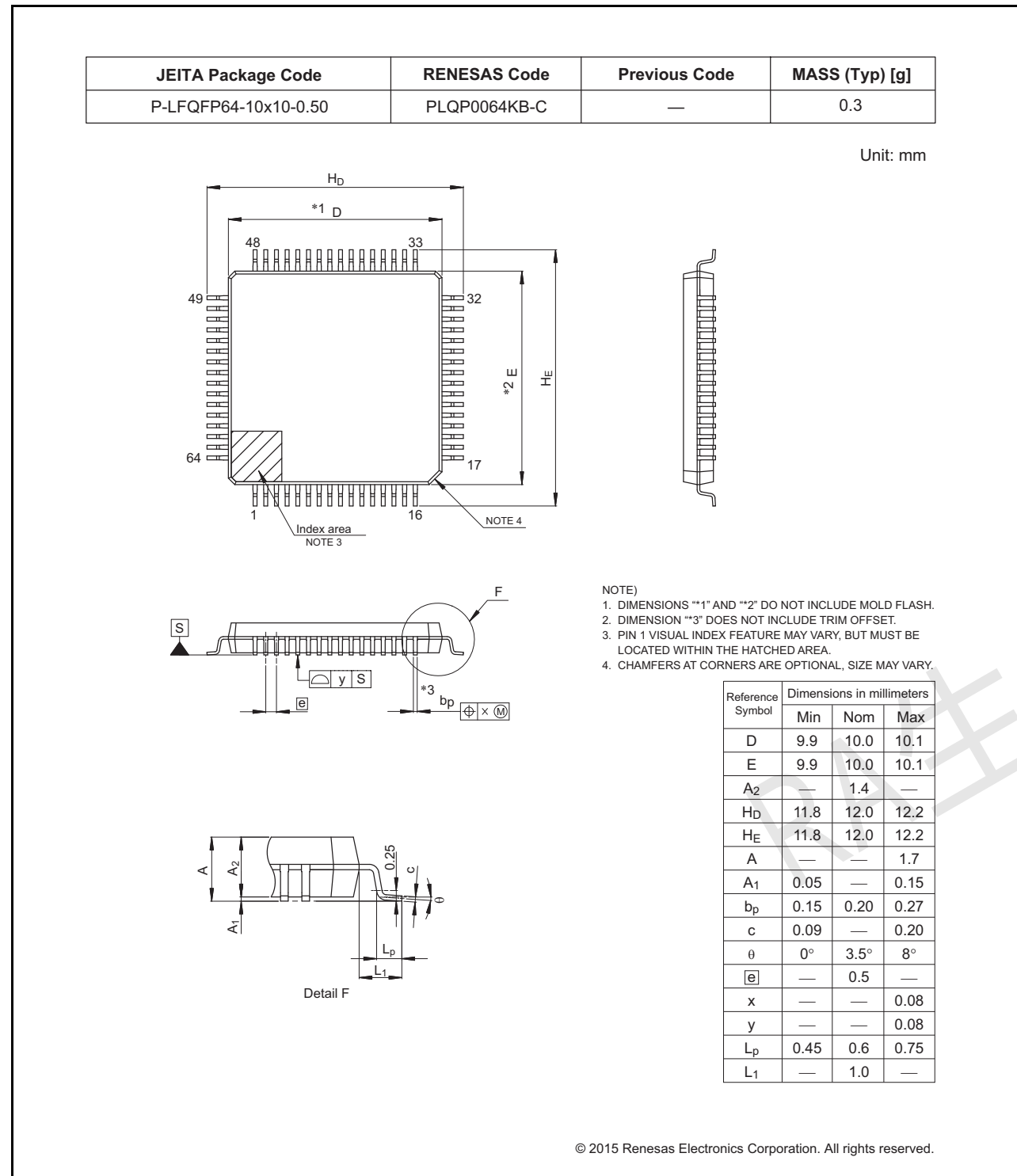


Figure 1.1 LQFP 64-pin

### 附录1.包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨电子的“封装”中电子公司网站。

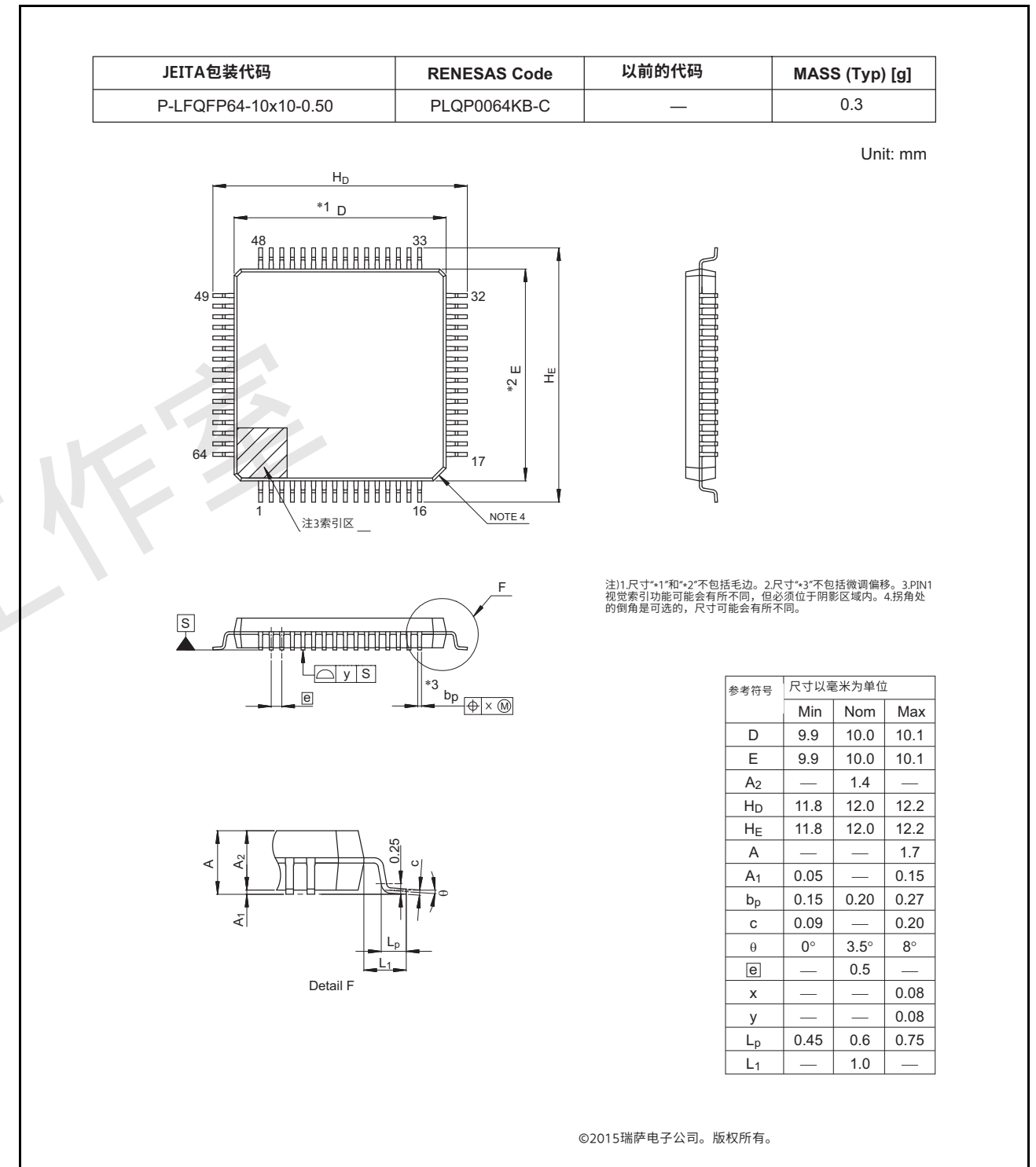


Figure 1.1 LQFP 64-pin

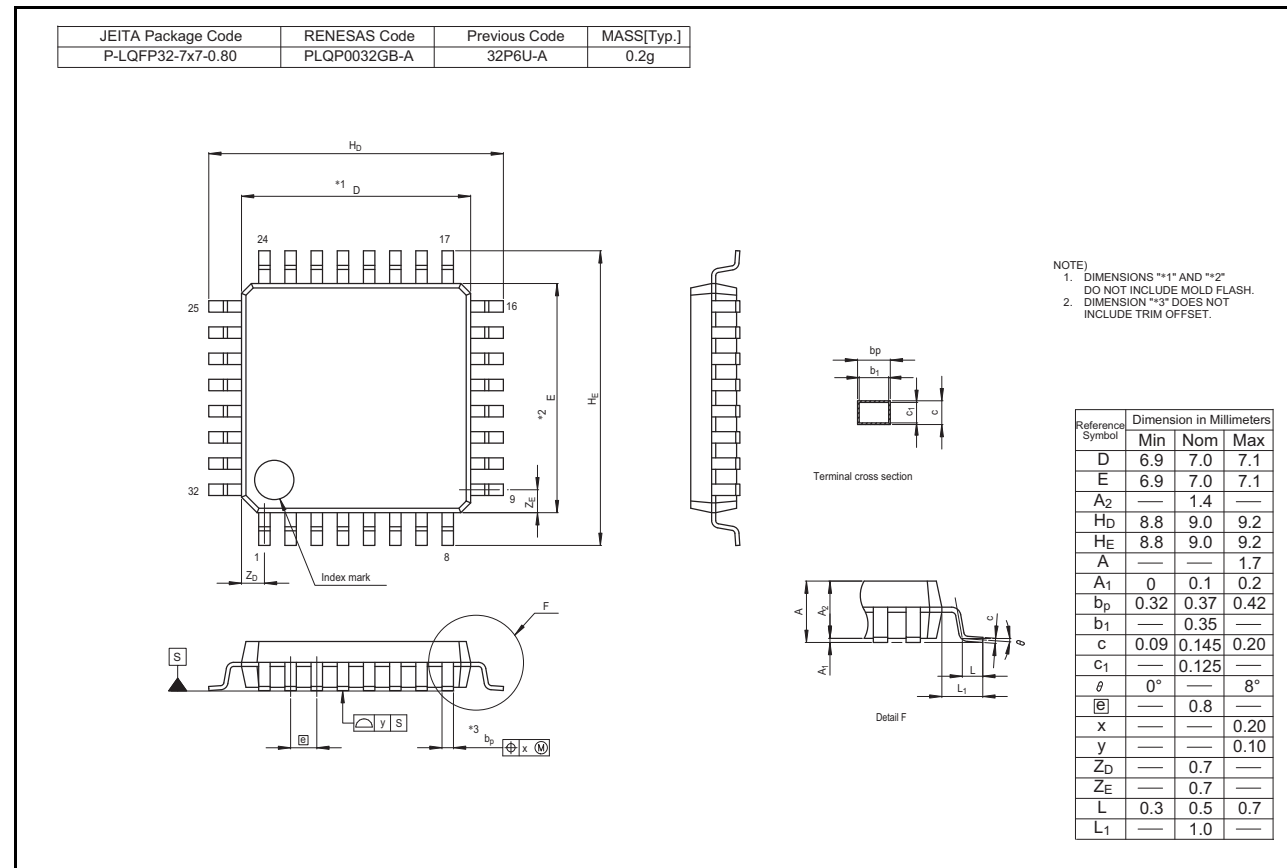


Figure 1.2 LQFP 32-pin

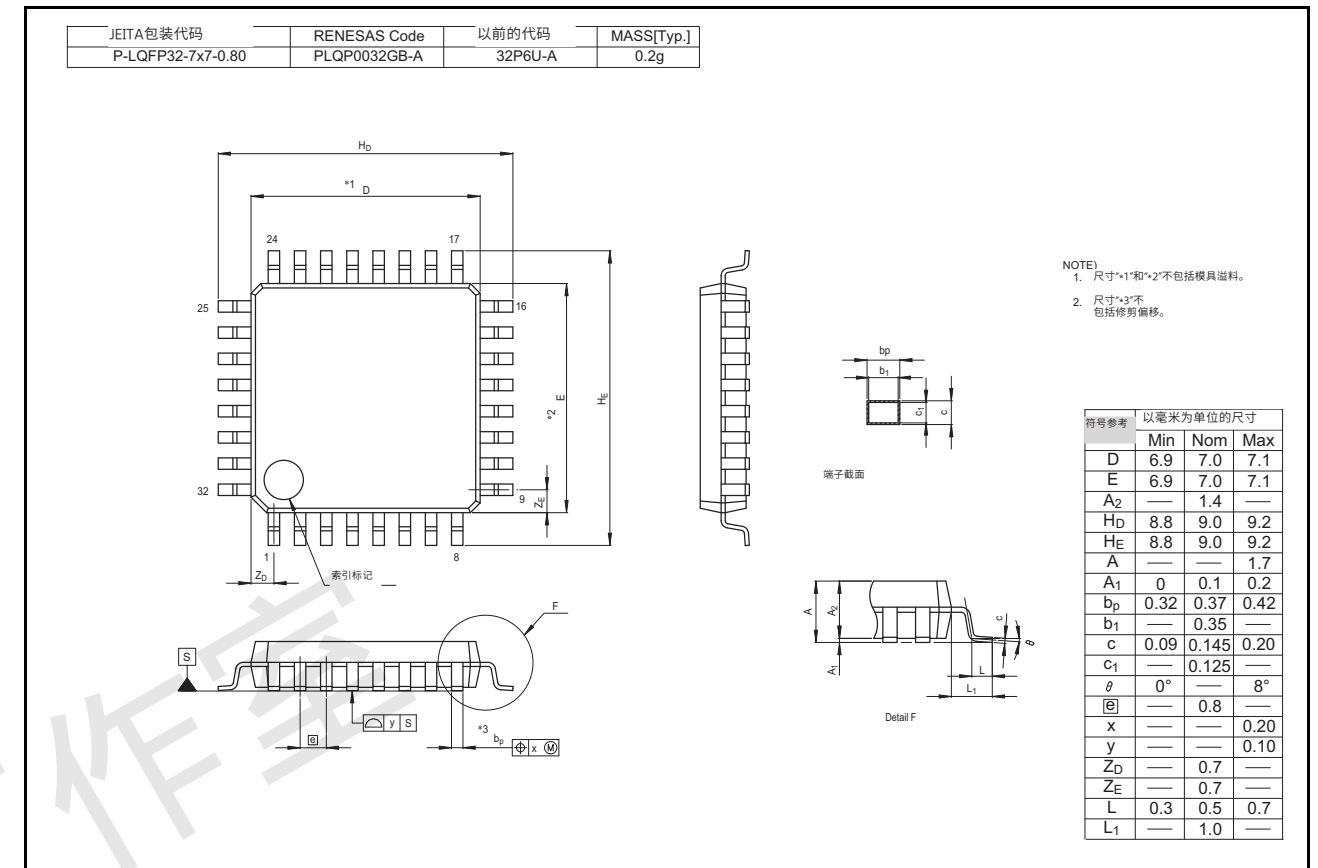


Figure 1.2 LQFP 32-pin

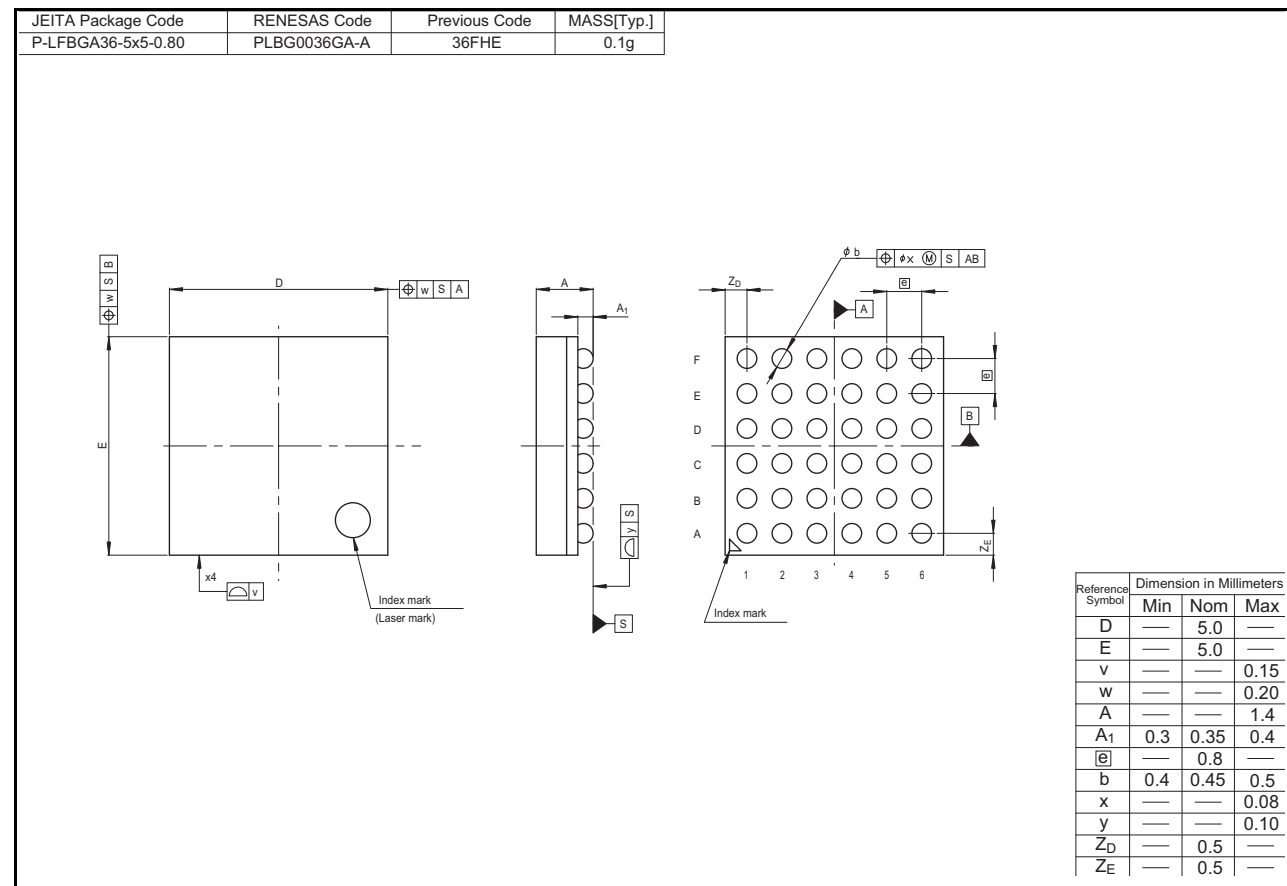


Figure 1.3 BGA 36-pin

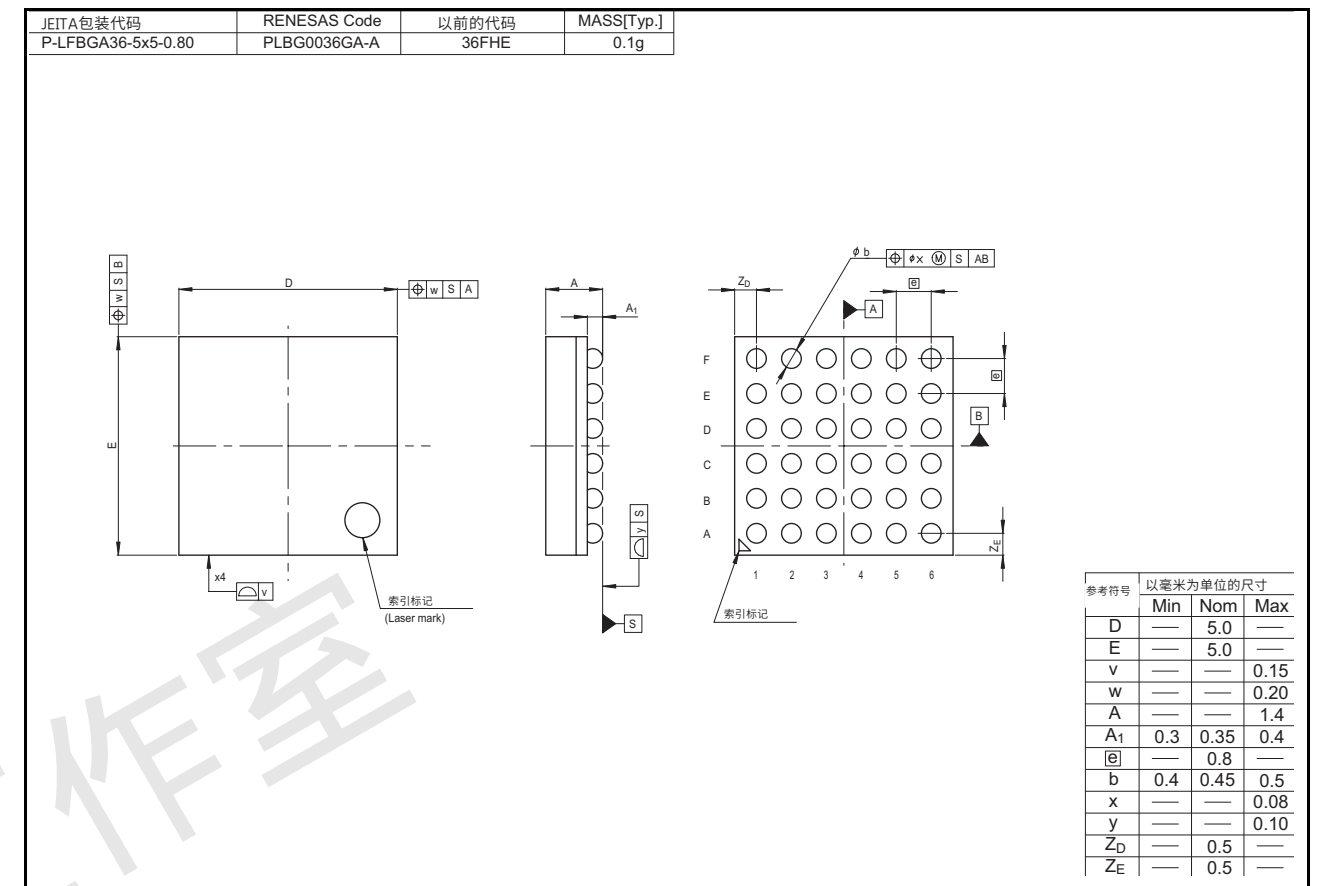


Figure 1.3 BGA 36-pin

RA生态工作室

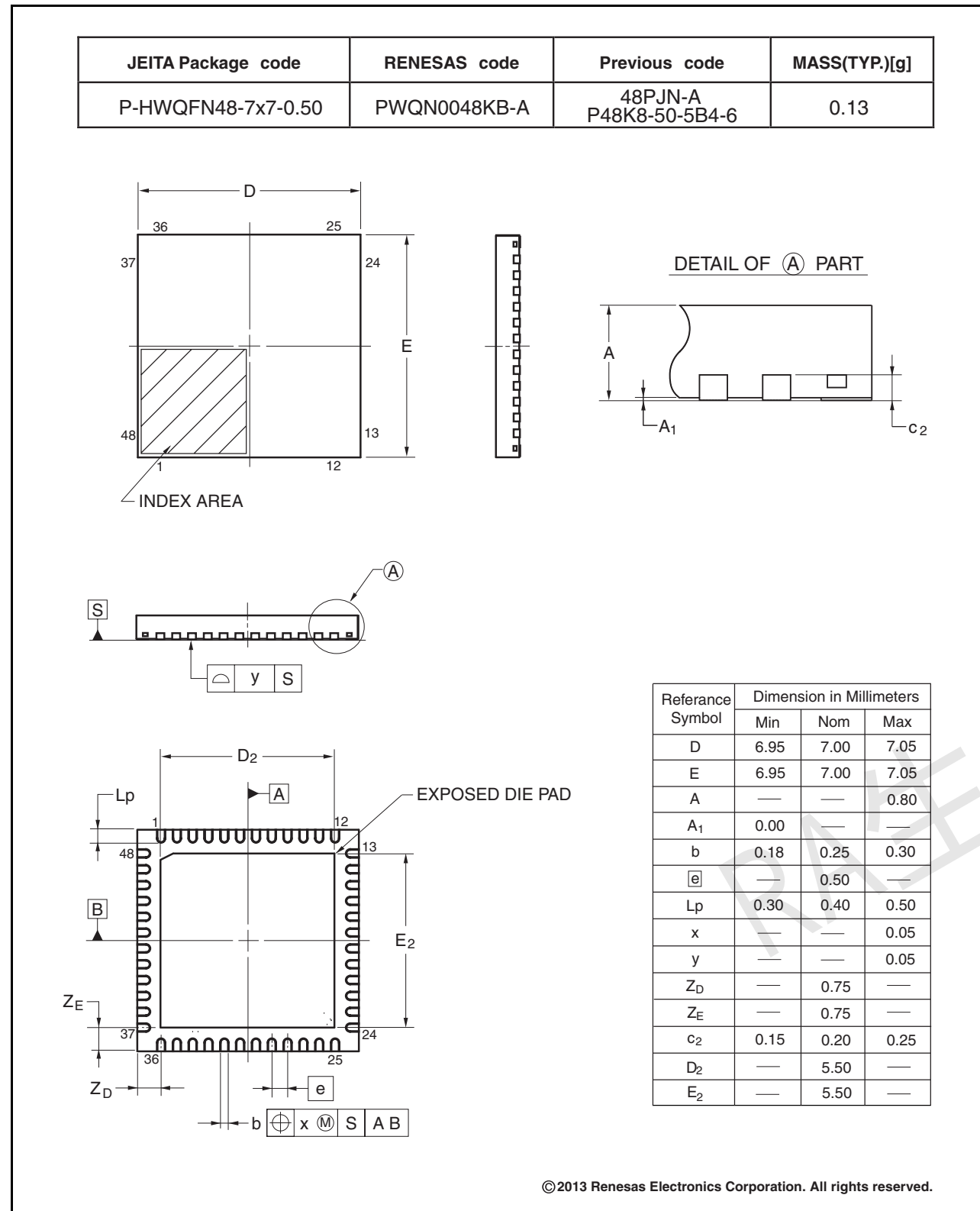


Figure 1.4 QFN 48-pin

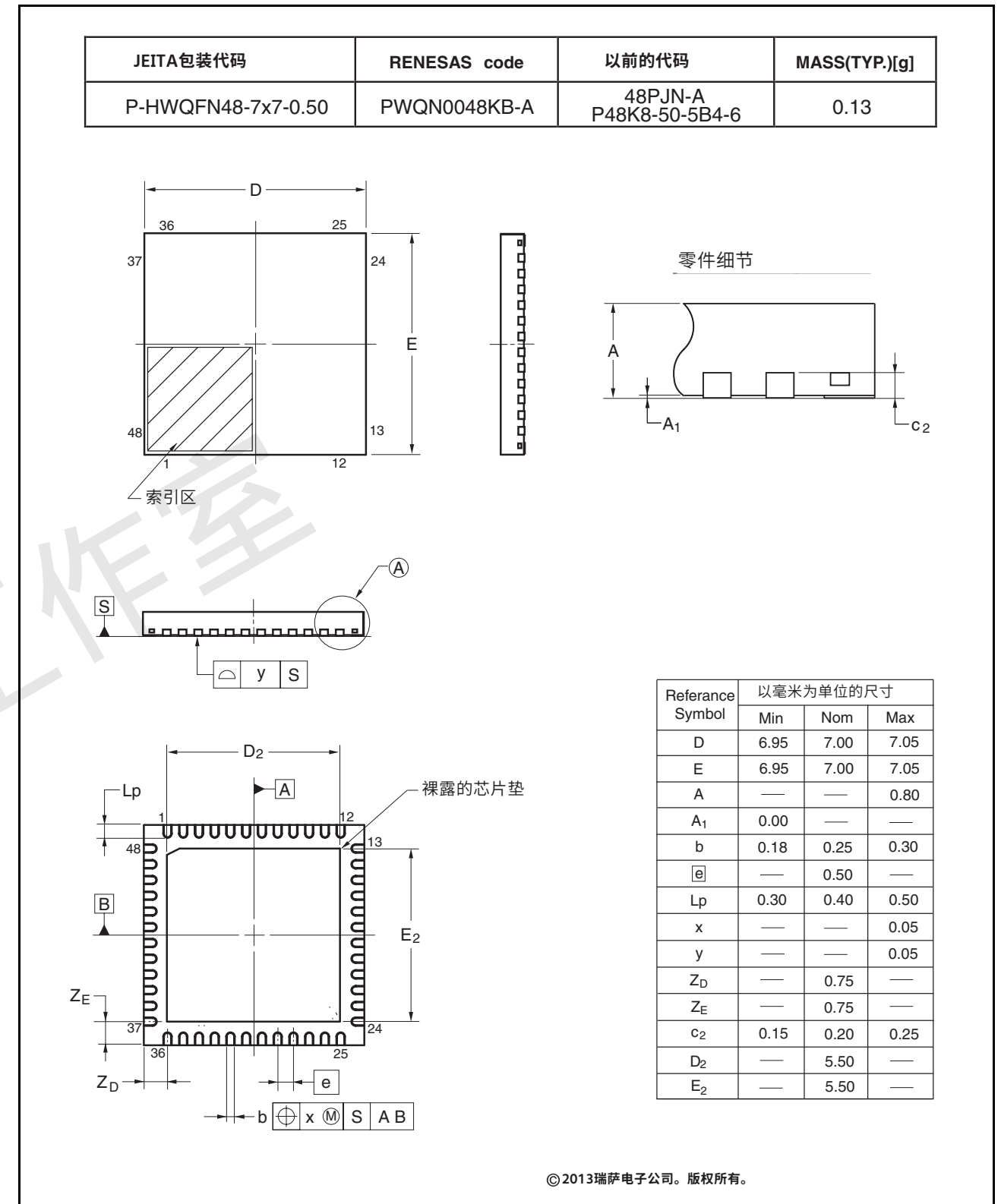


Figure 1.4 QFN 48-pin

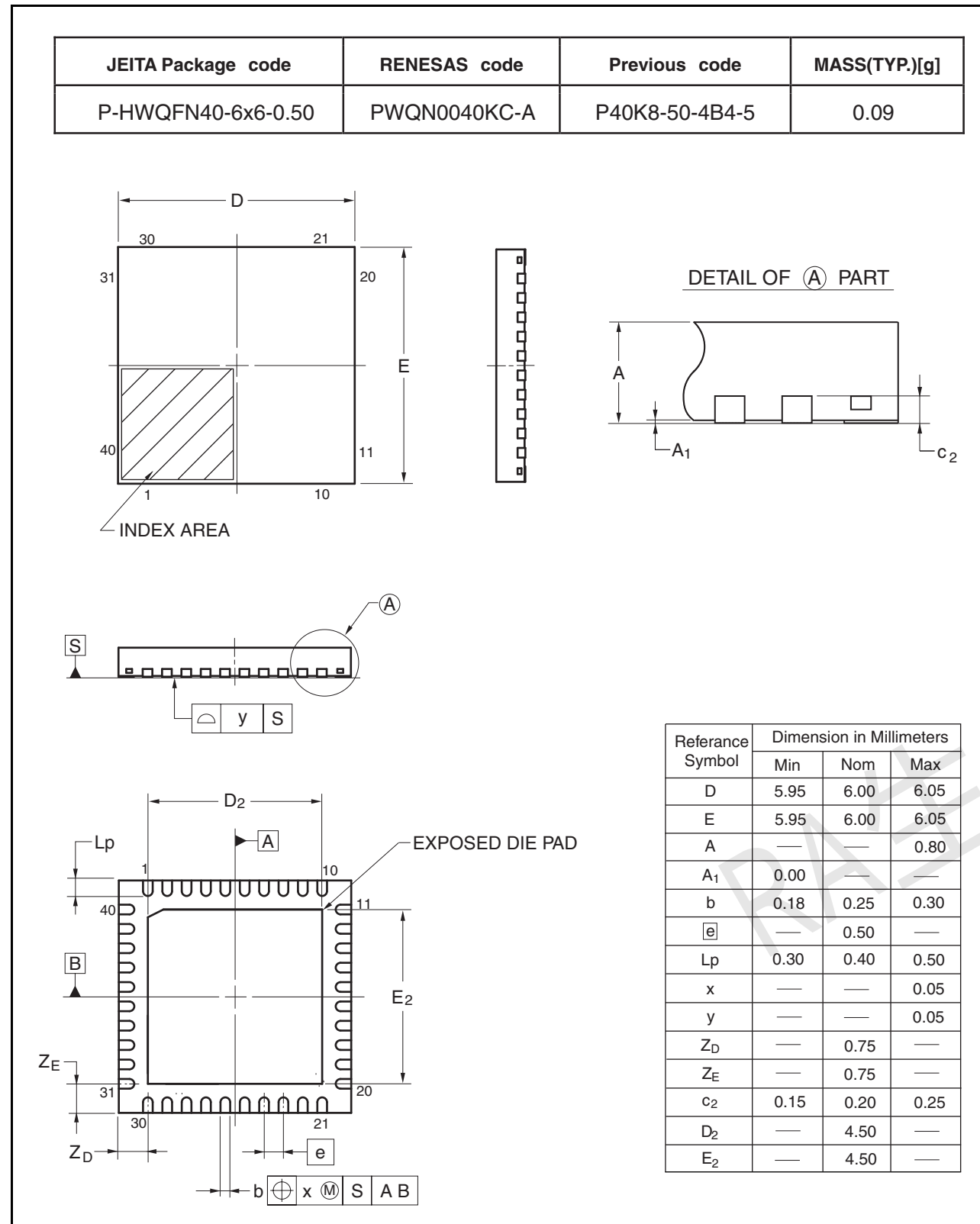


Figure 1.5 QFN 40-pin

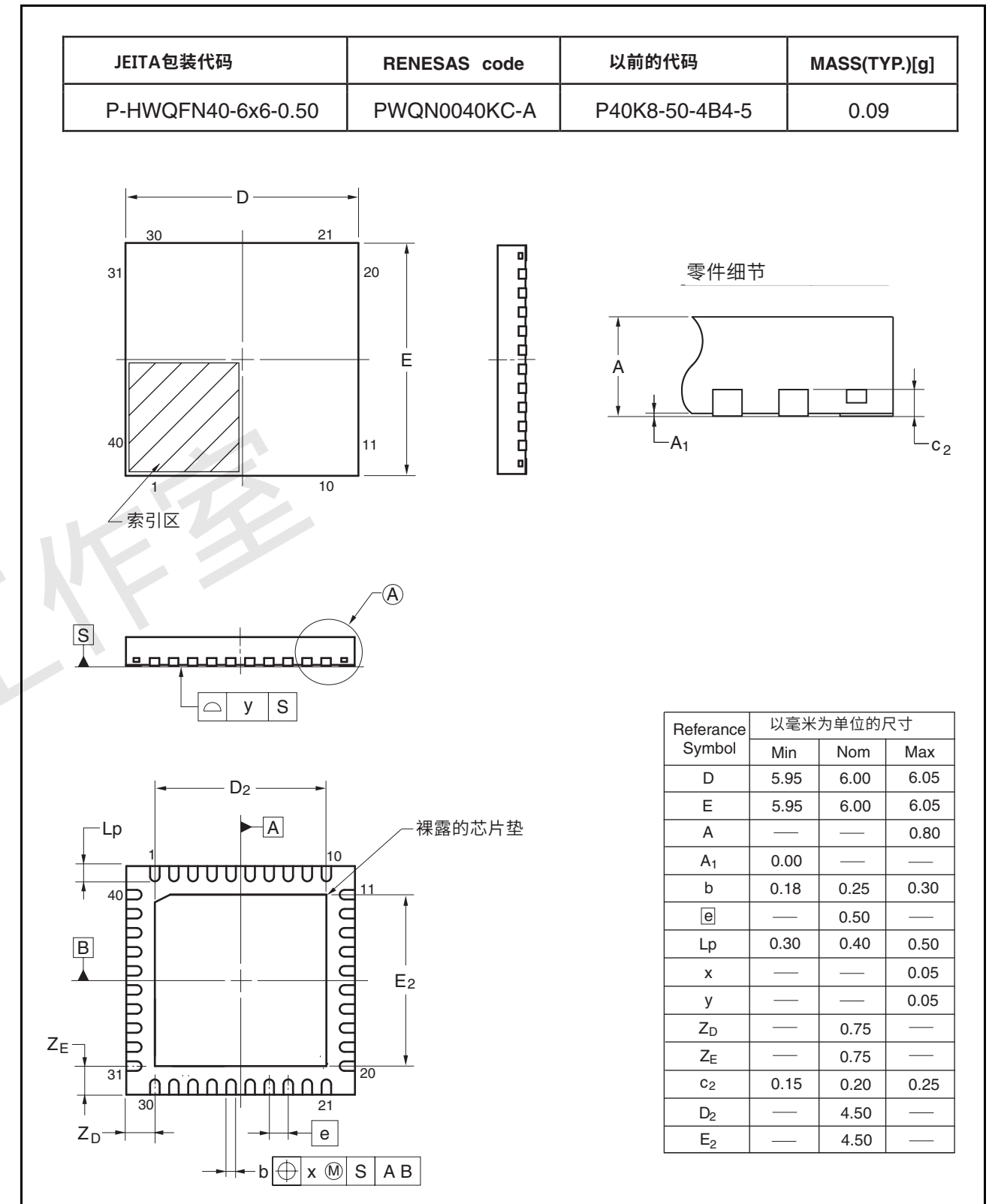


Figure 1.5 QFN 40-pin

Revision History	RA2A1 Group Datasheet
------------------	-----------------------

Rev.	Date	Summary
1.00	Oct 8, 2019	First release
1.10	Mar 16, 2020	Updated for 1.10

### Proprietary Notice

All text, graphics, photographs, trademarks, logos, artwork and computer code, collectively known as content, contained in this document is owned, controlled or licensed by or to Renesas, and is protected by trade dress, copyright, patent and trademark laws, and other intellectual property rights and unfair competition laws. Except as expressly provided herein, no part of this document or content may be copied, reproduced, republished, posted, publicly displayed, encoded, translated, transmitted or distributed in any other medium for publication or distribution or for any commercial enterprise, without prior written consent from Renesas.

Arm® and Cortex® are registered trademarks of Arm Limited. CoreSight™ is a trademark of Arm Limited.

CoreMark® is a registered trademark of the Embedded Microprocessor Benchmark Consortium.

Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

SuperFlash® is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Other brands and names mentioned in this document may be the trademarks or registered trademarks of their respective holders.

修订记录	RA2A1 Group Datasheet
------	-----------------------

Rev.	Date	Summary
1.00	Oct 8, 2019	首次发布
1.10	Mar 16, 2020	更新为1.10

### 专有通知

本文件中包含的所有文本、图形、照片、商标、徽标、艺术品和计算机代码（统称为内容）均归瑞萨电子所有、控制或许可，并受商业外观、版权、专利和商标法的保护，以及其他知识产权和不正当竞争法。除非在此明确规定，否则未经事先书面同意，不得将本文件或内容的任何部分复制、复制、再版、张贴、公开展示、编码、翻译、传输或分发到任何其他媒体中以供出版或分发或用于任何商业企业瑞萨电子的同意。Arm®和Cortex®是ArmLimited的注册商标。CoreSight 是ArmLimited的商标。

CoreMark®是嵌入式微处理器基准联盟的注册商标。

MagicPacket 是AdvancedMicroDevices Inc.的商标。

SuperFlash®是SiliconStorageTechnology Inc.在包括美国和日本在内的多个国家的注册商标。本文件中提及的其他品牌和名称可能是其各自所有者的商标或注册商标。

RA生态工作室



RA生态工作室

---

RA2A1 Microcontroller Group Datasheet

Publication Date: Rev.1.10 Mar 16, 2020

Published by: Renesas Electronics Corporation

---

---

RA2A1 Microcontroller Group Datasheet

Publication Date: Rev.1.10 Mar 16, 2020

Published by: 瑞萨电子公司

---

## General Precautions

- 1. Precaution against Electrostatic Discharge (ESD)**

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
- 2. Processing at power-on**

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
- 3. Input of signal during power-off state**

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
- 4. Handling of unused pins**

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
- 5. Clock signals**

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
- 6. Voltage application waveform at input pin**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).
- 7. Prohibition of access to reserved addresses**

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
- 8. Differences between products**

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

## 地址列表

### 一般注意事项

- 1.防止静电放电(ESD)强电场暴露于CMOS器件时，会导致栅极氧化物的破坏，并最终导致**

降级设备操作。必须采取措施，尽可能地阻止静电的产生，并在产生时迅速消散。环境控制必须充分。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具，包括工作台和地板都必须接地。操作员还必须使用腕带接地。不得赤手触摸半导体器件。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。

- 2.通电时的处理通电时产品的状态是不确定的。LSI内部电路的状态为**

indeterminate并且在供电时寄存器设置和引脚的状态未定义。在将复位信号施加到外部复位管脚的成品中，从通电到复位过程完成，管脚的状态不能得到保证。同样，通过片内上电复位功能复位的产品，从通电到电源达到指定的复位电平，其引脚的状态也无法保证。

- 3.关机状态下的信号输入不要在设备关机状态下输入信号或IO上拉电源。输入此类信号或IO上拉电源导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件退化。遵循产品文档中所述的断电状态下输入信号指南。**

- 4.未使用引脚的处理按照手册中未使用引脚处理中的说明处理未使用引脚。CMOS产品的输入引脚一般处于高阻状态。在未使用的引脚处于开路状态的情况下，在LSI附近会感应出额外的电磁噪声，相关的直通电流会在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。**

- 5.时钟信号应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序执行过程中切换时钟信号时，请等待目标时钟信号稳定。在复位期间使用外部谐振器或外部振荡器生成时钟信号时，请确保仅在时钟信号完全稳定后才释放复位线。此外，在程序执行过程中切换到由外部谐振器或外部振荡器产生的时钟信号时，请等待目标时钟信号稳定。**

- 6.输入引脚的电压施加波形由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS设备的输入**

由于噪声等原因，会停留在 $V_{IL}$ (Max.)和 $V_{IH}$ (Min.)之间的区域内，例如，设备可能会发生故障。当输入电平固定时，以及输入电平通过 $V_{IL}$ (Max.)和 $V_{IH}$ (Min.)之间的区域时，请注意防止颤振噪声进入器件。

- 7.禁止访问保留地址**

禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些地址，因为不能保证LSI的正确操作。

- 8.产品之间的差异在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。同一组中的微处理单元或微控制器单元产品的特性可能会在内部存储器容量、布局图案和其他因素方面有所不同，这些因素会影响电气特性的范围，例如特性值、工作裕度、抗噪声能力和辐射噪声量。当更改为具有不同部件号的产品时，对给定产品实施系统评估测试。**

## Notice

- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
- Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
- No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
- Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.  
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
- When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
- Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
- Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
- It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
- Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.  
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev. 4.0-1 November 2017)



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics Corporation**  
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

**Renesas Electronics America Inc.**  
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852-2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia  
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338

## Notice

- 本文档中的电路、软件和其他相关信息的描述仅用于说明半导体产品的操作和应用示例。您全权负责在您的产品或系统设计中加入或以任何其他方式使用电路、软件和信息。瑞萨电子对由以下人员造成的任何损失和损害不承担任何责任  
您或第三方因使用这些电路、软件或信息而引起的。
- 瑞萨电子在此明确声明不对侵权或涉及第三方专利、版权或其他知识产权的任何其他索赔提供任何保证和责任，或因使用本文档中描述的瑞萨电子产品或技术信息而引起的，包括但不限于产品数据、图纸、图表、程序、算法和应用程序 examples。
- 根据瑞萨电子或其他方的任何专利、版权或其他知识产权，特此未授予任何明示、暗示或其他许可。
- 您不得更改、修改、复制或反向工程任何瑞萨电子产品，无论是全部还是部分。瑞萨电子对由以下人员造成的任何损失或损害不承担任何责任  
您或第三方因此类更改、修改、复制或逆向工程而引起的。
- 瑞萨电子产品根据以下两个质量等级进行分类：“标准”和“高质量”。每个瑞萨电子产品的预期应用取决于产品的质量等级，如下所示。  
"Standard": 电脑;办公用品;通讯设备; 测试和测量设备; 视听设备; 家用电器; 机械工具;个人电子设备;工业机器人; 等等  
"高品质": 运输设备 (汽车、火车、轮船等) ; 交通管制 (红绿灯) ; 大型通讯设备; 关键金融终端系统; 安全控制设备; 等等  
除非在瑞萨电子数据表或其他瑞萨电子文档中明确指定为高可靠性产品或适用于恶劣环境的产品，否则瑞萨电子产品是不打算或授权用于可能对人类生命或身体伤害构成直接威胁的产品或系统 (人工生命支持设备或系统; 外科植入物等) , 或可能导致严重的财产损失 (空间系统; 海底中继器; 核电控制系统; 飞机控制系统; 关键工厂系统; 军事装备等) 。瑞萨电子否认任何和所有您或任何第三方因使用与任何瑞萨电子产品数据表、用户手册或其他瑞萨电子文件。
- 使用瑞萨电子产品时, 请参阅最新的产品信息 (数据表、用户手册、应用说明、“处理和使用半导体器件的一般说明”) 可靠性手册等) , 并确保使用条件在瑞萨电子规定的最大额定值、工作电源电压范围、散热范围内  
瑞萨电子不承担因在上述规定之外使用瑞萨电子产品而引起的任何故障、故障或事故的任何和所有责任 ranges。
- 尽管瑞萨电子努力提高瑞萨电子产品的质量和可靠性, 但半导体产品具有特定的特性, 例如在运行时会发生故障。特定使用条件下的特定速率和故障。除非在瑞萨电子数据表或其他瑞萨电子文档中指定为高可靠性产品或适用于恶劣环境的产品电子文档, 瑞萨电子产品不受抗辐射设计。您有责任实施安全措施以防止人身伤害、受伤的可能性  
瑞萨电子产品出现故障或故障, 例如硬件和软件的安全设计, 包括但不限于:  
冗余、火灾控制和故障预防、老化退化的适当处理或其他其他适当的措施。因为单评估微机电软件是很困难的并且不切实际, 您有责任评估您制造的最终产品或系统的安全性。
- 请联系瑞萨电子销售办事处了解有关环境问题的详细信息, 例如每个瑞萨电子产品的环境兼容性。您有责任认真负责充分调查规范受控物质的包含或使用的适用法律和法规, 包括但不限于欧盟RoHS指令, 以及使用瑞萨电子产品符合所有这些适用的法律和法规。瑞萨电子不承担因您不遵守适用的法律法规。
- 瑞萨电子的产品和技术不得用于或整合到任何适用的国内或国外法律禁止制造、使用或销售的产品或系统中或法规。您应遵守主张对当事人具有管辖权的任何国家/地区的政府颁布和管理的任何适用的出口管制法律和法规, 或 transactions。
- 瑞萨电子产品的买方或分销商, 或任何其他向第三方分销、处置或以其他方式出售或转让产品的第三方有责任通知此类第三方在本文中规定的内容和条件之前的一方。
- 未经瑞萨电子事先书面同意, 不得以任何形式全部或部分翻印、复制或复制本文档。
- 如果您对本文档中包含的信息或瑞萨电子产品有任何疑问, 请联系瑞萨电子销售办事处。  
(注1) 本文中使用的“瑞萨电子”是指瑞萨电子公司, 还包括其直接或间接控制的子公司。  
(注2) “瑞萨电子产品”是指由瑞萨电子开发或制造或为瑞萨电子制造的任何产品

(Rev.4.0-1 November 2017)



### 销售办事处

Renesas Electronics Corporation

<http://www.renesas.com>

有关最新和详细信息, 请参阅"<http://www.renesas.com/>”。

瑞萨电子株式会社TOYOSUFORESIA 3-2-24Toyosu Koto-ku Tokyo1  
35-0061 Japan

瑞萨电子美国公司1001MurphyRanchRoad Milpitas C  
A95035 U.S.A.电话: +1-408-432-8888, 传真: +1-408-434-5351

瑞萨电子加拿大有限公司9251YongeStreet Suite8309RichmondHill O  
ntarioCanadaL4C9T3电话: +1-905-237-2004

**瑞萨电子欧洲有限公司**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**瑞萨电子 (中国) 有限公司**  
中国北京市海淀区上地8街7号院7号楼1层101-T01室100085  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**瑞萨电子 (上海) 有限公司**  
中国上海市普陀区岚皋路555号中央大厦A座301单元200333  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

瑞萨电子香港有限公司香港九龙旺角太子道西193号世纪广场2座16楼1601-1611室

Tel: +852-2265-6688, Fax: +852-2886-9022  
RenesasElectronicsTaiwanCo.Ltd.13F No.363 FuShingNor  
thRoad Taipei10543 Taiwan电话: +886-2-8175-9600  
, 传真: +8862-8175-9670

瑞萨电子新加坡私人有限公司Ltd 80BendemeerRoad Unit#06-02HyfluxInno  
vationCentre Singapore339949电话: +65-6213-0200, 传真: +65-6213-0300RenesasElectronicsMalaysiaSdn.Bhd.

UnitNo3A-1Level3ATower8UOABusinessPark No1JalanPengaturcaraU151A SeksyenU1 40150ShahAlam Selangor Malaysia  
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

**瑞萨电子印度列兵. 有限公司**  
No.777C 100FeetRoad HAL2ndStage Indiranagar Bangalore560038 India  
Tel: +91-80-67208700

RenesasElectronicsKoreaCo.Ltd.17F KAMCOYangjaeTower 262 Gangnam-daero Gan  
gnam-gu Seoul 06265KoreaTel:+82-2-558-3737 Fax:+82-2-558-5338

封底

Renesas RA Family  
RA2A1 Group

瑞萨电子RA家族  
RA2A1 Group

RA生态工作室