Datasheet

RA6E2 Group

Renesas Microcontrollers

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Rev.1.10
Feb 28, 2023

The RA6E2 Group delivers up to 200 MHz of CPU performance using an Arm® Cortex®-M33 core with a code flash memory ranging from 128 KB to 256 KB, 4 KB of data flash memory, and 40 KB of SRAM. The RA6E2 Group offers a wide set of peripherals, including USB Full Speed, CANFD, Quad SPI, I3C, and ADC.

Features

■ Arm® Cortex®-M33 Core
- Armv8-M architecture with the main extension
- Maximum operating frequency: 200 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory
- Up to 256-KB code flash memory
- 4-KB data flash memory (100,000 program/erase (P/E) cycles)
- 40-KB SRAM

■ Connectivity
- Serial Communications Interface (SCI) × 2
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
- I3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2
- Quad Serial Peripheral Interface (QSPI)
- USB 2.0 Full-Speed Module (USBFS)
- CAN with Flexible Data-rate (CANFD)
- Serial Sound Interface Enhanced (SSIE)
- Consumer Electronics Control (CEC)

■ Analog
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 16-bit Enhanced (GPT16E) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

■ Security
- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- 128-bit unique ID
- True Random Number Generator (TRNG)
- Pin function
  - Secure pin multiplexing

■ System and Power Management
- Low power modes
- RealTime Clock (RTC) with calendar
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

■ General-Purpose I/O Ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage
- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages
- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)
- Ta = -40°C to +85°C
  - 64-pin BGA (5 mm × 5 mm, 0.5 mm pitch)
  - 36-pin BGA (4 mm × 4 mm, 0.5 mm pitch)

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RA6E2组使用Arm®Cortex®-M33内核提供高达200MHz的CPU性能，该内核具有128KB至256KB的代码闪存、4KB数据闪存和40KBSRAM。RA6E2组提供广泛的外围设备，包括USB全速、CANFD、四SPI、I3C和ADC。

Features

■Arm®Cortex®-M33核心

●主扩展的Armv8-M架构●最大工作频率：200MHz●Arm内存保护单元（ArmMPU）

-受保护的存储器系统架构(PMSAv8)-安全MPU(MPU_S):8个区域-非安全MPU(MPU_NS):8个区域●SysTick定时器

-嵌入两个Systick定时器：安全和非安全实例-由LOCO或系统时钟驱动●CoreSight ETM-M33

■ Memory

●高达256-KB代码闪存●4-KB数据闪存（100 000个程序擦除（PE）周期）●40-KBSRAM

■ Connectivity

●串行通信接口(SCI)×2-异步接口-8位时钟同步接口 智能卡接口-简单IIC-简单SPI-曼彻斯特编码●I3c总线接口(I3C)●串行外设接口(SPI)×2●四路串行外设接口(QSPI)●USB2.0全速模块(USBFS)●具有灵活数据速率(CANFD)●串行声音接口增强(SSIE)●消费电子控制(CEC)

■ Analog

●12位AD转换器(ADC12)●12位DA转换器(DAC12)×2●温度传感器(TSN)

■ Timers

●通用PWM定时器16位增强型(GPT16E)×6●低功耗异步通用定时器(AGT)×2

■ Security

® ®

-代码闪存最多三个区域-数据闪存最多两个区域-SRAM最多三个区域-每个外设的独立安全或非安全安全归因●128位唯一ID●真随机数发生器（TRNG）●Pin功能

-安全引脚复用

■系统和电源管理●低功耗模式●实时时钟(RTC)带日历●事件链路控制器(ELC)●数据传输控制器(DTC)●DMA控制器(DMAC)×8●上电复位●低压检测(LVD)带电压设置●看门狗定时器(WDT)●独立看门狗定时器(IWDT)

■多个时钟源

●主时钟振荡器(MOSC)(8至24MHz)●子时钟振荡器(SOSC)(32.768kHz)●高速片上振荡器(HOCO)(161820MHz)●中速片上振荡器(MOCO)(8MHz)●低速片上振荡器(LOCO)(32.768kHz)●IWDT专用片上

●HocoMOCOLOCO的时钟修剪功能●PLL●时钟输出支持

■ General-Purpose I/O Ports

●5v容差，漏极开路，输入上拉，可切换驱动能力

■工作电压●VCC：2.7〜3.6V

■工作温度和封装●Ta=-40℃至+105℃

64针LQFP(10毫米×10毫米 0.5毫米间距）48针QFN(7毫米×7毫米 0.5毫米间距)-32针QFN(5毫米×5毫米 0.5毫米间距)●Ta=-40℃至+85℃

64-pin BGA (5 mm × 5 mm, 0.5 mm pitch)
- 36-pin BGA (4 mm × 4 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 200 MHz with the following features:

- Up to 256 KB code flash memory
- 40 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- USBFS
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	● Maximum operating frequency: up to 200 MHz ● Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 ● Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions ● SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) ● CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory.
Data flash memory	4 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section x, Standby SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: ● Single-chip mode ● SCI/USB/SWD boot mode
Resets	The MCU provides 14 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

1. Overview

该MCU集成了多个系列的软件和引脚兼容的基于Arm®的32位内核，这些内核共享一组通用的
瑞萨电子外设可促进设计可扩展性和基于平台的高效产品开发。

该系列中的MCU采用高性能ArmCortex®-M33内核，运行频率高达200MHz，具有以下特性:

- 高达256KB代码闪存
- 40 KB SRAM
- 四串行外设接口(QSPI)
- USBFS
- 模拟外设
- 保安及安全功能

1.1 功能大纲

Table 1.1 臂芯

Feature	功能描述
手臂皮层-M33核心	● 最大工作频率：高达200MHz ● Arm Cortex-M33 core: – 具有安全扩展的Armv8-M架构 – Revision: r0p4-00rel0 ● Arm内存保护单元(ArmMPU) – 受保护内存系统架构(PMSAv8) – 安全MPU(MPU_S)：8个区域 – Non-secure MPU (MPU_NS): 8 regions ● SysTick timer – 嵌入两个系统定时器：安全和非安全实例 – 由SysTick定时器时钟(SYSICCLK)或系统时钟(ICLK)驱动 ● CoreSight™ ETM-M33

Table 1.2 Memory

Feature	功能描述
代码闪存	最大256KB的代码闪存。
数据闪存	4KB的数据闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。
SRAM	具有奇偶校验位或纠错码(ECC)的片内高速SRAM。
Standby SRAM	可在深度软件待机模式下保留数据的片上SRAM。 请参见第x节备用SRAM。

Table 1.3 系统(1/2)

Feature	功能描述
操作模式	两种操作模式：● ● SCIUSBSWD启动模式
Resets	MCU提供14次复位。
低压检测(LVD)	低压检测(LVD)模块监控输入到VCC引脚的电压电平。检测电平可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器(LVD0、LVD1、LVD2)组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用配置在各种电压阈值下检测VCC变化。

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	● Main clock oscillator (MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● IWDT-dedicated on-chip oscillator ● PLL ● Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External buses	● QSPI area (EQBIU): Connected to the QSPI (external device interface)

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16E × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 1.3 系统(2/2)

Feature	功能描述
Clocks	● 主时钟振荡器(MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● IWDT-dedicated on-chip oscillator ● PLL ● 时钟输出支持
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(Cac)在选择为测量基准的时钟(测量基准时钟)产生的时间内计数待测量时钟(测量目标时钟)的脉冲，并根据脉冲数是否在允许范围内当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，产生中断请求。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽中断。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择功率控制模式以及过渡到低功率模式。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被复盖。要保护的寄存器是用保护寄存器(PRCR)设置的.
内存保护单元(MPU)	MCU有一个存储器保护单元(MPU)。

Table 1.4 活动连结

Feature	功能描述
事件链路控制器(ELC)	事件链路控制器(ELC)使用各种外围模块生成的事件请求作为源信号，将它们连接到不同的模块，允许模块之间的直接链路，而无需CPU干预。

Table 1.5 直接内存访问

Feature	功能描述
数据传输控制器(DTC)	提供了数据传输控制器(DTC)模块，用于在被中断请求激活时传输数据。
DMA Controller (DMAC)	该MCU包括一个8通道直接存储器访问控制器(DMAC)，可以在不受CPU干预的情况下传输数据。当产生DMA传送请求时，DMAC将存储在传送源地址处的数据传送到传送目的地址。

Table 1.6 外部总线接口

Feature	功能描述
外部巴士	● QSPI区（EQBIU）：连接到QSPI（外部设备接口）

Table 1.7 计时器(1的2)

Feature	功能描述
通用PWM定时器(GPT)	通用PWM定时器(GPT)是具有GPT16E×6通道的16位定时器。PWM波形可以通过控制上计数器、下计数器或上下计数器来产生.此外，可以生成用于控制无刷直流电动机的PWM波形。GPT也可以用作通用定时器。
端口输出启用GPT(POEG)	端口输出使能(POEG)功能可将通用PWM定时器(GPT)输出引脚置于输出禁用状态
低功耗异步通用 用途定时器(AGT)	低功耗异步通用定时器(AGT)是一款32位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及计数外部事件。该定时器由一个重新加载寄存器和一个向下计数器组成。重新加载寄存器和向下计数器被分配到相同的地址，并且可以用AGT寄存器访问。

Table 1.7 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.8 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffers.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a device controller. The module supports full-speed transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 5 pipes. Pipe 0 and pipe 4 to pipe 7 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission.
Consumer Electronics Control module (CEC)	The CEC transmission/reception module can generate and receive CEC signals complied with the High-Definition Multimedia Interface (HDMI) Version 1.4b. The module can also automatically detect communication states.

Table 1.7 计时器(2的2)

Feature	功能描述
实时时钟(RTC)	实时时钟（rtc）有两种计数模式，日历计数模式和二进制计数模式，用于切换寄存器设置。对于日历计数模式，RTC具有从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC计数秒并且保留信息作为串行值。二进制计数模式可用于公历（西方）日历以外的日历。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位向下计数器，可用于在计数器下溢时重置MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。
独立看门狗定时器(IWDT)	独立看门狗定时器（IWDT）由一个14位下降计数器组成，必须定期维护，以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此在系统失控时，它特别适用于将MCU返回到已知的故障安全机制状态。IWDT可以通过复位、下溢、刷新错误或刷新寄存器中的计数值自动触发。

Table 1.8 通信接口

Feature	功能描述
串行通信接口(SCI)	串行通信接口(SCI)×2通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） ● 8位时钟同步接口 ● Simple IIC (master-only) ● 简单的SPI ● 智能卡接口 ● 曼彻斯特接口 智能卡接口符合isoIEC7816-3电子信号和传输协议标准。SCIn(n=0 9)具有FIFO缓冲器，可实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。
I3C总线接口(I3C)	I3C总线接口(I3C)有一个通道。I3C模块符合并提供恩智浦I2C（集成电路间）总线接口功能的子集和mipiI3C的子集。
串行外设接口(SPI)	串行外设接口(SPI)有2个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。
灵活的控制区域网络 Data-Rate Module (CANFD)	具有灵活数据速率（CANFD）模块的CAN可以处理经典的CAN帧和 CANFD框架符合ISO11898-1标准。 该模块支持4个发送缓冲器和32个接收缓冲器。
USB2.0全速模块(USBFS)	USB2.0全速模块(USBFS)可用作设备控制器。该模块支持通用串行总线规范2.0中定义的全速传输。该模块具有内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，提供最多5个管道。 管道0和管道4到管道7可以根据用于通信的外围设备或根据您的系统分配任何端点编号。
四串行外设接口(QSPI)	四串行外设接口(QSPI)是一个存储器控制器，用于连接具有SPI兼容接口的串行ROM（非易失性存储器，如串行闪存、串行EEPROM或串行FeRAM）。
串行声音接口增强(SSIE)串行声音接口增强(SSIE)外设提供与数字音频设备接口的功能，用于通过串行总线传输I2S单声道TDM音频数据。SSIE支持高达50MHz的音频时钟频率，可作为从站或主站接收器、发射器或收发器操作，以适应各种应用。SSIE在接收器和发送器中包含32级FIFO缓冲器，并支持中断和DMA驱动的数据接收和发送。	
消费电子控制模块(cec)	CEC传输接收模块可以生成和接收符合高清多媒体接口(HDMI)1.4b版的CEC信号，该模块还可以自动检测通信状态。

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) is provided. Up to 12 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.11 I/O ports

Feature	Functional description
Programmable I/O ports	• I/O ports for the 64-pin LQFP – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • I/O ports for the 48-pin QFN – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin QFN – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4 • I/O ports for the 64-pin BGA – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • I/O ports for the 36-pin BGA – I/O pins: 20 – Input pins: 4 – Pull-up resistors: 21 – N-ch open-drain outputs: 20 – 5-V tolerance: 5

Table 1.9 Analog

Feature	功能描述
12-bit A/D Converter (ADC12)	提供了一个12位逐次逼近AD转换器(ADC12)。最多可选择12个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。
12-bit D/A Converter (DAC12)	提供12位DA转换器(DAC12)。
温度传感器(TSN)	片上温度传感器(TSN)可确定并监控管芯温度，确保器件的可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压提供给ADC12进行转换，可供终端应用进一步使用。

Table 1.10 资料处理

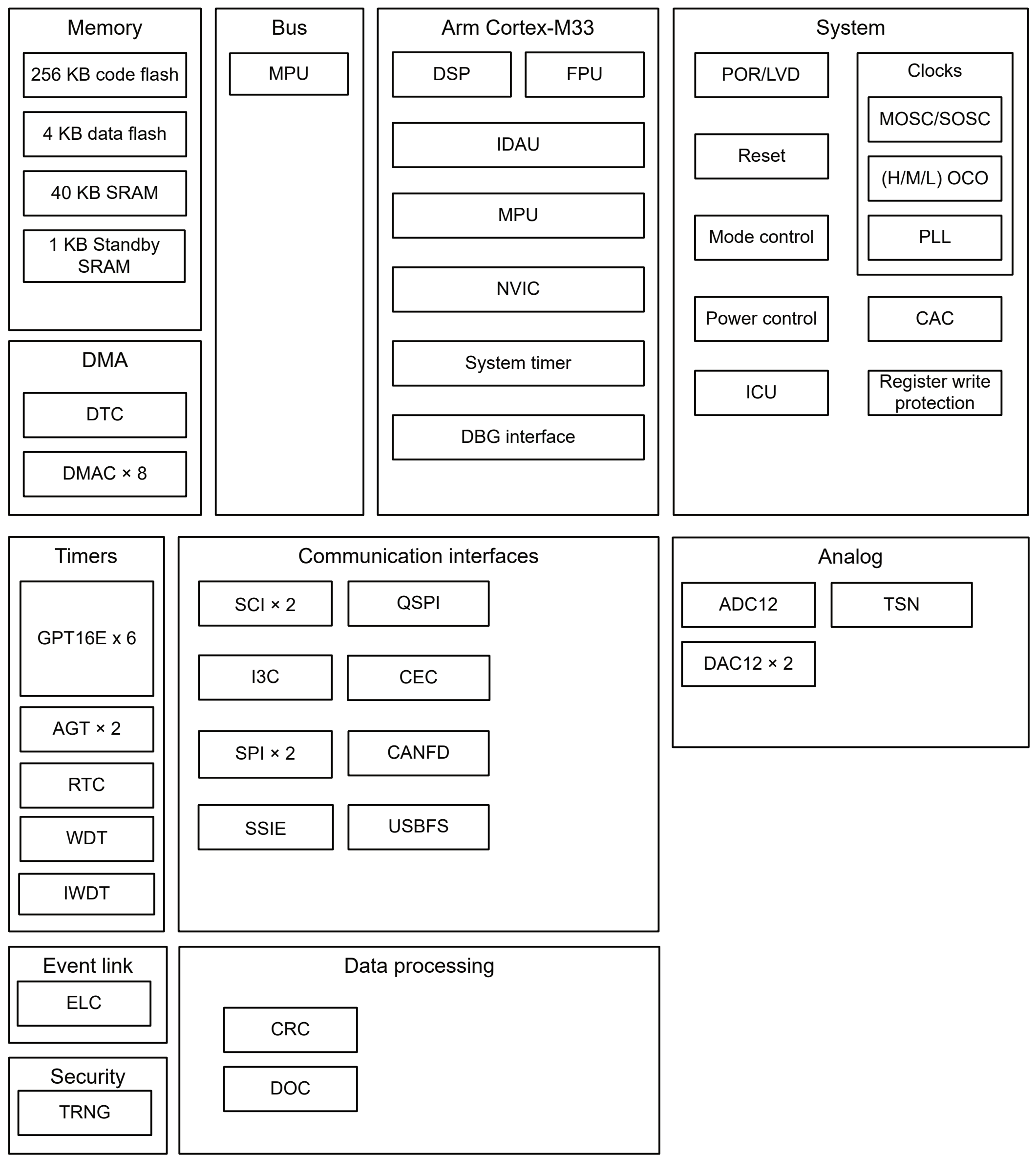
Feature	功能描述
循环冗余校验(CRC)计算器	循环冗余校验(CRC)生成CRC码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB优先或MSB优先通信。此外，还提供各种CRC生成多项式。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法运算。当所选条件适用时，将比较16位数据并生成中断。

Table 1.11 I/O ports

Feature	功能描述
可编程IO端口	• 用于64引脚LQFP的IO端口 – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • 用于48引脚QFN的IO端口 – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • 用于32引脚QFN的IO端口 – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4 • 用于64引脚BGA的IO端口 – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • 36引脚BGA的IO端口 – I/O pins: 20 – Input pins: 4 – Pull-up resistors: 21 – N-ch open-drain outputs: 20 – 5-V tolerance: 5

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.



Note: Not available on all parts

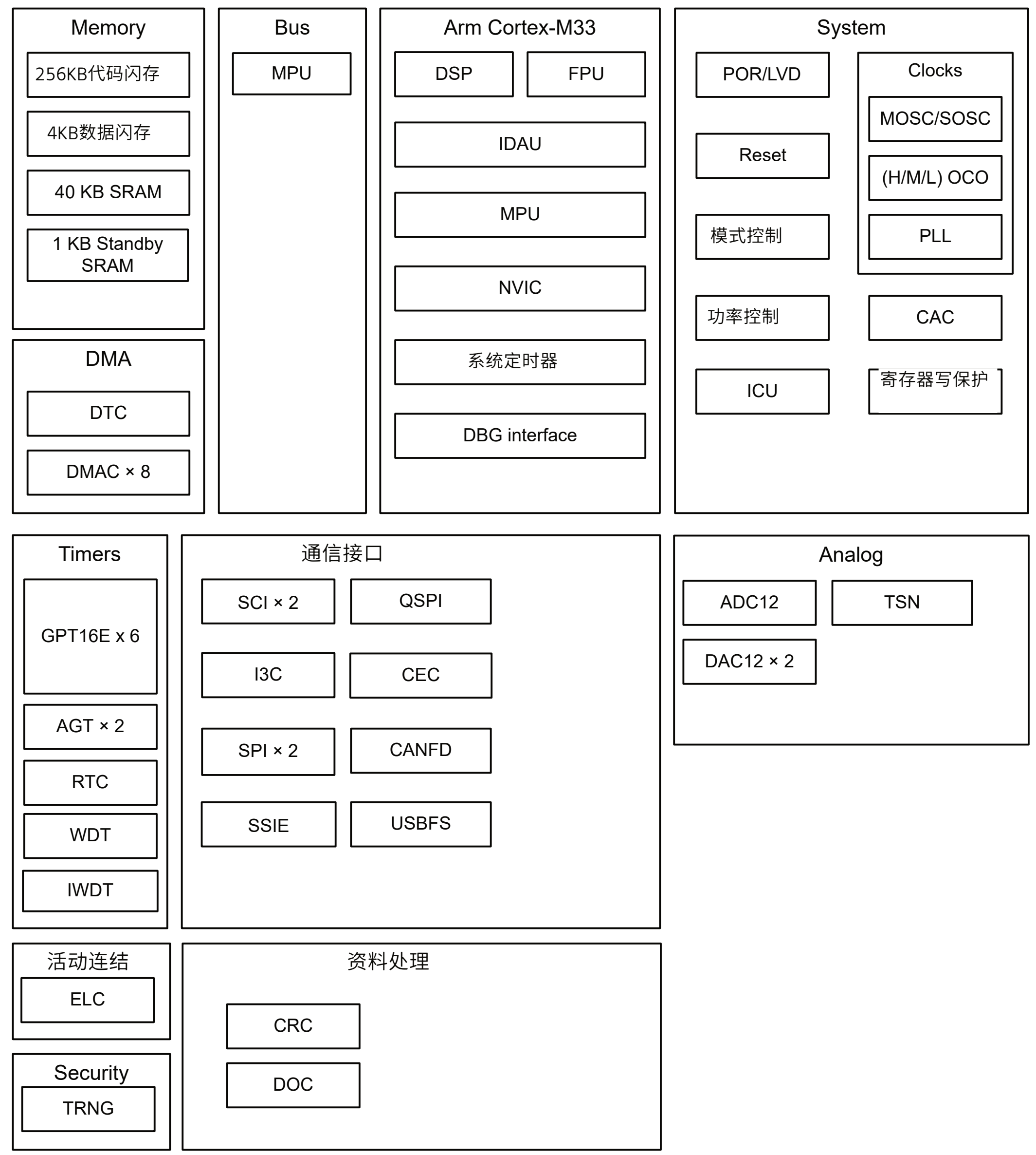
Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图.组内的某些单独设备具有所述功能的子集。

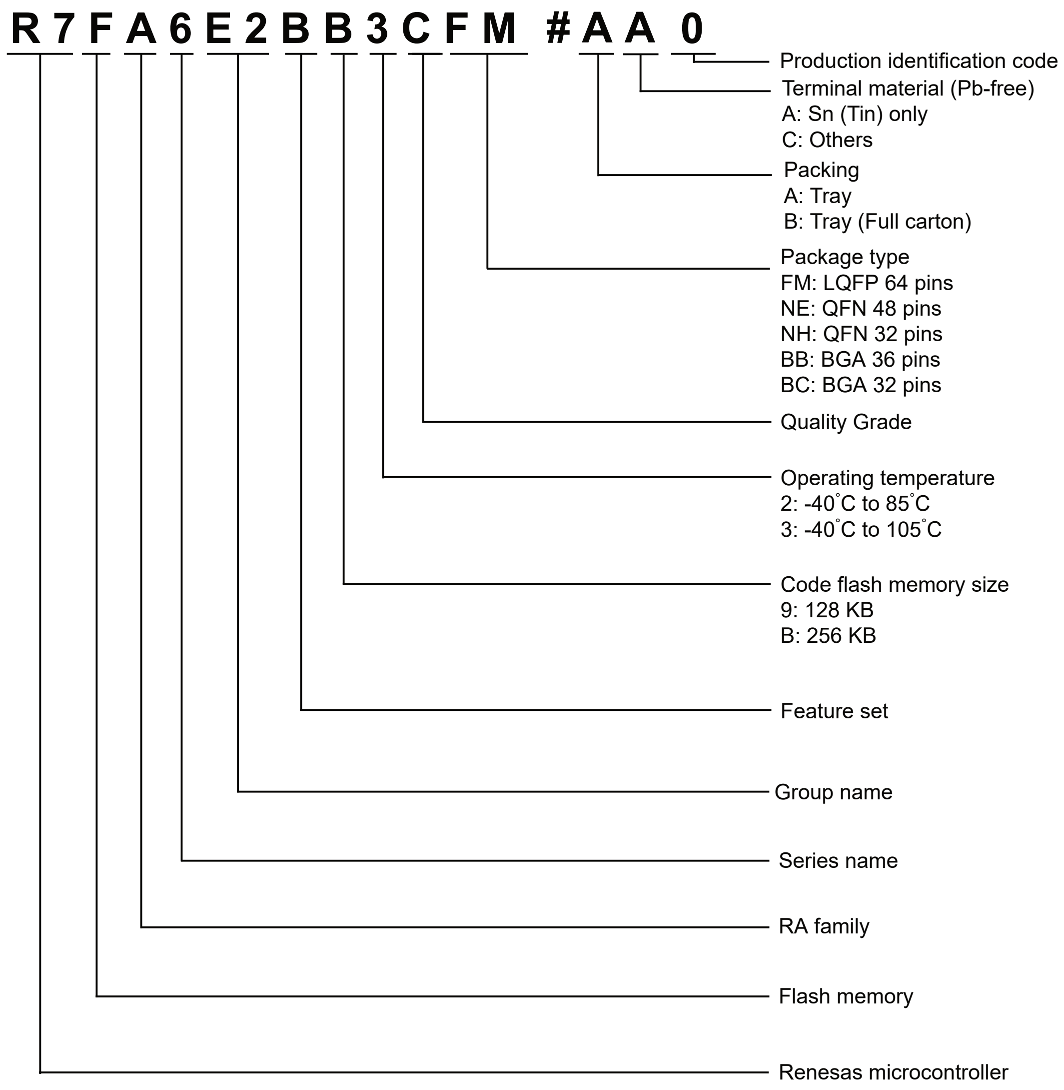


Note: 并非所有部件都有

Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.12显示了产品列表。

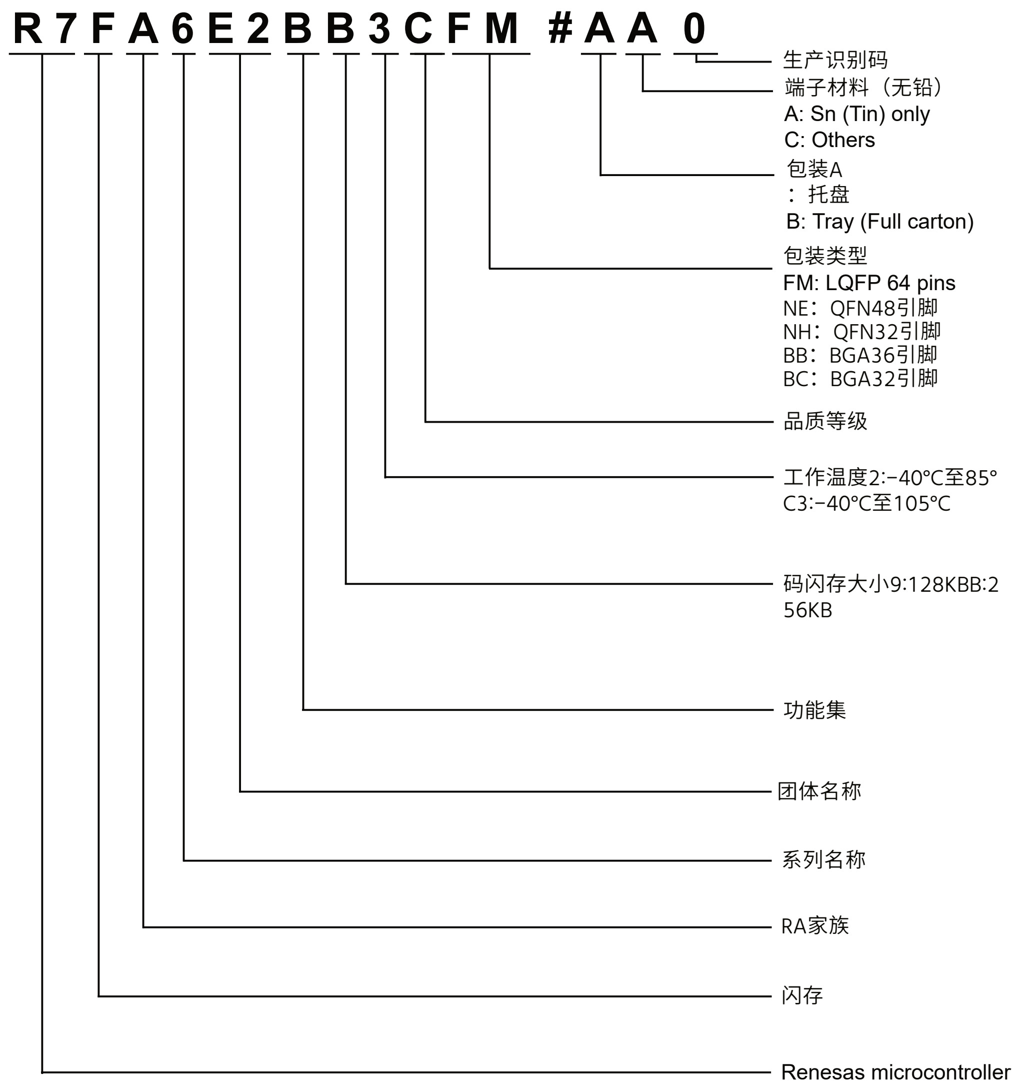


Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6E2BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 to +105°C
R7FA6E2BB3CNE	PWQN0048KC-A				
R7FA6E2BB3CNH	PWQN0032KE-A				
R7FA6E2BB2CBB	PLBG0064KB-A				-40 to +85°C
R7FA6E2BB2CBC	PLBG0036KA-A				
R7FA6E2B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 to +105°C
R7FA6E2B93CNE	PWQN0048KC-A				
R7FA6E2B93CNH	PWQN0032KE-A				
R7FA6E2B92CBB	PLBG0064KB-A				-40 to +85°C
R7FA6E2B92CBC	PLBG0036KA-A				



Note: 在瑞萨网站上查看每个产品的订单屏幕，以获取#后的有效符号。

Figure 1.2 零件编号方案

Table 1.12 产品目录

产品零件编号	包装代码	代码闪光	数据闪	SRAM	操作温度
R7FA6E2BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 to +105°C
R7FA6E2BB3CNE	PWQN0048KC-A				
R7FA6E2BB3CNH	PWQN0032KE-A				
R7FA6E2BB2CBB	PLBG0064KB-A				-40 to +85°C
R7FA6E2BB2CBC	PLBG0036KA-A				
R7FA6E2B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 to +105°C
R7FA6E2B93CNE	PWQN0048KC-A				
R7FA6E2B93CNH	PWQN0032KE-A				
R7FA6E2B92CBB	PLBG0064KB-A				-40 to +85°C
R7FA6E2B92CBC	PLBG0036KA-A				

1.4 Function Comparison

Table 1.13 Function Comparison

Part numbers		R7FA6E2BB3CFM/ R7FA6E2BB2CBB R7FA6E2B93CFM/ R7FA6E2B92CBB	R7FA6E2BB3CNE R7FA6E2B93CNE	R7FA6E2BB2CBC R7FA6E2B92CBC	R7FA6E2BB3CNH R7FA6E2B93CNH
Pin count		64	48	36	32
Package		LQFP/BGA	QFN	BGA	QFN
Code flash memory		256 KB, 128 KB			
Data flash memory		4 KB			
SRAM		40 KB			
	Parity	32 KB			
	ECC	8 KB			
Standby SRAM		1 KB			
DMA	DTC	Yes			
	DMAC	8			
System	CPU clock	200 MHz (max.)			
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL			
	CAC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	2			
	I3C	1			
	SPI	2			
	CANFD	1			
	USBFS	Yes			No
	QSPI	Yes			
	SSIE	Yes			
	CEC	Yes			
Timers	GPT16E*1	6		5	4
	AGT*1	2			
	RTC*1	Yes			
Analog	ADC12	12	8	4	5
	DAC12	2		1	
	TSN	Yes			
Data processing	CRC	Yes			
	DOC	Yes			
Event control	ELC	Yes			
Security		TrustZone			
I/O ports	I/O pins	45	29	20	16
	Input pins	5	5	4	5
	Pull-up resistors	46	30	21	17
	N-ch open-drain outputs	45	29	20	16
	5-V tolerance	11	6	5	4

Note 1. Available pins depend on the pin count, see section 1.7. Pin Lists for details.

1.4 功能比较

Table 1.13 功能比较

零件编号		R7FA6E2BB3CFM/ R7FA6E2BB2CBB R7FA6E2B93CFM/ R7FA6E2B92CBB	R7FA6E2BB3CNE R7FA6E2B93CNE	R7FA6E2BB2CBC R7FA6E2B92CBC	R7FA6E2BB3CNH R7FA6E2B93CNH
针数		64	48	36	32
Package		LQFP/BGA	QFN	BGA	QFN
代码闪存		256 KB, 128 KB			
数据闪存		4 KB			
SRAM		40 KB			
	Parity	32 KB			
	ECC	8 KB			
Standby SRAM		1 KB			
DMA	DTC	Yes			
	DMAC	8			
System	CPU时钟	200 MHz (max.)			
	CPU时钟源	MOSC, SOSC, HOCO, MOCO, LOCO, PLL			
	CAC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	2			
	I3C	1			
	SPI	2			
	CANFD	1			
	USBFS	Yes			No
	QSPI	Yes			
	SSIE	Yes			
	CEC	Yes			
Timers	GPT16E*1	6		5	4
	AGT*1	2			
	RTC*1	Yes			
Analog	ADC12	12	8	4	5
	DAC12	2		1	
	TSN	Yes			
资料处理	CRC	Yes			
	DOC	Yes			
事件控制	ELC	Yes			
Security		TrustZone			
I/O ports	I/O pins	45	29	20	16
	输入引脚	5	5	4	5
	Pull-up resistors	46	30	21	17
	N-ch open-drain outputs	45	29	20	16
	5-V tolerance	11	6	5	4

注1。可用引脚取决于引脚数，请参阅第1.7节。详细信息的Pin列表。

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-µF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins

1.5 引脚功能

Table 1.14 引脚功能(1/3)

Function	Signal	I/O	Description
电力供应	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1µf电容将此引脚连接到VSS。电容器应靠近引脚放置。
	VCL	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚。
	VSS	Input	接地销。将其连接到系统电源（0V）。
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可通过EXTAL引脚输入。
	EXTAL	Input	
	XCIN	Input	子时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置工作模式的引脚。该引脚上的信号电平在从复位状态释放后的工作模式转换期间不得改变。
系统控制	RES	Input	复位信号输入引脚。当此信号变为低电平时MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
On-chip emulator	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQn	Input	可屏蔽中断请求引脚
	IRQn-DS	Input	可屏蔽中断请求引脚，也可用于深软件待机模式
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOCnA, GTIOCnB	I/O	输入捕获、输出比较或PWM输出引脚
	GTADSM0, GTADSM1	Output	Ad转换启动请求监控输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的三相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的三相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEEn	Input	外部事件输入使能信号
	AGTIOn	I/O	外部事件输入和脉冲输出引脚
	AGTOn	Output	脉冲输出引脚
	AGTOAn	Output	输出比较匹配输出引脚
	AGTOBn	Output	输出比较匹配b输出引脚

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn	Input	Time capture event input pins
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
I3C	I3C_SCL	I/O	Input/output pins for the I3C clock
	I3C_SDA	I/O	Input/output pins for the I3C data
	SCL0	I/O	Input/output pins for the I2C clock
	SDA0	I/O	Input/output pins for the I2C data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3

Table 1.14 引脚功能(2/3)

Function	Signal	I/O	Description
RTC	RTCOUT	Output	1Hz或64Hz时钟的输出引脚
	RTCICn	Input	时间捕获事件输入引脚
SCI	SCKn	I/O	时钟输入输出引脚（时钟同步模式）
	RXDn	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXDn	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTSn_RTSn	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效。
	CTSn	Input	输开始的输入。
	SCLn	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDAn	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCKn	I/O	时钟输入输出引脚（简单SPI模式）
	MISOn	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSIn	I/O	用于主数据传输的输入输出引脚（简单SPI模式）
	SSn	Input	片选输入引脚（简单SPI模式），低电平有效
I3C	I3C_SCL	I/O	I3C时钟的输入输出引脚
	I3C_SDA	I/O	I3c数据的输入输出引脚
	SCL0	I/O	I2c时钟的输入输出引脚
	SDA0	I/O	I2c数据的输入输出引脚
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	输入或输出引脚，用于从主机输出数据
	MISOA, MISOB	I/O	输入或输出引脚，用于从从机输出数据
	SSLA0, SSLB0	I/O	用于从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	用于从机选择的输出引脚
CANFD	CRX0	Input	接收数据
	CTX0	Output	传输数据
USBFS	VCC_USB	Input	电源引脚
	VSS_USB	Input	接地销
	USB_DP	I/O	USB片上收发器的D+引脚。将此引脚连接到USB总线的D+引脚。
	USB_DM	I/O	USB片上收发器的Dpin。将此引脚连接到USB总线的Dpin。
	USB_VBUS	Input	USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测到VBUS引脚状态（连接或断开）。
QSPI	QSPCLK	Output	QSPI时钟输出引脚
	QSSL	Output	QSPI从机输出引脚
	QIO0 to QIO3	I/O	Data0 to Data3

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	SSIDATA0	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)
CEC	CECIO	I/O	CEC data communication
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the D/A Converter.
	VREFL	Input	Analog reference ground pin for the D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter. (n: pin number)
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

Table 1.14 引脚功能(3/3)

Function	Signal	I/O	Description
SSIE	SSIBCK0	I/O	SSIE串行位时钟引脚
	SSILRCK0/SSIFS0	I/O	LR时钟帧同步引脚
	SSITXD0	Output	串行数据输出引脚
	SSIRXD0	Input	串行数据输入引脚
	SSIDATA0	I/O	串行数据输入输出引脚
	AUDIO_CLK	Input	用于音频的外部时钟引脚（输入过采样时钟）
CEC	CECIO	I/O	CEC数据通信
模拟电源	AVCC0	Input	模拟电压电源引脚。这被用作各个模块的模拟电源.为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各自模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH	Input	DA转换器的模拟基准电压源引脚。
	VREFL	Input	DA转换器的模拟参考接地引脚。
	VREFH0	Input	ADC12的模拟基准电压源引脚。不使用ADC12时将此引脚连接到AVCC0。
	VREFL0	Input	ADC12的模拟基准接地引脚。将此引脚连接到 不使用ADC12时的AVSS0。
ADC12	AN0n	Input	AD转换器要处理的模拟信号的输入引脚。(n:密码)
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚，有效-低电平。
DAC12	DAn	Output	Da转换器处理的模拟信号的输出引脚。
I/O ports	Pmn	I/O	通用输入输出引脚（m：端口号，n：引脚号）
	P200	Input	通用输入引脚

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

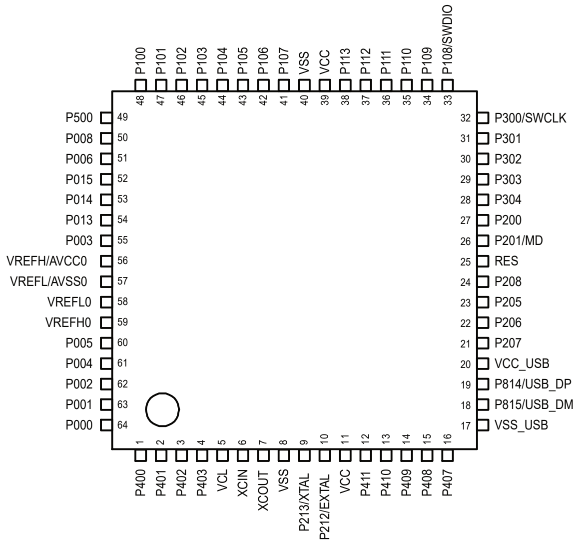


Figure 1.3 Pin assignment for LQFP 64-pin

	A	B	C	D	E	F	G	H	
8	P407	P212/ EXTAL	P213/ XTAL	XCOUT	XCIN	VCL	P400	P000	8
7	P815/ USB_DM	P408	P409	VCC	VSS	P401	P002	P001	7
6	P814/ USB_DP	P207	P410	P411	P403	P402	P004	P005	6
5	P205	P206	P208	VSS_USB	VSS	VREFL/ AVSS0	VREFL0	P003	5
4	P200	P201/ MD	RES	VCC_USB	VCC	VREFH/ AVCC0	VREFH0	P013	4
3	P304	P303	P302	P107	P106	P103	P015	P014	3
2	P300/ SWCLK	P301	P111	P113	P105	P102	P008	P006	2
1	P108/ SWDIO	P109	P110	P112	P104	P101	P100	P500	1
	A	B	C	D	E	F	G	H	

Figure 1.4 Pin assignment for BGA 64-pin

1.6 引脚分配

下图显示了顶视图中的引脚分配。

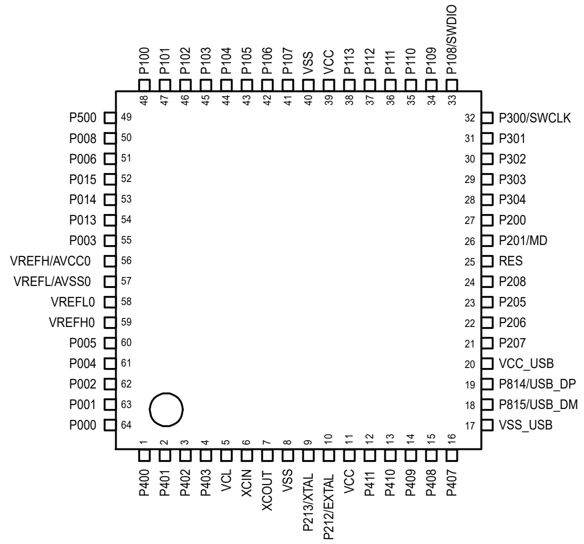


Figure 1.3 Lqfp64引脚的引脚分配

	A	B	C	D	E	F	G	H	
8	P407	P212/ EXTAL	P213/ XTAL	XCOUT	XCIN	VCL	P400	P000	8
7	P815/ USB_DM	P408	P409	VCC	VSS	P401	P002	P001	7
6	P814/ USB_DP	P207	P410	P411	P403	P402	P004	P005	6
5	P205	P206	P208	VSS_USB	VSS	VREFL/ AVSS0	VREFL0	P003	5
4	P200	P201/ MD	RES	VCC_USB	VCC	VREFH/ AVCC0	VREFH0	P013	4
3	P304	P303	P302	P107	P106	P103	P015	P014	3
2	P300/ SWCLK	P301	P111	P113	P105	P102	P008	P006	2
1	P108/ SWDIO	P109	P110	P112	P104	P101	P100	P500	1
	A	B	C	D	E	F	G	H	

Figure 1.4 Bga64引脚的引脚分配

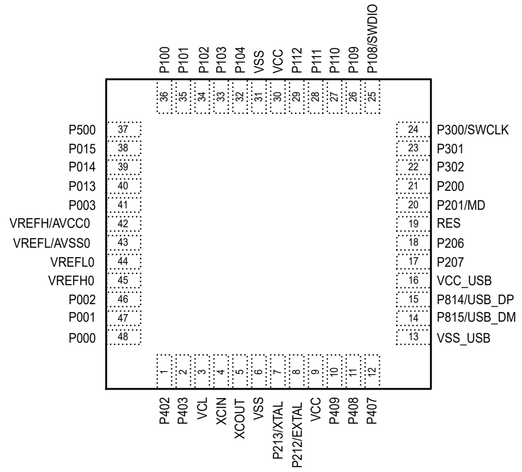
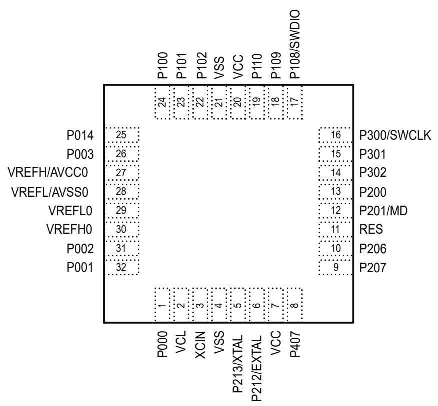


Figure 1.5 Pin assignment for QFN 48-pin

	A	B	C	D	E	F	
6	P407	P212/ EXTAL	P213/ XTAL	XOUT	XCIN	P000	6
5	P815/ USB_DM	P408	P207	P201/ MD	VCL	P001	5
4	P814/ USB_DP	P206	VSS_USB	VSS	VREF/ AVSS0	VREFL0	4
3	P200	RES	VCC_USB	VCC	VREFH /AVCC0	VREFH0	3
2	P300/ SWCLK	P301	P302	P103	P014	P003	2
1	P108/ SWDIO	P109	P110	P102	P101	P100	1
	A	B	C	D	E	F	

Figure 1.6 Pin assignment for BGA 36-pin



Note: XCIN cannot be used in QFN32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.7 Pin assignment for QFN 32-pin

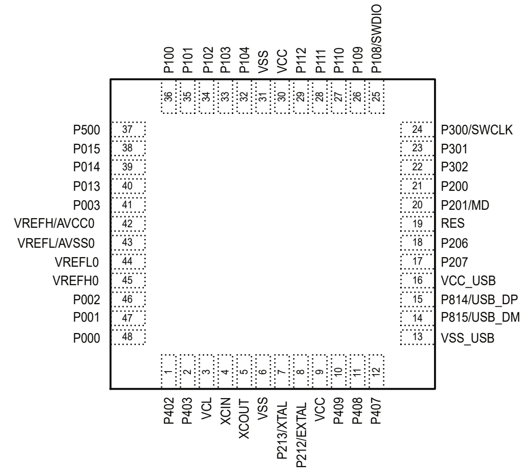
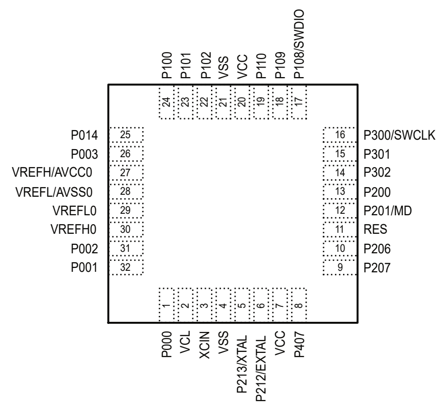


Figure 1.5 Qfn48引脚的引脚分配

	A	B	C	D	E	F	
6	P407	P212/ EXTAL	P213/ XTAL	XOUT	XCIN	P000	6
5	P815/ USB_DM	P408	P207	P201/ MD	VCL	P001	5
4	P814/ USB_DP	P206	VSS_USB	VSS	VREF/ AVSS0	VREFL0	4
3	P200	RES	VCC_USB	VCC	VREFH /AVCC0	VREFH0	3
2	P300/ SWCLK	P301	P302	P103	P014	P003	2
1	P108/ SWDIO	P109	P110	P102	P101	P100	1
	A	B	C	D	E	F	

Figure 1.6 Bga36引脚的引脚分配



Note: XCIN不能在QFN32中使用。XCIN必须通过电阻（下拉）连接到VSS。

Figure 1.7 Qfn32引脚的引脚分配

1.7 Pin Lists

Table 1.15 Pin list (1 of 2)

LQFP64	BGA64	QFN48	BGA36	QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD/USBFS/QSPI/SSIE/CEC	GPT/AGT/RTC	ADC12/DAC12
1	G8	—	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	F7	—	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	F6	1	—	—	CACREF	P402	IRQ4-DS	CRX0/AUDIO_CLK	AGTIO0/AGTIO1/RTCIC0/GTADSM1	—
4	E6	2	—	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/AGTIO1/RTCIC1	—
5	F8	3	E5	2	VCL	—	—	—	—	—
6	E8	4	E6	3	XCIN*1	—	—	—	—	—
7	D8	5	D6	—	XCOUT	—	—	—	—	—
8	E7	6	D4	4	VSS	—	—	—	—	—
9	C8	7	C6	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0/AUDIO_CLK	GTIOC0A/GTETRGC	—
10	B8	8	B6	6	EXTAL	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/AGTEE1	—
11	D7	9	D3	7	VCC	—	—	—	—	—
12	D6	—	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	C6	—	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	C7	10	—	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/AGTOA1	—
15	B7	11	B5	—	—	P408	IRQ7	SCL0_B/AUDIO_CLK	GTIOC1B/GTIW/AGTOB1	—
16	A8	12	A6	8	—	P407	—	SDA0_B/SSIBCK0_A/USB_VBUS	GTIV/AGTIO0/RTCOUT/GTADSM0	ADTRG0
17	D5	13	C4	—	VSS_USB	—	—	—	—	—
18	A7	14	A5	—	USB_DM	P815	—	—	GTIOC0A/GTETRGC	—
19	A6	15	A4	—	USB_DP	P814	—	—	GTIOC0B/GTETRGB	—
20	D4	16	C3	—	VCC_USB	—	—	—	—	—
21	B6	17	C5	9	CACREF	P207	—	SCK9/MOSIA_A/QSSL/SSILRCK0_A/SSIFS0_A	GTIOC5A/GTIW/AGTIO1	—
22	B5	18	B4	10	—	P206	IRQ0-DS	CTS9/SDA0_C/MISOA_A/SSIDATA0_A/CECIO	GTIOC5B/GTIU	—
23	A5	—	—	—	CLKOUT	P205	IRQ1-DS	CTS_RTS9/SS9/SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	C5	—	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	C4	19	B3	11	RES	—	—	—	—	—
26	B4	20	D5	12	MD	P201	—	—	—	—
27	A4	21	A3	13	—	P200	NMI	—	—	—
28	A3	—	—	—	—	P304	IRQ9	—	GTOWLO	—
29	B3	—	—	—	—	P303	—	CTS9	—	—
30	C3	22	C2	14	—	P302	IRQ5	CTS0/SCK9/RSPCKA_A/SSITXD0_A	GTIOC4A/GTOUUP/RTCOUT	—
31	B2	23	B2	15	—	P301	IRQ6	CTS_RTS9/SS9/SSLA0_A/SSIRXD0_A	GTIOC4B/GTOULO/AGTIO0	—
32	A2	24	A2	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	A1	25	A1	17	SWDIO	P108	—	CTS_RTS9/SS9/SSLA0_B	GTIOC0B/GTOULO	—
34	B1	26	B1	18	CLKOUT	P109	—	TXD9/MOSI9/SDA9/MOSIA_B/CTX0/SSITXD0_B	GTIOC1A/GTOVUP/AGTOA0	—
35	C1	27	C1	19	—	P110	IRQ3	RXD9/MISO9/SCL9/MISOA_B/CRX0/SSIRXD0_B	GTIOC1B/GTOVLO/AGTOB0	—

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1.7 密码列表

Table 1.15 引脚列表(1的2)

LQFP64	BGA64	QFN48	BGA36	QFN32	电源、系统、时钟、调试 CAC	I/O ports	前。中断	SCI/I3C/SPI/CANFD/USBFS/QSPI/SSIE/CEC	GPT/AGT/RTC	ADC12/DAC12
1	G8	—	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	F7	—	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	F6	1	—	—	CACREF	P402	IRQ4-DS	CRX0/AUDIO_CLK	AGTIO0/AGTIO1/RTCIC0/GTADSM1	—
4	E6	2	—	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/AGTIO1/RTCIC1	—
5	F8	3	E5	2	VCL	—	—	—	—	—
6	E8	4	E6	3	XCIN*1	—	—	—	—	—
7	D8	5	D6	—	XCOUT	—	—	—	—	—
8	E7	6	D4	4	VSS	—	—	—	—	—
9	C8	7	C6	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0/AUDIO_CLK	GTIOC0A/GTETRGC	—
10	B8	8	B6	6	EXTAL	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/AGTEE1	—
11	D7	9	D3	7	VCC	—	—	—	—	—
12	D6	—	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	C6	—	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	C7	10	—	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/AGTOA1	—
15	B7	11	B5	—	—	P408	IRQ7	SCL0_B/AUDIO_CLK	GTIOC1B/GTIW/AGTOB1	—
16	A8	12	A6	8	—	P407	—	SDA0_B/SSIBCK0_A/USB_VBUS	GTIV/AGTIO0/RTCOUT/GTADSM0	ADTRG0
17	D5	13	C4	—	VSS_USB	—	—	—	—	—
18	A7	14	A5	—	USB_DM	P815	—	—	GTIOC0A/GTETRGC	—
19	A6	15	A4	—	USB_DP	P814	—	—	GTIOC0B/GTETRGB	—
20	D4	16	C3	—	VCC_USB	—	—	—	—	—
21	B6	17	C5	9	CACREF	P207	—	SCK9/MOSIA_A/QSSL/SSILRCK0_A/SSIFS0_A	GTIOC5A/GTIW/AGTIO1	—
22	B5	18	B4	10	—	P206	IRQ0-DS	CTS9/SDA0_C/MISOA_A/SSIDATA0_A/CECIO	GTIOC5B/GTIU	—
23	A5	—	—	—	CLKOUT	P205	IRQ1-DS	CTS_RTS9/SS9/SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	C5	—	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	C4	19	B3	11	RES	—	—	—	—	—
26	B4	20	D5	12	MD	P201	—	—	—	—
27	A4	21	A3	13	—	P200	NMI	—	—	—
28	A3	—	—	—	—	P304	IRQ9	—	GTOWLO	—
29	B3	—	—	—	—	P303	—	CTS9	—	—
30	C3	22	C2	14	—	P302	IRQ5	CTS0/SCK9/RSPCKA_A/SSITXD0_A	GTIOC4A/GTOUUP/RTCOUT	—
31	B2	23	B2	15	—	P301	IRQ6	CTS_RTS9/SS9/SSLA0_A/SSIRXD0_A	GTIOC4B/GTOULO/AGTIO0	—
32	A2	24	A2	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	A1	25	A1	17	SWDIO	P108	—	CTS_RTS9/SS9/SSLA0_B	GTIOC0B/GTOULO	—
34	B1	26	B1	18	CLKOUT	P109	—	TXD9/MOSI9/SDA9/MOSIA_B/CTX0/SSITXD0_B	GTIOC1A/GTOVUP/AGTOA0	—
35	C1	27	C1	19	—	P110	IRQ3	RXD9/MISO9/SCL9/MISOA_B/CRX0/SSIRXD0_B	GTIOC1B/GTOVLO/AGTOB0	—

Table 1.15 Pin list (2 of 2)

LQFP64	BGA64	QFN48	BGA36	QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/ CANFD/USBFS/ QSPI/SSIE/CEC	GPT/AGT/RTC	ADC12/DAC12
36	C2	28	—	—	—	P111	IRQ4	SCK9/RSPCKA_B/ SSIDATA0_B	GTIOC3A	—
37	D1	29	—	—	—	P112	—	SSLA0_B/QSSL	GTIOC3B/ GTETRGD/AGTO1	—
38	D2	—	—	—	—	P113	—	—	GTIOC2A	—
39	E4	30	C3	20	VCC	—	—	—	—	—
40	E5	31	C4	21	VSS	—	—	—	—	—
41	D3	—	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	E3	—	—	—	—	P106	—	SSLB3	AGTOB0	—
43	E2	—	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	E1	32	—	—	—	P104	IRQ1	SSLB1/QIO2	GTIOC1B/ GTETRGB/AGTIO1	—
45	F3	33	D2	—	—	P103	—	CTS_RTS0/SS0/ SSLB0/CTX0/QIO3/ SSILRCK0_B/ SSIFS0_B	GTIOC2A/GTOWUP	—
46	F2	34	D1	22	—	P102	—	SCK0/RSPCKB/ CRX0/QIO0/ SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	F1	35	E1	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB/QIO1	GTIOC5A/ GTETRGB/AGTEE0	—
48	G1	36	F1	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB/QSPCLK/ AUDIO_CLK	GTIOC5B/ GTETRGA/AGTIO0	—
49	H1	37	—	—	CACREF	P500	—	QSPCLK	GTIU/AGTOA0	AN016
50	G2	—	—	—	—	P008	IRQ12-DS	—	—	AN008
51	H2	—	—	—	—	P006	IRQ11-DS	—	—	AN006
52	G3	38	—	—	—	P015	IRQ13	—	—	AN013/DA1
53	H3	39	E2	25	—	P014	—	—	—	AN012/DA0
54	H4	40	—	—	—	P013	—	—	—	AN011
55	H5	41	F2	26	—	P003	—	—	—	AN007
56	F4	42	E3	27	VREFH/AVCC0	—	—	—	—	—
57	F5	43	E4	28	VREFL/AVSS0	—	—	—	—	—
58	G5	44	F4	29	VREFL0	—	—	—	—	—
59	G4	45	F3	30	VREFH0	—	—	—	—	—
60	H6	—	—	—	—	P005	IRQ10-DS	—	—	AN005
61	G6	—	—	—	—	P004	IRQ9-DS	—	—	AN004
62	G7	46	—	31	—	P002	IRQ8-DS	—	—	AN002
63	H7	47	F5	32	—	P001	IRQ7-DS	—	—	AN001
64	H8	48	F6	1	—	P000	IRQ6-DS	—	—	AN000

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.
Note 1. XCIN cannot be used in QFN32. XCIN must be connected to VSS through a resistor (pull down).

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Table 1.15 Pin列表(2的2)

LQFP64	BGA64	QFN48	BGA36	QFN32	电源、系统、时钟、调试 CAC	I/O ports	前。中断	SCI/I3C/SPI/ CANFD/USBFS/ QSPI/SSIE/CEC	GPT/AGT/RTC	ADC12/DAC12
36	C2	28	—	—	—	P111	IRQ4	SCK9/RSPCKA_B/ SSIDATA0_B	GTIOC3A	—
37	D1	29	—	—	—	P112	—	SSLA0_B/QSSL	GTIOC3B/ GTETRGD/AGTO1	—
38	D2	—	—	—	—	P113	—	—	GTIOC2A	—
39	E4	30	C3	20	VCC	—	—	—	—	—
40	E5	31	C4	21	VSS	—	—	—	—	—
41	D3	—	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	E3	—	—	—	—	P106	—	SSLB3	AGTOB0	—
43	E2	—	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	E1	32	—	—	—	P104	IRQ1	SSLB1/QIO2	GTIOC1B/ GTETRGB/AGTIO1	—
45	F3	33	D2	—	—	P103	—	CTS_RTS0/SS0/ SSLB0/CTX0/QIO3/ SSILRCK0_B/ SSIFS0_B	GTIOC2A/GTOWUP	—
46	F2	34	D1	22	—	P102	—	SCK0/RSPCKB/ CRX0/QIO0/ SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	F1	35	E1	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB/QIO1	GTIOC5A/ GTETRGB/AGTEE0	—
48	G1	36	F1	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB/QSPCLK/ AUDIO_CLK	GTIOC5B/ GTETRGA/AGTIO0	—
49	H1	37	—	—	CACREF	P500	—	QSPCLK	GTIU/AGTOA0	AN016
50	G2	—	—	—	—	P008	IRQ12-DS	—	—	AN008
51	H2	—	—	—	—	P006	IRQ11-DS	—	—	AN006
52	G3	38	—	—	—	P015	IRQ13	—	—	AN013/DA1
53	H3	39	E2	25	—	P014	—	—	—	AN012/DA0
54	H4	40	—	—	—	P013	—	—	—	AN011
55	H5	41	F2	26	—	P003	—	—	—	AN007
56	F4	42	E3	27	VREFH/AVCC0	—	—	—	—	—
57	F5	43	E4	28	VREFL/AVSS0	—	—	—	—	—
58	G5	44	F4	29	VREFL0	—	—	—	—	—
59	G4	45	F3	30	VREFH0	—	—	—	—	—
60	H6	—	—	—	—	P005	IRQ10-DS	—	—	AN005
61	G6	—	—	—	—	P004	IRQ9-DS	—	—	AN004
62	G7	46	—	31	—	P002	IRQ8-DS	—	—	AN002
63	H7	47	F5	32	—	P001	IRQ7-DS	—	—	AN001
64	H8	48	F6	1	—	P000	IRQ6-DS	—	—	AN000

Note: 多个引脚名称添加了_a、_B、_C和_D后缀。在分配功能时可以忽略后缀。
注1。XCIN不能在QFN32中使用。XCIN必须通过电阻（下拉）连接到VSS。

2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = 2.7 to 3.6
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

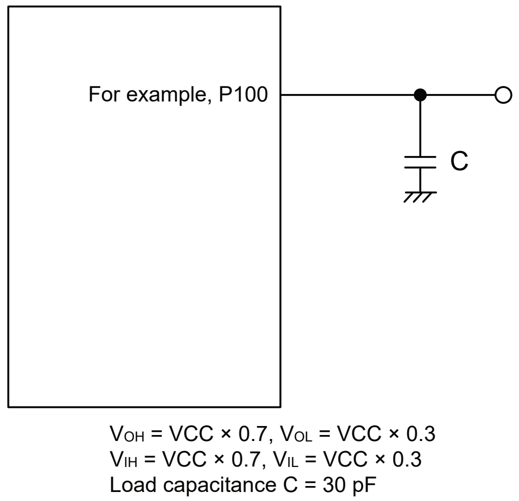


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB[*2]	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports[*1])	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports[*1])	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0[*2]	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature[*3 *4 *5]	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P100, P101, P205, P206, P400, P401 and P407 to P411 are 5 V tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section x.x. Part Numbering.

2. 电气特性

支持的外围功能和引脚因产品名称而异。

除非另有说明，否则MCU的电气特性是在以下条件下定义的:

- VCC = AVCC0 = VCC_USB = 2.7 to 3.6
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$

图2.1显示了时序条件。

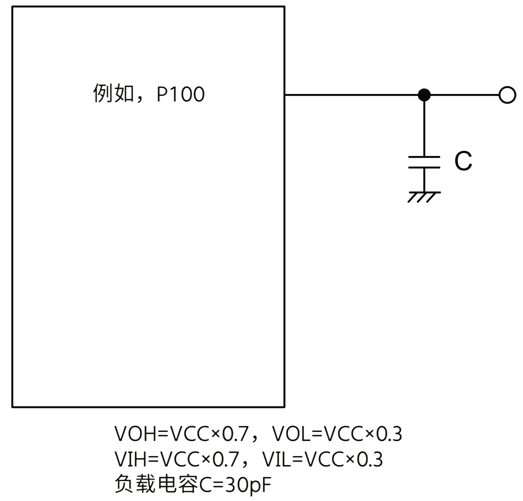


Figure 2.1 输入或输出定时测量条件

所提供的每个外设的定时规范的推荐测量条件是为了最佳的外设操作。确保调整每个引脚的驾驶能力，以满足您的条件。

2.1 绝对最大额定值

Table 2.1 绝对最大额定值

Parameter	Symbol	Value	Unit
电源电压	VCC, VCC_USB[*2]	–0.3 to +4.0	V
输入电压(5v容差端口除外*1)	V_{in}	–0.3 to VCC + 0.3	V
输入电压(5v容差端口*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
参考电源电压	VREFH/VREFH0	–0.3 to VCC + 0.3	V
模拟电源电压	AVCC0[*2]	–0.3 to +4.0	V
模拟输入电压	V_{AN}	–0.3 to AVCC0 + 0.3	V
操作温度*3*4*5	T_{opr}	–40 to +105	°C
储存温度	T_{stg}	–55 to +125	°C

注1。端口P100、P101、P205、P206、P400、P401和P407至P411具有5V容限。
注2。将AVCC0和VCC_USB连接到VCC。
注3。请参阅第2.2.1节。TjTa定义。
注4。有关Ta=+85°C至+105°C时降额操作的信息，请联系瑞萨电子销售办公室。降额是系统地减少负载以提高可靠性。注5。工作温度的上限为+85°C或+105°C，具体取决于产品。有关详细信息，请参阅第x.x部分

Numbering.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB is not used	2.7	—	3.6	V
		When USB is used	3.0	—	3.6	V
	VSS		—	0	—	V
USB power supply voltages	VCC_USB		—	VCC	—	V
	VSS_USB		—	0	—	V
Analog power supply voltages	AVCC0[*1]		—	VCC	—	V
	AVSS0		—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/ VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105[*1]		

Note: Make sure that $T_j = T_a + θja$ × total power consumption (W), where total power consumption = (VCC - V_{OH}) × $ΣI_{OH}$ + V_{OL} × $ΣI_{OL}$ + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. If the part number shows the operation temperature to 85°C, then Tj max is 105°C, otherwise, 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Table 2.2 建议操作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC	不使用USB时	2.7	—	3.6	V
		使用USB时	3.0	—	3.6	V
	VSS		—	0	—	V
USB电源电压	VCC_USB		—	VCC	—	V
	VSS_USB		—	0	—	V
模拟电源电压	AVCC0[*1]		—	VCC	—	V
	AVSS0		—	0	—	V

注1。将AVCC0连接到VCC。当AD转换器和Da转换器不使用时，不要离开AVCC0，VREFHVREFH0 AVSS0，和VREFLVREFL0引脚打开。将AVCC0和VREFHVREFH0引脚连接到VCC，以及AVSS0和VREFL VREFL0引脚分别到VSS。

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105[*1]		

Note: 确保Tj=Ta+θja×总功耗（W），其中总功耗=（VCCVOH）×ΣIOH+VOL×ΣIOL+ I_{CC}max × VCC.

注1。工作温度的上限为85°C或105°C，具体取决于产品。如果零件编号显示工作温度为85°C，则Tjmax为105°C，否则为125°C。

2.2.2 IOVIH VIL

Table 2.4 IOVIH VIL(1的2)

Parameter			Symbol	Min	Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外围功能引脚	EXTAL（外部时钟输入），SPI（RSPCK除外）	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports[*1 *5]	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins[*2]	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports[*3 *5]	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		Other input pins[*4]	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P100, P101, P205, P206, P400, P401, P407 to P411 (total 12 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P100, P101, P205, P206, P400, P401, P407 to P411 (total 11pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

Table 2.4 IOVIH VIL(2的2)

Parameter			Symbol	Min	Typ	Max	Unit
施密特触发输入电压	外围功能引脚	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports[*1 *5]	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		其他输入引脚*2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports[*3 *5]	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		其他输入引脚*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

注1。与P100、P101、P205、P206、P400、P401、P407到P411相关联的RES和外围功能引脚（共12个引脚）。
注2。除表中已描述的外围功能引脚外的所有输入引脚。
注3。P100 P101 P205 P206 P400 P401 P407至P411(共11pins)。
注4。除表中已描述的端口外的所有输入引脚。
注5。当VCC小于2.7v时，5个v容端口的输入电压应小于3.6v，否则可能会发生击穿，因为5个v容端口是电气控制的，以免违反击穿电压
。

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
Permissible output current (max value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

2.2.3 我哦，我哦，我哦

Table 2.5 IOIOH IOL(1of2)

Parameter			Symbol	最小Typ最大单位			
允许输出电流（每个引脚的平均值）	I3C pins	IIC标准模式*4	I_{OL}	—	—	3.0	mA
		IIC快速模式*4	I_{OL}	—	—	6.0	mA
		IIC快速模式加*4	I_{OL}	—	—	20	mA
		IIC高速模式*4	I_{OL}	—	—	3.0	mA
	端口P004至P006、P008、P013至P015、P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	端口P205，P206，P407到P411（共7个引脚）	低驱动*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中路*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	其他输出引脚*5	低驱动*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中路*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高驱动器*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
允许输出电流（每引脚最大值）	I3C pins	IIC标准模式*4	I_{OL}	—	—	3.0	mA
		IIC快速模式*4	I_{OL}	—	—	6.0	mA
		IIC快速模式加*4	I_{OL}	—	—	20	mA
		IIC高速模式*4	I_{OL}	—	—	3.0	mA
	端口P004至P006、P008、P013至P015、P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	端口P205，P206，P407到P411（共7个引脚）	低驱动*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		中路*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	其他输出引脚*5	低驱动*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		中路*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		高驱动器*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	$\Sigma I_{OH (max)}$	—	—	–80	mA
		$\Sigma I_{OL (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. SCL0_D, SDA0_D (total 2 pins). This is the value when IIC function is selected.
Note 5. Except for P000 to P003, P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	I3C*1	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2	V_{OH}	VCC - 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0)
		V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
		V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.HSME = 1)
		V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0)
	Ports P205, P206, P407 to P411(total 7 pins)*3	V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC - 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\lvert I_{in}\rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000 to P003, P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports (except for port P100, P101)	$\lvert I_{TSI}\rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	5 V-tolerant ports (P100, P101)		—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P000 to P003, P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to P5, P8 (except for ports P000 to P003)	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V

Table 2.5 IOIOH IOL(2的2)

Parameter		Symbol	最小	Typ	最大	单位
允许输出电流（所有引脚总数的最大值）	所有输出引脚的最大值	$\Sigma I_{OH (max)}$	—	—	–80	mA
		$\Sigma I_{OL (max)}$	—	—	80	mA

注1。这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。选择的驾驶能力保留在深度软件待机模式下。注2。这是在PmnPFS寄存器的端口驱动能力位中选择中间驱动能力时的值。选择的驾驶能力保留在深度软件待机模式下。注3。这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。选择的驾驶能力保留在深度软件待机模式下。注4。SCL0_D，SDA0_D（共2个引脚）。这是选择IIC函数时的值。

注5。除了P000到P003，P200，这是一个输入端口。

Caution: 为了保护MCU的可靠性，输出电流值不应超过此表中的值。
平均输出电流表示在100μs期间测量的电流平均值。

2.2.4 IOVOH、VOL等特性

Table 2.6 IOVOH VOL 和其他特性(1的2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出电压	I3C*1	V_{OL}	—	—	0.4	V	IOL=3.0mA
		V_{OL}	—	—	0.6		IOL=6.0mA
	I3C*2	V_{OH}	VCC - 0.27	—	—		IOH=3.0mA(PRTS.PRTMD=0)
		V_{OL}	—	—	0.4		IOL=15.0mA(PRTS.PRTMD=1 BFCTL.FMPE = 1)
		V_{OL}	—	0.4	—		IOL=20.0mA(PRTS.PRTMD=1 BFCTL.FMPE = 1)
		V_{OL}	—	—	0.4		IOL=3.0mA(PRTS.PRTMD=1 BFCTL.HSME = 1)
		V_{OL}	—	—	0.27		IOL=3.0mA(PRTS.PRTMD=0)
	端口P205，P206，P407到P411（共7个引脚）*3	V_{OH}	VCC - 1.0	—	—		IOH=–20mA VCC=3.3V
		V_{OL}	—	—	1.0		IOL=20mAV CC=3.3V
	其他输出引脚	V_{OH}	VCC - 0.5	—	—		IOH=–1.0mA
		V_{OL}	—	—	0.5		IOL=1.0mA
输入漏电流	RES	$\lvert I_{in}\rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	端口P000至P003，P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关断状态）	5个v容端口（P100、P101端口除外）	$\lvert I_{TSI}\rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	5 V-tolerant ports (P100, P101)		—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	其他端口（P000至P003端口除外 P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0到P5，P8（端口P000到P003除外）	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up current serving as the SCL current source	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P003, P014, P015,P814, P815	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Other input pins		—	—	8		

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, and SDA0_C (total 6 pins).
Note 2. I3C_SCL/SCL0_D, I3C_SDA/SDA0_D (total 2 pins).
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. I3C_SCL/SCL0_D (1 pin). This is the value when IIC high speed mode is selected.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	65	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®*5 *6			—	16	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		—	18.6	—		
			All peripheral clocks disabled, while (1) code executing from flash*5 *6		—	14.7	—		
		Sleep mode*5 *6			—	7.5	43		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode*5 *9				—	1.8	—		ICLK = 1 MHz
	Subosc-speed mode*5 *10				—	1.6	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	35		—
			SNZCR.RXDREQEN = 0		—	1.4	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			—	16	96	μA	—
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		—	11	25.6		—
			Power-on reset circuit low power function enabled		—	4.2	20.4		—
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.5	—		—
			When a crystal oscillator for low clock loads is in use		—	1.0	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.4	—		—
	Inrush current on returning from deep software standby mode		Inrush current*7	I_{RUSH}	—	160	—	mA	—
			Energy of inrush current*7	E_{RUSH}	—	1.0	—	μC	—

Table 2.6 IOVOH VOL 和其他特性(2的2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上拉电流作为SCL电流源	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin=0.3×VCC至0.7×VCC
输入电容	Ports P003, P014, P015,P814, P815	C_{in}	—	—	16	pF	Vbias = 0 V Vamp=20mVf =1MHzTa=25° C
	其他输入引脚		—	—	8		

注1。SCL0_A，SCL0_B，SCL0_C，SDA0_A，SDA0_B和SDA0_C（总共6个引脚）。
Note 2. I3C_SCL/SCL0_D, I3C_SDA/SDA0_D (total 2 pins).
注3。这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。选择的驾驶能力保留在深度软件待机模式下。注4。I3C_SCLSCL 0_D(1引脚)。这是选择iic高速模式时的值。

2.2.5 工作和待机电流

Table 2.7 工作和待机电流(1/2)

Parameter				Symbol	Min	Typ	最大单元测试条件		
电源电流*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	65	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®*5 *6			—	16	—		
		正常模式	所有外围时钟启用，而（1）代码从flash*4执行		—	18.6	—		
			所有外设时钟禁用，而（1）代码从flash*5*6执行		—	14.7	—		
		睡眠模式*5*6			—	7.5	43		
		BGO运行期间增加	数据闪存PE		—	6	—		
			代码闪存PE		—	8	—		
	Low-speed mode*5 *9				—	1.8	—		ICLK = 1 MHz
	Subosc-speed mode*5 *10				—	1.6	—		ICLK = 32.768 kHz
	软件待机模式		SNZCR.RXDREQEN = 1		—	—	35		—
			SNZCR.RXDREQEN = 0		—	1.4	—		—
	Deep 软件待机模式	为备用SRAM和USB恢复检测单元供电			—	16	96	μA	—
		未向SRAM或USB恢复检测单元供电	上电复位电路低功耗功能禁用		—	11	25.6		—
			上电复位电路低功耗功能使能		—	4.2	20.4		—
		Rtc和AGT运行时增加	当低速片上振荡器（LOCO）在使用		—	4.5	—		—
			当用于低时钟负载的晶体振荡器在使用时		—	1.0	—		—
			当用于标准时钟负载的晶体振荡器在使用时		—	1.4	—		—
	从深度软件待机模式返回时的浪涌电流		Inrush current*7	I_{RUSH}	—	160	—	mA	—
			涌流能量*7	E_{RUSH}	—	1.0	—	μC	—

Table 2.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion		AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	Temperature sensor			—	0.1	0.2	mA	—
	During D/A conversion (per unit)	Without AMP output		—	0.2	0.6	mA	—
		With AMP output		—	0.7	1.5	mA	—
	Waiting for A/D, D/A conversion (all units)			—	0.5	1.0	mA	—
	ADC12, DAC12 in standby modes (all units)*8			—	0.4	6	μA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)		AI_{REFH0}	—	70	120	μA	—
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	μA	—
	ADC12 in standby modes (unit 0)			—	0.07	0.5	μA	—
USB operating current	Full speed	USB	$I_{CCUSBFS}$	—	4.0	10.0	mA	VCC_USB

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.
I_{CC} Max. = 0.14 × f + 37 (max. operation in high-speed mode)
I_{CC} Typ. = 0.06 × f + 2.75 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.1× f + 1.71 (low-speed mode)
I_{CC} Max. = 0.03 × f + 37 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 7. Reference value
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) is in the module-stop state.
Note 9. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 10. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.

Table 2.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark*2		I_{CC}	80	μA/MHz	ICLK = 200 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.125 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2		74		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2		66		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Table 2.7 工作和待机电流（2/2）

Parameter			Symbol	Min	Typ	最大单元测试条件		
模拟电源电流	在12位AD转换期间		AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	温度传感器			—	0.1	0.2	mA	—
	在Da转换期间（每单位）	没有放大器输出		—	0.2	0.6	mA	—
		带放大器输出		—	0.7	1.5	mA	—
	等待一个D，Da转换（所有单位）			—	0.5	1.0	mA	—
	Adc12，dac12在待机模式下（所有单元）*8			—	0.4	6	μA	—
参考电源电流(VREFH0)	在12位AD转换（单位0）		AI_{REFH0}	—	70	120	μA	—
	等待12位AD转换（单元0）			—	0.07	0.5	μA	—
	待机模式下的ADC12(单元0)			—	0.07	0.5	μA	—
USB工作电流	全速前进	USB	$I_{CCUSBFS}$	—	4.0	10.0	mA	VCC_USB

注1。电源电流值是所有输出引脚卸载和所有输入上拉MOSs在关闭状态。
注2。用提供给外围功能的时钟测量。这不包括BGO操作。
注3。ICC取决于f(ICLK)如下。
我CC最大.=0.14×f+37（最大。高速模式下操作）
我抄送Typ。=0.06×f+2.75(高速模式下正常工作，所有外设时钟禁用)
I_{CC} Typ. = 0.1× f + 1.71 (low-speed mode)
I_{CC} Max. = 0.03 × f + 37 (sleep mode)
注4。这不包括BGO操作。
注5。在这种状态下，时钟信号到外围设备的供应停止。这不包括BGO操作。
注6。FCLK、PCLKA、PCLKB、PCLKC和PCLKD被设置为除以64(3.125MHz)。
注7。参考价值
注8。当MCU处于软件待机模式或MSTPCRD时.MSTPD16(12位AD转换器0模块停止位)处于模块停止状态。注9。FCLK、PCLKA、PCLKB、PCLKC和PCLKD被设置为除以64(15.6kHz)。

注10。PCLKA、PCLKB、PCLKC和PCLKD设置为除以64(512Hz)。FCLK与ICLK的频率相同。

Table 2.8 Coremark和正常模式电流

Parameter			Symbol	Typ	Unit	测试条件
电源电流*1	Coremark*2		I_{CC}	80	μA/MHz	ICLK = 200 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.125 MHz
	正常模式	所有外设时钟禁用，缓存打开，而（1）代码从flash*2执行		74		
		所有外设时钟禁用，缓存关闭，而（1）代码从flash*2执行		66		

注1。电源电流值是所有输出引脚卸载和所有输入上拉MOSs在关闭状态。
注2。在这种状态下，时钟信号到外围设备的供应停止。这不包括BGO操作。

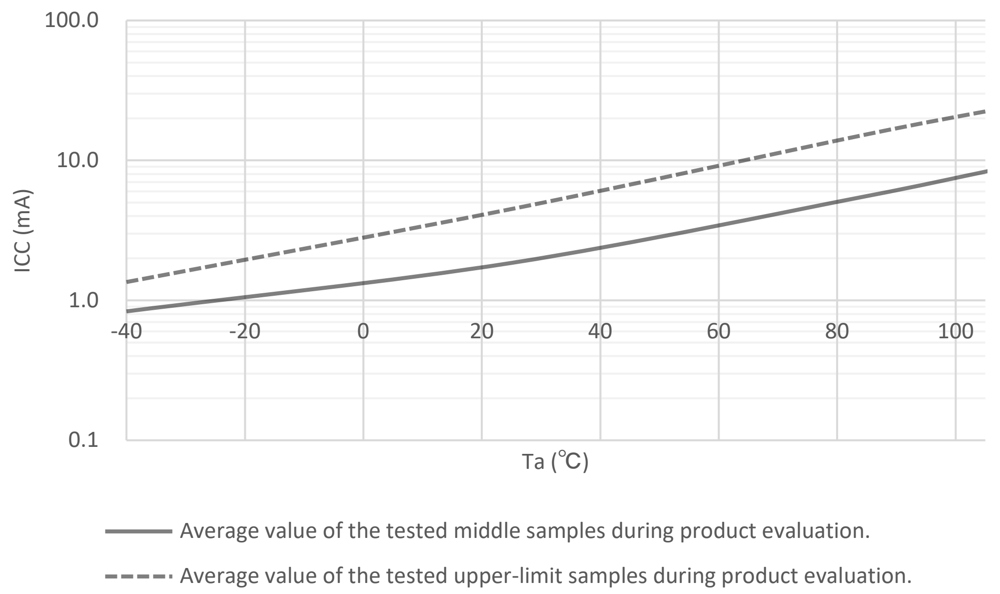


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

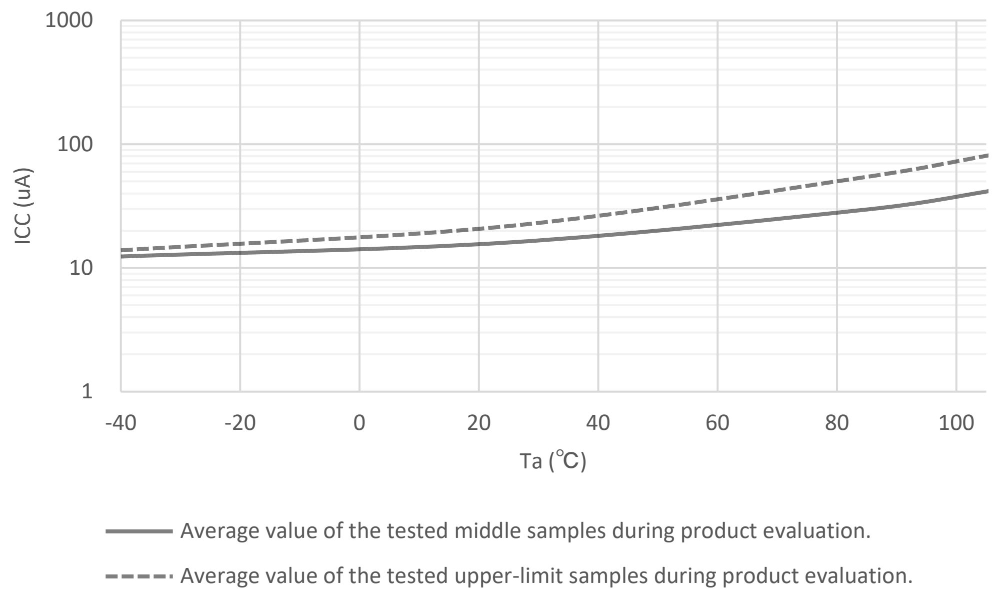


Figure 2.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

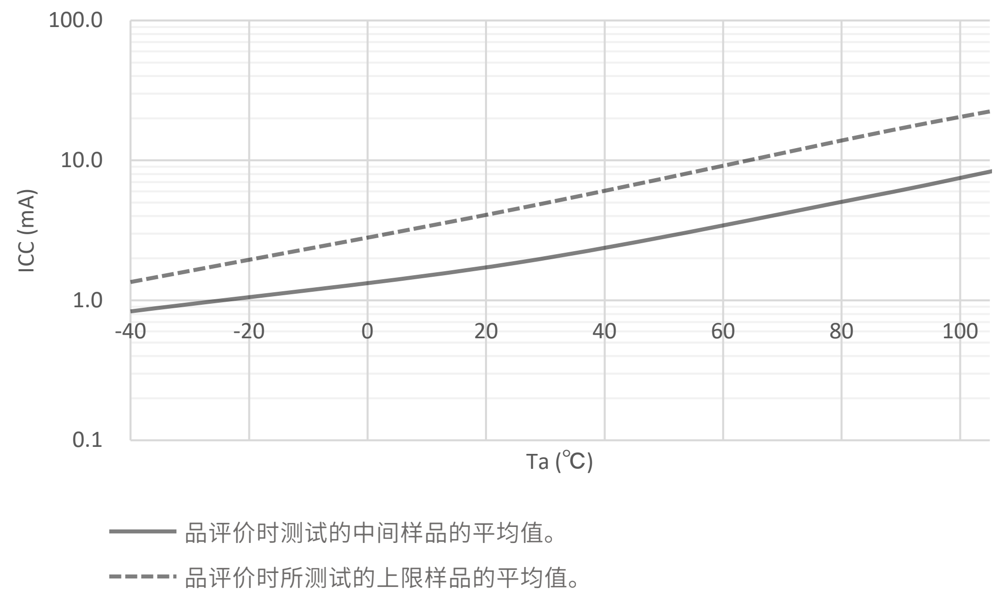


Figure 2.2 软件待机模式下的温度依赖性（参考数据）

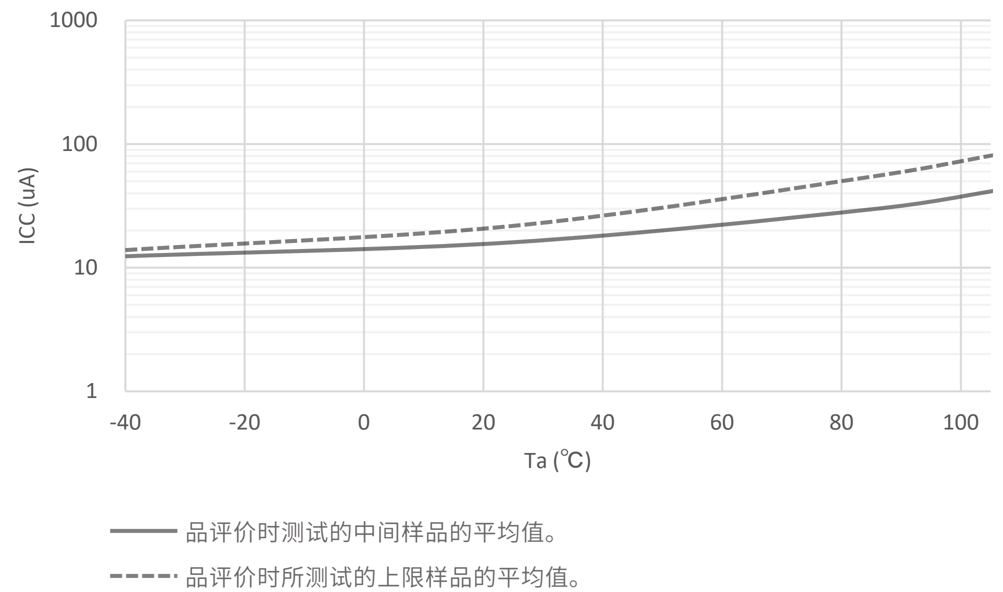


Figure 2.3 深度软件待机模式下的温度依赖性，为待机SRAM和USB恢复检测单元供电（参考数据）

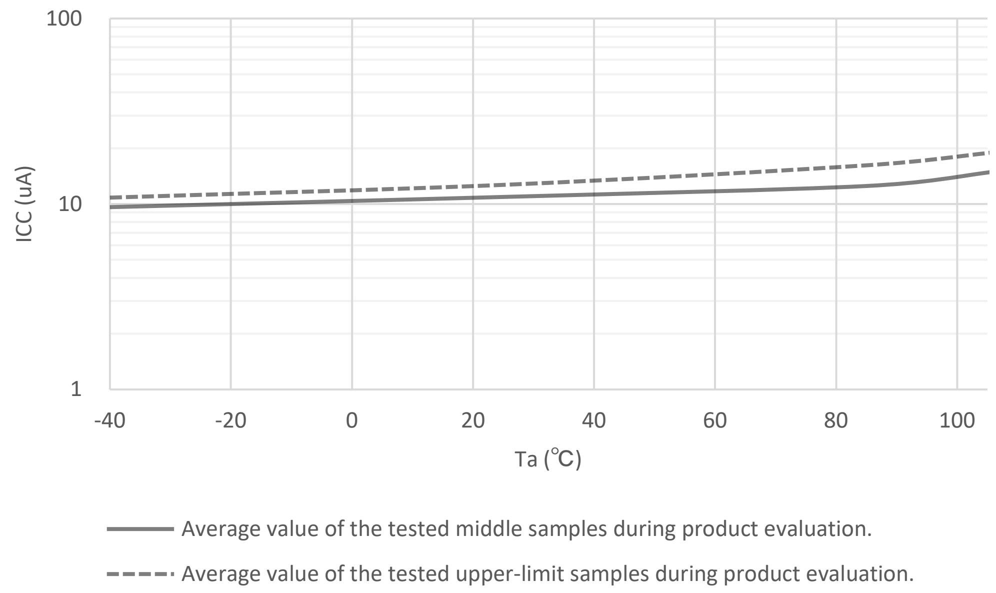


Figure 2.4 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)**

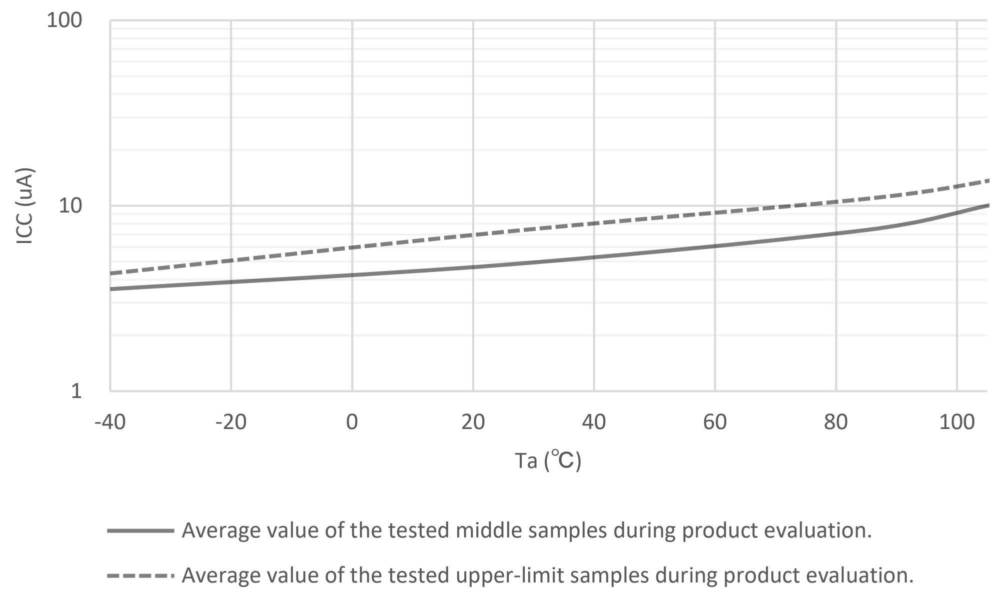


Figure 2.5 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)**

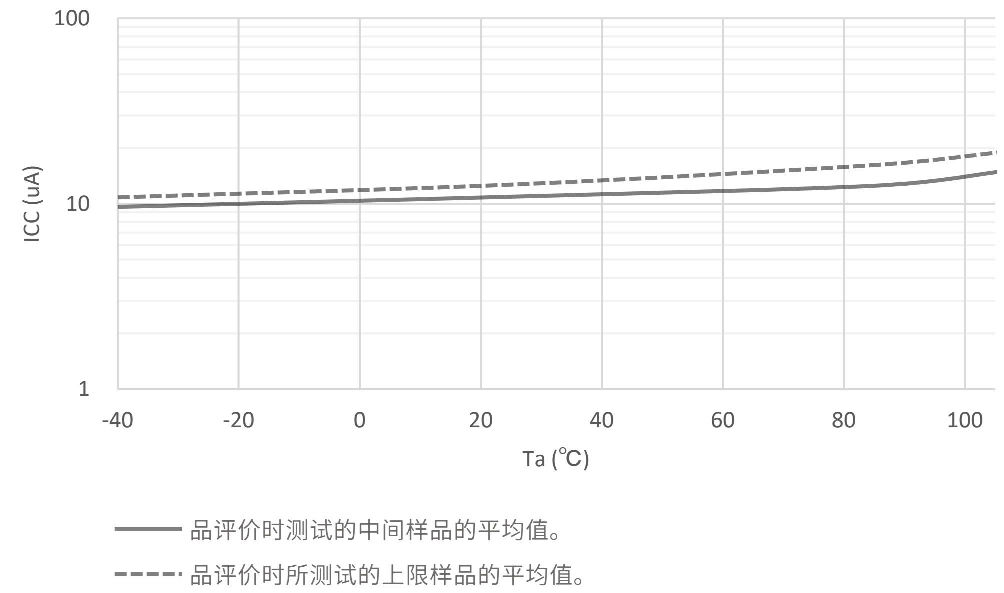


Figure 2.4 深度软件待机模式下的温度依赖性，未向SRAM或USB恢复检测单元供电，上电复位电路低功耗功能禁用（参考数据）

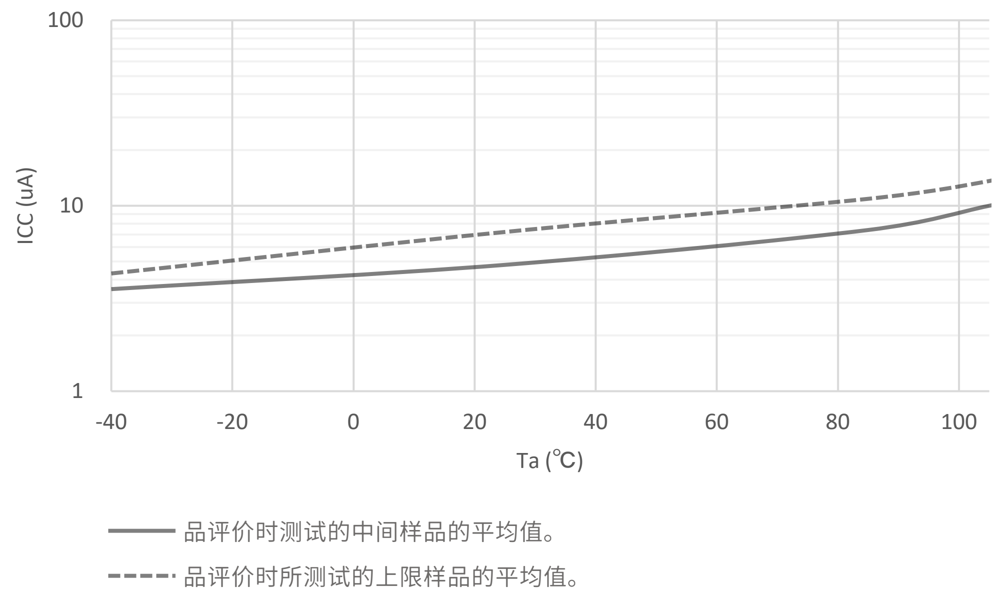


Figure 2.5 温度依赖性在深软件待机模式下，电源不提供给SRAM或USB恢复检测单元，上电复位电路低功耗功能启用（参考数据）

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI/USB boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

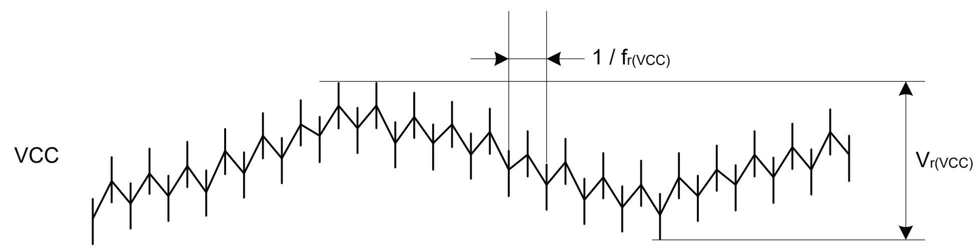


Figure 2.6 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 2.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)

2.2.6 VCC上升和下降梯度和纹波频率

Table 2.9 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	—	20	ms/V	—
	启动时启用电压监视器0复位		0.0084	—	—		—
	SCIUSB启动模式*1		0.0084	—	20		—
VCC下降梯度		SfVCC	0.0084	—	—	ms/V	—

注1。在引导模式下，无论OFS1的值如何，电压监视器0的复位都被禁用。LVDAS位。

Table 2.10 上升和下降梯度和纹波频率特性

纹波电压必须在VCC上限(3.6V)和下限(2.7V)之间的范围内满足允许的纹波频率fr(VCC V)。当VCC变化超过VCC±10%时，必须满足dVCC的允许电压变化上升和下降梯度dt。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
允许电压变化上升和下降梯度	dt/dVCC	1.0	—	—	ms/V	当VCC变化超过VCC ±10%

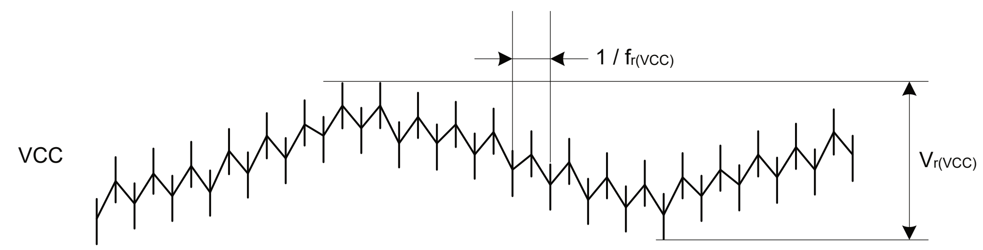


Figure 2.6 纹波波形

2.2.7 热特性

结温（Tj）的最大值不得超过"第2.2.1节的值。TjTa定义"。

Tj由以下任一方程式计算。

●Tj=Ta+θja×总功耗

●Tj=Tt+△Jt×总功耗

- Tj:结温(°C)
- Ta:环境温度(°C)
- Tt:顶部中心外壳温度(°C)
- θja:"结"到"环境"的热阻(°Cw)
- Jt:"结"至"顶部中心壳"的热阻(°Cw)

●总功耗=电压×(漏电流+动态电流)

- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 2.11.

Table 2.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	32-pin QFN (PWQN0032KE-A)	θja	36.8	°C/W	JESD 51-2 and 51-7 compliant
	48-pin QFN (PWQN0048KC-A)		29.7		
	64-pin LQFP (PLQP0064KB-C)		41.3		
	36-pin BGA (PLBG0036KA-A)		53.7		
	64-pin BGA (PLBG0064KB-A)		51.6		
	32-pin QFN (PWQN0032KE-A)	Ψjt	0.36	°C/W	JESD 51-2 and 51-7 compliant
	48-pin QFN (PWQN0048KC-A)		0.27		
	64-pin LQFP (PLQP0064KB-C)		1.39		
	36-pin BGA (PLBG0036KA-A)		1.70		
	64-pin BGA (PLBG0064KB-A)		1.70		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.2.7.1 Calculation guide of I_{CC}max

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit (1 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60

●IO的漏电流=Σ(IOL×VOL)电压+Σ(IOH×VCC-VOH)电压

●IO的动态电流=ΣIO(cin+c负载)×IO开关频率×电压

-Cin：输入电容

-C负载：输出电容

关于θja和Ψjt，参见表2.11。

Table 2.11 热阻

Parameter	Package	Symbol	Value*1	Unit	测试条件
热阻	32-pin QFN (PWQN0032KE-A)	θja	36.8	°C/W	符合JESD51-2和51-7
	48-pin QFN (PWQN0048KC-A)		29.7		
	64-pin LQFP (PLQP0064KB-C)		41.3		
	36-pin BGA (PLBG0036KA-A)		53.7		
	64-pin BGA (PLBG0064KB-A)		51.6		
	32-pin QFN (PWQN0032KE-A)	Ψjt	0.36	°C/W	符合JESD51-2和51-7
	48-pin QFN (PWQN0048KC-A)		0.27		
	64-pin LQFP (PLQP0064KB-C)		1.39		
	36-pin BGA (PLBG0036KA-A)		1.70		
	64-pin BGA (PLBG0064KB-A)		1.70		

注1。这些值是使用4层板时的参考值。热阻取决于板的层数或尺寸。有关详细信息，请参阅JEDEC标准。

2.2.7.1 ICCmax的计算指南

表2.12显示了每个单元的功耗。

Table 2.12 每个单元的耗电量(1/2)

动态电流泄漏电流	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
漏电流	Analog	LDO和泄漏*2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60

Table 2.12 Power consumption of each unit (2 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	200	56.885	11.38
	Peripheral Unit	Timer	GPT16 (6ch)*4	100	8.480	0.85
			POEG (4 Groups)*4	50	1.171	0.06
			AGT (2ch)*4	50	3.967	0.20
			RTC	50	2.711	0.27
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		Communication interfaces	USBFS	50	4.969	0.25
			SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			CEC	100	0.213	0.01
			SPI (2ch)*4	100	5.739	0.57
			QSPI	100	2.379	0.24
			SSIE	50	2.831	0.14
		Analog	ADC12	100	2.229	0.22
			DAC12 (2ch)*4	100	0.602	0.06
			TSN	50	0.277	0.01
		Event link	ELC	50	0.562	0.06
		Security	TRNG	100	0.013	1.27
		Data processing	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		System	CAC	50	0.777	0.04
		DMA	DMAC	200	4.450	0.89
			DTC	200	4.382	0.88

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 shows the outline of operation for each unit.

Table 2.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
RTC	RTC is operating with LOCO.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.

Table 2.12 每个单元的耗电量(2/2)

动态电流泄漏电流	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
动态电流	CPU	操作与 闪存和SRAM	Coremark	200	56.885	11.38
	外围设备	Timer	GPT16 (6ch)*4	100	8.480	0.85
			POEG (4 Groups)*4	50	1.171	0.06
			AGT (2ch)*4	50	3.967	0.20
			RTC	50	2.711	0.27
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		通信接口	USBFS	50	4.969	0.25
			SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			CEC	100	0.213	0.01
			SPI (2ch)*4	100	5.739	0.57
			QSPI	100	2.379	0.24
			SSIE	50	2.831	0.14
		Analog	ADC12	100	2.229	0.22
			DAC12 (2ch)*4	100	0.602	0.06
			TSN	50	0.277	0.01
		活动连结	ELC	50	0.562	0.06
		Security	TRNG	100	0.013	1.27
		资料处理	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		System	CAC	50	0.777	0.04
		DMA	DMAC	200	4.450	0.89
			DTC	200	4.382	0.88

注1。这些值是由设计保证的。
注2。LDO和Leak是内部稳压器的电流和MCU的泄漏电流。
根据Ta的温度来选择。
注3。Δ(Tj-Ta)=20°c被认为是测量电流。
注4。要确定每个通道或单位的电流消耗，请将电流[mA]除以通道、组或单位的数量。

表2.13显示了每个单元的操作概要。

Table 2.13 每个单位的运作大纲(1/2)

Peripheral	运作大纲
GPT	操作模式设置为锯波PWM模式. GPT正在使用PCLKD操作。
POEG	只有清除模块停止位。
AGT	AGT正在使用PCLKB操作。
RTC	RTC正在使用LOCO进行操作。
WDT	WDT正在使用PCLKB操作。
IWDT	IWDT正在使用IWDTCLK操作。

Table 2.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
USBFS	Transfer types is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps).
SCI	SCI is transmitting data in clock synchronous mode.
I3C	Communication format is set to I3C-bus format. I3C is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
QSPI	QSPI is issuing Fast Read Quad I/O Instruction.
SSIE	Communication mode is set to Master. System word length is set to 32 bits. Data word length is set to 20 bits. SSIE is transmitting data using I2S format.
CEC	CEC operation clock is set to CECCLK. CEC is transmitting and receiving header block and data block.
ADC12	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
TSN	TSN is operating.
ELC	Only clear module stop bit.
TRNG	TRNG is executing built-in self test.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data addition mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.2.7.2 Example of T_j calculation

Assumption :

- Package 64-pin LQFP : θja = 41.3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3.5 V (VCC = AVCC0 = VCC_USB)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 8 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 6 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 8 Outputs
- C_{in} = 8 pF, 8 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 8 pins, Output frequency = 10 MHz

Table 2.13 每个单位的运作大纲(2/2)

Peripheral	运作大纲
USBFS	传输类型设置为批量传输。 USBFS正在使用全速传输（12Mbps）运行。
SCI	SCI以时钟同步模式传输数据。
I3C	通信格式设置为I3C-bus格式。 I3C正在主模式下传输数据。
CANFD	CANFD正在自检模式1中发送和接收数据。
SPI	SPI模式设置为SPI操作(4线方法). SPI主从模式设置为主模式。 SPI正在传输8位宽的数据。
QSPI	QSPI正在发出快速读取QuadIO指令。
SSIE	通信模式设置为Master。 系统字长设置为32位。 数据字长设置为20位。 SSIE正在使用I2S格式传输数据。
CEC	CEC操作时钟设置为CECCLK。 CEC正在发送和接收报头块和数据块。
ADC12	分辨率设置为12位精度。 数据寄存器设置为D转换的加值模式。 ADC12在连续扫描模式下转换模拟输入。
DAC12	DAC12正在输出转换结果，同时更新数据寄存器的值。
TSN	TSN正在运行。
ELC	只有清除模块停止位。
TRNG	TRNG正在执行内置自检。
CRC	CRC是使用32位CRC32-c多项式生成CRC码。
DOC	DOC在数据添加模式下运行。
CAC	测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。CAC正在测量时钟 频率精度。
DMAC	传输数据的位长设置为32位。 传送模式设置为块传送模式。 DMAC正在将数据从SRAM0传输到SRAM0。
DTC	传输数据的位长设置为32位。 传送模式设置为块传送模式。 DTC正在将数据从SRAM0传输到SRAM0。

2.2.7.2 Tj计算示例

Assumption :

- Package 64-pin LQFP : θja = 41.3 °C/W
- Ta = 100 °C
- ICCmax=40mA
- VCC = 3.5 V (VCC = AVCC0 = VCC_USB)
- IOH=1mA VOH=VCC-0.5V 8路输出
- IOL=20mA VOL=1.0V 6路输出
- IOL=1mA VOL=0.5V 8路输出
- Cin=8pF，8引脚，输入频率=10MHz
- C负载=30pF，8引脚，输出频率=10MHz

Leakage current of IO $= \Sigma (V_{OL} \times I_{OL}) / \text{Voltage} + \Sigma ((VCC - V_{OH}) \times I_{OH}) / \text{Voltage}$

= (20 mA × 1 V) × 6 / 3.5 V + (1 mA × 0.5 V) × 8 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 8 / 3.5 V

= 34.29 mA + 1.14 mA + 1.14 mA

= 36.6 mA

Dynamic current of IO $= \Sigma \text{IO} (C_{in} + C_{load}) \times \text{IO switching frequency} \times \text{Voltage}$

= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz) × 3.5 V

= 10.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)

= (40 mA × 3.5 V) + (36.6 mA + 10.6 mA) × 3.5 V

= 305 mW (0.305 W)

Tj = Ta + θja × Total power consumption

= 100 °C + 41.3 °C/W × 0.305 W

= 112.6 °C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	200	MHz
	Peripheral module clock (PCLKA)		—	—	100	
	Peripheral module clock (PCLKB)		—	—	50	
	Peripheral module clock (PCLKC)		—*2	—	50	
	Peripheral module clock (PCLKD)		—	—	100	
	Flash interface clock (FCLK)		—*1	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC) *2		—*2	—	1	
	Peripheral module clock (PCLKD)		—	—	1	
	Flash interface clock (FCLK)*1		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

IO的漏电流=Σ(VOL×IOL)电压+Σ((VCCVOH)×IOH)电压

= (20 mA × 1 V) × 6 / 3.5 V + (1 mA × 0.5 V) × 8 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 8 / 3.5 V

= 34.29 mA + 1.14 mA + 1.14 mA

= 36.6 mA

IO的动态电流 =ΣIO(cin+c负载)×IO开关频率×电压

= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz) × 3.5 V

= 10.6 mA

总耗电量 =电压×(漏电流+动态电流)

= (40 mA × 3.5 V) + (36.6 mA + 10.6 mA) × 3.5 V

= 305 mW (0.305 W)

Tj =Ta+θja×总功耗

= 100 °C + 41.3 °C/W × 0.305 W

= 112.6 °C

2.3 交流特性

2.3.1 Frequency

Table 2.14 高速模式下的操作频率值

Parameter		Symbol	Min	Typ	Max	Unit
操作频率	系统时钟(ICLK)	f	—	—	200	MHz
	外设模块时钟(PCLKA)		—	—	100	
	外设模块时钟(PCLKB)		—	—	50	
	外设模块时钟(PCLKC)		—*2	—	50	
	外设模块时钟(PCLKD)		—	—	100	
	闪存接口时钟(FCLK)		—*1	—	50	

注1。FCLK在编程或擦除闪存时必须以至少4MHz的频率运行。
注2。使用ADC12时，PCLKC频率必须至少为1MHz。

Table 2.15 低速模式下的工作频率值

Parameter		Symbol	Min	Typ	Max	Unit
操作频率	系统时钟(ICLK)	f	—	—	1	MHz
	外设模块时钟(PCLKA)		—	—	1	
	外设模块时钟(PCLKB)		—	—	1	
	外设模块时钟(PCLKC)*2		—*2	—	1	
	外设模块时钟(PCLKD)		—	—	1	
	Flash接口时钟(FCLK)*1		—	—	1	

注1。编程或擦除闪存在低速模式下被禁用。
注2。使用ADC12时，PCLKC频率必须设置为至少1MHz。

Table 2.16 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	29.4	—	36.1	kHz
	Peripheral module clock (PCLKA)		—	—	36.1	
	Peripheral module clock (PCLKB)		—	—	36.1	
	Peripheral module clock (PCLKC) *2		—	—	36.1	
	Peripheral module clock (PCLKD)		—	—	36.1	
	Flash interface clock (FCLK)*1		29.4	—	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.17 Clock timing except for sub-clock oscillator

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 2.7
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.8
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	μs	Figure 2.9
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	μs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	μs	—
HOCO period jitter		—	—	±85	—	ps	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency		f_{PLL}	120	—	240	MHz	—
PLL clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	μs	Figure 2.10
PLL period jitter	f_{PLL}	—	—	±100	—	ps	—
PLL long term jitter		—	—	±300	—	ps	Term: 1μs, 10μs

Table 2.16 低速模式下的工作频率值

Parameter		Symbol	Min	Typ	Max	Unit
操作频率	系统时钟(ICLK)	f	29.4	—	36.1	kHz
	外设模块时钟(PCLKA)		—	—	36.1	
	外设模块时钟(PCLKB)		—	—	36.1	
	外设模块时钟(PCLKC)*2		—	—	36.1	
	外设模块时钟(PCLKD)		—	—	36.1	
	Flash接口时钟(FCLK)*1		29.4	—	36.1	

注1。在高速模式下禁用对闪存的编程或擦除。
注2。不能使用ADC12。

2.3.2 时钟定时

Table 2.17 子时钟振荡器除外的时钟定时

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间		t_{EXcyc}	41.66	—	—	ns	Figure 2.7
外部时钟输入高脉冲宽度		t_{EXH}	15.83	—	—	ns	
外部时钟输入低脉冲宽度		t_{EXL}	15.83	—	—	ns	
外部时钟上升时间		t_{EXr}	—	—	5.0	ns	
EXTAL外部时钟下降时间		t_{EXf}	—	—	5.0	ns	
主时钟振荡器频率		f_{MAIN}	8	—	24	MHz	—
主时钟振荡稳定等待时间(晶振)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.8
LOCO时钟振荡频率		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO时钟振荡稳定等待时间		t_{LOCOWT}	—	—	60.4	μs	Figure 2.9
ILOCO时钟振荡频率		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO时钟振荡稳定等待时间		t_{MOCOWT}	—	—	15.0	μs	—
HOCO时钟振荡器振荡频率	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40≤Ta≤105°C子时钟频率精度为±50ppm。
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO时钟振荡稳定等待时间*2		t_{HOCOWT}	—	—	64.7	μs	—
HOCO周期抖动		—	—	±85	—	ps	—
FLL稳定等待时间		t_{FLLWT}	—	—	1.8	ms	—
PLL时钟频率		f_{PLL}	120	—	240	MHz	—
PLL时钟振荡稳定等待时间		t_{PLLWT}	—	—	174.9	μs	Figure 2.10
PLL周期抖动	f_{PLL}	—	—	±100	—	ps	—
PLL长期抖动		—	—	±300	—	ps	Term: 1μs, 10μs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.18 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.11

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

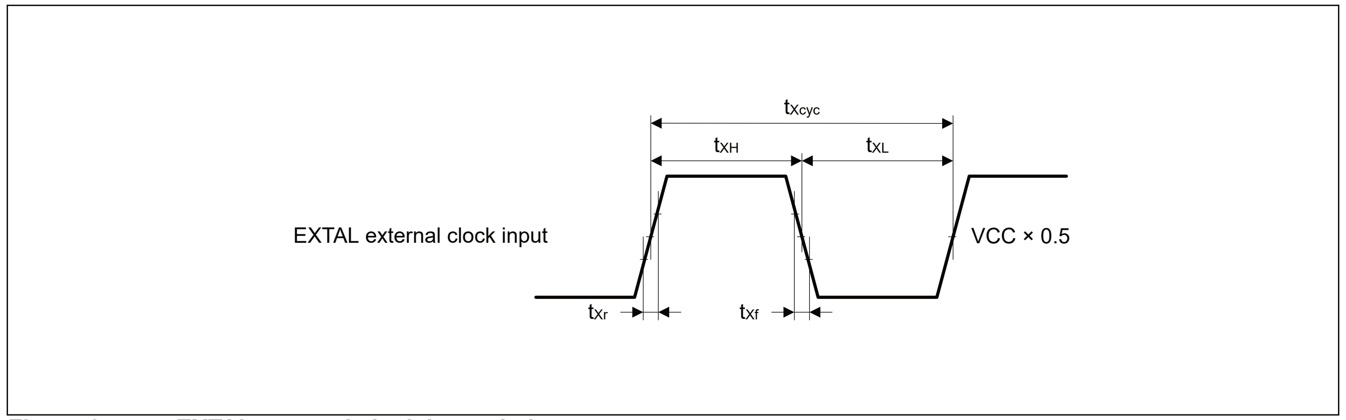


Figure 2.7 EXTAL external clock input timing

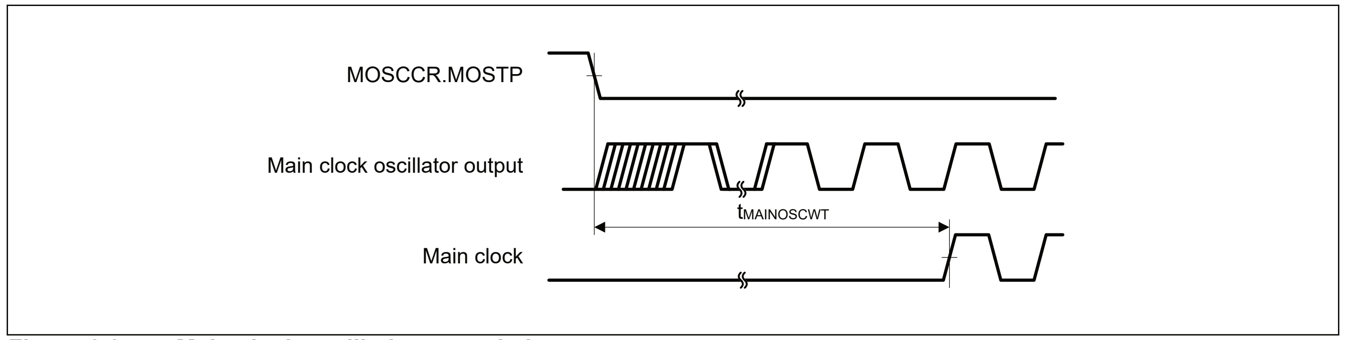


Figure 2.8 Main clock oscillation start timing

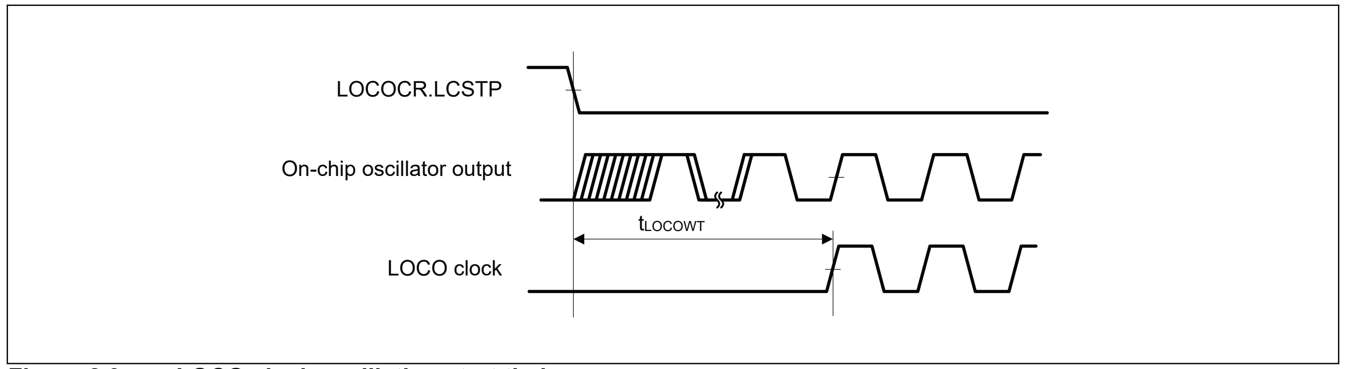


Figure 2.9 LOCO clock oscillation start timing

注1。在设置主时钟振荡器时，请振荡器制造商进行振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于建议值的值。在MOSCCR中更改设置后。MOSTP位开始主时钟操作，读取OSCSF。MOSCSF标志确认为1，然后开始使用主时钟振荡器。注2。这是从复位状态释放到hoco振荡频率（fHOCO）达到保证工作范围的时间。

Table 2.18 子时钟振荡器的时钟定时

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
子时钟振荡稳定等待时间	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.11

注1。在设置子时钟振荡器时，请振荡器制造商进行振荡评估，并将结果作为推荐的振荡稳定时间。在SOSCCR中更改设置后。SOSTP位开始子时钟操作，只有在子时钟振荡稳定时间过了足够裕量后才开始使用子时钟振荡器。建议使用两倍于所示值的值。

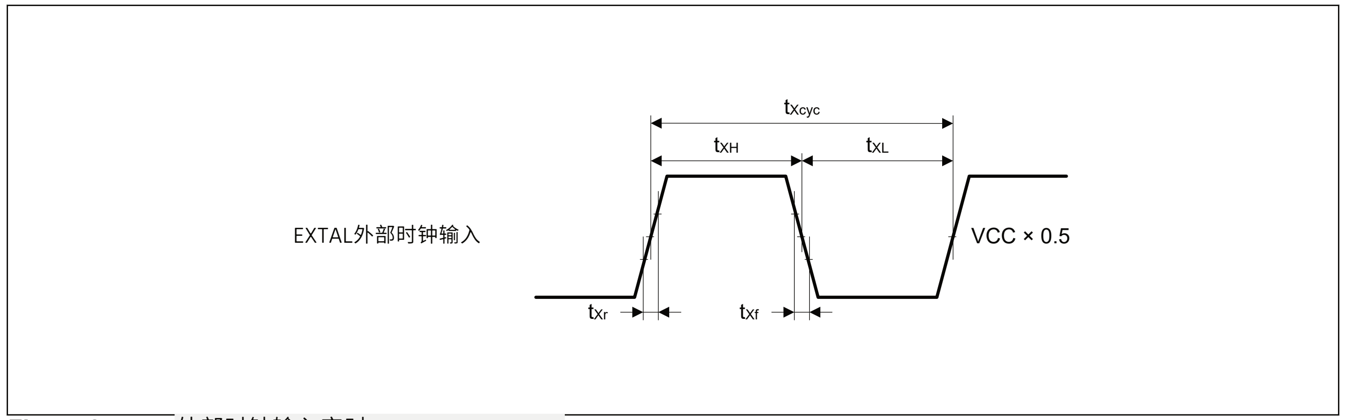


Figure 2.7 外部时钟输入定时

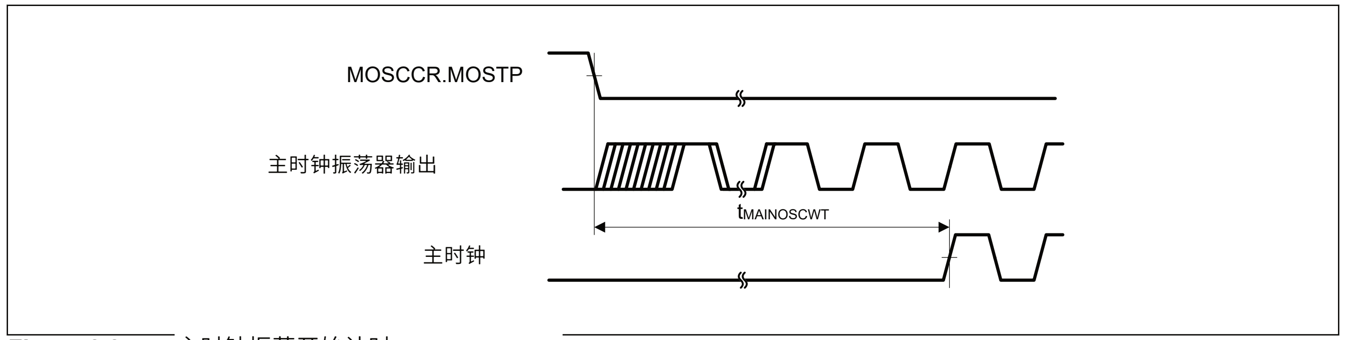


Figure 2.8 主时钟振荡开始计时

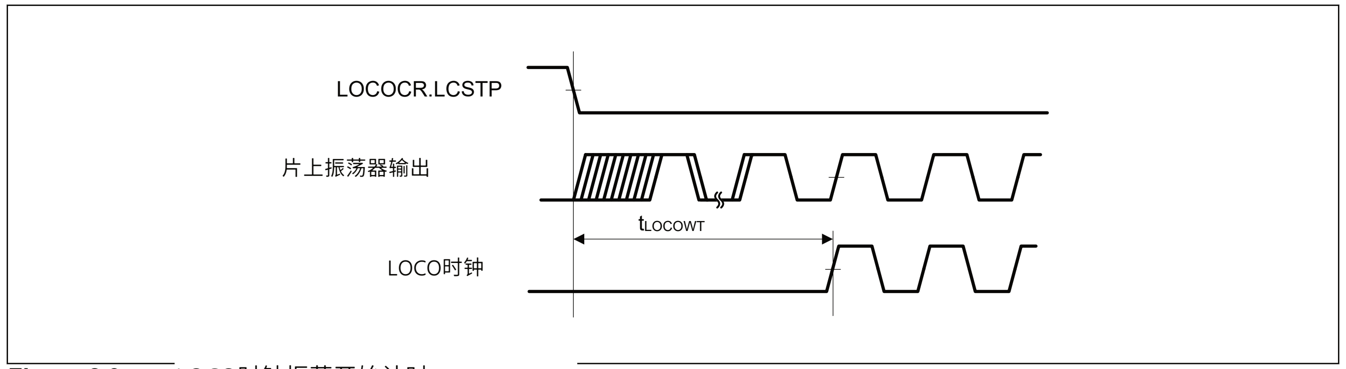


Figure 2.9 LOCO时钟振荡开始计时

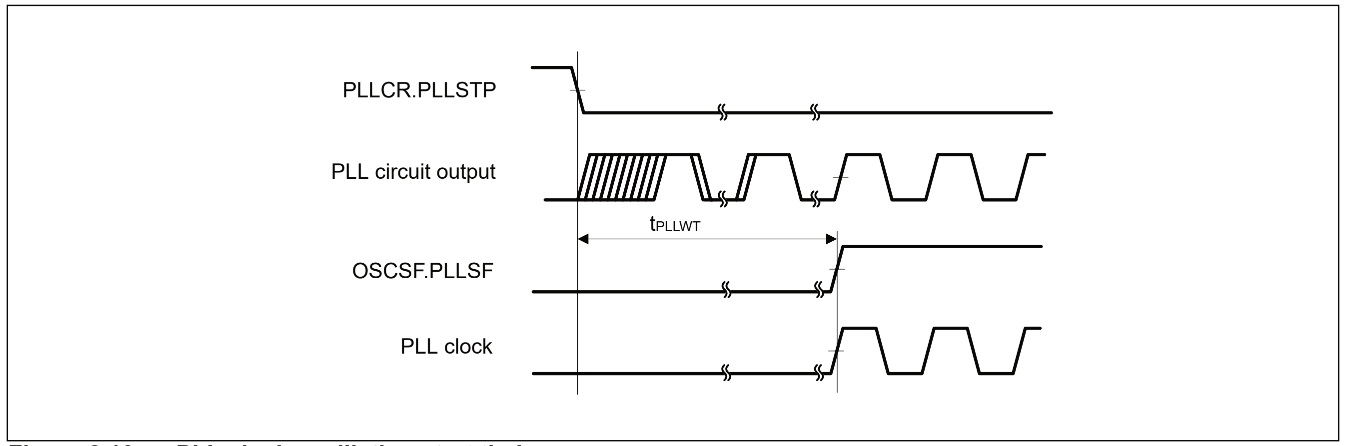


Figure 2.10 PLL clock oscillation start timing

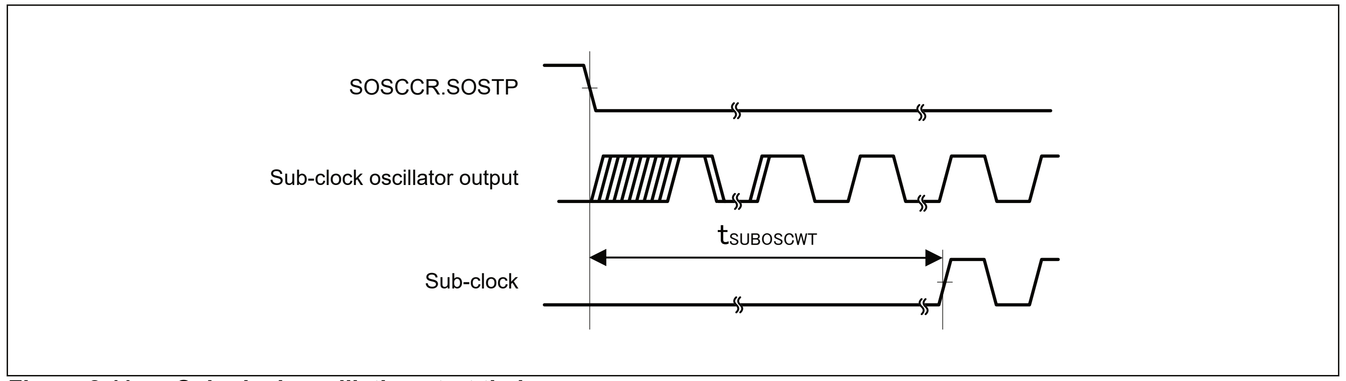


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.19 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.12
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.13
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	μs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	μs	Figure 2.12
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)		t_{RESW2}	—	324	397.7	μs	—

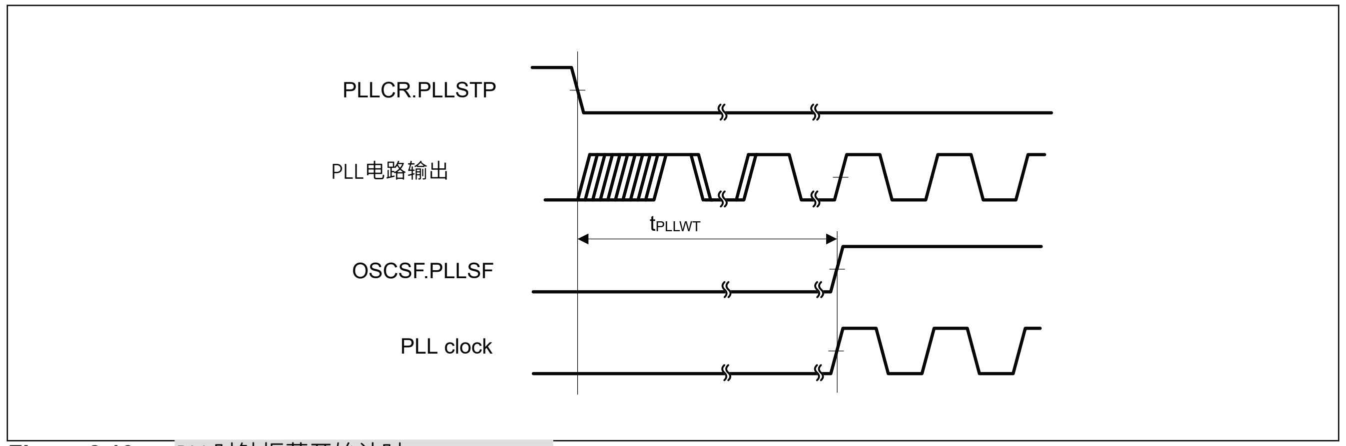


Figure 2.10 PLL时钟振荡开始计时

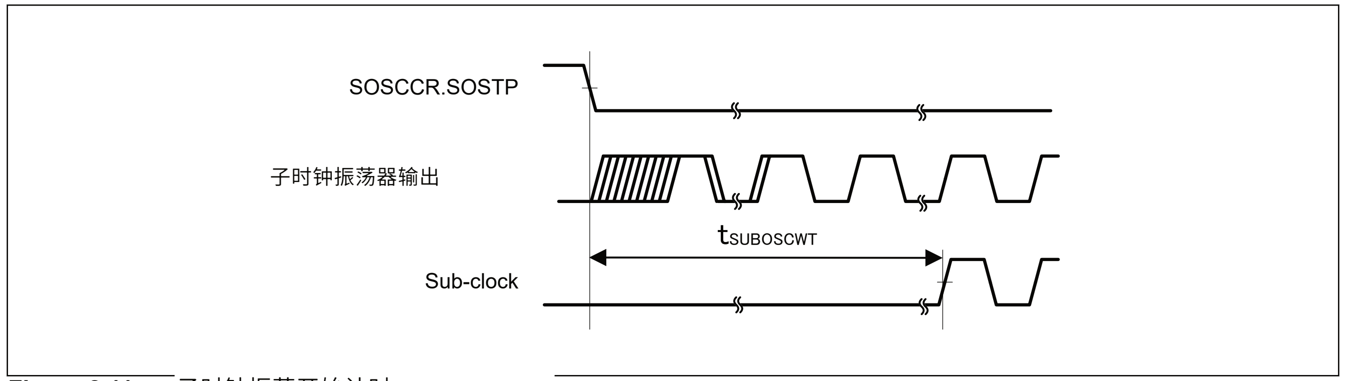


Figure 2.11 子时钟振荡开始计时

2.3.3 复位定时

Table 2.19 复位定时

Parameter		符号MinTyp			Max	单元测试条件	
RES脉冲宽度	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.12
	深度软件待机模式	t_{RESWD}	0.6	—	—	ms	Figure 2.13
	软件待机模式，高速模式	t_{RESWS}	0.3	—	—	ms	
	所有其他	t_{RESW}	200	—	—	μs	
RES取消后的等待时间		t_{RESWT}	—	37.3	41.2	μs	Figure 2.12
内部复位取消后的等待时间（IWDT复位，WDT复位，软件复位，SRAM奇偶校验错误复位，SRAMECC错误复位，总线主MPU错误复位，TrustZone错误复位，缓存奇偶校验错误复位）		t_{RESW2}	—	324	397.7	μs	—

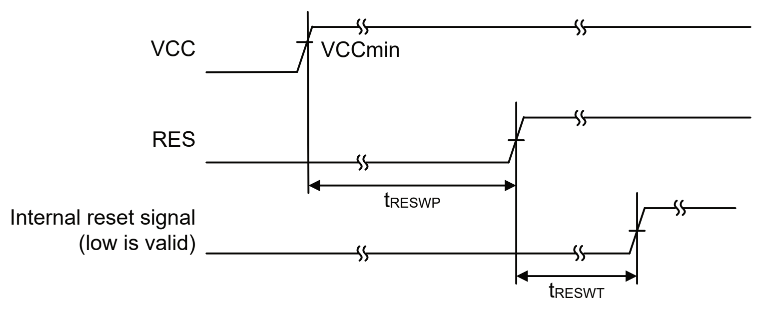


Figure 2.12 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

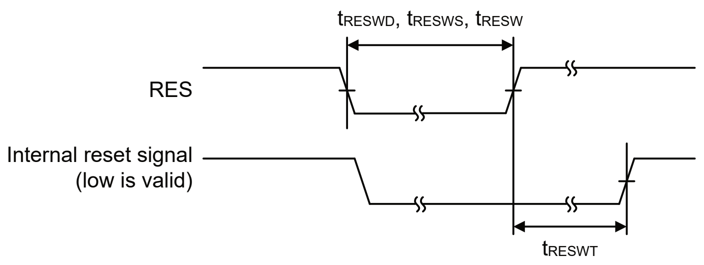


Figure 2.13 Reset input timing

2.3.4 Wakeup Timing

Table 2.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 2.14 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	µs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	µs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	µs	
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 2.15
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	56	—	57	t_{cyc}	

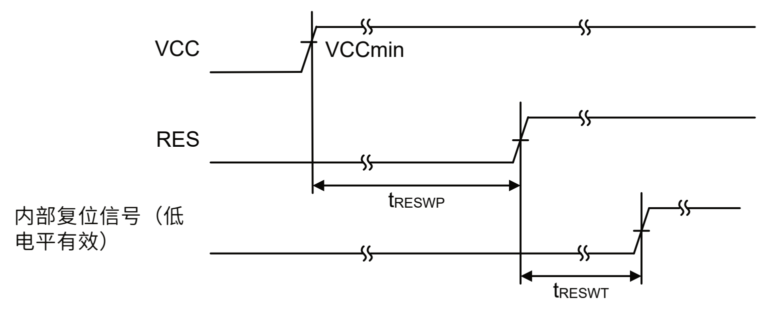


Figure 2.12 在VCC超过VPOR电压阈值的条件下RES引脚输入时序

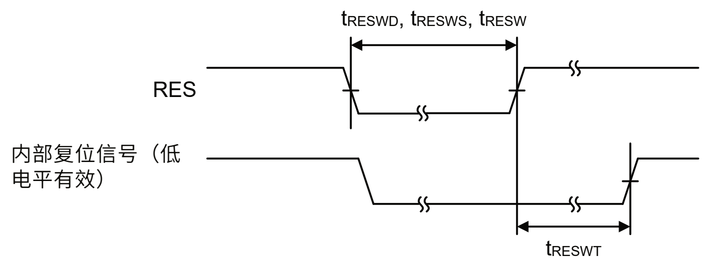


Figure 2.13 复位输入定时

2.3.4 唤醒时间

Table 2.20 从低功耗模式恢复的时序（1/2）

Parameter			Symbol	Min	Typ	Max	单元	测试条件
恢复时间 软件待机模式*1	晶体谐振器连接到主时钟振荡器	系统时钟源为主时钟振荡器*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 2.14 所有振荡器的分频比为1。
		系统时钟源是带主时钟振荡器的PLL*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	外部时钟输入到主时钟振荡器	系统时钟源为主时钟振荡器*4	t_{SBYEX}*13	—	45	125	µs	
		系统时钟源是带主时钟振荡器的PLL*5	t_{SBYPE}*13	—	170	255	µs	
	系统时钟源为子时钟振荡器*6*11		t_{SBYSC}*13	—	0.7	0.8	ms	
	系统时钟源为LOCO*7*11		t_{SBYLO}*13	—	0.7	0.9	ms	
	系统时钟源为HOCO时钟振荡器*8		t_{SBYHO}*13	—	55	130	µs	
	系统时钟源是PLL与HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	系统时钟源为MOCO时钟振荡器*10		t_{SBYMO}*13	—	35	65	µs	
恢复时间 深度软件待机模式	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E		t_{DSBY}	—	0.38	0.54	ms	Figure 2.15
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19		t_{DSBY}	—	0.55	0.73	ms	
取消深度软件待机模式后的等待时间			t_{DSBYWT}	56	—	57	t_{cyc}	

Table 2.20 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	—	35[*12]	70[*12]	µs	Figure 2.16
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	—	11[*12]	14[*12]	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

Table 2.20 从低功耗模式恢复的时间（2/2）

Parameter		Symbol	Min	Typ	Max	单元	测试条件
恢复时间 软件待机模式到 打盹模式	高速模式时，系统时钟源是 HOCO (20 MHz)	t_{SNZ}	—	35[*12]	70[*12]	µs	Figure 2.16
	高速模式时，系统时钟源是 MOCO (8 MHz)	t_{SNZ}	—	11[*12]	14[*12]	µs	

注1。恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以用下面的公式来确定：总恢复时间=作为系统时钟源的振荡器的恢复时间+系统时钟的有源振荡器中最长的tSBYOSCWT+2个LOCO周期（当LOCO工作时）+Subosc振荡，MSTPC0=0（CAC模块停止）注2。当晶振的频率为24MHz(主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x05)且内部时钟分频设置的最大值为1时。注3。当PLL的频率为200MHz(主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x05)且内部时钟分频设置的最大值为4时。注4。当外部时钟的频率为24MHz(主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x00)且内部时钟分频设置的最大值为1时。注5。当PLL的频率为200MHz(主时钟振荡器等待控制寄存器(MOSCWTCR)设置为0x00)且内部时钟分频设置的最大值为4时。注6。子时钟振荡器频率为32.768khz，内部时钟分频设置的最大值为1。

注7。LOCO频率为32.768kHz，内部时钟分频设置的最大值为1。
注8。HOCO频率为20MHz，内部时钟分频设置的最大值为1。注9。PLL频率为200MHz，内部时钟分频设置的最大值为4。注10。MOCO频率为8MHz，内部时钟分频设置的最大值为1。

注11。在高速模式下，子时钟振荡器或LOCO在软件待机模式下继续振荡。
注12。时的SNZCR。RXDREQEN位设置为0，将以下时间添加为电源恢复时间：16µs（典型值），48µs（最大值）。注13。恢复时间可以用tSBYOSCWT+tSBYSEQ的方程计算。并且它们可以用下面的值和方程来确定。对于n，从内部时钟分频设置中选择最大值。

唤醒时间TYP			MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

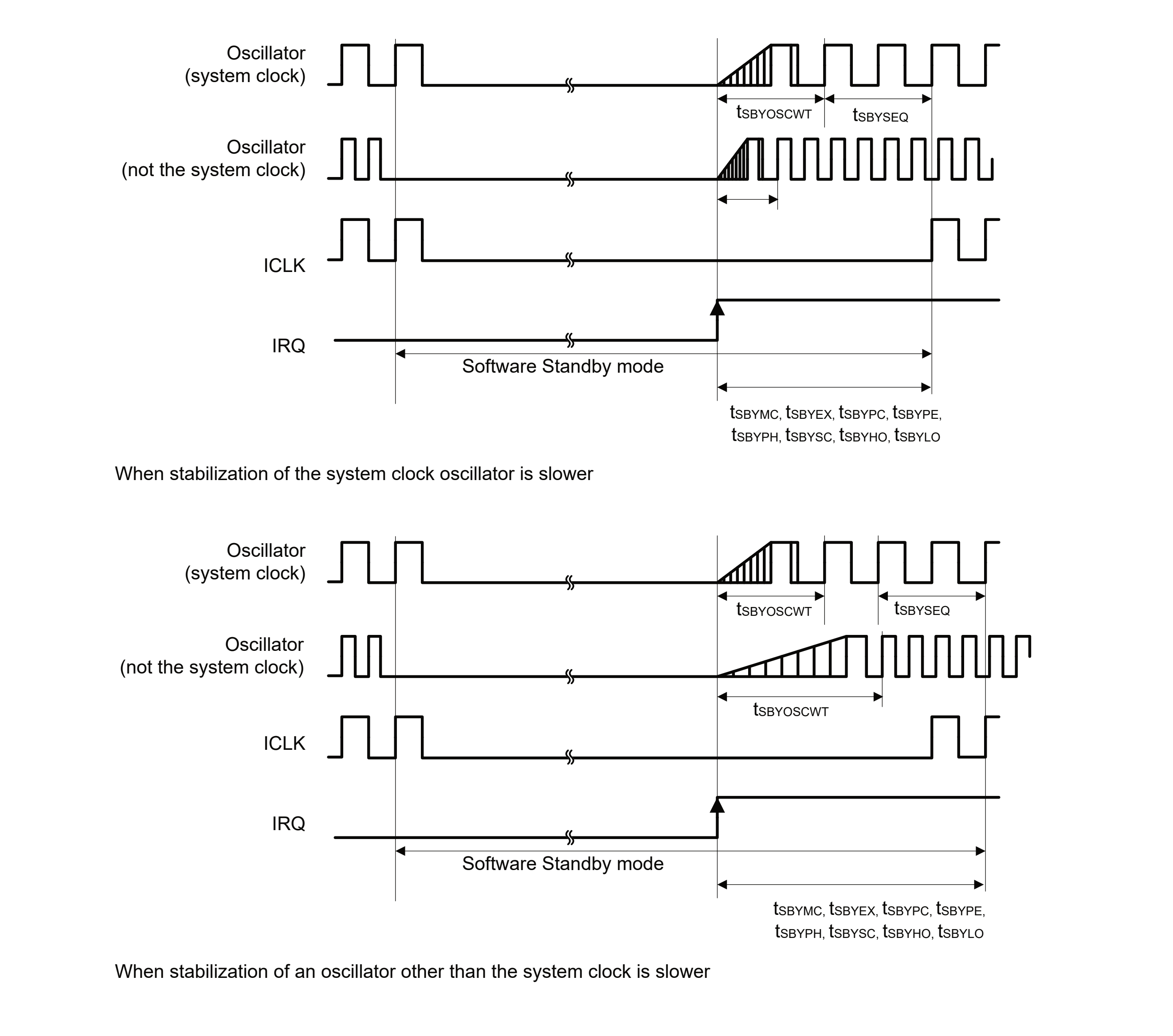


Figure 2.14 Software Standby mode cancellation timing

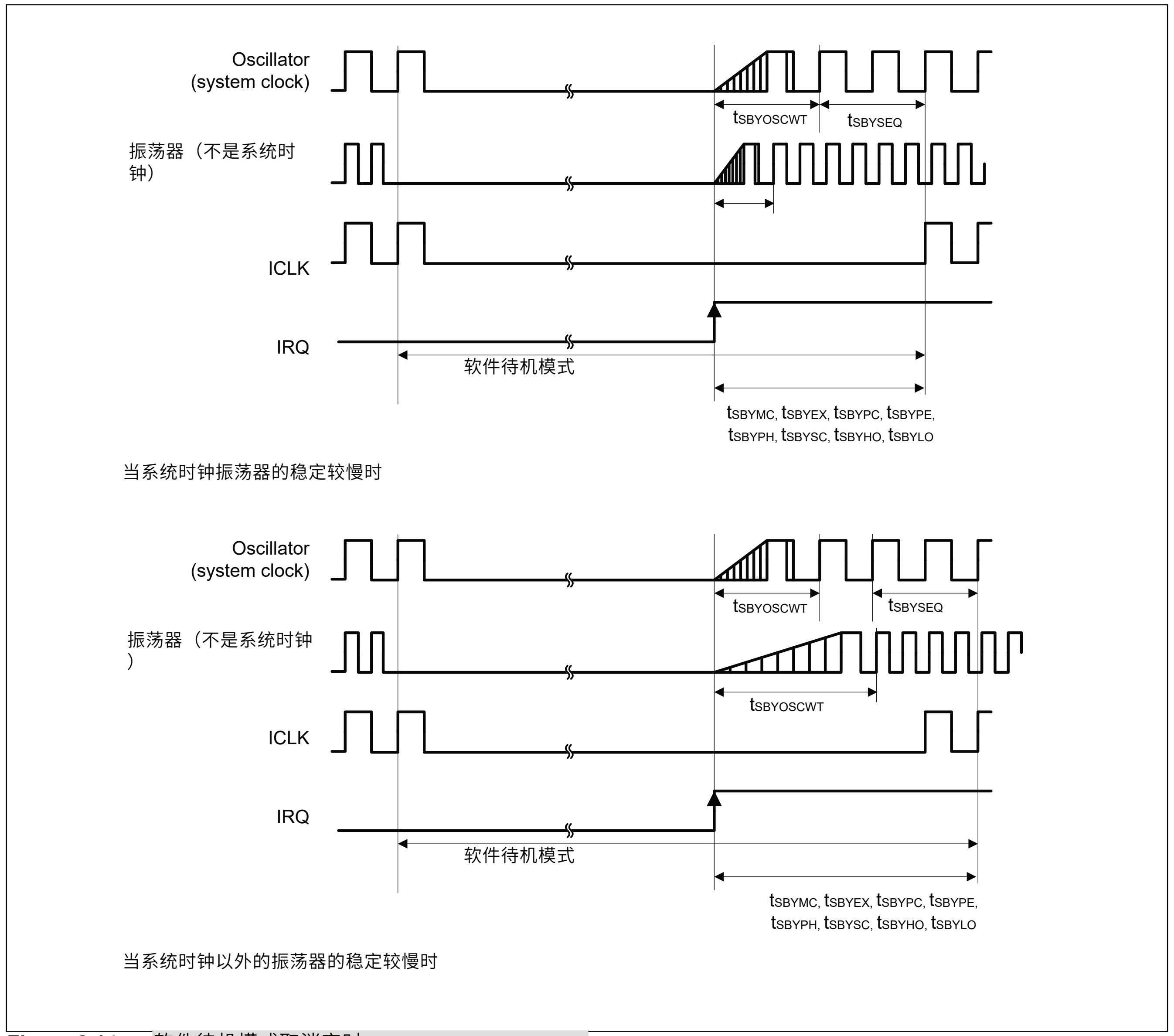


Figure 2.14 软件待机模式取消定时

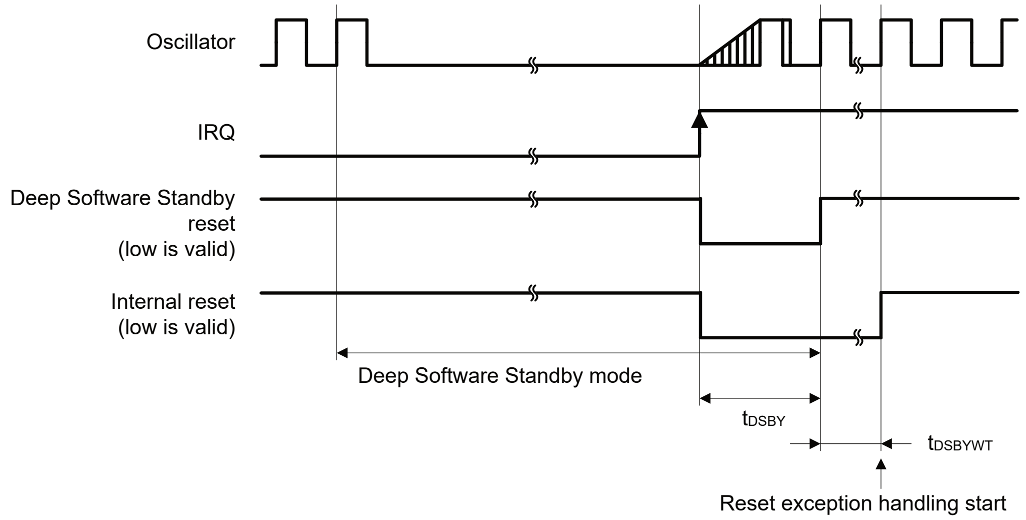
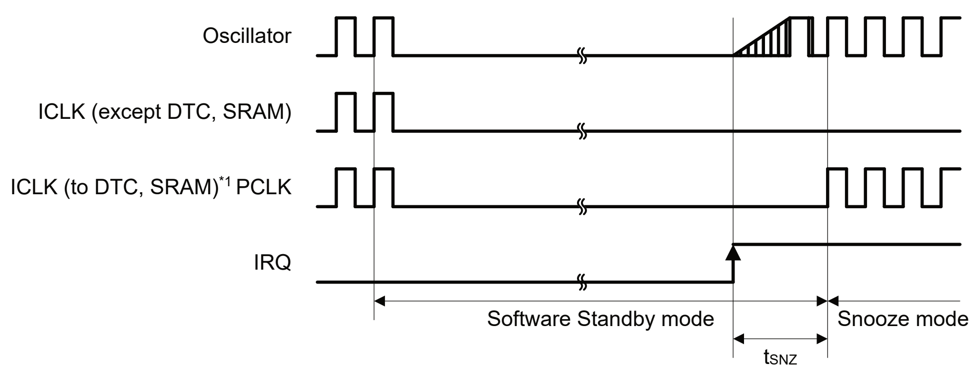


Figure 2.15 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$[*1]	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$[*2]	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$[*1]	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$[*3]	—	—			$t_{IRQCK} \times 3 > 200$ ns

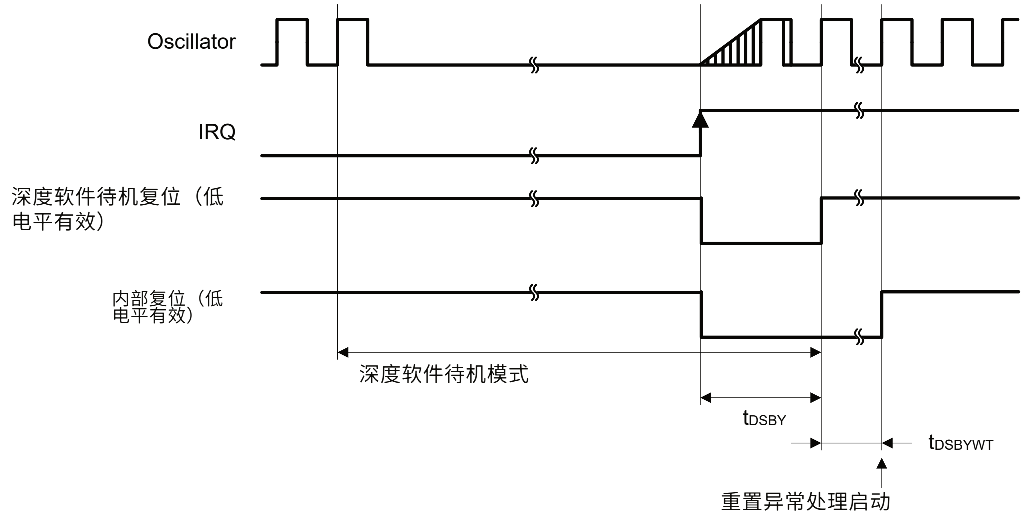
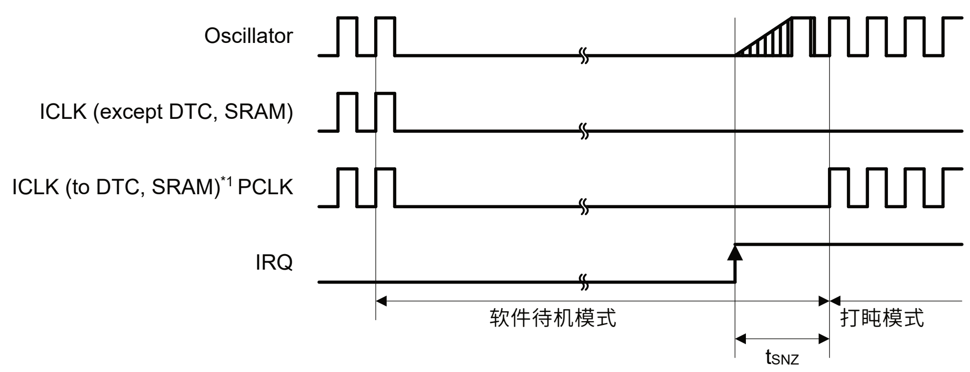


Figure 2.15 深度软件待机模式取消定时



注1。当SNZCR。SNZDTCEN位被设置为1，ICLK被提供给DTC和SRAM。

Figure 2.16 从软件待机模式恢复定时到打盹模式

2.3.5 NMI和IRQ噪声滤波器

Table 2.21 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	—	—	ns	Nmi数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$[*1]	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$[*2]	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	—	—	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$[*1]	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$[*3]	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

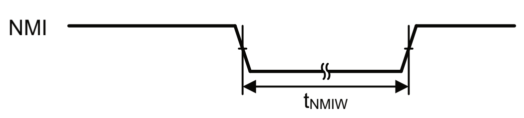


Figure 2.17 NMI interrupt input timing

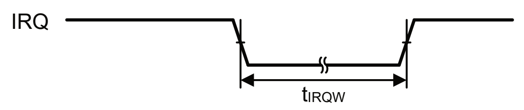


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT16E Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.19
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.20
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.21
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 2.22
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4, 5, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 5, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 2.23
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*2	100	—	ns	Figure 2.24
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.25

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.

Note: 软件待机模式下最低200ns。
Note: 如果时钟源切换，则添加切换源的4个时钟周期。
注1。tPcyc表示PCLKB周期。
注2。tNMICK表示NMI数字滤波器采样时钟的周期。注3。tIRQCK表示IRQi
数字滤波器采样时钟的周期。

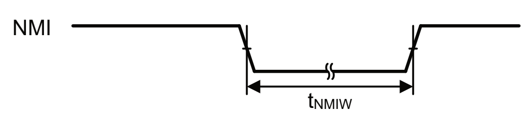


Figure 2.17 Nmi中断输入定时

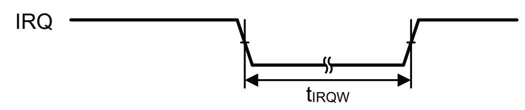


Figure 2.18 IRQ中断输入定时

2.3.6 IO端口、POEG、GPT、AGT和ADC12触发定时

Table 2.22 IO端口、POEG、GPT、AGT和ADC12触发定时

GPT16E Conditions:
高驱动输出在PmnPFS寄存器的端口驱动能力位中选择。
AGT Conditions:
中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter			Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度		t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.19
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	—	t_{Pcyc}	Figure 2.20
GPT	输入捕获脉冲宽度	单边缘	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.21
		双重边缘		2.5	—		
	GTIOCxY输出偏斜（x=0到3，Y=A或B）	中间驱动缓冲器	t_{GTISK}*1	—	4	ns	Figure 2.22
		高驱动缓冲器		—	4		
	GTIOCxY输出偏斜(x=4 5 Y=A或B)	中间驱动缓冲器		—	4		
		高驱动缓冲器		—	4		
	GTIOCxY输出偏斜（x=0到5，Y=A或B）	中间驱动缓冲器		—	6		
		高驱动缓冲器		—	6		
	OPS输出偏斜 GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 2.23
AGT	AGTIO，AGTEE输入周期		t_{ACYC}*2	100	—	ns	Figure 2.24
	AGTIO，AGTEE输入高宽度，低宽度		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO AGTO AGTOA AGTOB输出周期		t_{ACYC2}	62.5	—	ns	
ADC12	ADC12触发输入脉冲宽度		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.25

注：tPcyc：PCLKB循环，tPDcyc：PCLKD循环。注1。当使用相同的驱动程序IO时，此偏斜适用。如果中高驱动器的IO混合，则不能保证操作。
注2。输入周期的约束:
不切换源时钟时：tPcyc×2 tACYC应满足。

When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

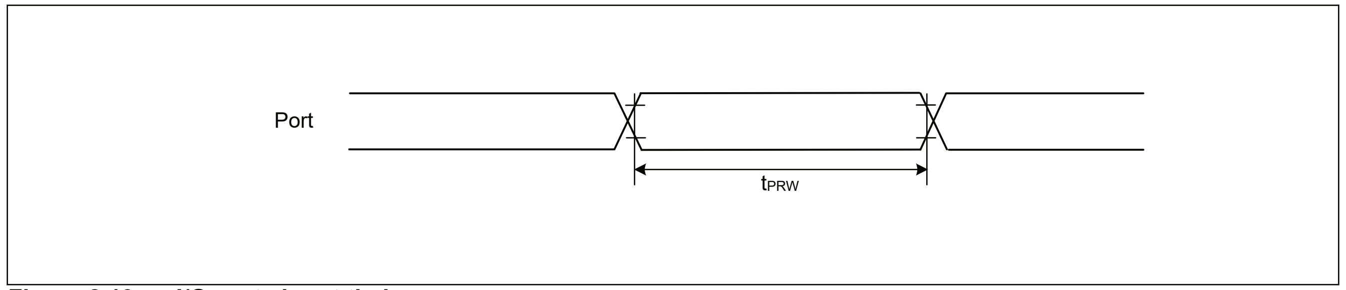


Figure 2.19 I/O ports input timing

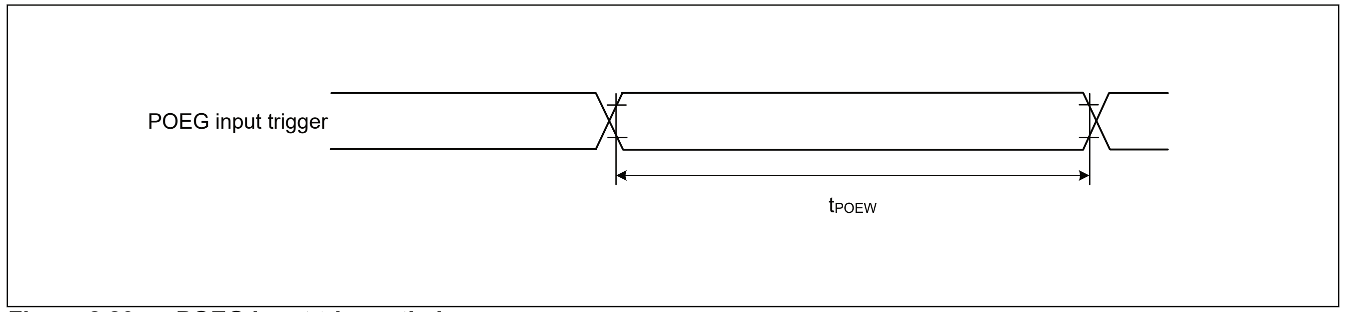


Figure 2.20 POEG input trigger timing

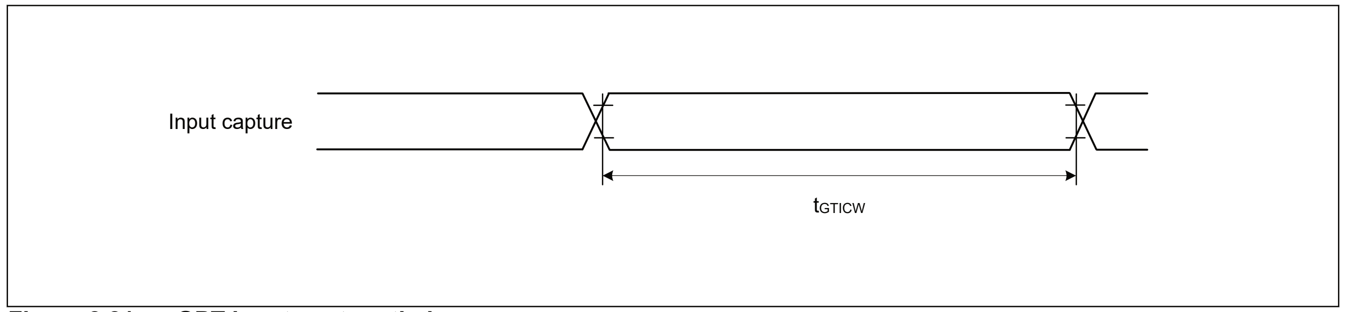


Figure 2.21 GPT input capture timing

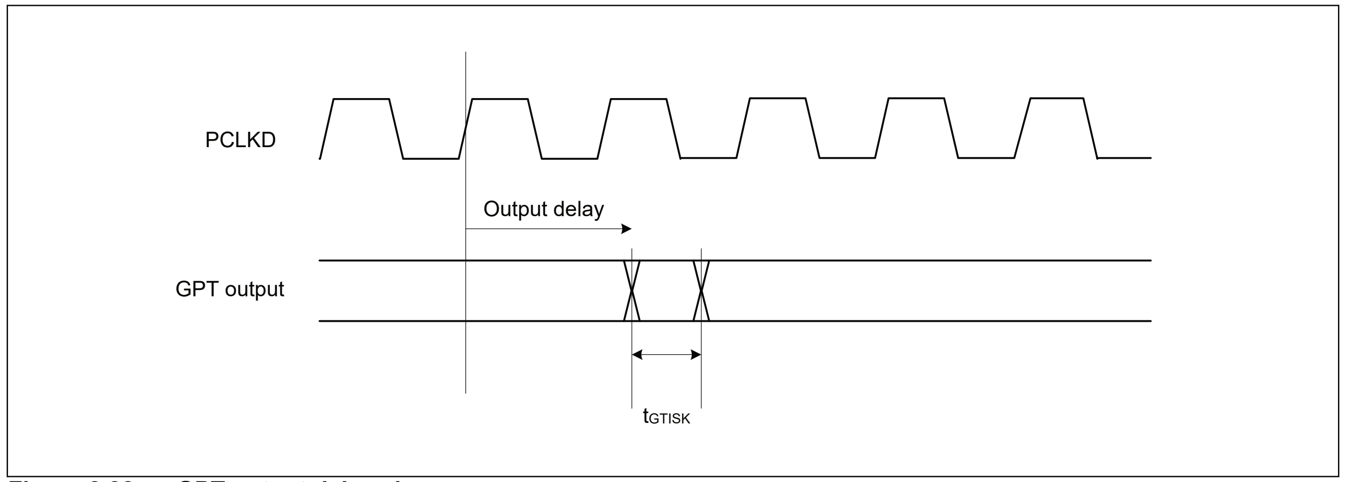


Figure 2.22 GPT output delay skew

切换源时钟时：tPcyc×6　TACYC应满足。

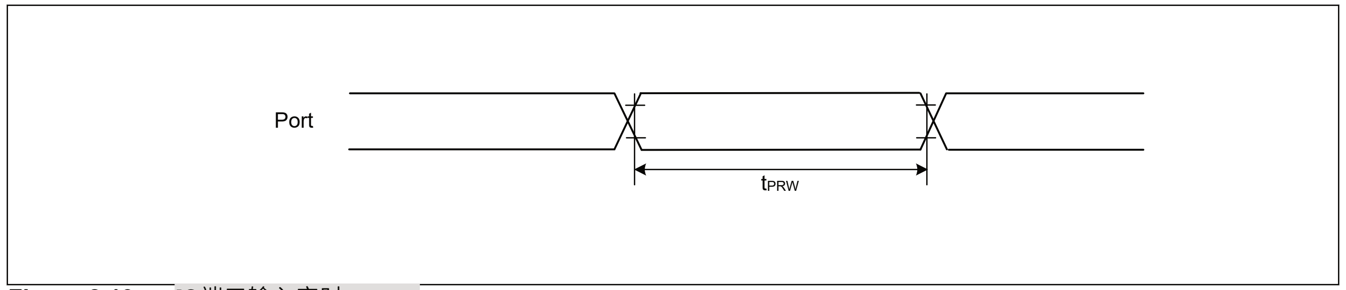


Figure 2.19 IO端口输入定时

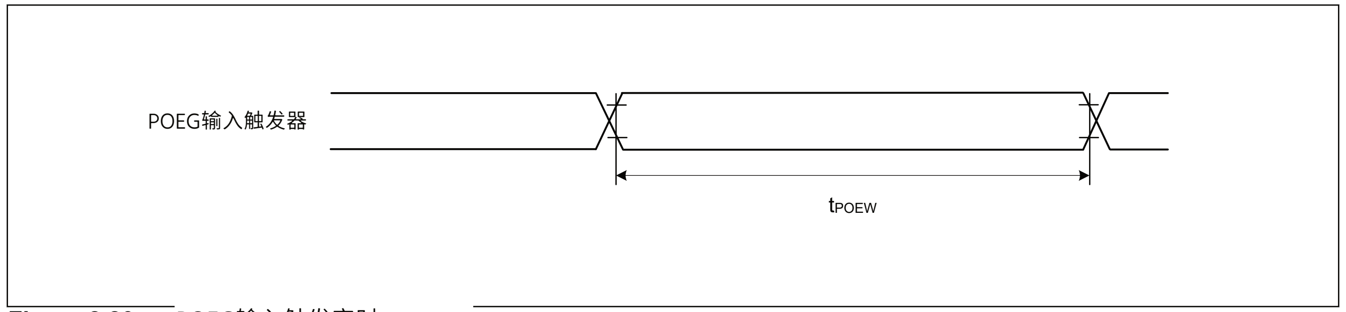


Figure 2.20 POEG输入触发定时

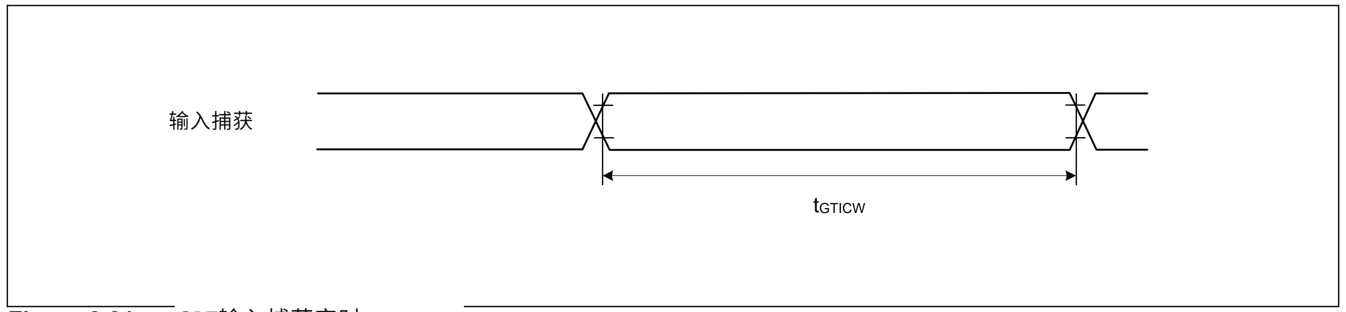


Figure 2.21 GPT输入捕获定时

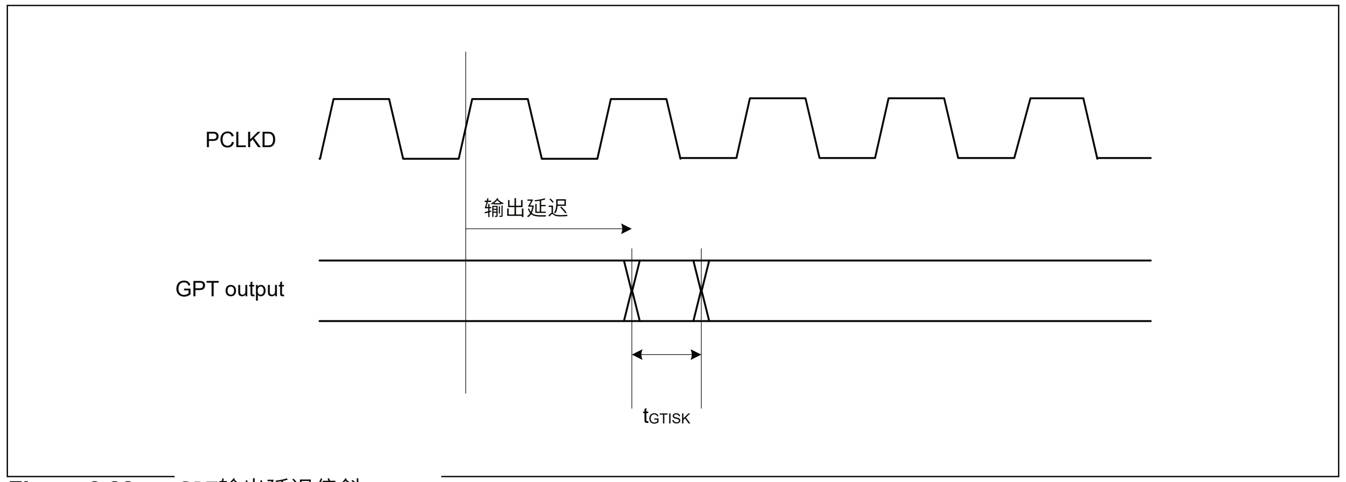


Figure 2.22 GPT输出延迟偏斜

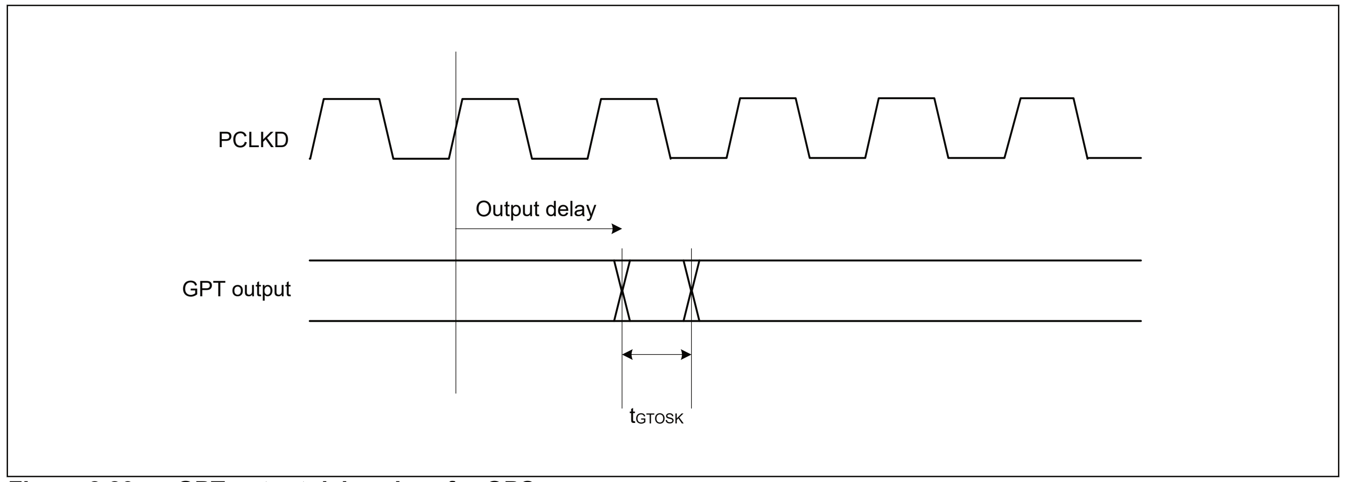


Figure 2.23 GPT output delay skew for OPS

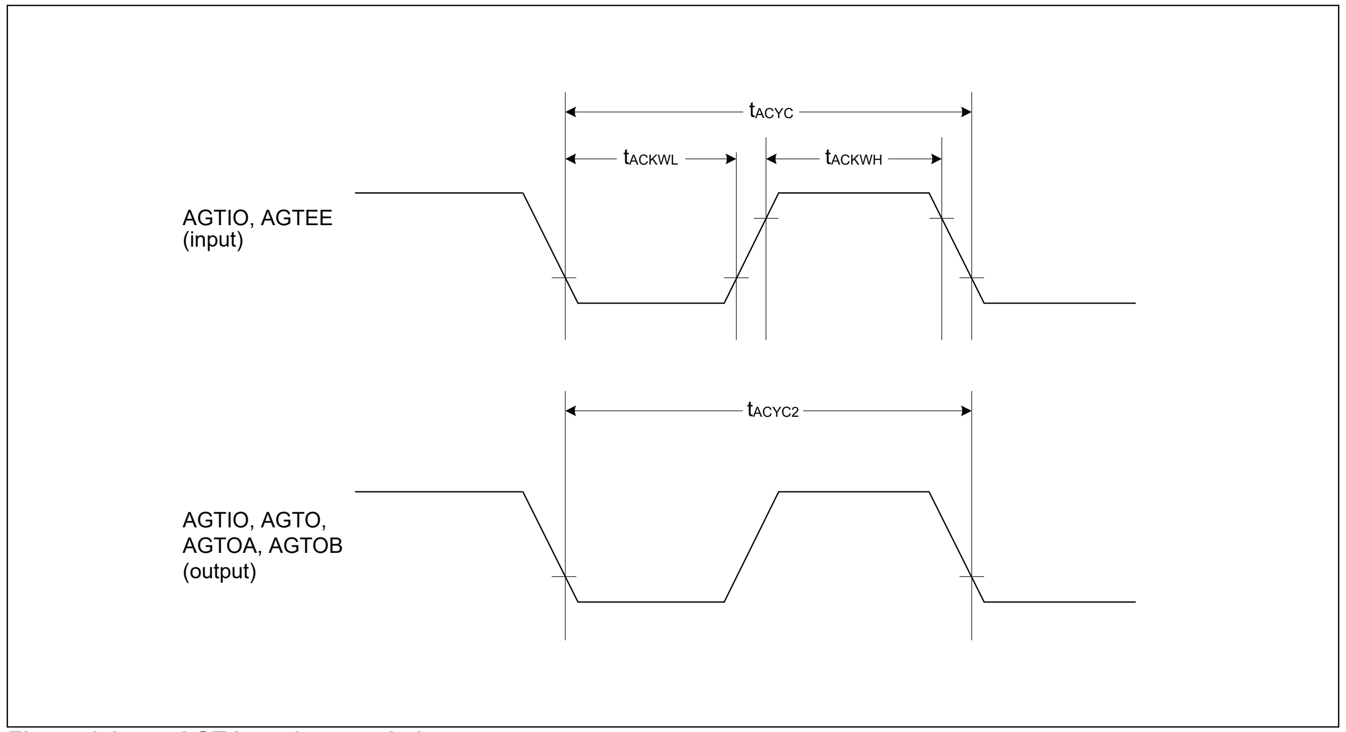


Figure 2.24 AGT input/output timing

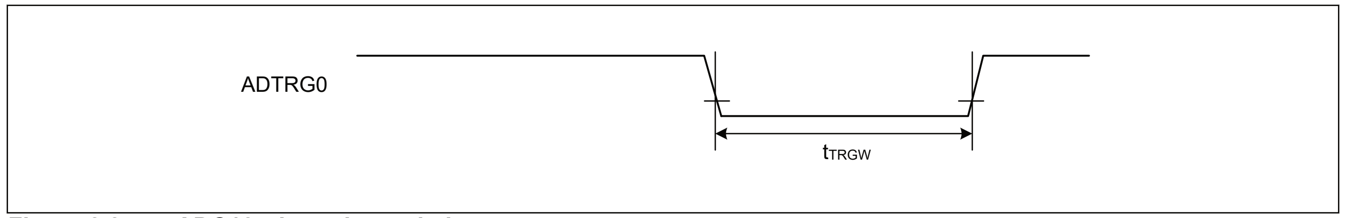


Figure 2.25 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.23 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

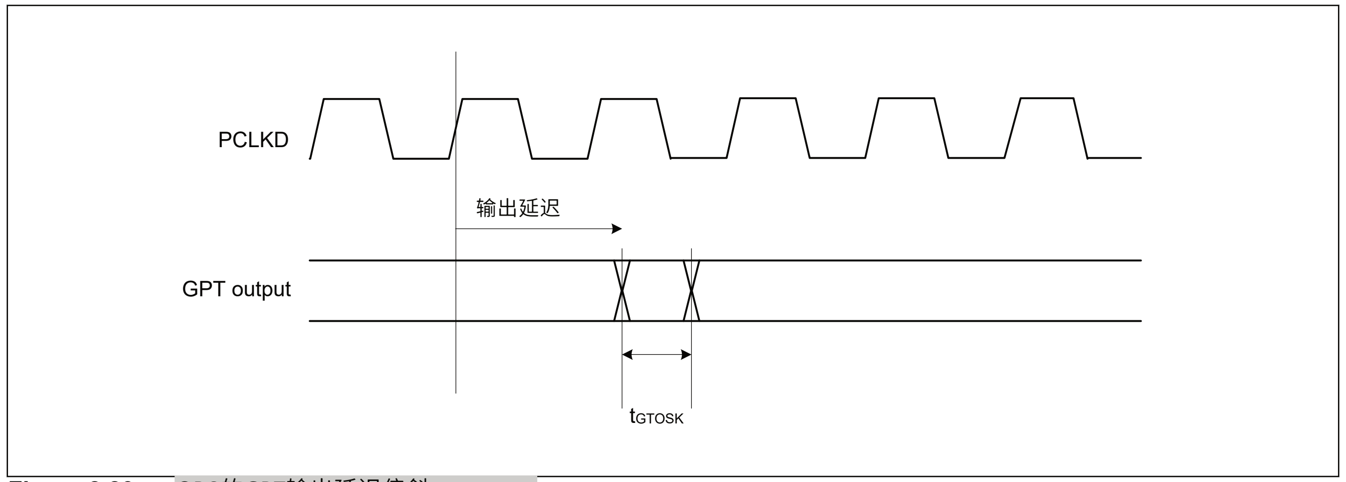


Figure 2.23 OPS的GPT输出延迟偏斜

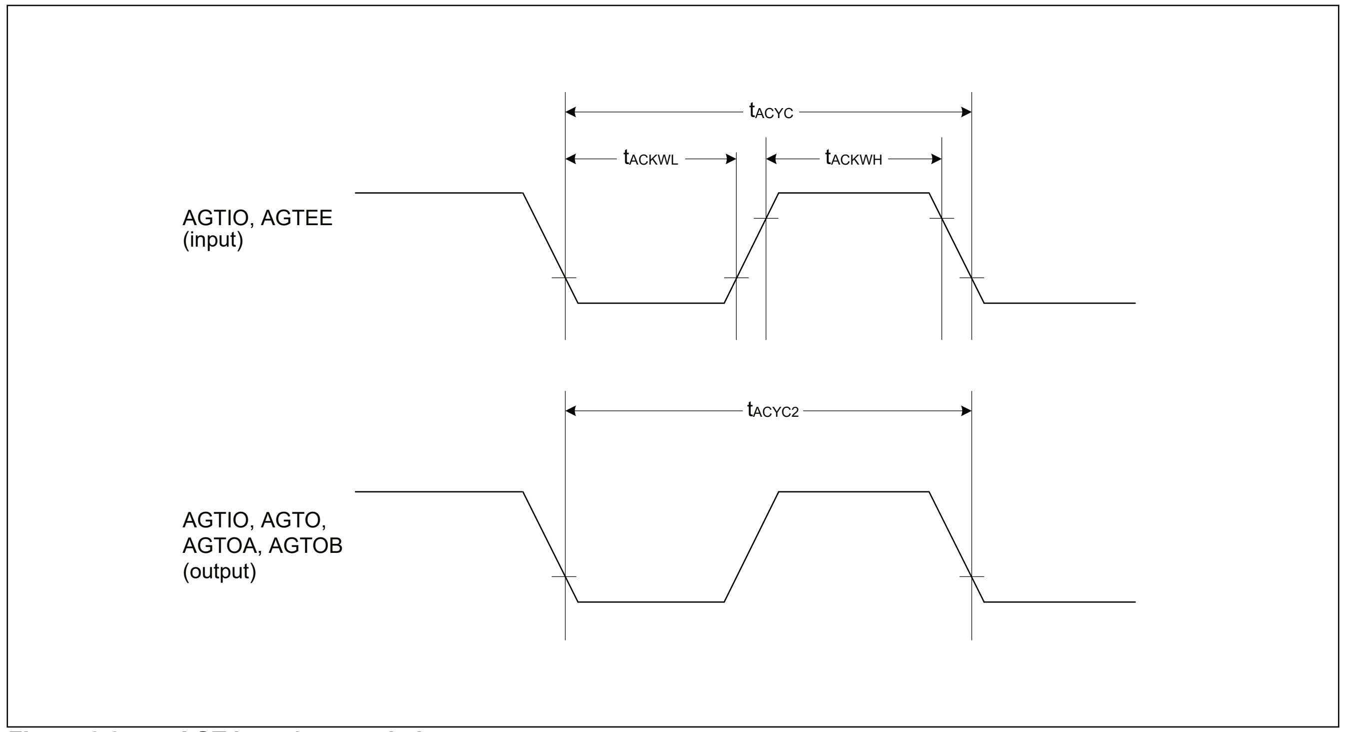


Figure 2.24 AGT input/output timing

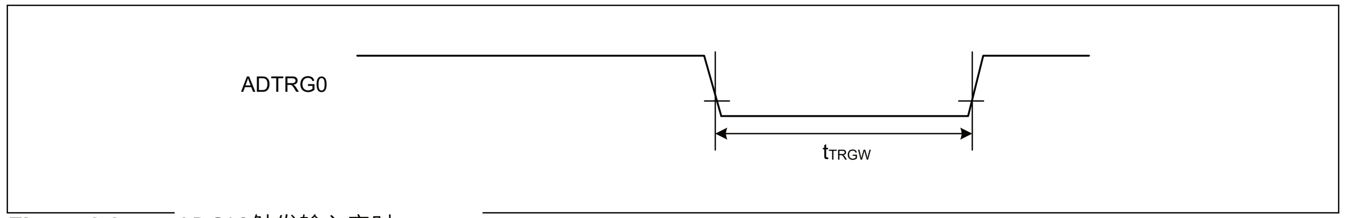


Figure 2.25 ADC12触发输入定时

2.3.7 CAC时间

Table 2.23 CAC时间

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

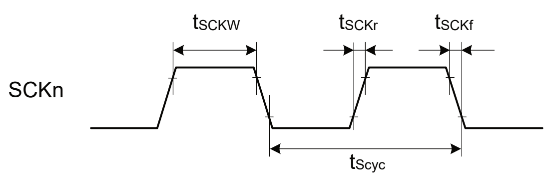
2.3.8 SCI Timing

Table 2.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.26
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 2.27
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

Figure 2.26 SCK clock input/output timing

注：tPBcyc：PCLKB循环。注1。tcac:cac计数时钟源周期。

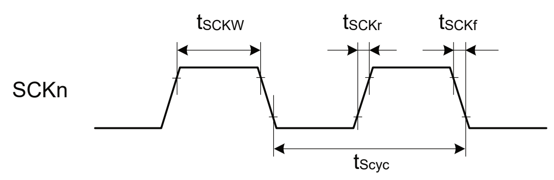
2.3.8 SCI计时

Table 2.24 SCI计时(1)

条件：在PmnPFS寄存器的端口驱动能力位选择高驱动输出。

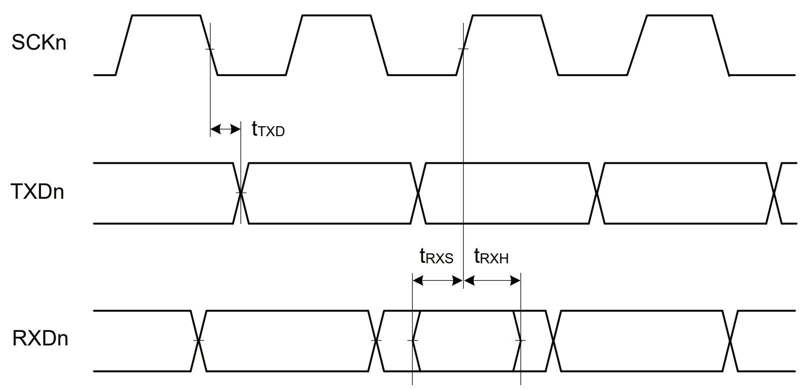
Parameter		符号最小最大单位				测试条件
SCI输入时钟周期	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.26
	时钟同步		6	—		
输入时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
输入时钟上升时间		t_{SCKr}	—	5	ns	
输入时钟下降时间		t_{SCKf}	—	5	ns	
输出时钟周期	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
	时钟同步		4	—		
输出时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
输出时钟上升时间		t_{SCKr}	—	5	ns	
输出时钟下降时间		t_{SCKf}	—	5	ns	
传输数据延迟	时钟同步主模式（内部时钟）tTXD		—	5	ns	Figure 2.27
	时钟同步从模式（外部时钟）	t_{TXD}	—	25	ns	
接收数据建立时间时钟同步主模式（内部时钟）tRXS			15	—	ns	
	时钟同步从模式（外部时钟）	t_{RXS}	5	—	ns	
接收数据保持时间	时钟同步	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

Figure 2.26 SCK时钟输入输出时序



Note: n = 0, 9

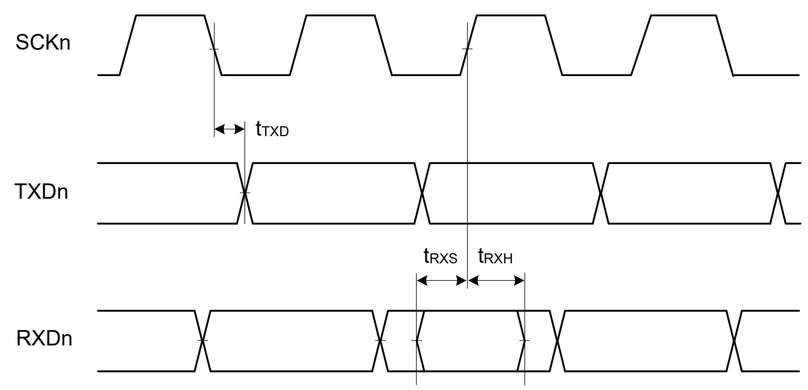
Figure 2.27 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.28
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time	master	t_{SU}	15	—	ns	Figure 2.29 to Figure 2.32
		slave		5	—	ns	
	Data input hold time		t_H	5	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	Data output hold time		t_{OH}	-5	—	ns	
	Data rise and fall time		t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time		t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time		t_{SA}	—	$3 \times t_{Pcyc} + 25$	ns	Figure 2.32
	Slave output release time		t_{REL}	—	$3 \times t_{Pcyc} + 25$	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

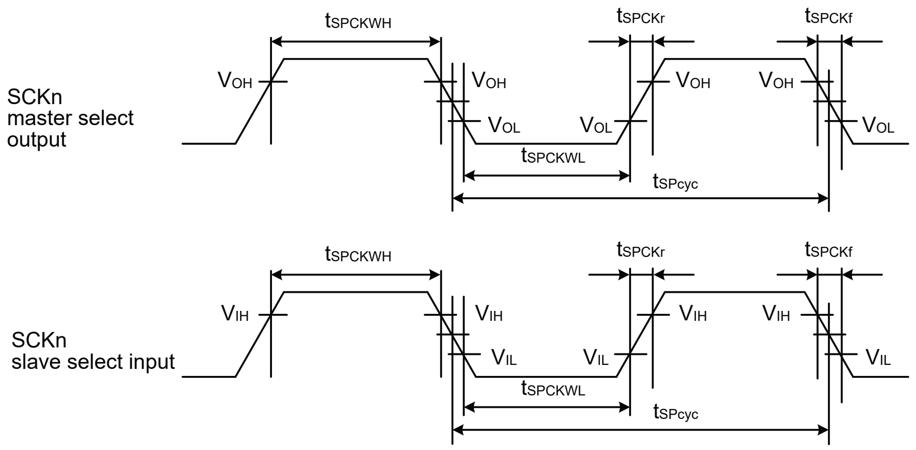
Figure 2.27 时钟同步模式下的SCI输入输出时序

Table 2.25 SCI计时(2)

条件：在PmnPFS寄存器的端口驱动能力位选择高驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
简单的SPI	SCK时钟周期输出(主)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.28
	SCK时钟周期输入(从)			6	65536		
	SCK时钟高脉冲宽度		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	数据输入设置时间	master	t_{SU}	15	—	ns	图2.29至图2.32
		slave		5	—	ns	
	数据输入保持时间		t_H	5	—	ns	
	SS输入设置时间		t_{LEAD}	1	—	t_{SPcyc}	
	SS输入保持时间		t_{LAG}	1	—	t_{SPcyc}	
	数据输出延迟	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	数据输出保持时间		t_{OH}	-5	—	ns	
	数据上升和下降时间		t_{Dr}, t_{Df}	—	5	ns	
	SS输入上升和下降时间		t_{SSLr}, t_{SSLf}	—	5	ns	
	从站访问时间		t_{SA}	—	$3 \times t_{Pcyc} + 25$	ns	Figure 2.32
	从机输出释放时间		t_{REL}	—	$3 \times t_{Pcyc} + 25$	ns	

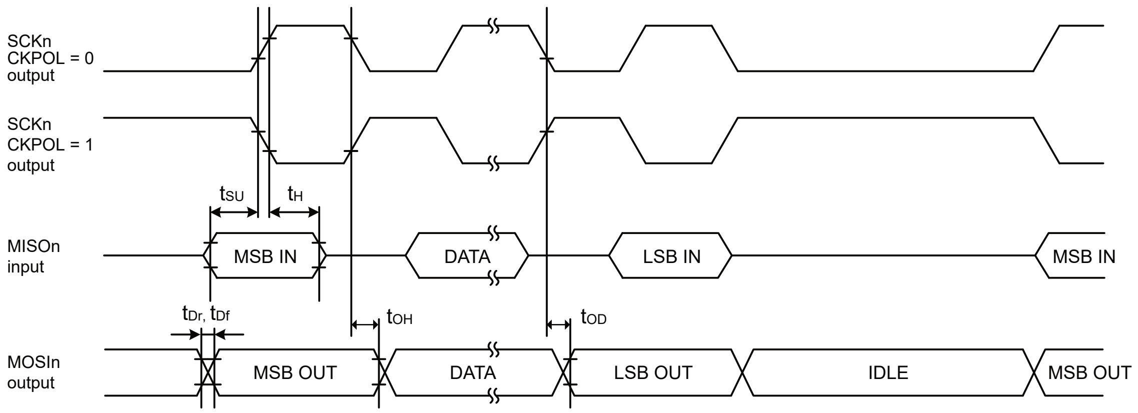
Note: t_{Pcyc}: PCLKA cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

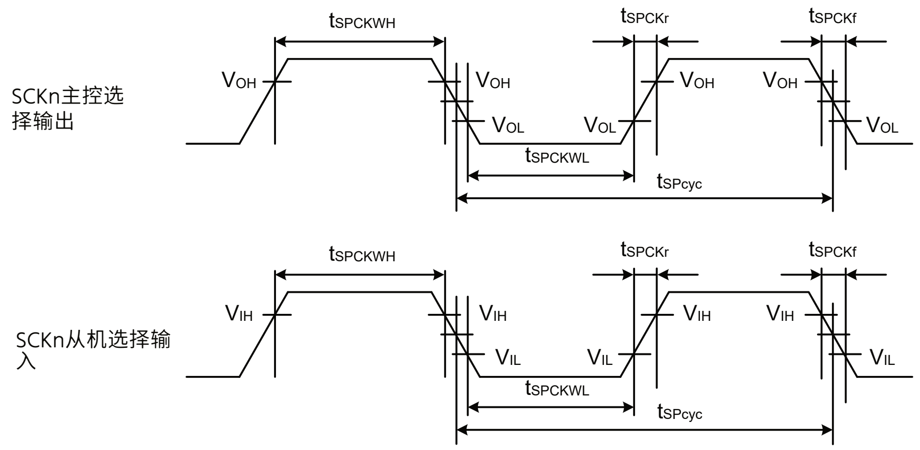
Note: n = 0, 9

Figure 2.28 SCI simple SPI mode clock timing



Note: n = 0, 9

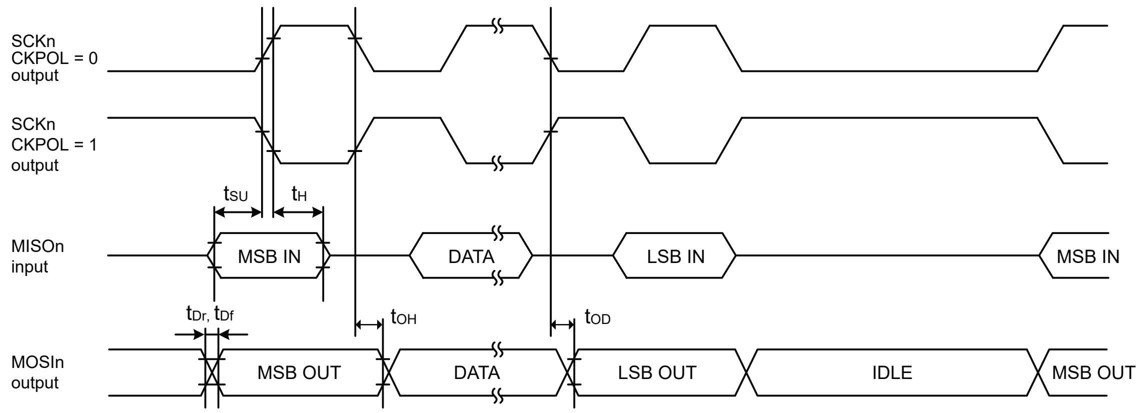
Figure 2.29 SCI simple SPI mode timing for master when CKPH = 1



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

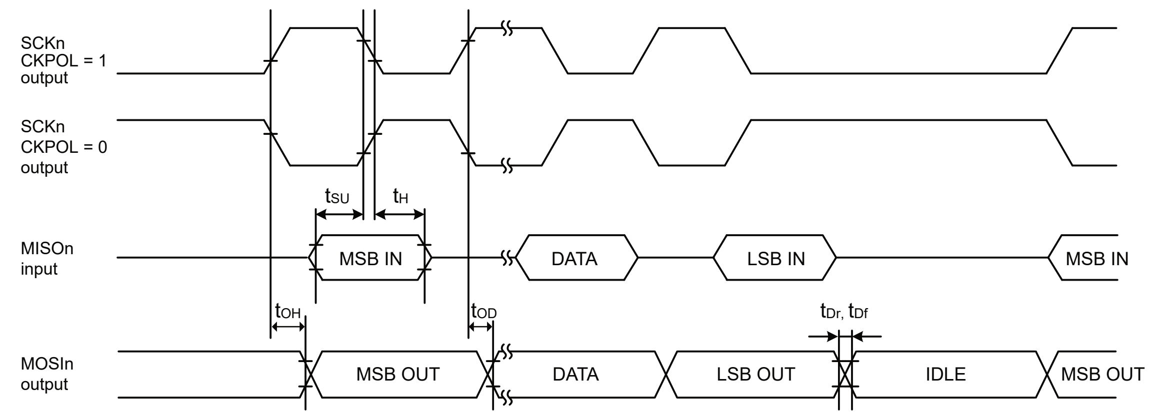
Note: n = 0, 9

Figure 2.28 SCI简单SPI模式时钟定时



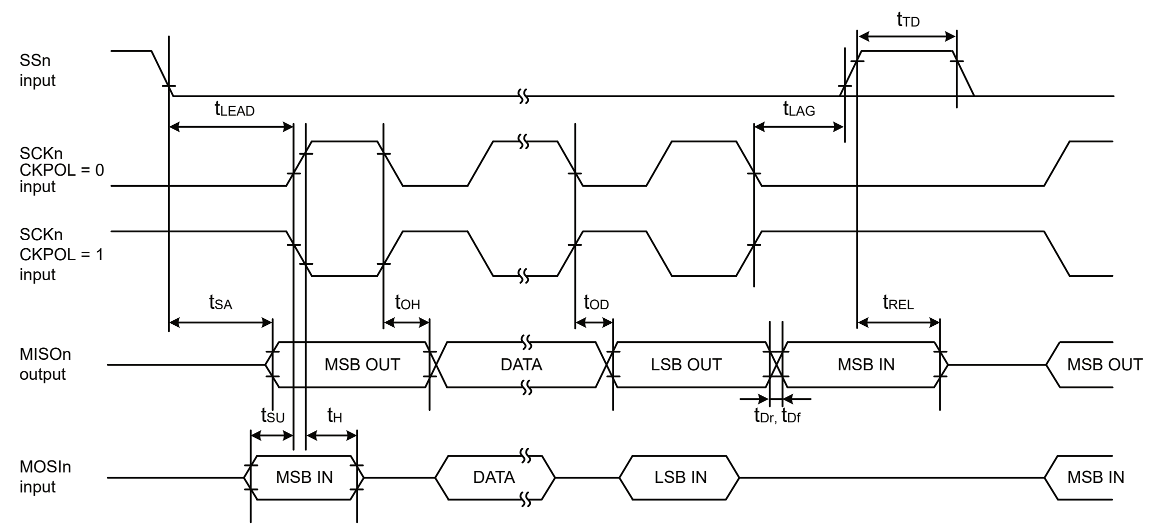
Note: n = 0, 9

Figure 2.29 当ckph=1时，主控制器的SCI简单SPI模式定时



Note: n = 0, 9

Figure 2.30 SCI simple SPI mode timing for master when CKPH = 0



Note: n = 0, 9

Figure 2.31 SCI simple SPI mode timing for slave when CKPH = 1

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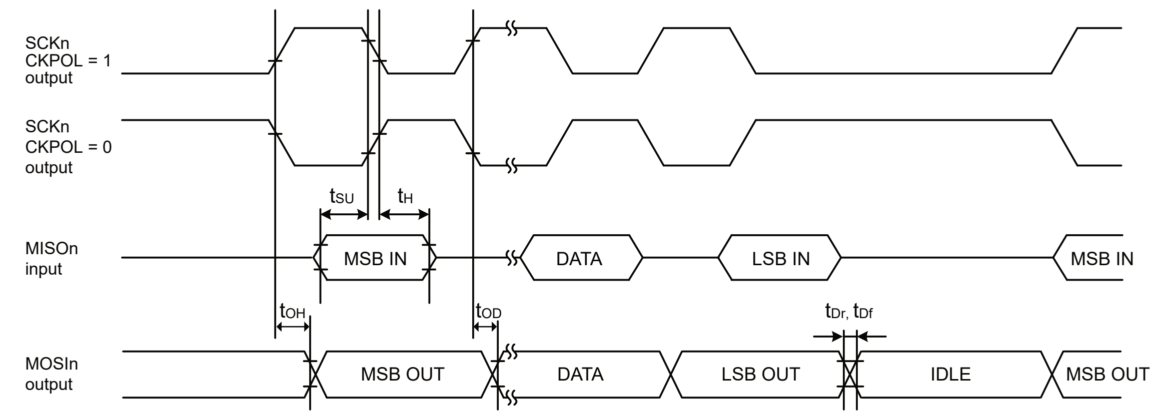
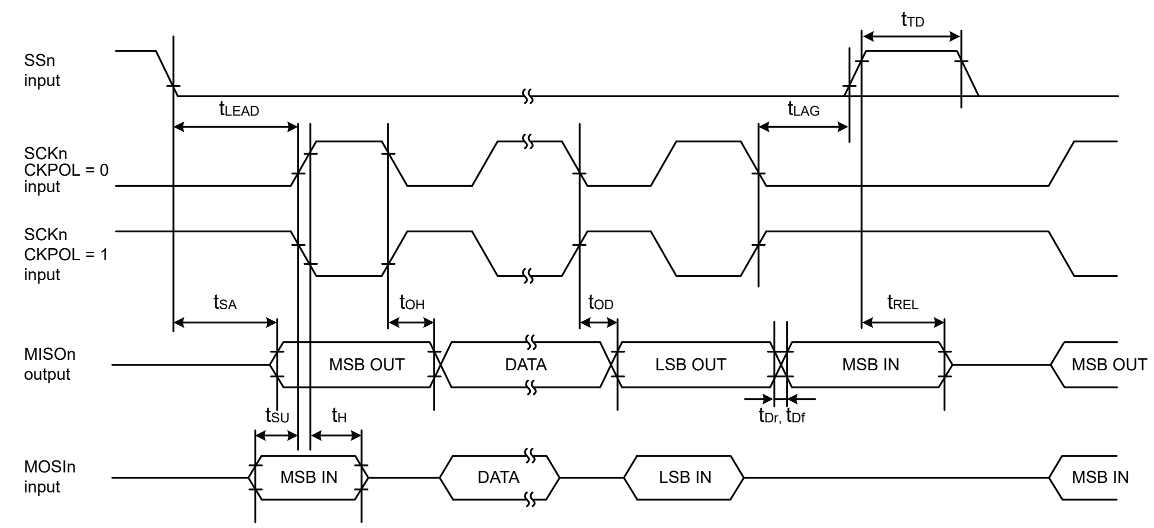


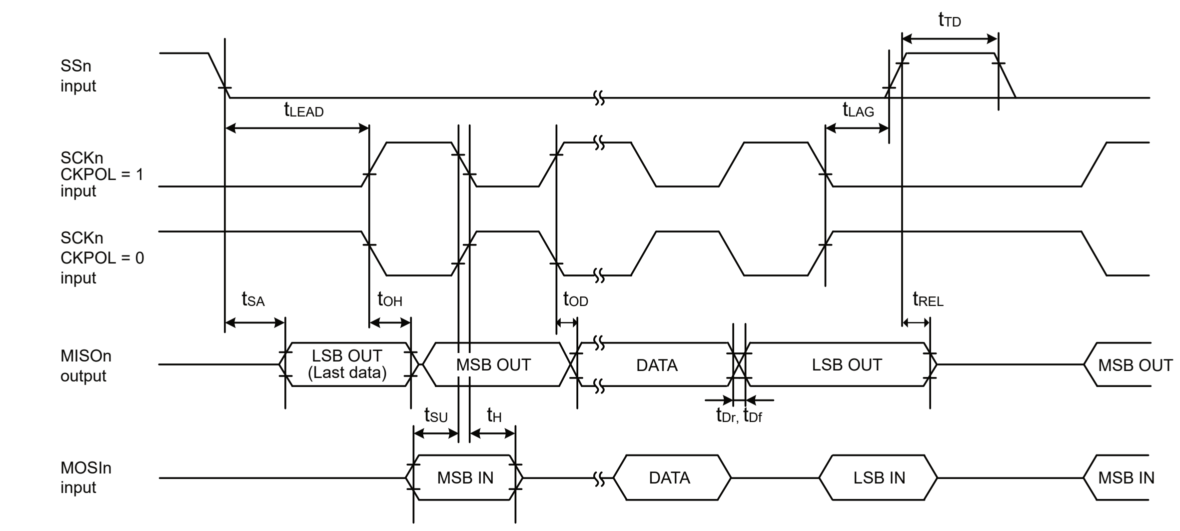
Note: n = 0, 9

Figure 2.30 当ckph=0时，主控制器的SCI简单SPI模式定时



Note: n = 0, 9

Figure 2.31 当ckph=1时，从机的SCI简单SPI模式定时



Note: n = 0, 9

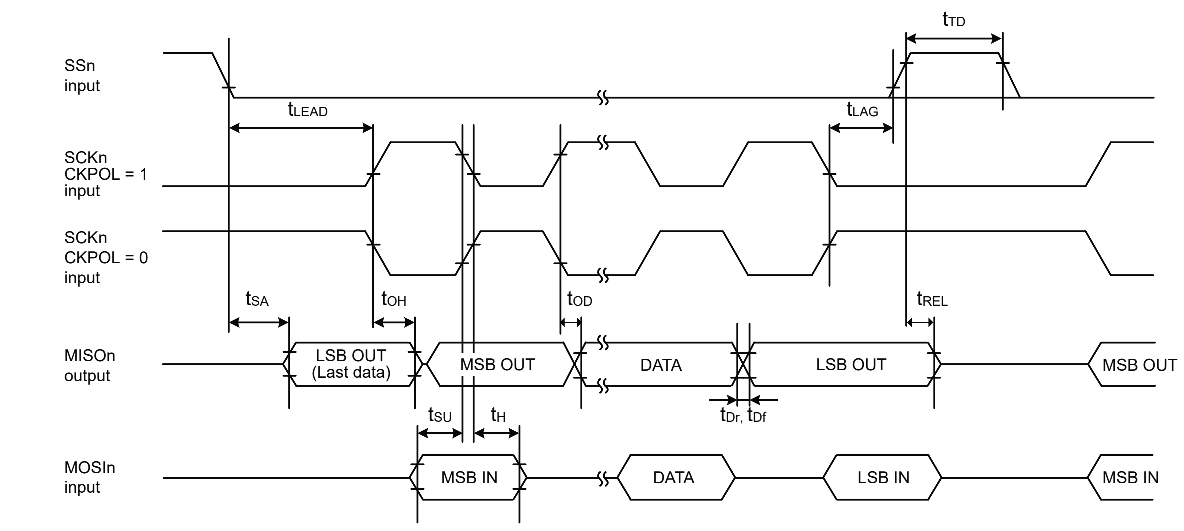
Figure 2.32 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



Note: n = 0, 9

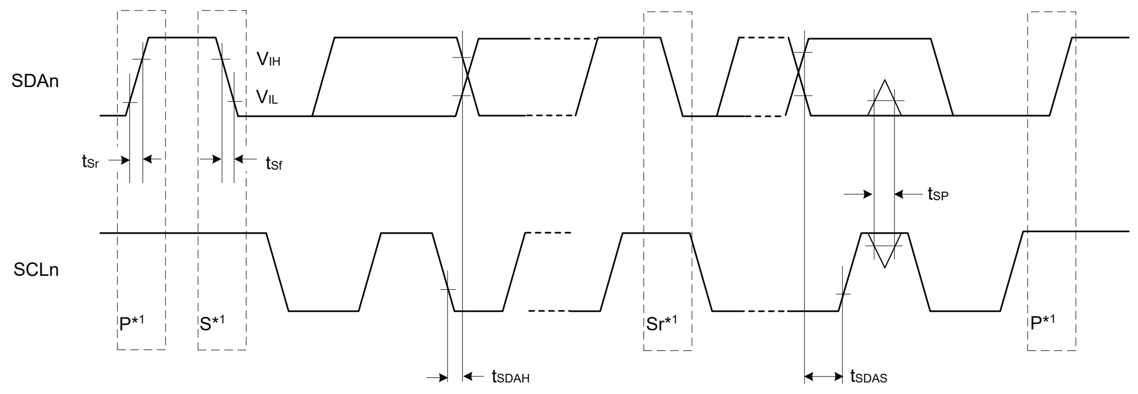
Figure 2.32 当ckph=0时，从机的SCI简单SPI模式定时

Table 2.26 SCI计时(3)

条件：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	—	1000	ns	Figure 2.33
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入设置时间	t_{SDAS}	250	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	—	300	ns	Figure 2.33
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入设置时间	t_{SDAS}	100	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

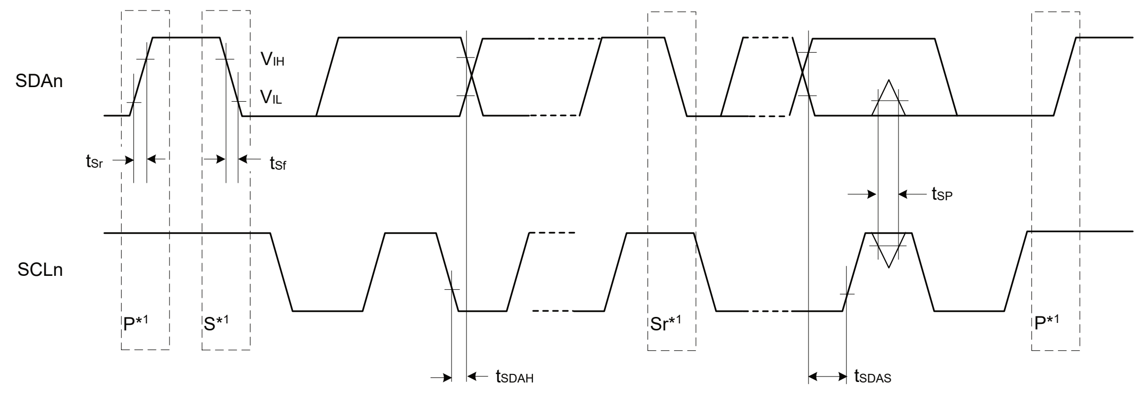
注：tIICcyc：IIC内部参考时钟（IICφ）周期。注1。Cb
表示公交线路的总容量。



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.33 SCI simple IIC mode timing



Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA

注：n=0，9注1。S、P和Sr表示以下条件:

S：启动条件P：
停止条件
Sr:重新启动条件

Figure 2.33 SCI简单IIC模式定时

2.3.9 SPI Timing

Table 2.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.34
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} – t_{SPCKr} – t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} – t_{SPCKr} – t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	μs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 2.35 to Figure 2.40
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	—		
		Slave	t_H	20	—		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10[*1]	N × t_{SPcyc} + 100[*1]	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10[*2]	N × t_{SPcyc} + 100[*2]	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		4 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	μs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	μs	
	Slave access time		t_{SA}	—	25	ns	Figure 2.39 and Figure 2.40
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

2.3.9 SPI定时

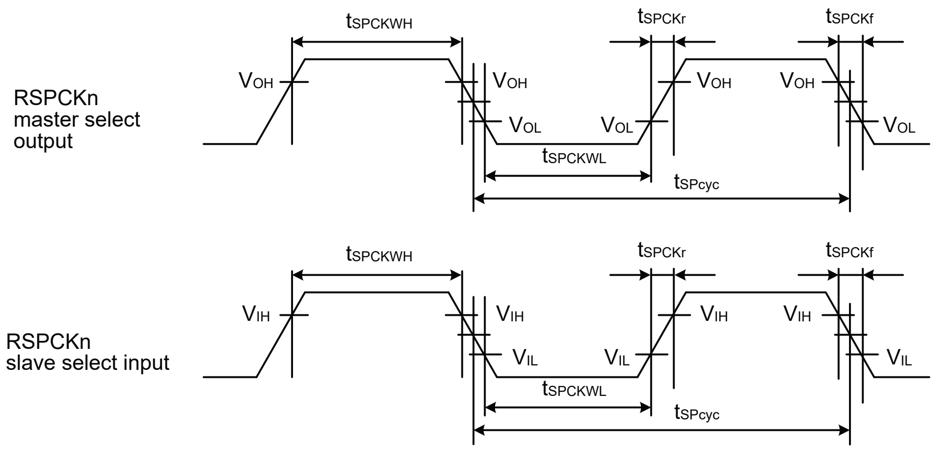
Table 2.27 SPI定时

条件：在PmnPFS寄存器的端口驱动能力位选择高驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
SPI	RSPCK时钟周期	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.34
		Slave		4	4096		
	RSPCK时钟高脉冲宽度	Master	t_{SPCKWH}	$(t_{SPcyc} – t_{SPCKr} – t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK时钟低脉冲宽度	Master	t_{SPCKWL}	$(t_{SPcyc} – t_{SPCKr} – t_{SPCKf})$ / 2 – 3	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK时钟上升和下降时间	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	μs	
	数据输入设置时间	Master	t_{SU}	4	—	ns	图2.35至图2.40
		Slave		5	—		
	数据输入保持时间	主（PCLKA除法比率设置为1/2）	t_{HF}	0	—	ns	
		主（PCLKA除法比设置为1/2以外的值）	t_H	t_{Pcyc}	—		
		Slave	t_H	20	—		
	SSL设置时间	Master	t_{LEAD}	N × t_{SPcyc} - 10[*1]	N × t_{SPcyc} + 100[*1]	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	SSL保留时间	Master	t_{LAG}	N × t_{SPcyc} - 10[*2]	N × t_{SPcyc} + 100[*2]	ns	
		Slave		4 × t_{Pcyc}	—	ns	
	数据输出延迟	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	数据输出保持时间	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	连续传输延迟	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		4 × t_{Pcyc}			
	MOSI和MISO上升和下降时间	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	μs	
	SSL上升和下降时间	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	μs	
	从站访问时间		t_{SA}	—	25	ns	图2.39和Figure 2.40
	从机输出释放时间		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

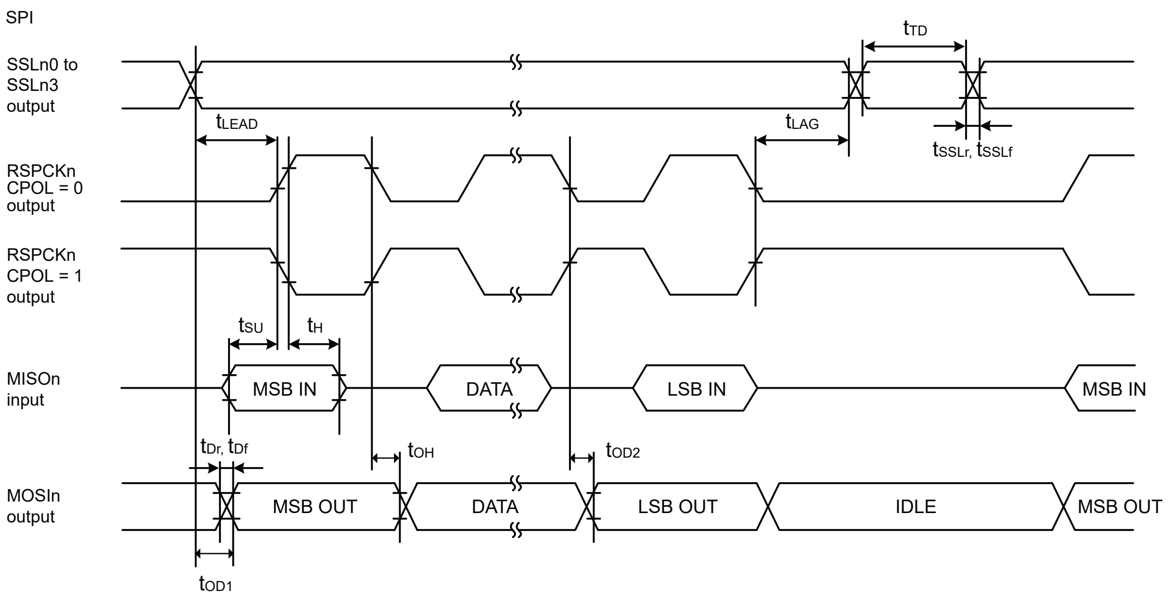
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

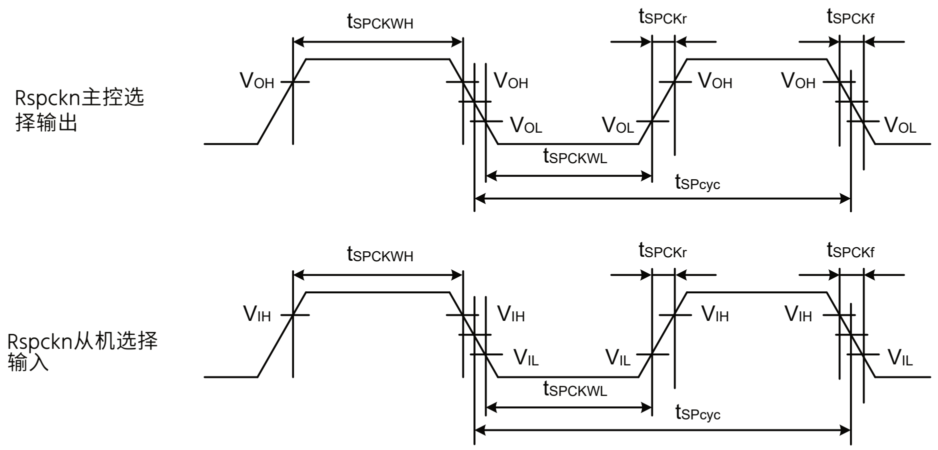
Figure 2.34 SPI clock timing



Note: n = A or B

Figure 2.35 SPI timing for master when CPHA = 0

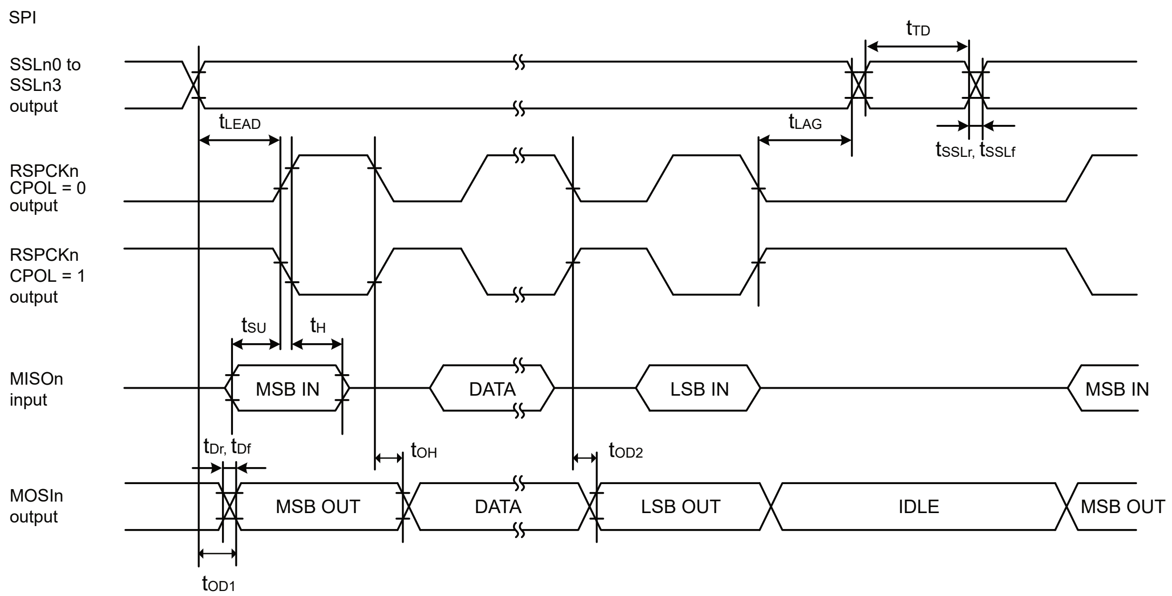
注意：必须使用在其名称后面附加了字母的引脚，例如_A、_B，以指示组成员身份。对于SPI接口，针对每个组测量电特性的AC部分。注1。N由SPCKD寄存器设置为从1到8的整数。注2。N由SSLND寄存器设置为从1到8的整数。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

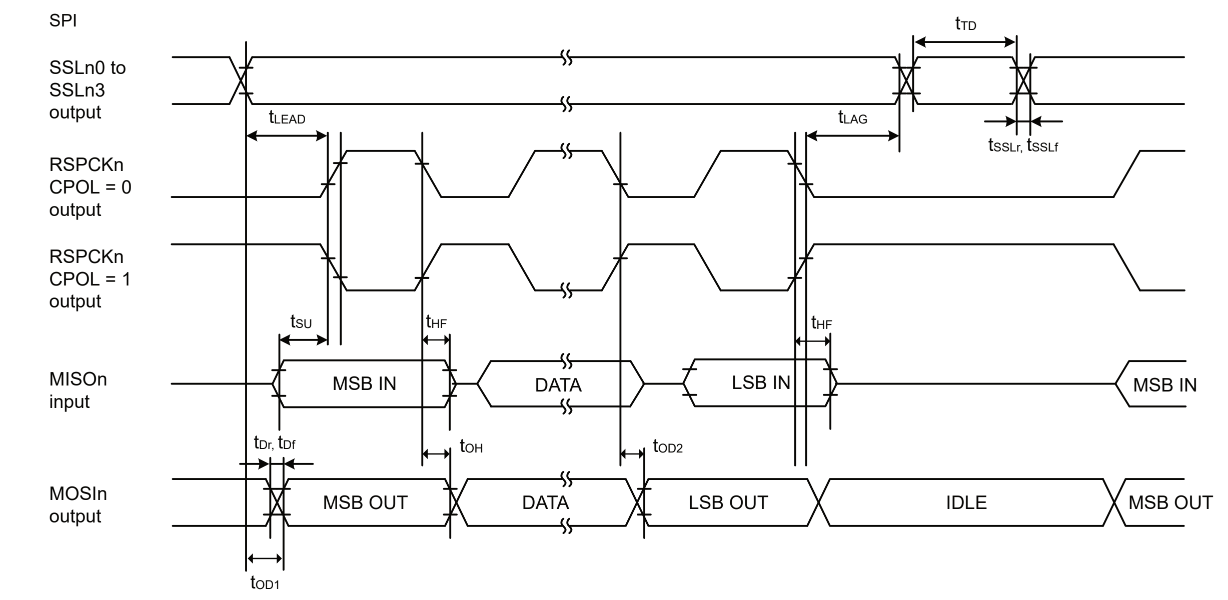
Note: n = A or B

Figure 2.34 SPI时钟定时



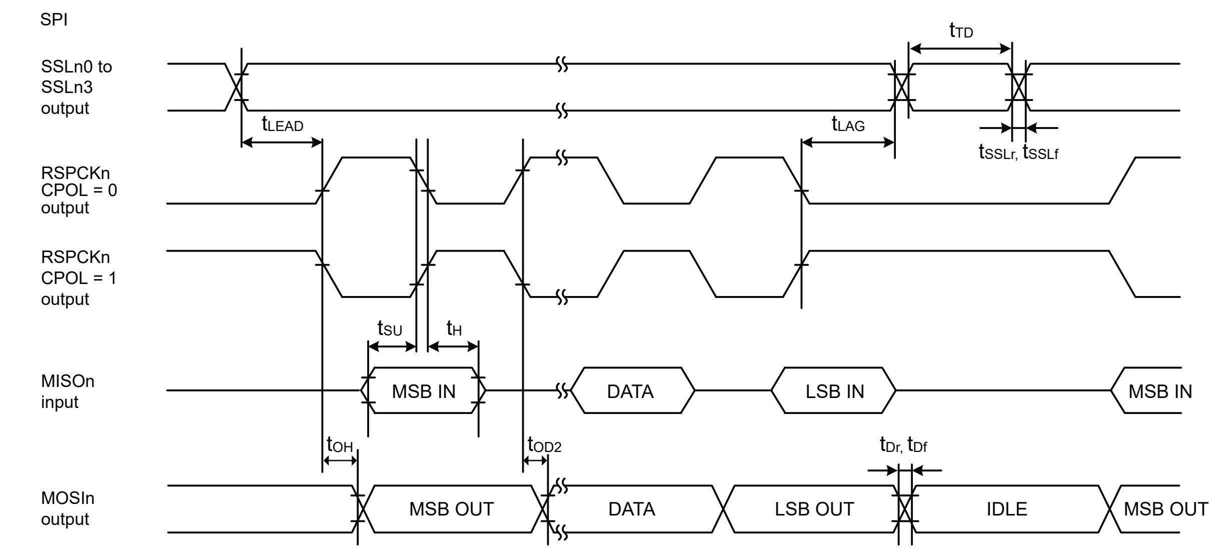
Note: n = A or B

Figure 2.35 CPHA=0时主机的SPI时序



Note: n = A or B

Figure 2.36 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



Note: n = A or B

Figure 2.37 SPI timing for master when CPHA = 1

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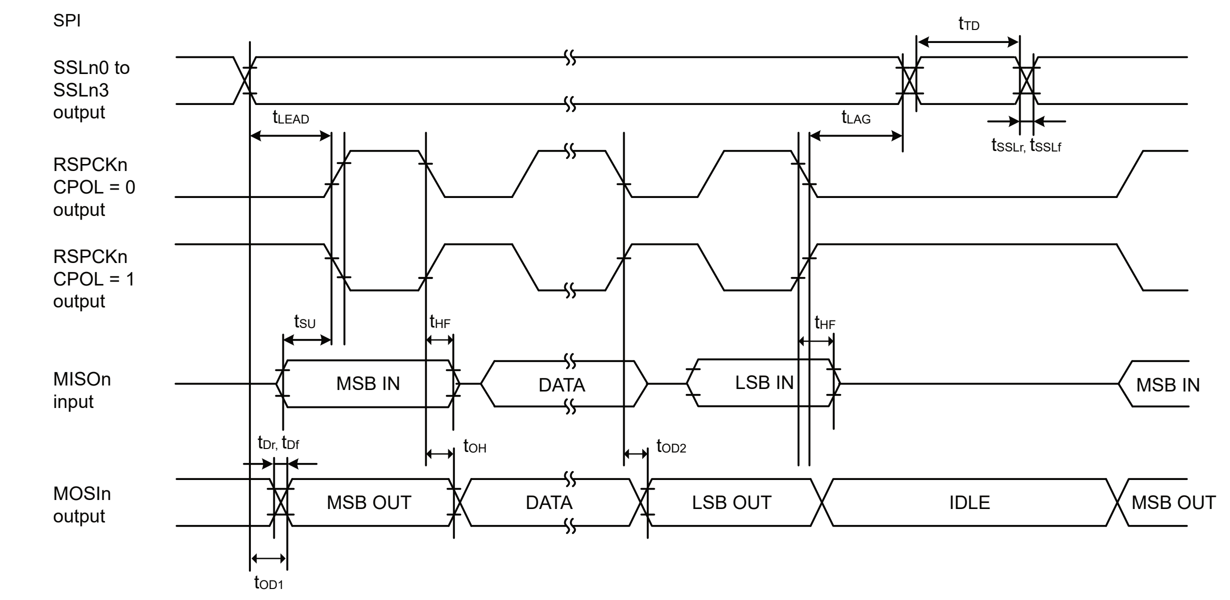
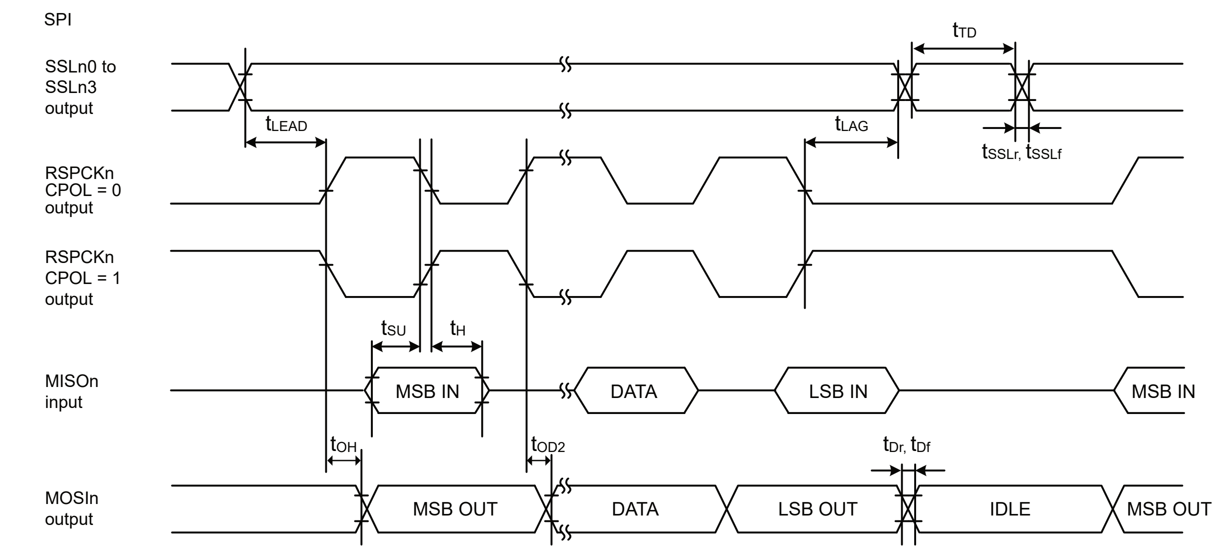


Note: n = A or B

Figure 2.36 当CPHA=0并且比特率设置为PCLKA2时，主机的SPI定时



Note: n = A or B

Figure 2.37 CPHA=1时主机的SPI时序

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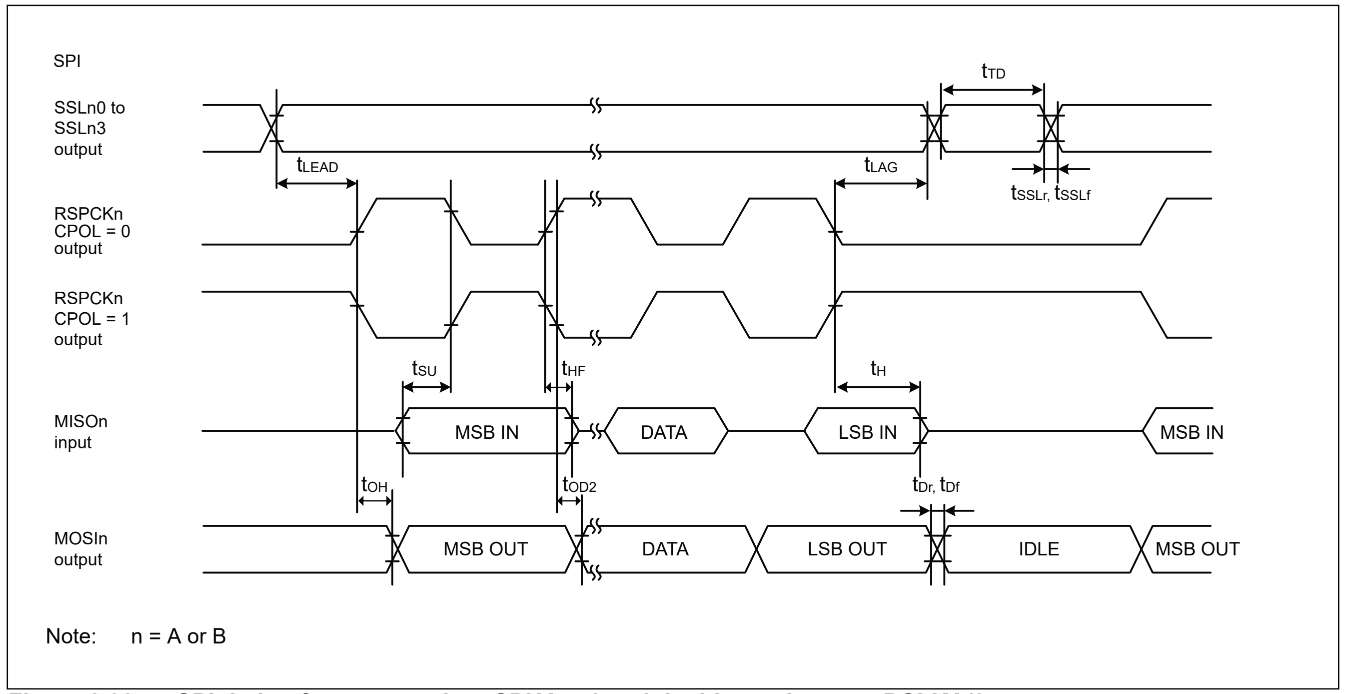


Figure 2.38 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

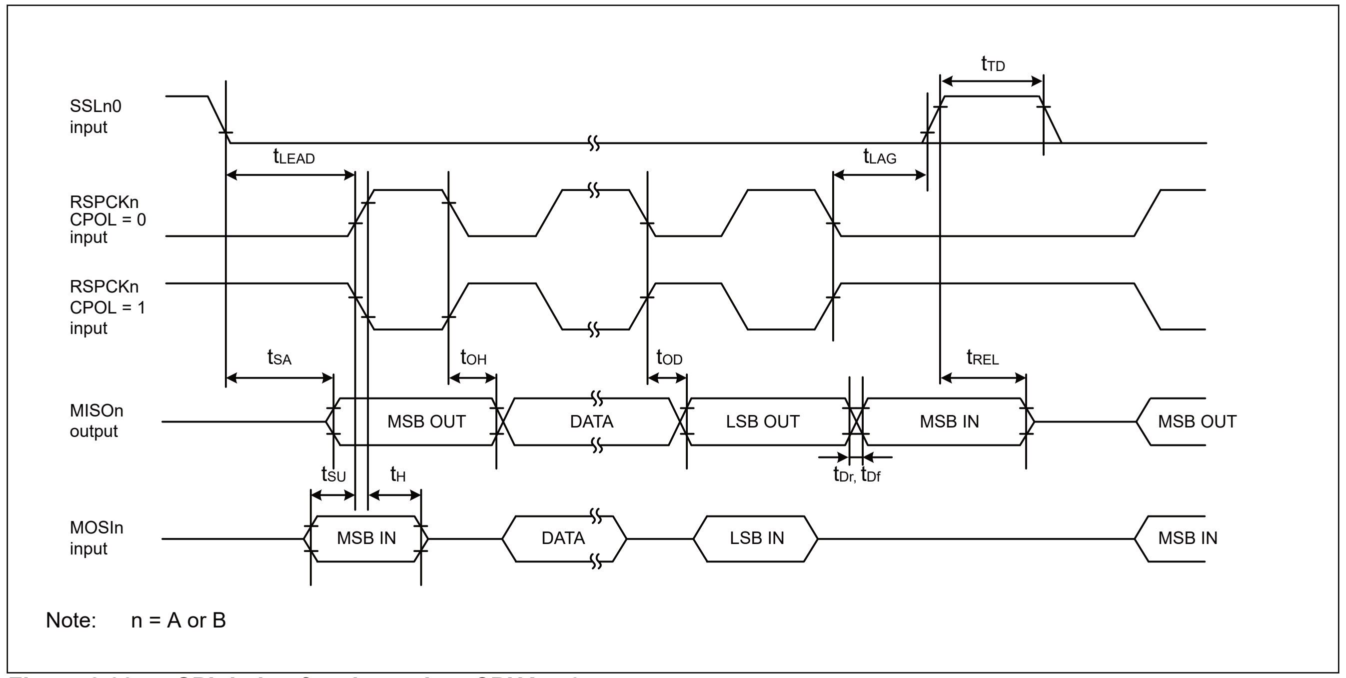


Figure 2.39 SPI timing for slave when CPHA = 0

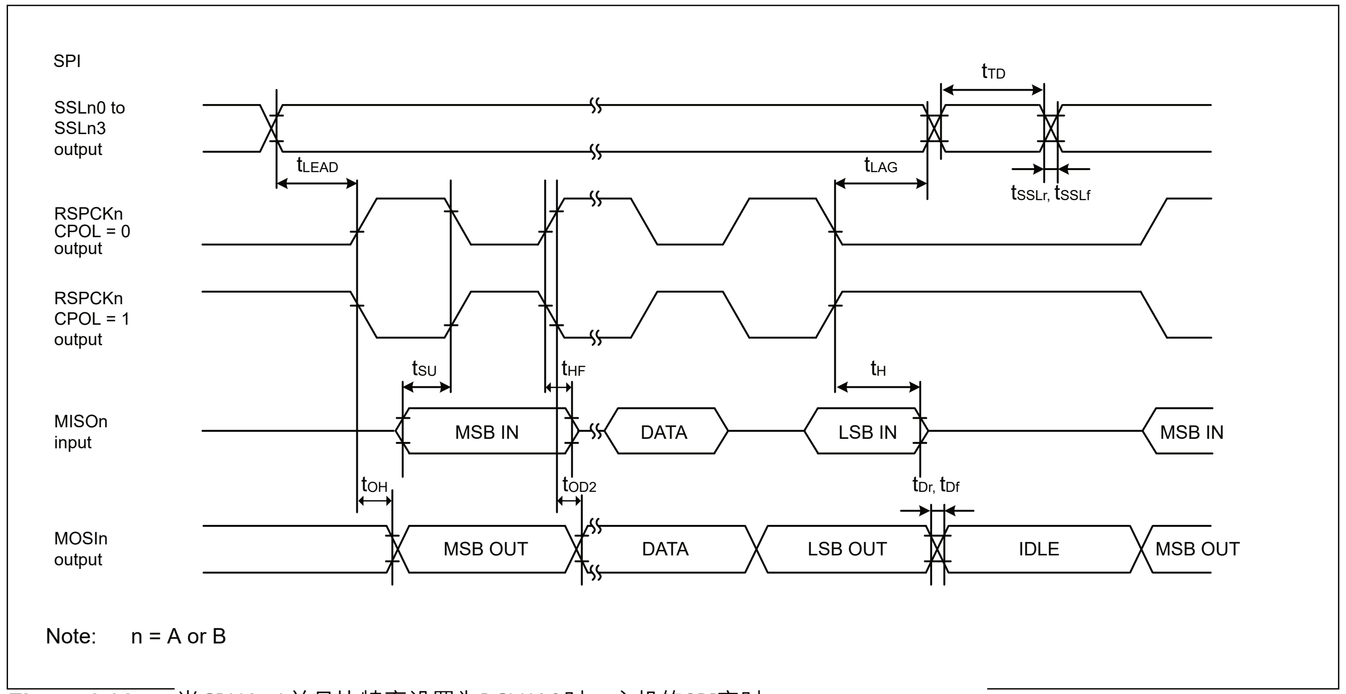


Figure 2.38 当CPHA=1并且比特率设置为PCLKA2时，主机的SPI定时

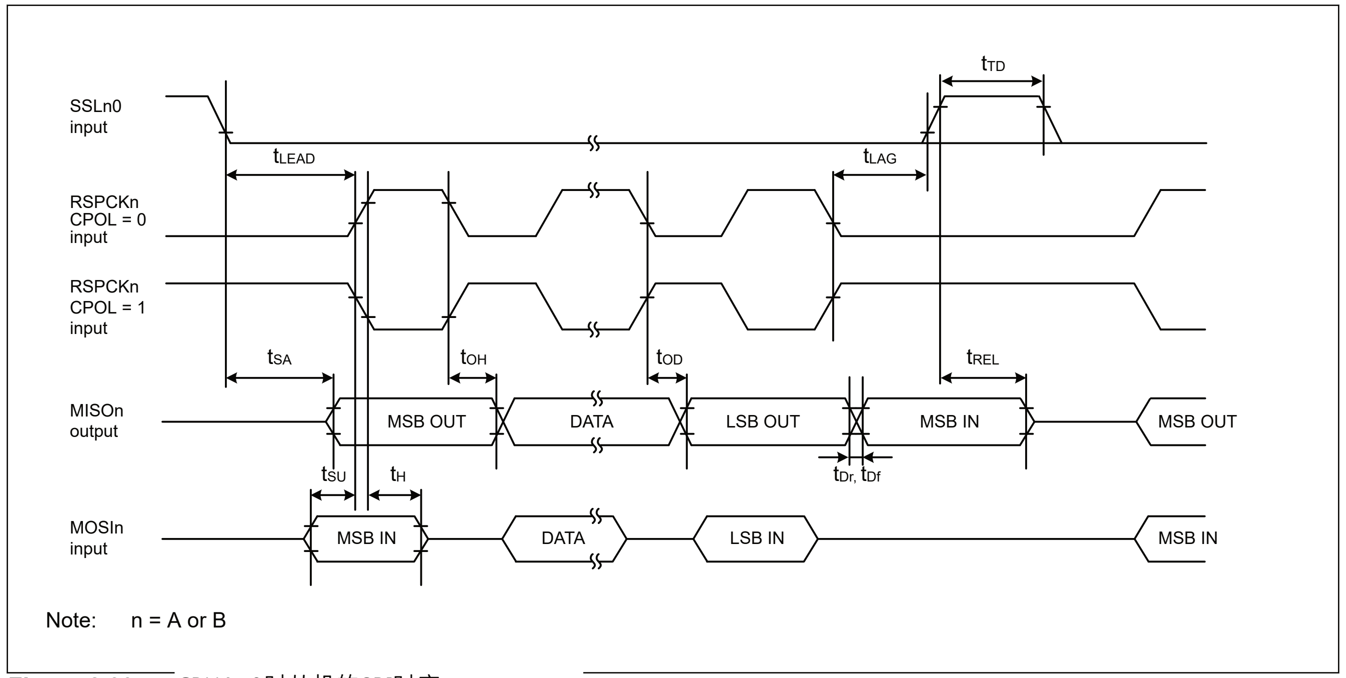
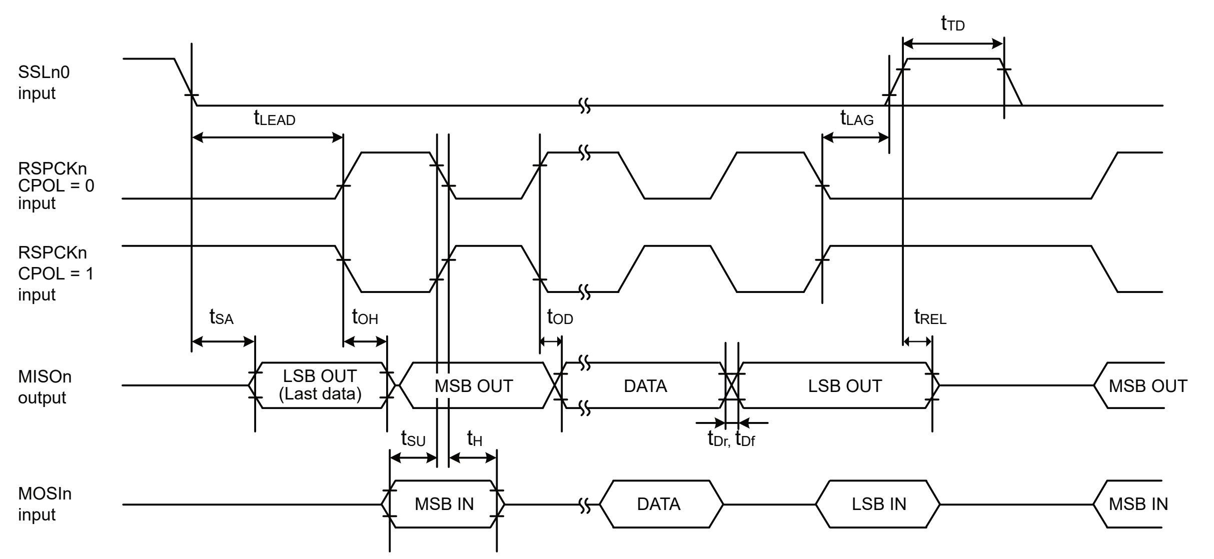


Figure 2.39 CPHA=0时从机的SPI时序



Note: n = A or B

Figure 2.40 SPI timing for slave when CPHA = 1

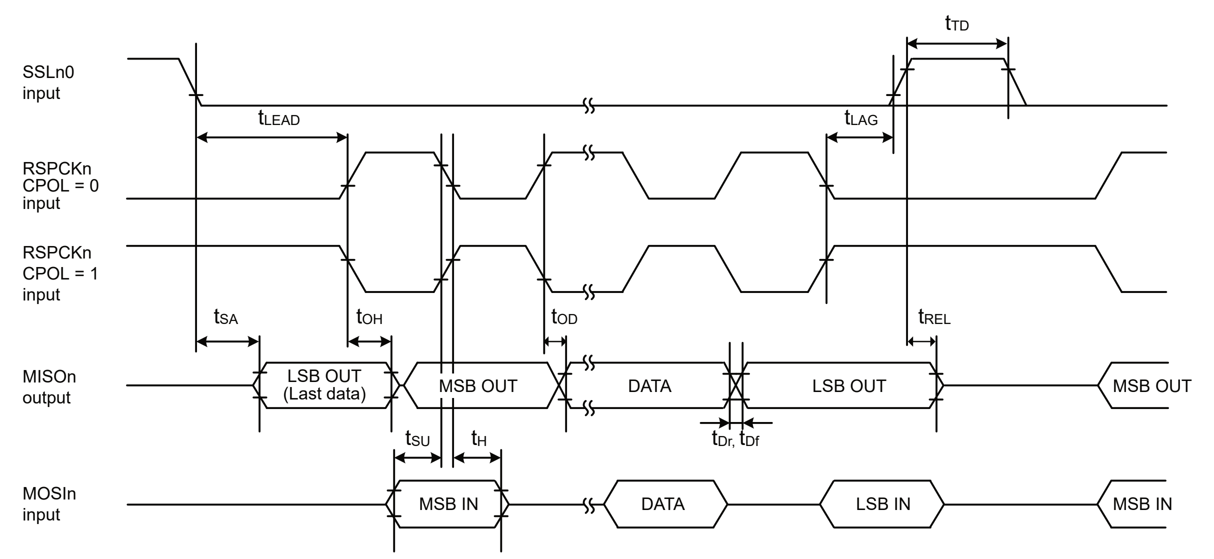
2.3.10 QSPI Timing

Table 2.28 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.41
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	Data input setup time	t_{Su}	10	—	ns	Figure 2.42
	Data input hold time	t_{IH}	0	—	ns	
	QSSL setup time	t_{LEAD}	(N + 0.5) × t_{Qscyc} - 5*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	QSSL hold time	t_{LAG}	(N + 0.5) × t_{Qscyc} - 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	Data output delay	t_{OD}	—	4	ns	
	Data output hold time	t_{OH}	–3.3	—	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.



Note: n = A or B

Figure 2.40 CPHA=1时从机的SPI时序

2.3.10 QSPI Timing

Table 2.28 QSPI timing

条件：在PmnPFS寄存器的端口驱动能力位选择高驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
QSPI	QSPCK时钟周期	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.41
	QSPCK时钟高脉冲宽度	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCK时钟低脉冲宽度	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	数据输入设置时间	t_{Su}	10	—	ns	Figure 2.42
	数据输入保持时间	t_{IH}	0	—	ns	
	QSSL设置时间	t_{LEAD}	(N + 0.5) × t_{Qscyc} - 5*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	QSSL保持时间	t_{LAG}	(N + 0.5) × t_{Qscyc} - 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	数据输出延迟	t_{OD}	—	4	ns	
	数据输出保持时间	t_{OH}	–3.3	—	ns	
	连续传输延迟	t_{TD}	1	16	t_{QScyc}	

注：tPcyc：PCLKA循环。注1。N在SFMSLD中设置为0或1。注2。N在SFMSHD中设置为0或1。

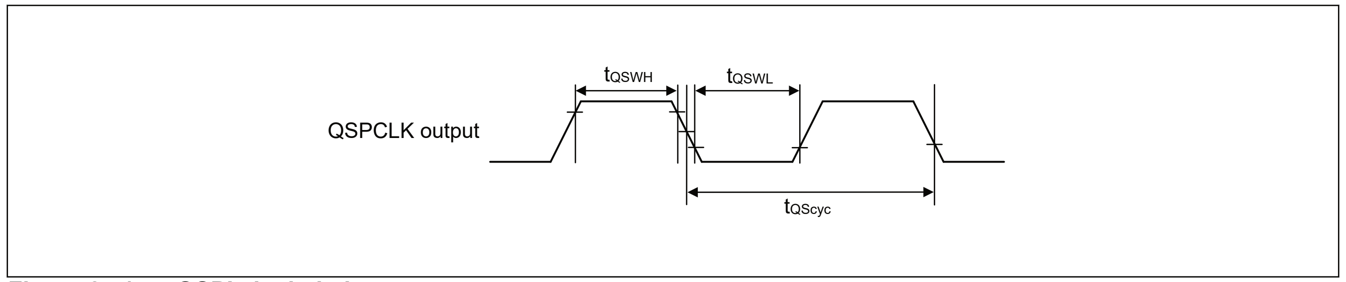


Figure 2.41 QSPI clock timing

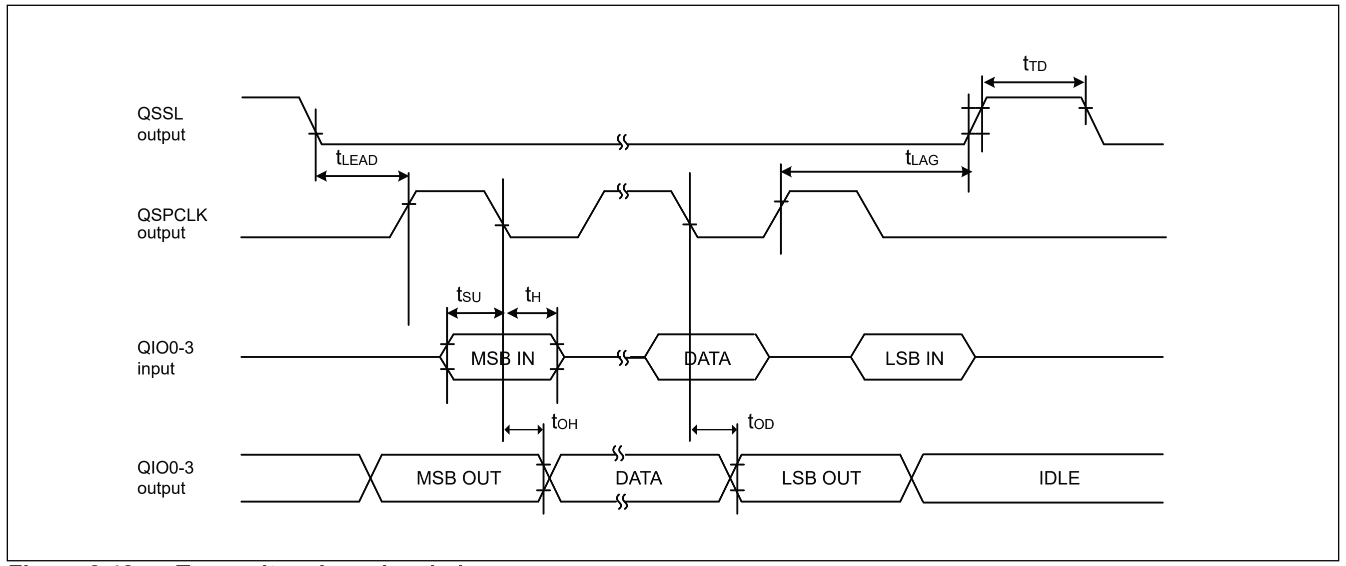


Figure 2.42 Transmit and receive timing

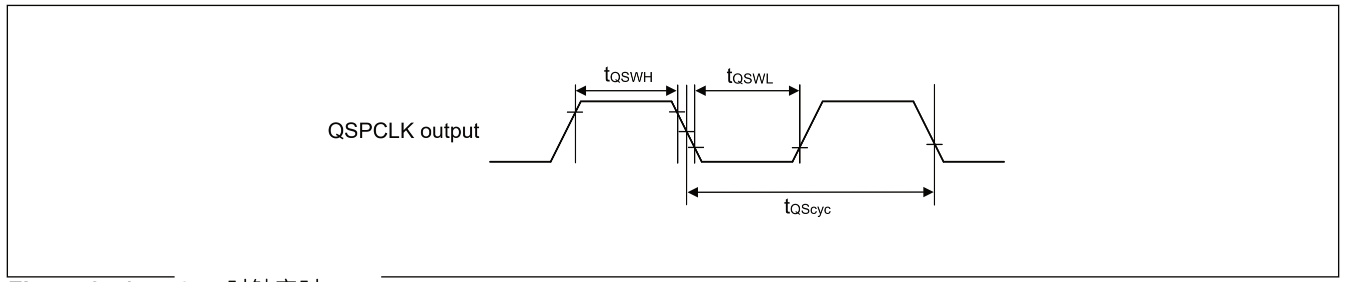


Figure 2.41 QSPI时钟定时

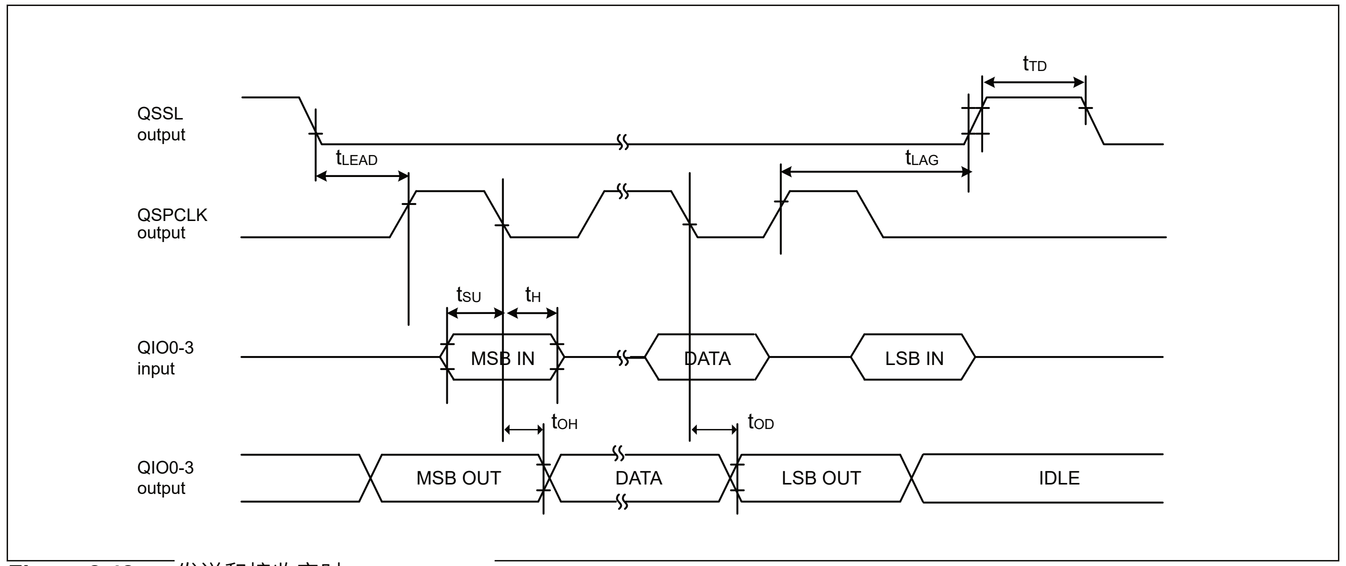


Figure 2.42 发送和接收定时

2.3.11 I3C Timing

Table 2.29 IIC timing(1)-1

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. C_b indicates the total capacity of the bus line.

2.3.11 I3C Timing

Table 2.29 IIC timing(1)-1

1.条件：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择以下引脚：SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。
2.以下引脚不需要设置：SDA0_D，SCL0_D。
3.使用在其名称后面附加了字母（例如"_A"或"_B"）的引脚来指示组成员身份。对于IIC接口，针对每个组测量电特性的AC部分。

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL输入周期时间	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL输入高脉冲宽度	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL输入低脉冲宽度	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL，SDA上升时间	t_{Sr}	—	1000	ns
	SCL SDA秋季时间	t_{Sf}	—	300	ns
	SCL，SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	禁用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	启用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	启动条件禁用唤醒功能时输入保持时间	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	启动条件启用唤醒功能时输入保持时间	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	重复启动条件输入设置时间	t_{STAS}	1000	—	ns
	停止条件输入设置时间	t_{STOS}	1000	—	ns
	数据输入设置时间	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	数据输入保持时间	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	400	pF

Note: tI3Ccyc:I3C内部参考时钟(I3Cф)周期，tTcyc:I3CCLK周期。
Note: 当INCTL时，括号中的值适用。DNFS[3:0]设置为0X3，而数字滤波器使用INCTL启用。DNFE设置为1。
注意：必须使用在其名称后面附加字母的引脚，例如"_A"、"_B"，以指示组成员身份。对于IIC接口，针对每个组测量电特性的AC部分。注1。Cb表示公交线路的总容量。

Table 2.30 IIC timing(1)-2

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)[*1]	300	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)[*1]	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b[*2]	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SDA0_D, SCL0_D.
Note 2. C_b indicates the total capacity of the bus line.

Table 2.30 IIC timing(1)-2

1.条件：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择以下引脚：SDA0_A、SCL0_A、SDA0_B、SCL0_B、SDA0_C、SCL0_C。

2.以下引脚不需要设置：SDA0_D，SCL0_D。

3.使用在其名称后面附加了字母（例如"_A"或"_B"）的引脚来指示组成员身份。对于IIC接口，针对每个组测量电特性的AC部分。

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode)	SCL输入周期时间	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL输入高脉冲宽度	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL输入低脉冲宽度	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL，SDA上升时间	t_{Sr}	20 × (external pullup voltage/5.5 V)[*1]	300	ns
	SCL SDA秋季时间	t_{Sf}	20 × (external pullup voltage/5.5 V)[*1]	300	ns
	SCL，SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	禁用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	启用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	启动条件禁用唤醒功能时输入保持时间	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	启动条件启用唤醒功能时输入保持时间	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	重复启动条件输入设置时间	t_{STAS}	300	—	ns
	停止条件输入设置时间	t_{STOS}	300	—	ns
	数据输入设置时间	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	数据输入保持时间	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b[*2]	—	400	pF

Note: tI3Ccyc:I3C内部参考时钟(I3Cϕ)周期，tTcyc:I3CCLK周期。
Note: 当INCTL时，括号中的值适用。DNFS[3:0]设置为0X3，而数字滤波器使用INCTL启用。DNFE设置为1。
注意：必须使用在其名称后面附加字母的引脚，例如"_A"、"_B"，以指示组成员身份。对于IIC接口，针对每个组测量电特性的AC部分。注1。仅支持SDA0_D、SCL0_D。

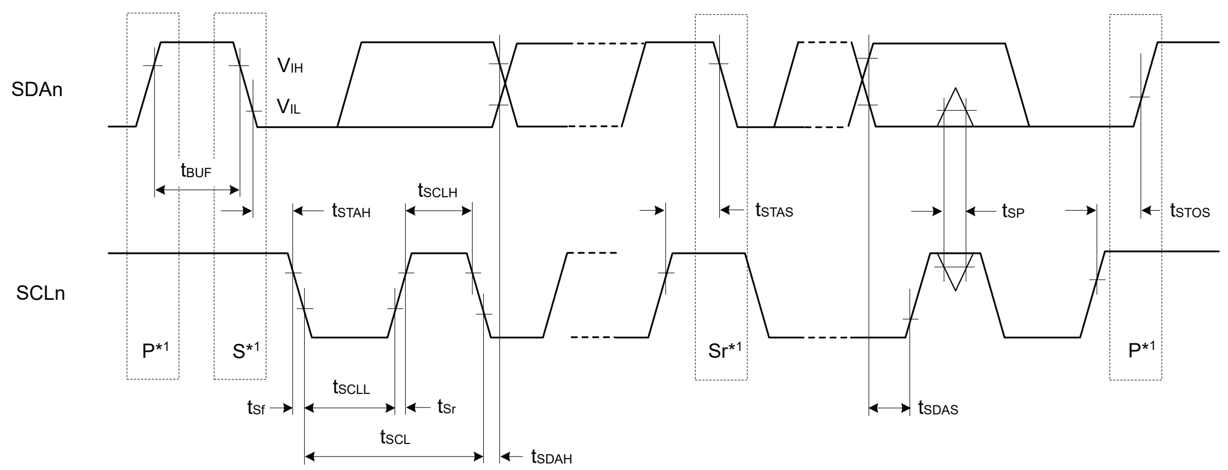
注2。Cb表示公交线路的总容量。

Table 2.31 IIC timing(1)-3

Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	Restart condition input setup time	t_{STAS}	120	—	ns
	Stop condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b *1	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

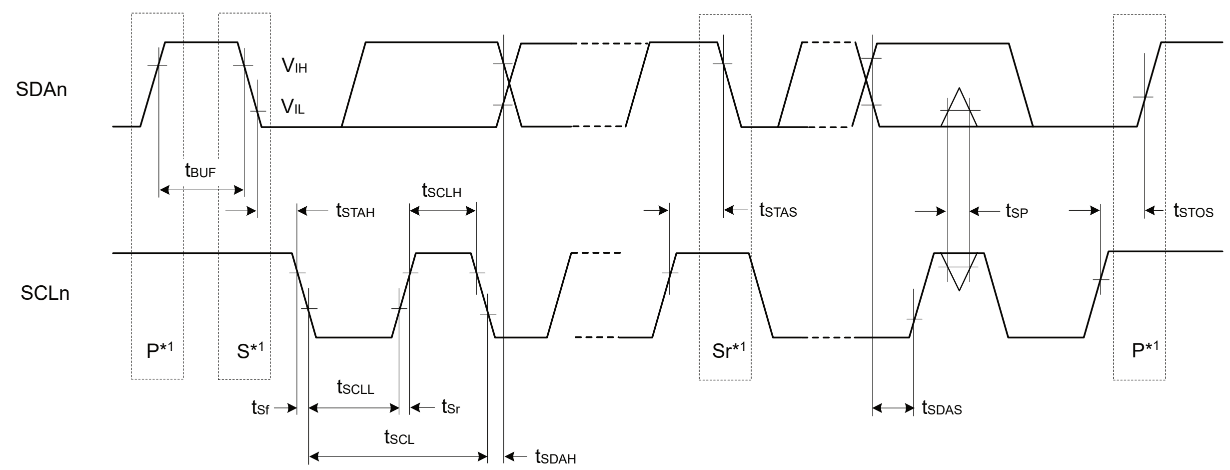
Figure 2.43 I²C bus interface input/output timing

Table 2.31 IIC timing(1)-3

PmnPFS寄存器中的端口驱动能力位不需要设置SDA0_D、SCL0_D引脚。

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL输入周期时间	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL输入高脉冲宽度	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL输入低脉冲宽度	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL，SDA上升时间	t_{Sr}	—	120	ns
	SCL SDA秋季时间	t_{Sf}	20 × (external pullup voltage/5.5 V)	120	ns
	SCL，SDA输入尖峰脉冲去除时间	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	禁用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	启用唤醒功能时SDA输入总线空闲时间	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	启动条件禁用唤醒功能时输入保持时间	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	启动条件启用唤醒功能时输入保持时间	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	重新启动条件输入设置时间	t_{STAS}	120	—	ns
	停止条件输入设置时间	t_{STOS}	120	—	ns
	数据输入设置时间	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	数据输入保持时间	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b *1	—	550	pF

Note: tI3Ccyc:I3C内部参考时钟(I3Cφ)周期，tTcyc:I3CCLK周期。
Note: 当INCTL时，括号中的值适用。DNFS[3:0]设置为0X3，而数字滤波器使用INCTL启用。DNFE设置为1。
注1。Cb表示公交线路的总容量。



注1。S、P和Sr表示以下条件:
S：启动条件P：
停止条件
Sr:重新启动条件

Figure 2.43 I2c总线接口输入输出时序

Table 2.32 IIC timing(2)

Conditions: VCC = 3.00 to 3.60 V
Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	10	—	ns
	Data input hold time	Cb = 400 pF	t_{SDAH}	0	150	ns
		Cb = 100 pF		0	70	
	SCL, SDA capacitive load		C_b *1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

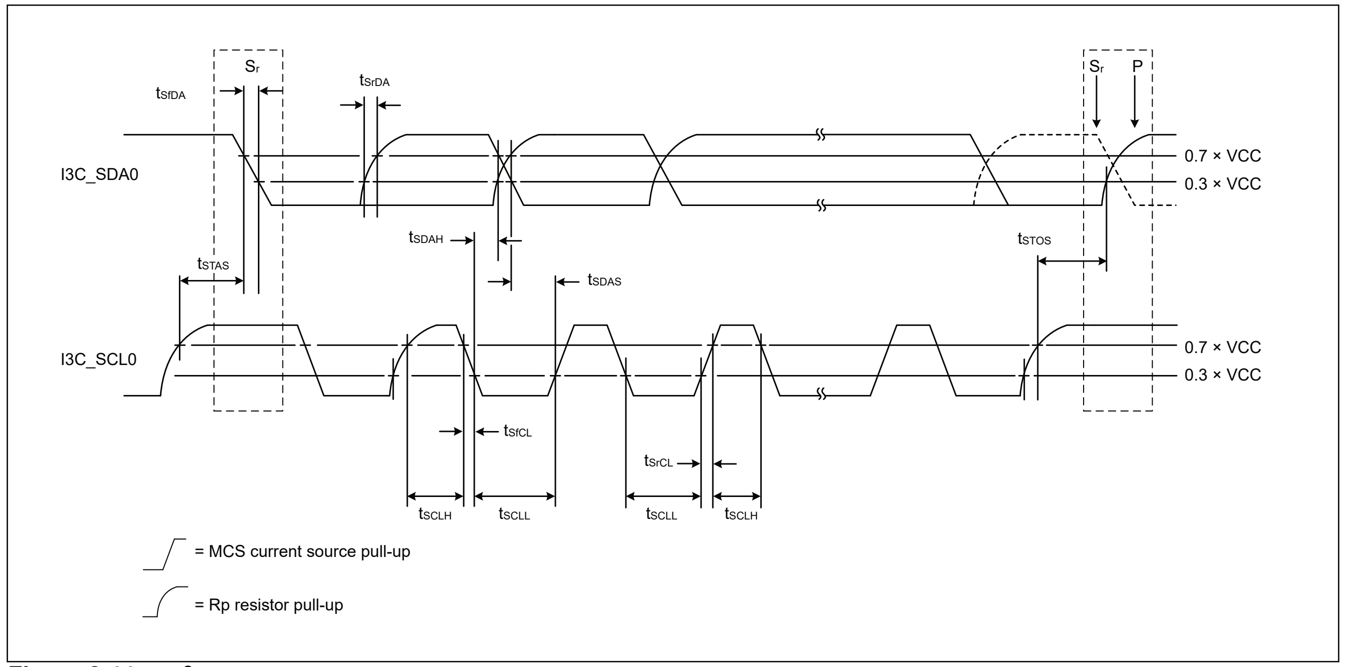


Figure 2.44 I²C bus interface input/output timing (Hs-mode)

Table 2.32 IIC timing(2)

Conditions: VCC = 3.00 to 3.60 V
PmnPFS寄存器中的端口驱动能力位不需要设置SDA0_D、SCL0_D引脚。

Parameter			Symbol	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL输入周期时间		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
	SCL输入高脉冲宽度	Cb = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL输入低脉冲宽度	Cb = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL上升时间	Cb = 400 pF	t_{SrCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA上升时间	Cb = 400 pF	t_{SrDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL秋季时间	Cb = 400 pF	t_{SfCL}	—	80	ns
		Cb = 100 pF		—	40	
	Sda秋季时间	Cb = 400 pF	t_{SfDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL，SDA输入尖峰脉冲去除时间		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	重复启动条件输入设置时间		t_{STAS}	40	—	ns
	停止条件输入设置时间		t_{STOS}	40	—	ns
	数据输入设置时间		t_{SDAS}	10	—	ns
	数据输入保持时间	Cb = 400 pF	t_{SDAH}	0	150	ns
		Cb = 100 pF		0	70	
	SCL, SDA capacitive load		C_b *1	—	400	pF

Note: tI3Ccyc:I3C内部参考时钟(I3Cφ)周期。
Note: 当INCTL时，括号中的值适用。DNFS[3:0]设置为0X3，而数字滤波器使用INCTL启用。DNFE设置为1。
注1。Cb表示公交线路的总容量。

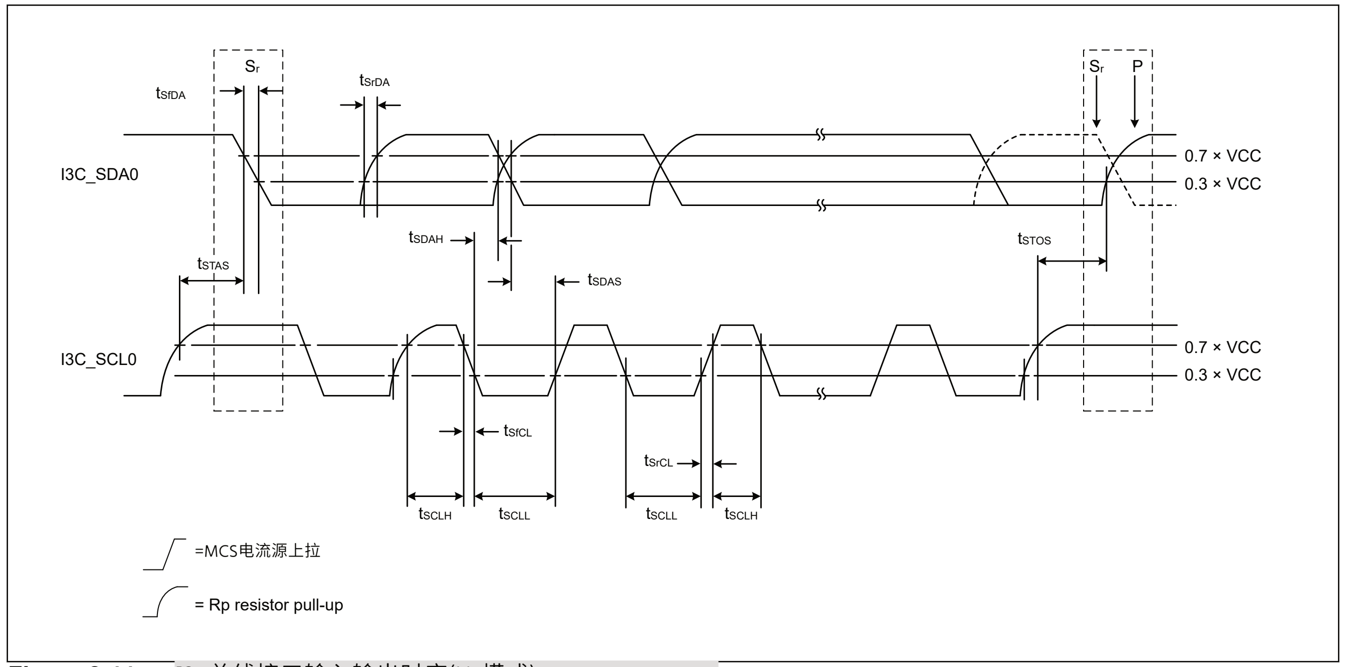


Figure 2.44 I2c总线接口输入输出时序(Hs模式)

Table 2.33 I3C timing (open drain timing parameters)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	200	—	ns	Figure 2.47
		$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 2.47
	SCL Clock High Period	t_{HIGH} *3 *4	—	41	ns	Figure 2.45
		t_{DIG_H}	—	$t_{HIGH} + t_{CF}$	ns	Figure 2.45
	SDA Signal Fall Time	t_{fDA_OD}	t_{CF}	12	ns	Figure 2.47
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	17	—	ns	Figure 2.46
	Clock After START (S) Condition	t_{CAS} *5 *6	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.47
				For ENAS1: 100 µ		
				For ENAS2: 2 milli		
				For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 2.48
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.53
	Bus Available Condition	t_{AVAL} *7	1	—	µs	—
	Bus Idle Condition	t_{IDLE}	1	—	ms	—
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 2.53

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.
Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH
Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect
Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^{2}C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.
Note 5. On a legacy bus where I^{2}C devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a mixed bus with Fm Legacy I^{2}C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.33 I3C时序（开漏时序参数）

Conditions: VCC = 3.00 to 3.60 V
PmnPFS寄存器中的端口驱动能力位不需要设置I3C_SDA、I3C_SCL引脚。

Parameter		Symbol	Min	Max	Unit	测试条件
I3C 开漏定时 Parameters	SCL时钟低周期	t_{LOW_OD} *1 *2	200	—	ns	Figure 2.47
		$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 2.47
	SCL时钟高周期	t_{HIGH} *3 *4	—	41	ns	Figure 2.45
		t_{DIG_H}	—	$t_{HIGH} + t_{CF}$	ns	Figure 2.45
	SDA信号下降时间	t_{fDA_OD}	t_{CF}	12	ns	Figure 2.47
	Sda数据设置时间打开排水模式	t_{SU_OD} *1	17	—	ns	Figure 2.46
	启动后的时钟条件	t_{CAS} *5 *6	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.47
				For ENAS1: 100 µ		
				对于ENAS2：2毫		
				对于ENAS3:50毫		
	停止前时钟(P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 2.48
	现任硕士至中学切换过程中的主重叠时间	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.53
	巴士可用条件	t_{AVAL} *7	1	—	µs	—
	总线空闲状态	t_{IDLE}	1	—	ms	—
	时间内部新的地方主不驾驶SDA低	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 2.53

注1。这大约等于tLOWmin+TDS_ODmin+trDA_ODtyp+tSU_Odmin。
注2。如果主机知道这是安全的，即SDA已经在VIH以上，则主机可以使用较短的低周期
注3。基于T尖峰、上升和下降时间和互连
注4。当传统的i2c设备可以安全地看到信号时，或者考虑到互连（例如短总线），这个最大高周期可能会被超过。作为产品规格，如果不能保证此最大值，请更改此最大值，并指定它不能在

混合总线。
注5。在传统总线上，i2c设备需要看到开始
注6。不支持可选ENTASxCCCs的奴隶应使用ENTAS3显示的tCAS最大值
注7。在具有FmLegacyI2C器件的混合总线上，tAVAL比Fm总线自由状态时间(tBUF)短300ns

Table 2.34 I3C timing (push-pull timing parameters for SDR mode)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR Mode	SCL Clock Frequency		f_{SCL} [*1]	0.01	12.5	MHz	—
	SCL Clock Low Period		t_{LOW}	24	—	ns	Figure 2.45
			t_{DIG_L} [*2 *4]	40	—	ns	Figure 2.45
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	—	ns	Figure 2.45
			$t_{DIG\_H\_MIXED}$ [*2 *3]	40	45	ns	Figure 2.45
	SCL Clock High Period		t_{HIGH}	24	—	ns	Figure 2.45
			t_{DIG_H} [*2]	40	—	ns	Figure 2.45
	Clock in to Data Out for Slave		t_{SCO}	—	12	ns	Figure 2.50
	SCL Clock Rise Time		t_{CR}	—	150 × 1 /f_{SCL} (capped at 60)	ns	Figure 2.45
	SCL Clock Fall Time		t_{CF}	—	150 × 1 /f_{SCL} (capped at 60)	μs	Figure 2.45
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} [*4]	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.49
		Slave	t_{HD_PP}	0	—	—	Figure 2.49
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	17	N/A	ns	Figure 2.51
	Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	Figure 2.52
	Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	Figure 2.52
	Capacitive Load per Bus Line (SDA/SCL)		C_b	—	50	pF	—

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

Table 2.34 I3C时序（SDR模式的推挽时序参数）

Conditions: VCC = 3.00 to 3.60 V
PmnPFS寄存器中的端口驱动能力位不需要设置I3C_SDA、I3C_SCL引脚。

Parameter			Symbol	Min	Max	Unit	测试条件
I3C Push-Pull Timing SDR模式的参数	SCL时钟频率		f_{SCL} [*1]	0.01	12.5	MHz	—
	SCL时钟低周期		t_{LOW}	24	—	ns	Figure 2.45
			t_{DIG_L} [*2 *4]	40	—	ns	Figure 2.45
	SCL时钟高周期为混合巴士		t_{HIGH_MIXED}	24	—	ns	Figure 2.45
			$t_{DIG\_H\_MIXED}$ [*2 *3]	40	45	ns	Figure 2.45
	SCL时钟高周期		t_{HIGH}	24	—	ns	Figure 2.45
			t_{DIG_H} [*2]	40	—	ns	Figure 2.45
	时钟输入到从站数据输出		t_{SCO}	—	12	ns	Figure 2.50
	SCL时钟上升时间		t_{CR}	—	150 × 1 /f_{SCL} (capped at 60)	ns	Figure 2.45
	SCL时钟下降时间		t_{CF}	—	150 × 1 /f_{SCL} (capped at 60)	μs	Figure 2.45
	Sda信号数据保持在推挽中 Mode	Master	t_{HD_PP} [*4]	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.49
		Slave	t_{HD_PP}	0	—	—	Figure 2.49
	SDA信号数据设置在 Push-Pull Mode		t_{SU_PP}	17	N/A	ns	Figure 2.51
	重复启动后的时钟(Sr)		t_{CASr}	t_{CASmin}	N/A	ns	Figure 2.52
	时钟重复之前 START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	Figure 2.52
	每条总线的容性负载(SDASCL)		C_b	—	50	pF	—

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
注2。tDIG_L和TDIG_H是使用VIL和VIH在i3c总线的接收器端看到的时钟低电平和高电平周期。
注3。在混合总线上与I3C设备通信时，必须限制TDIG_H_MIXED周期，以确保I2C设备不会将I3C信令解释为有效的I2c信令。
注4。由于使用了两个边沿，因此需要满足各自边沿的保持时间，即下降沿时钟为tCF+3，上升沿时钟为tCR+3。

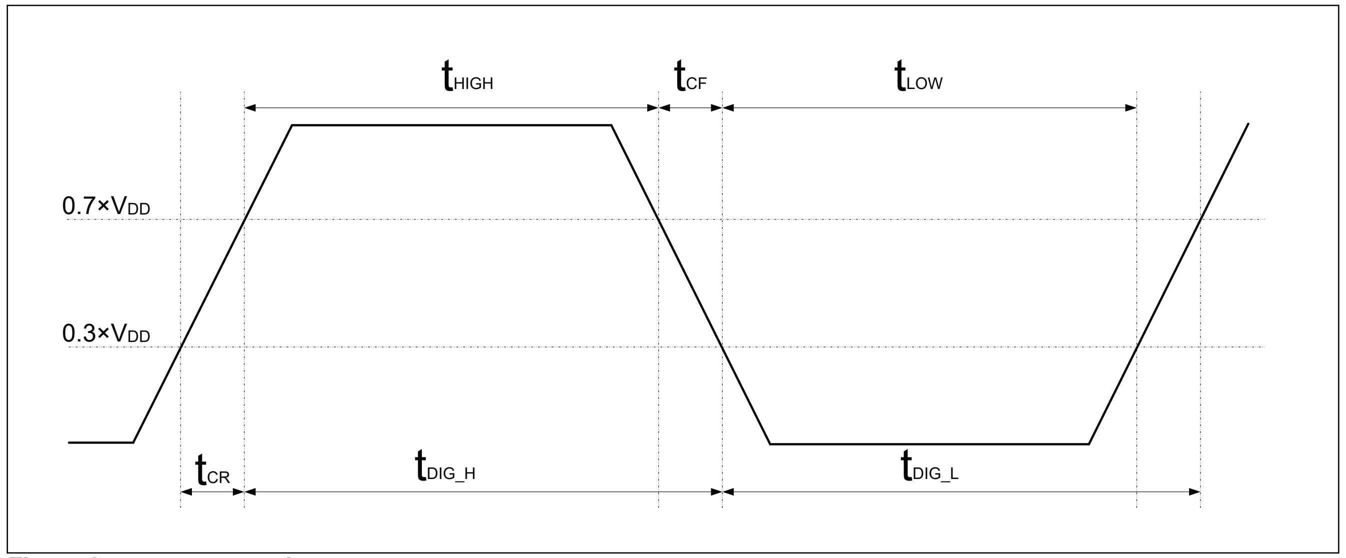


Figure 2.45 t_{DIG_H} and t_{DIG_L}

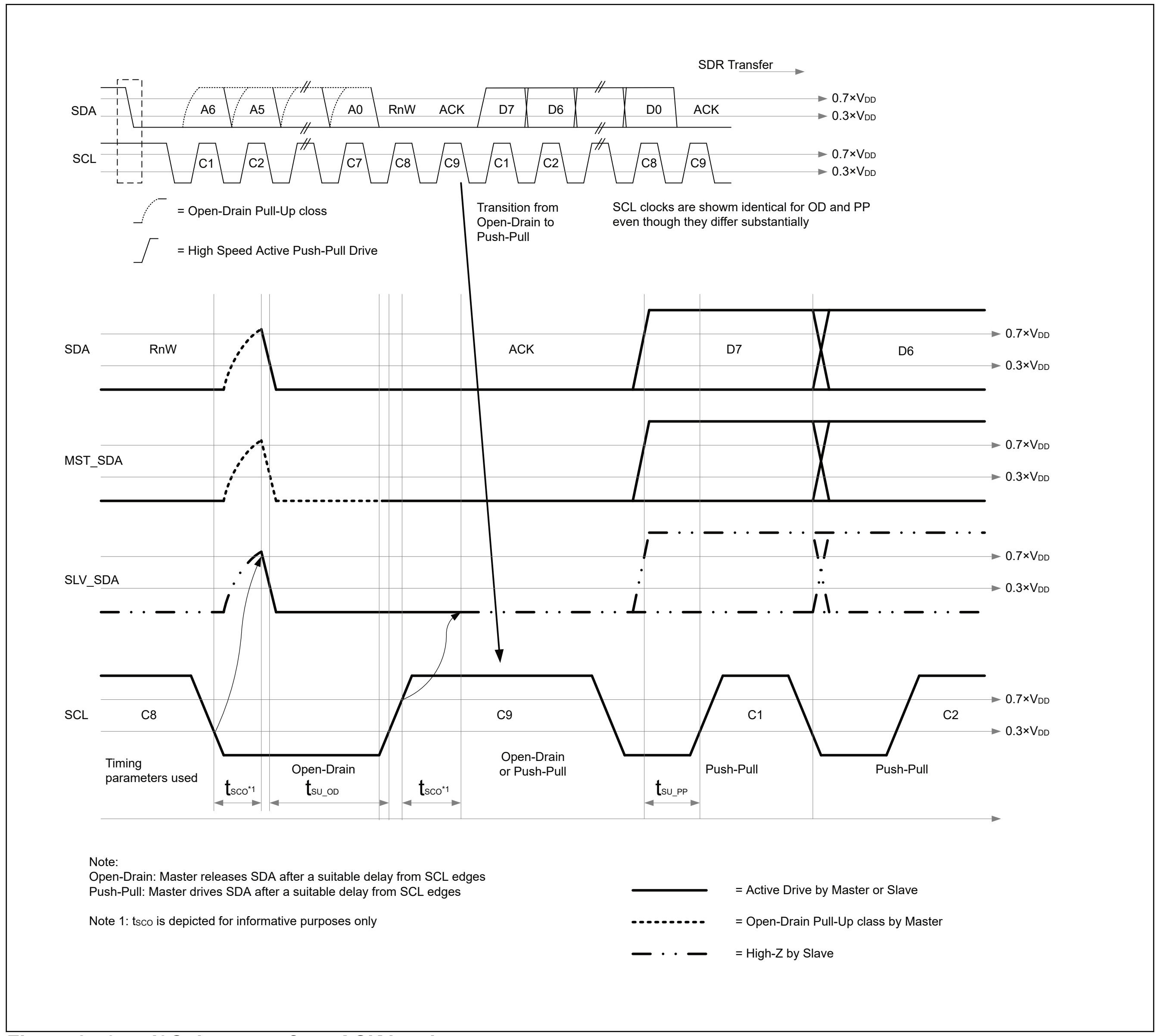


Figure 2.46 I3C data transfer – ACK by slave

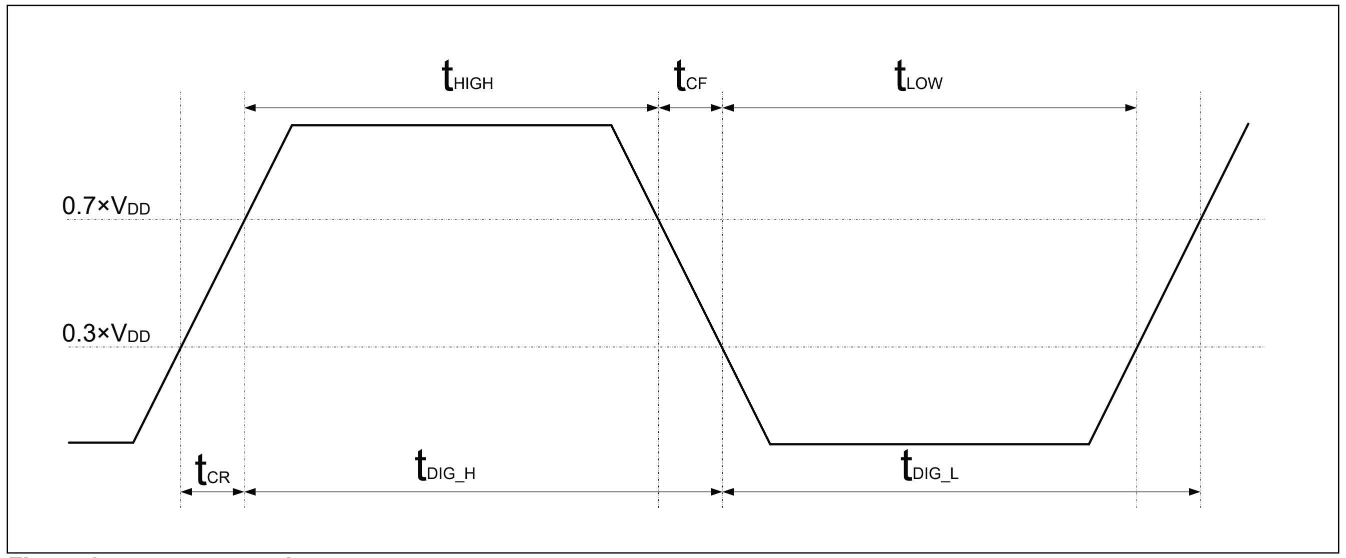


Figure 2.45 t_{DIG_H} and t_{DIG_L}

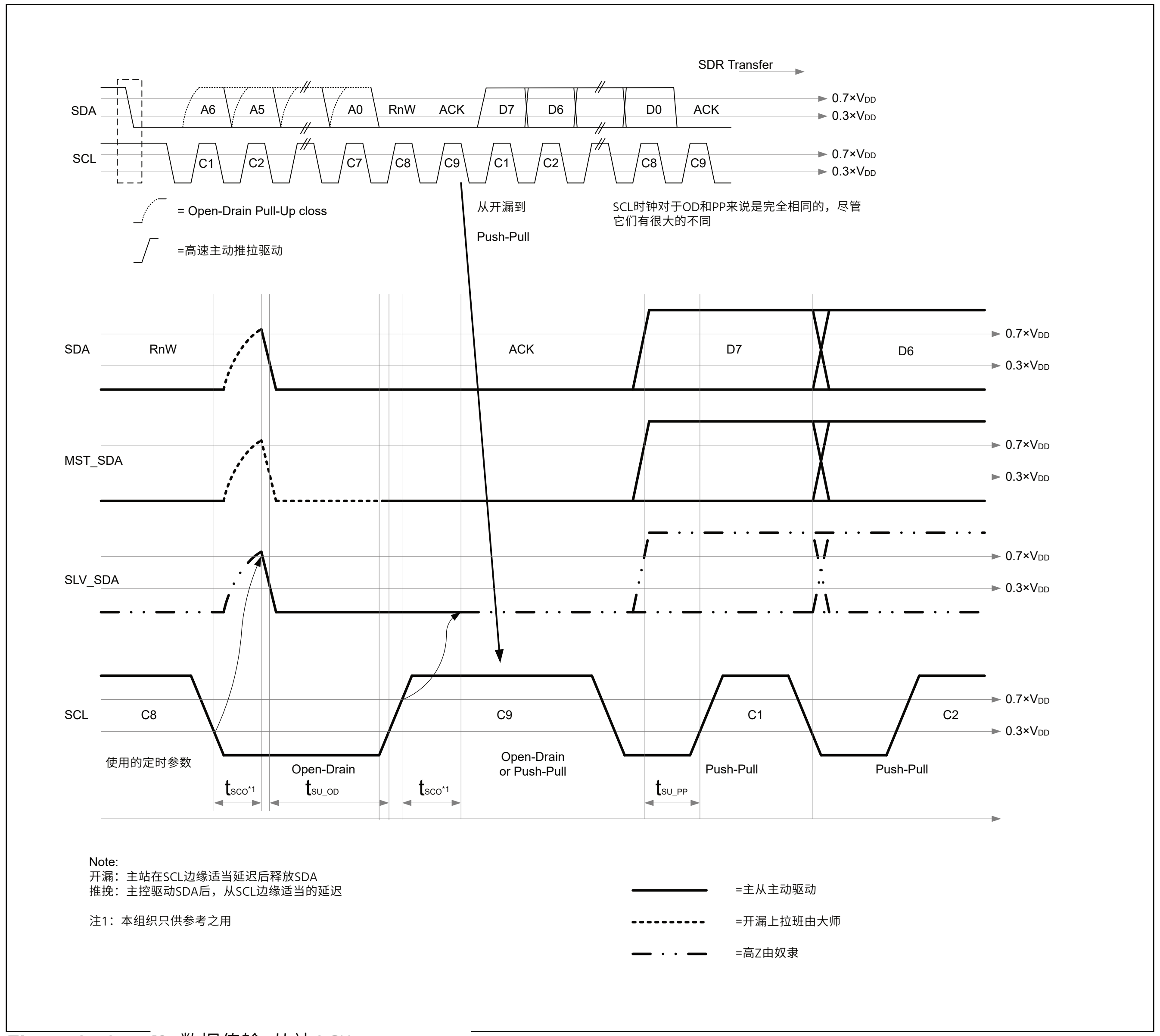


Figure 2.46 I3c数据传输 从站ACK

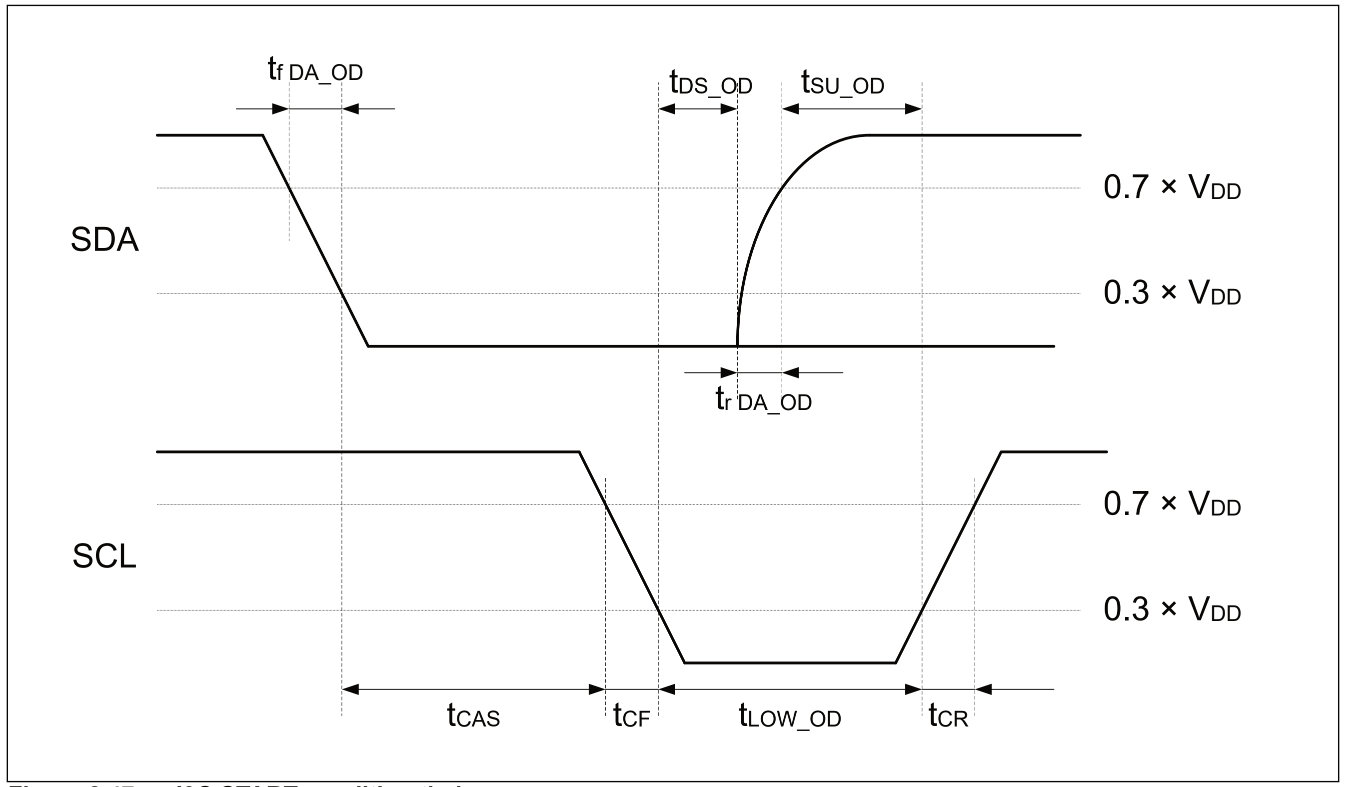


Figure 2.47 I3C START condition timing

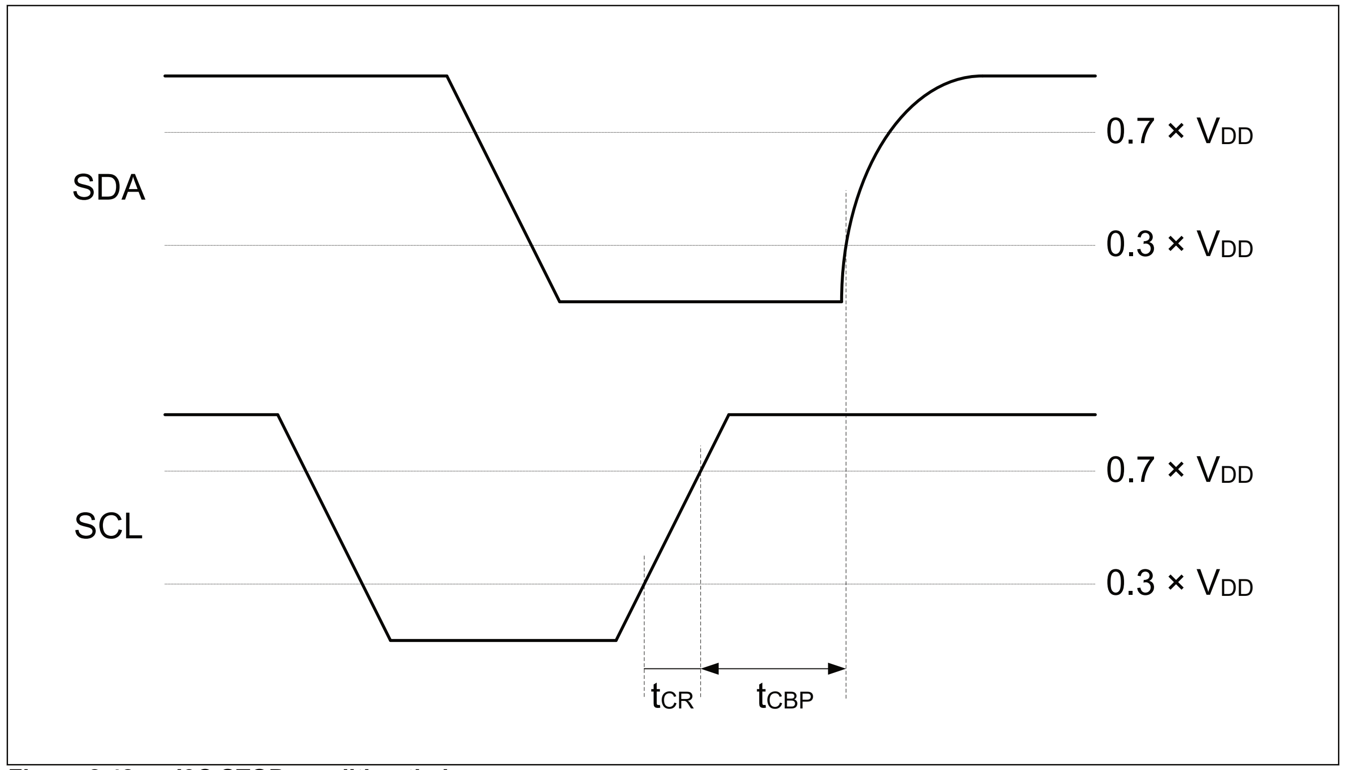


Figure 2.48 I3C STOP condition timing

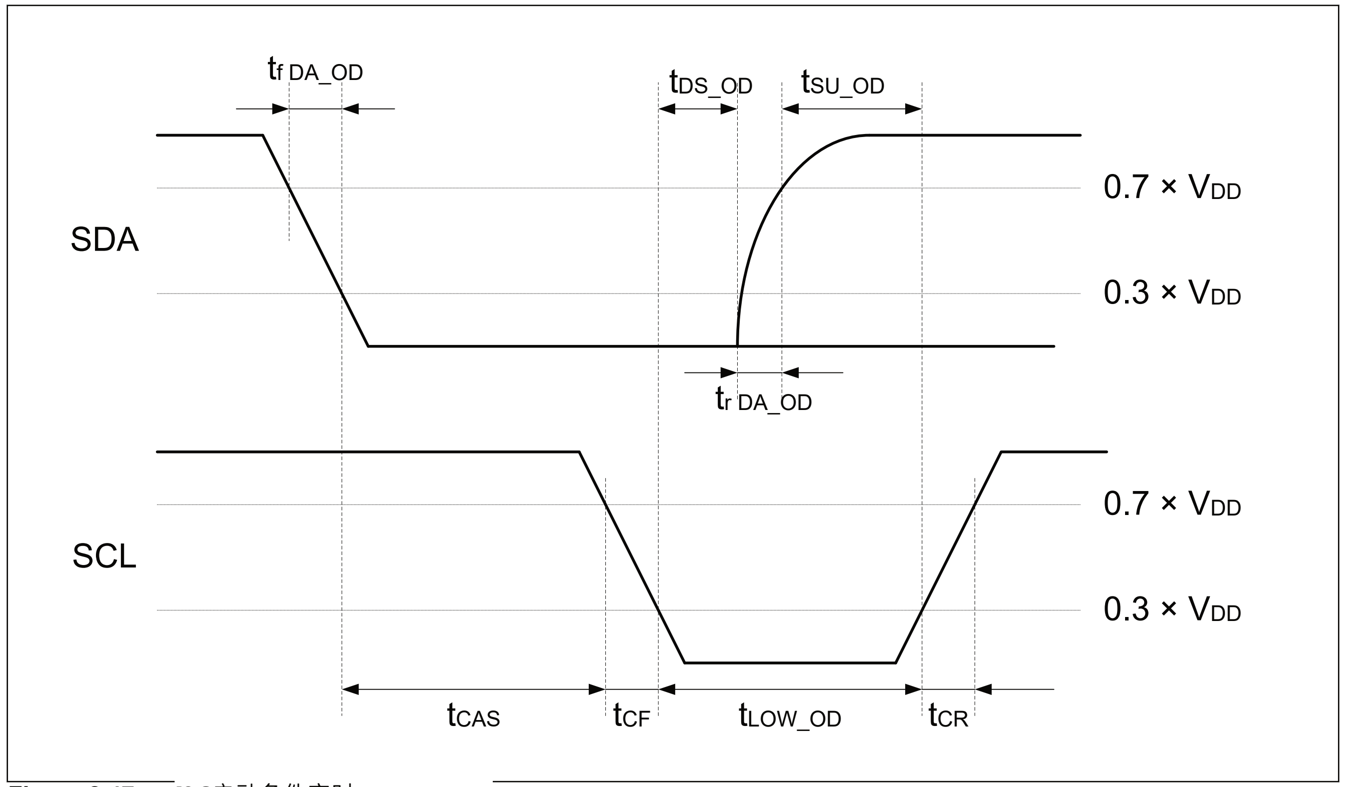


Figure 2.47 I3C启动条件定时

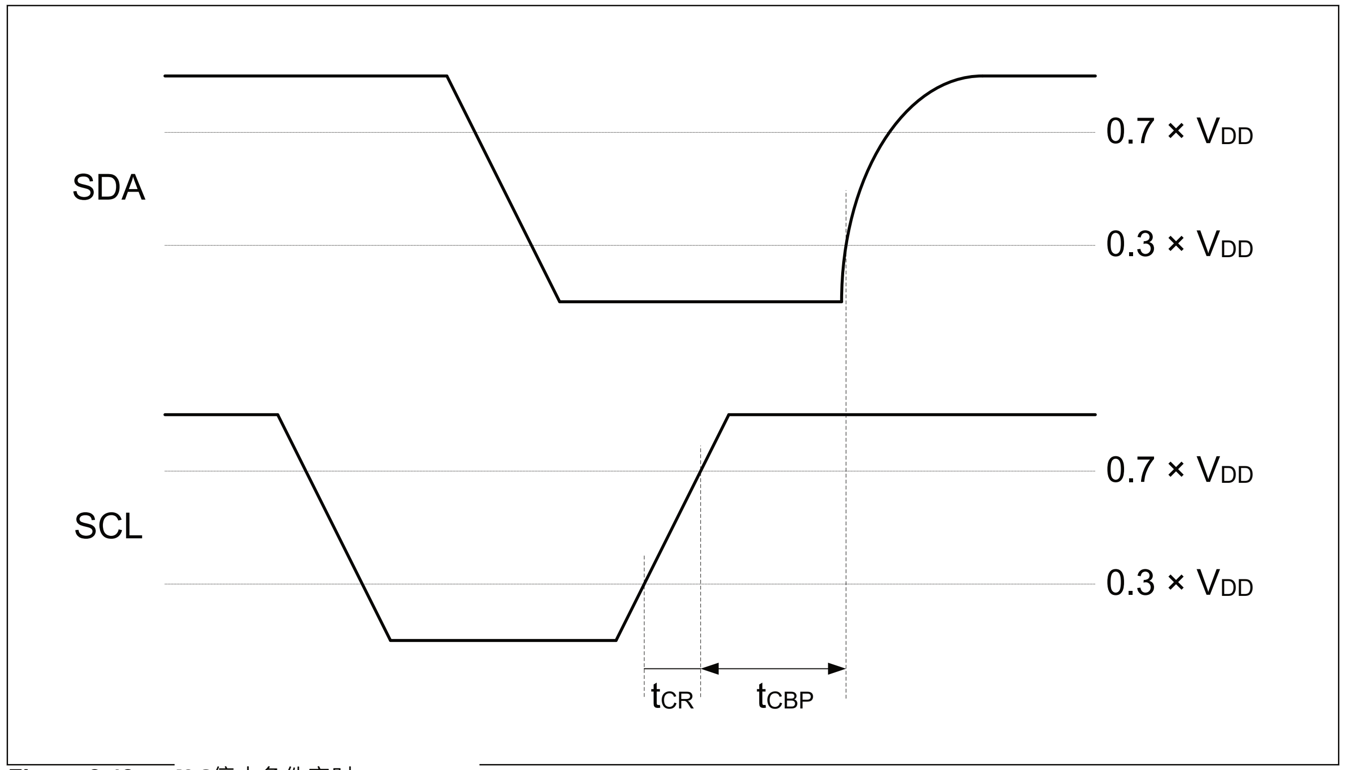


Figure 2.48 I3C停止条件定时

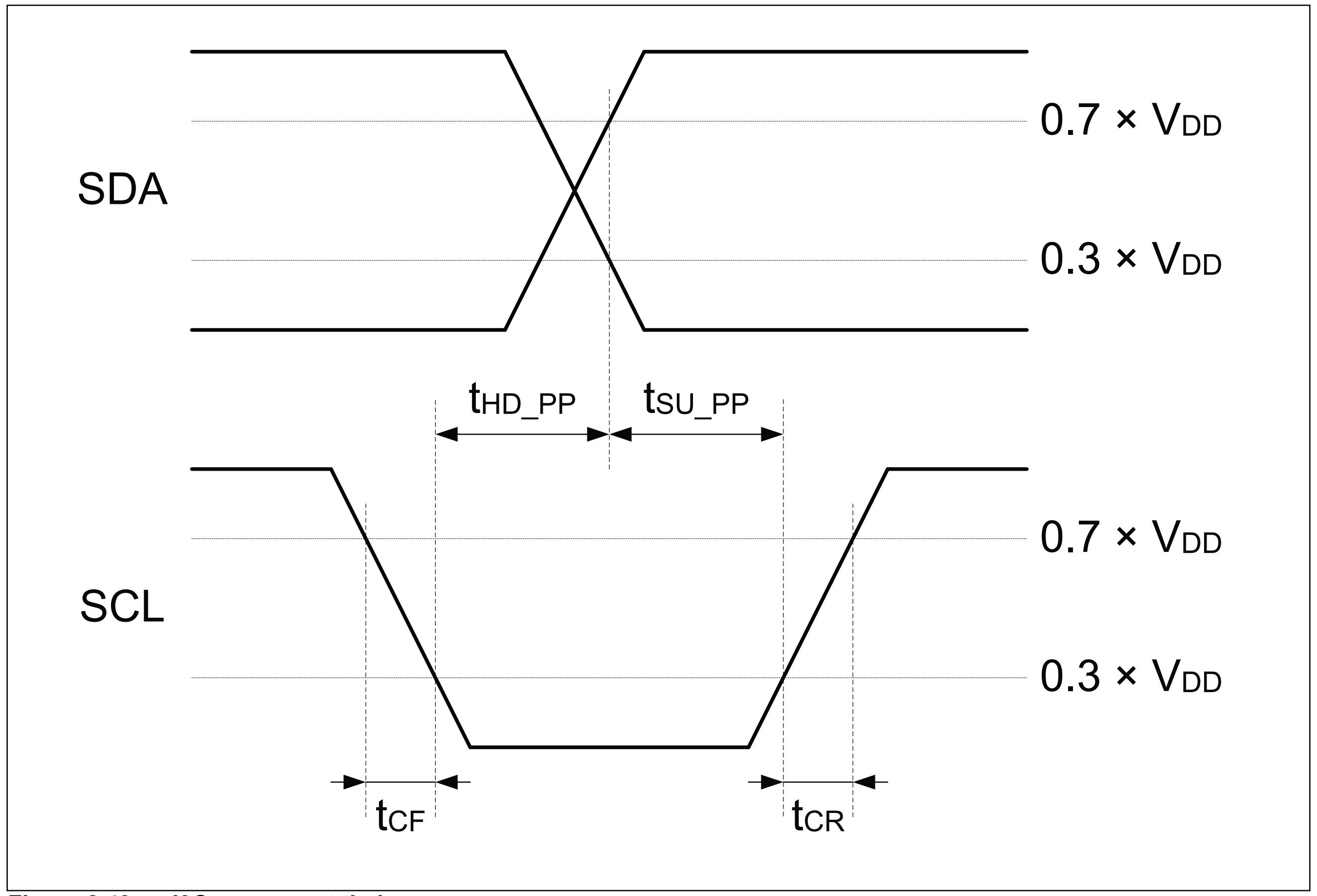


Figure 2.49 I3C master out timing

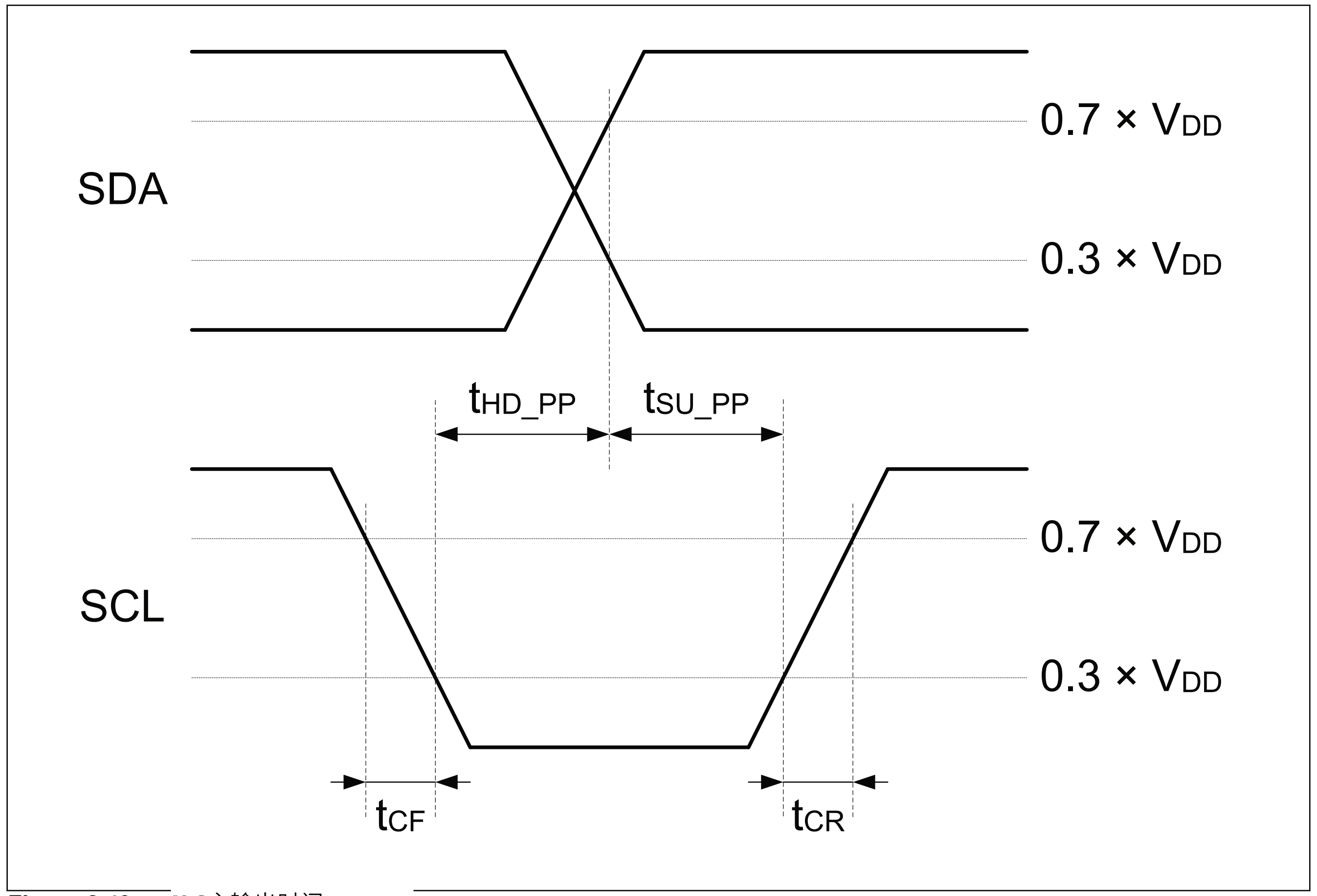


Figure 2.49 I3C主输出时间

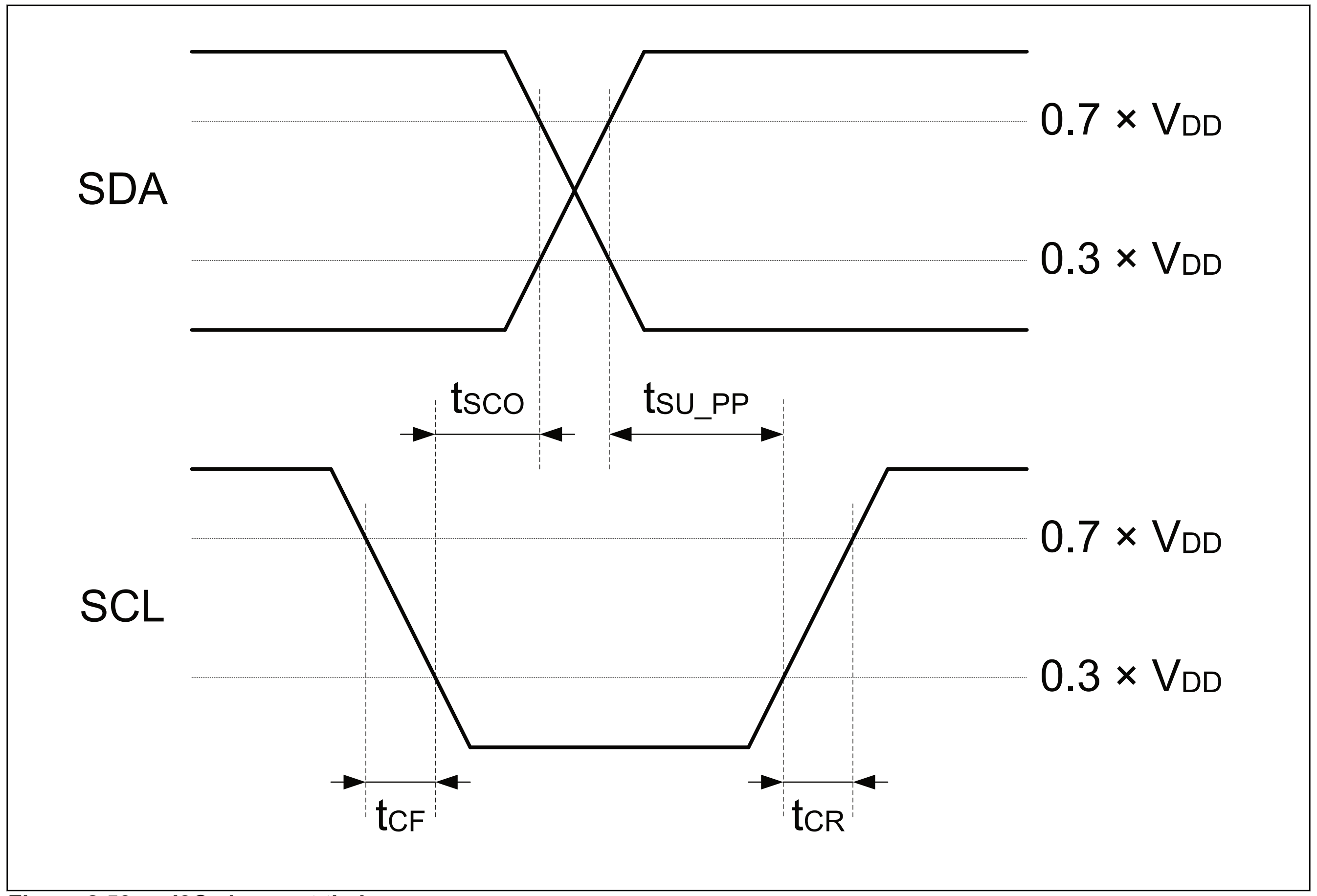


Figure 2.50 I3C slave out timing

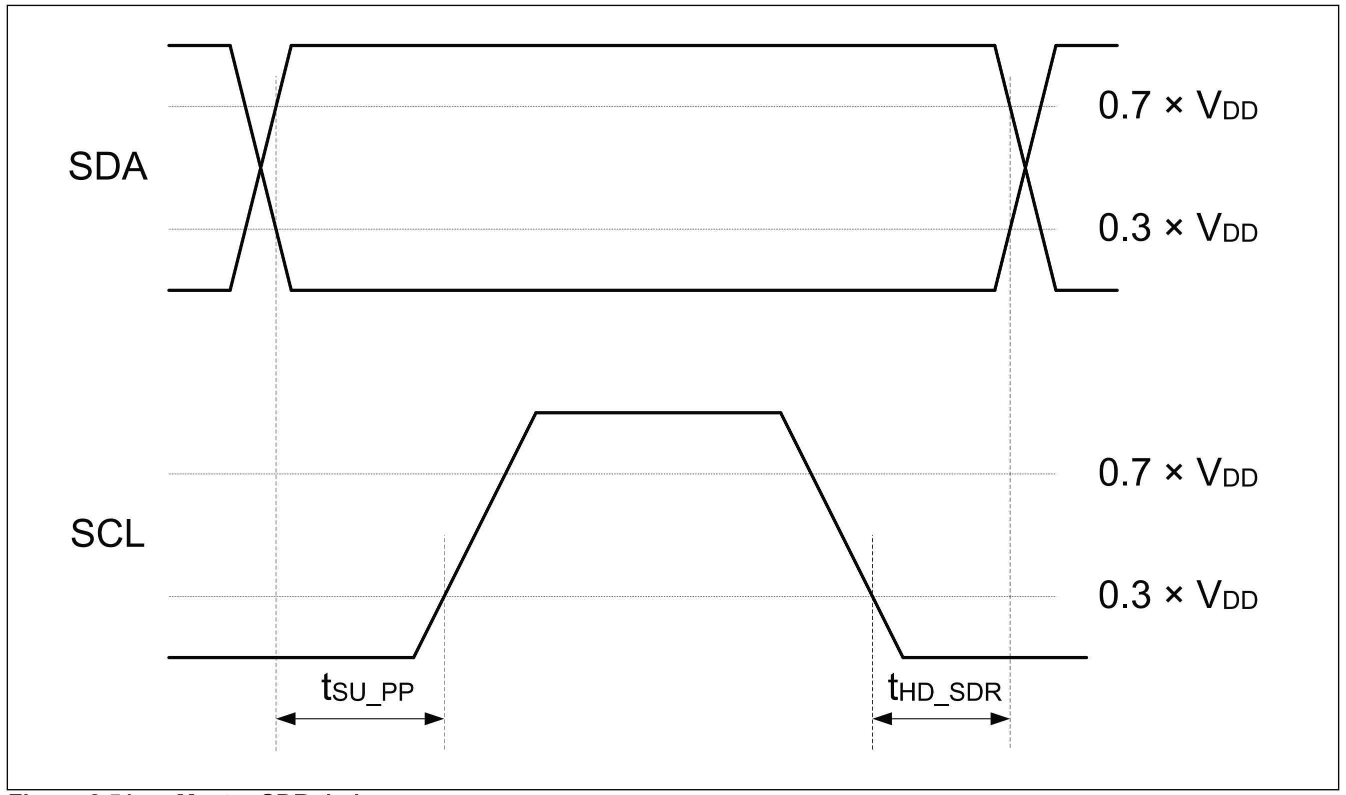


Figure 2.51 Master SDR timing

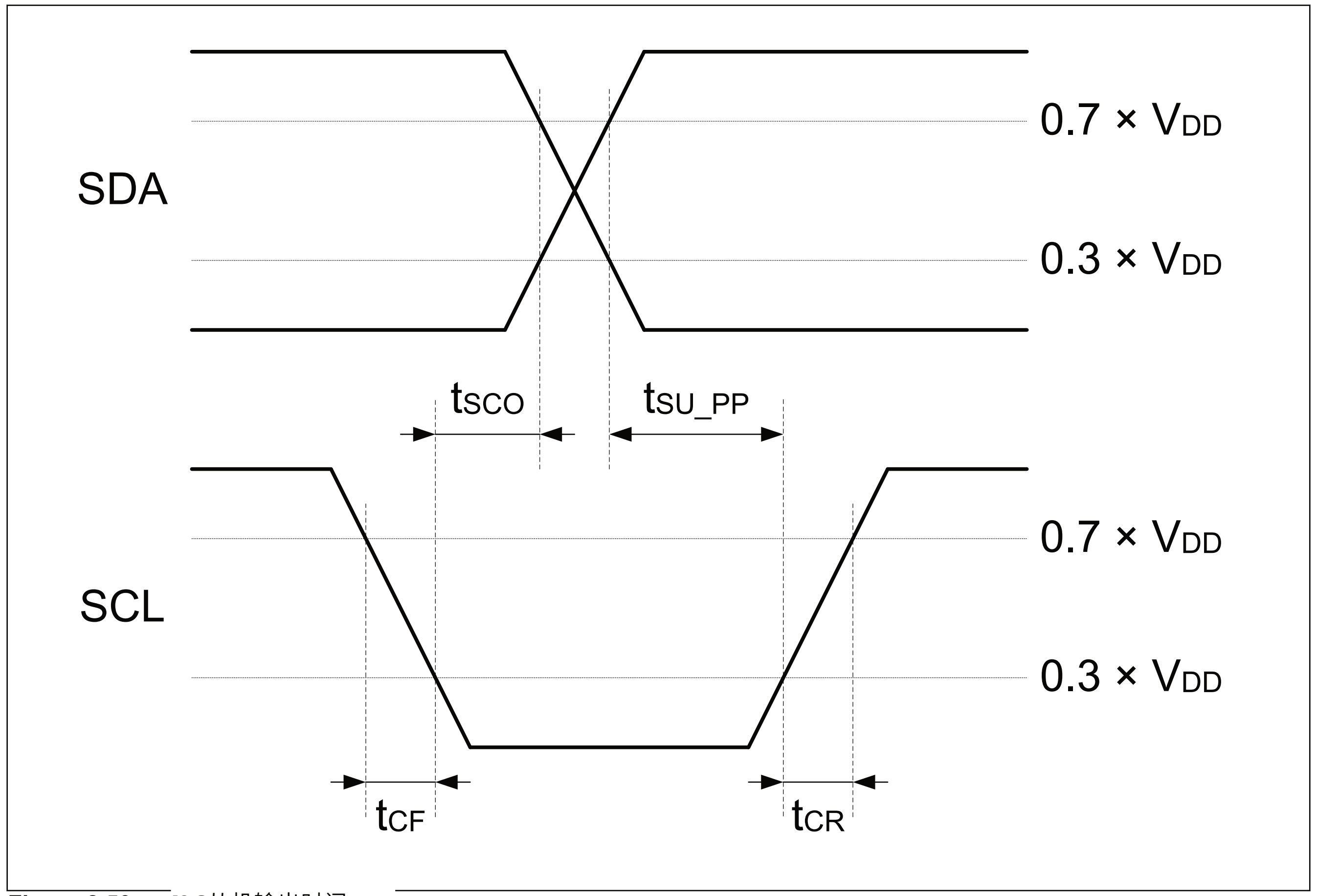


Figure 2.50 I3C从机输出时间

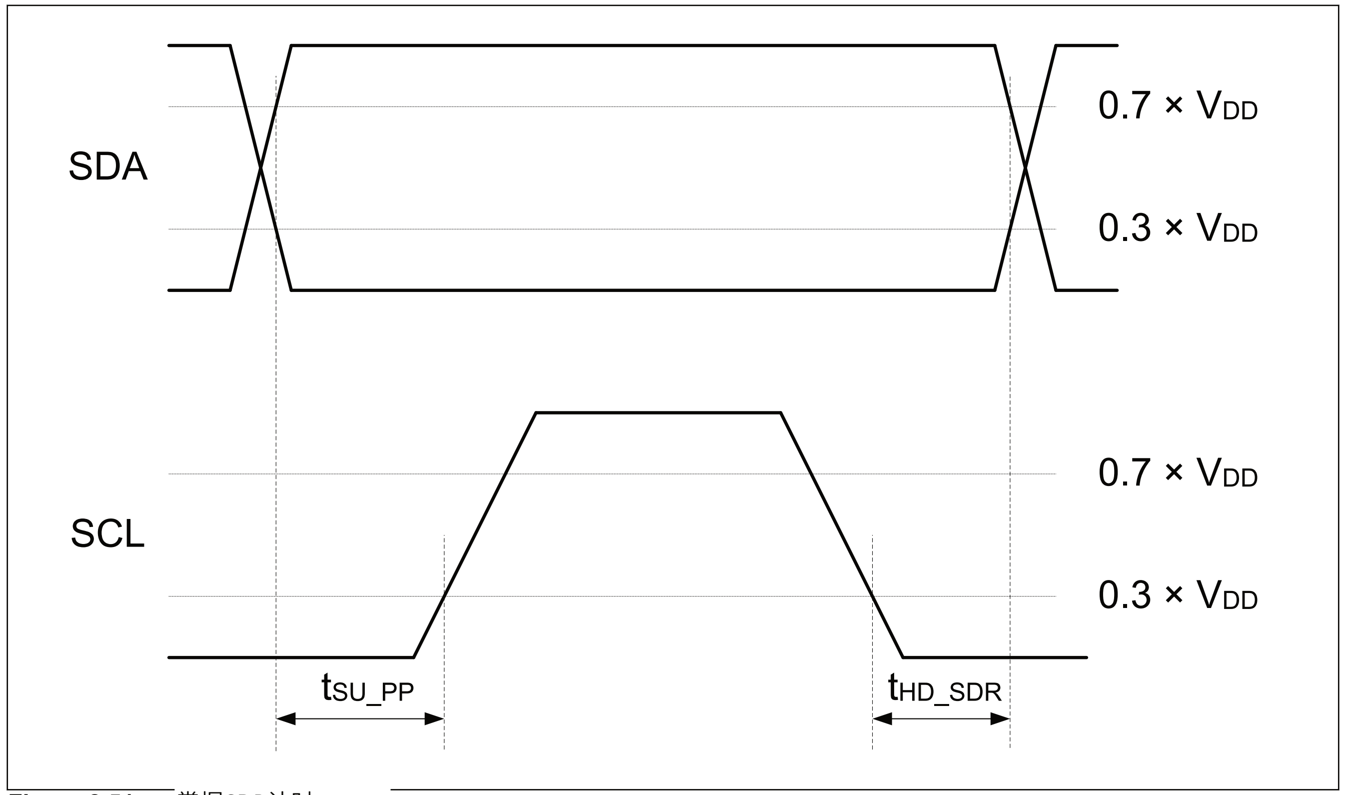


Figure 2.51 掌握SDR计时

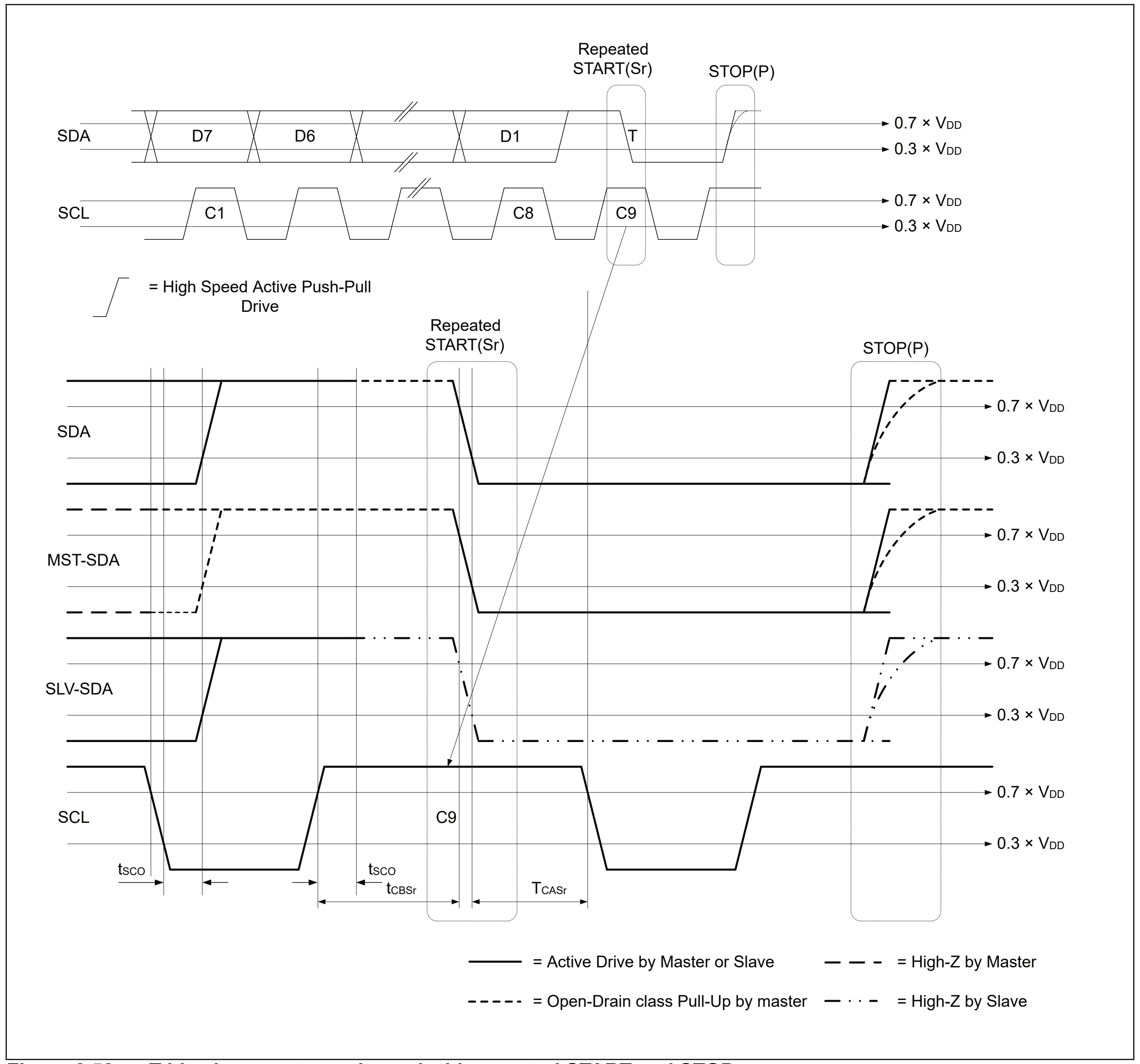


Figure 2.52 T-bit when master ends read with repeated START and STOP

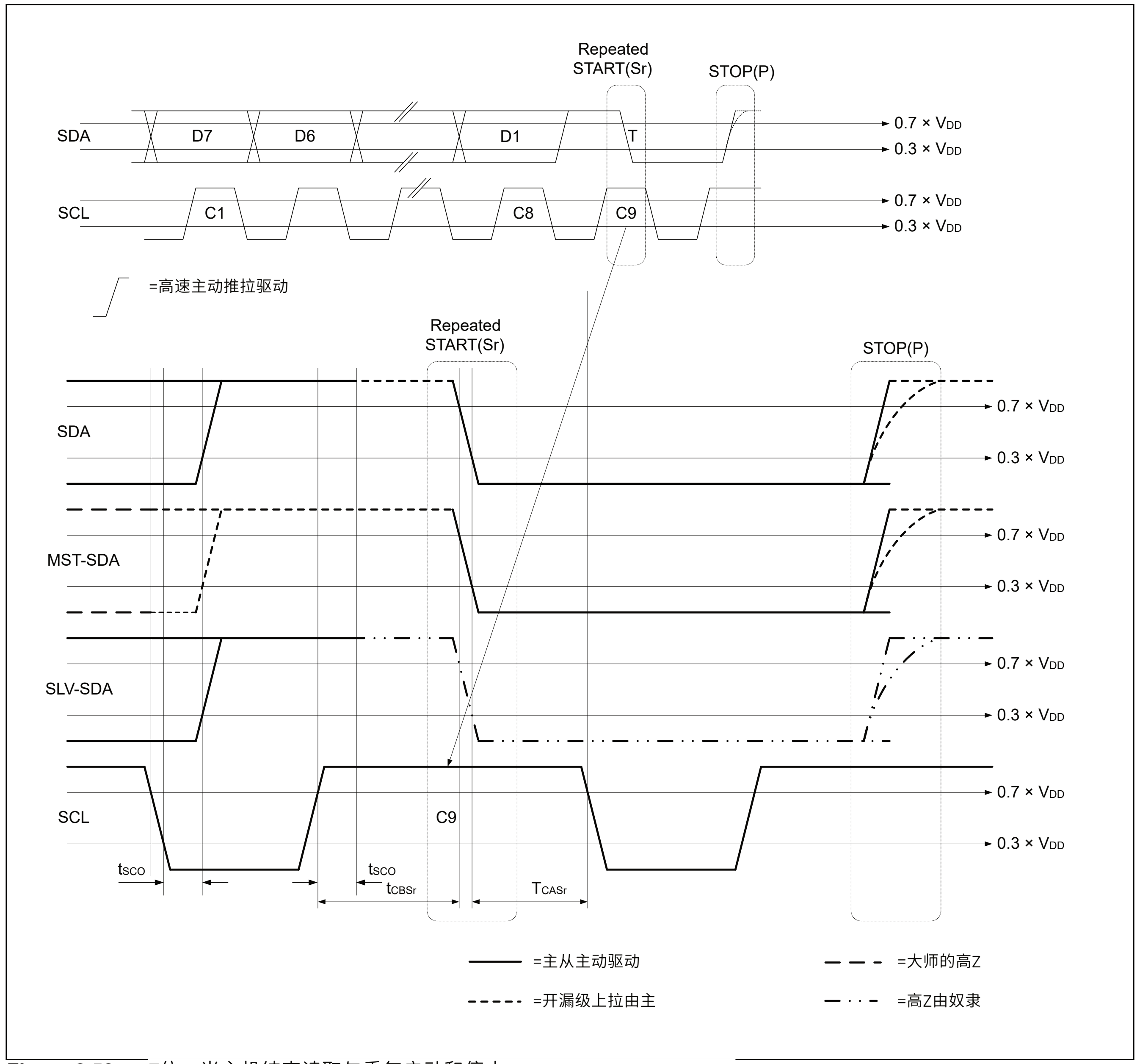


Figure 2.52 T位，当主机结束读取与重复启动和停止

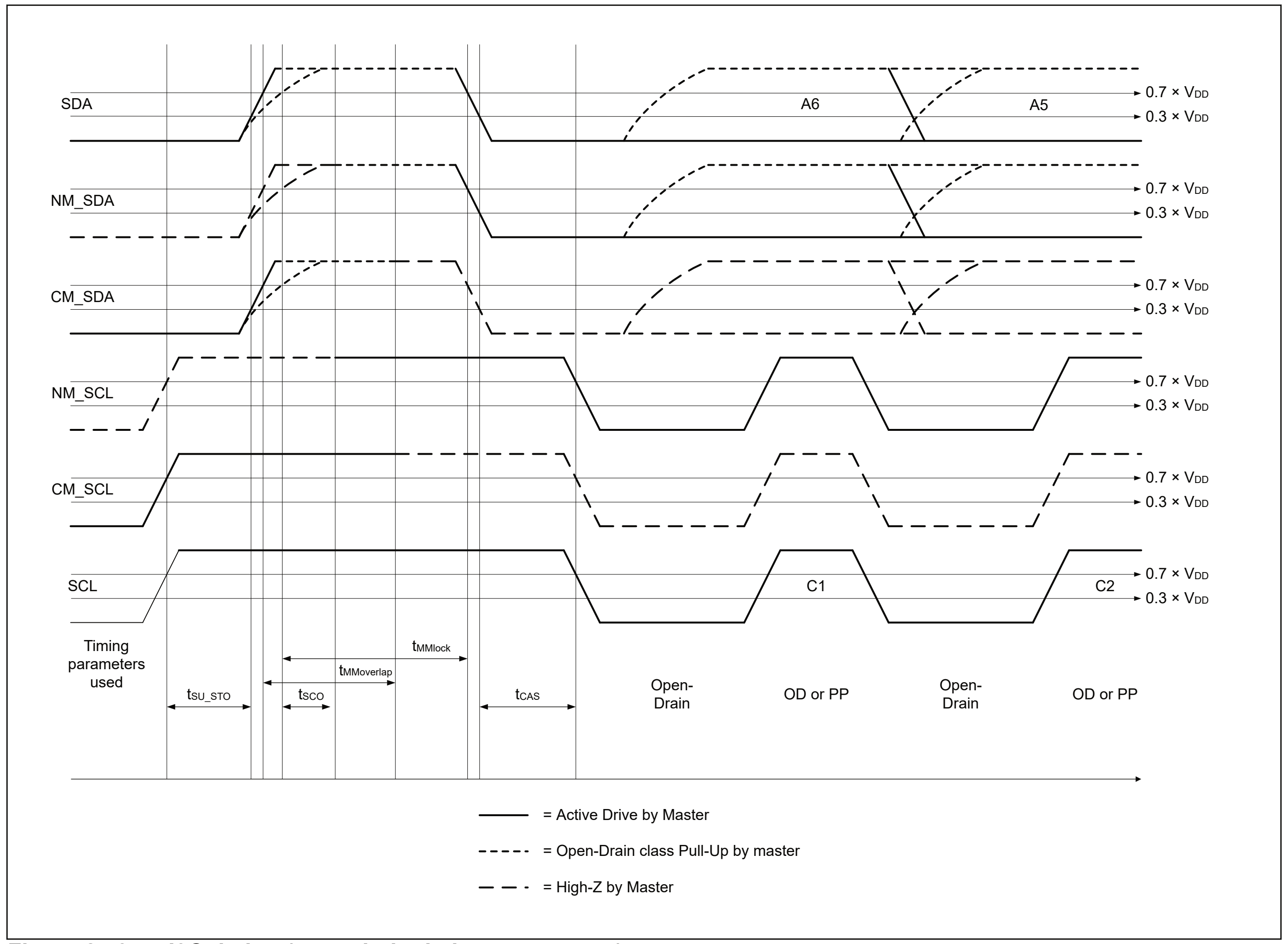


Figure 2.53 I3C timing (open drain timing parameters)

2.3.12 SSIE Timing

Table 2.35 SSIE timing (1 of 2)

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" , "_B" or "_C" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	t_O	80	—	ns	Figure 2.54
		Slave	t_I	80	—	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	Rising time/ falling time	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	

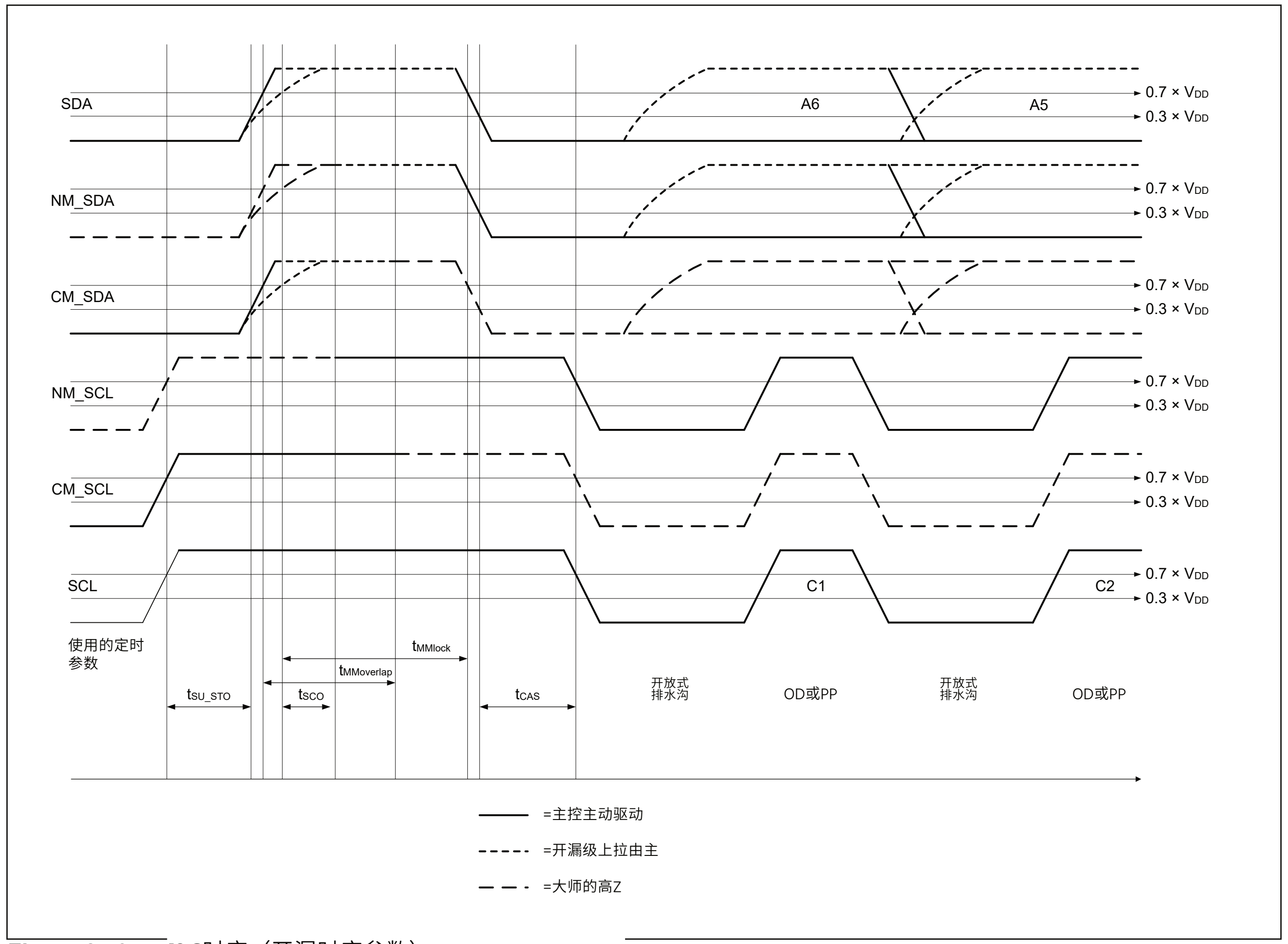


Figure 2.53 I3C时序（开漏时序参数）

2.3.12 SSIE Timing

Table 2.35 SSIE计时(1/2)

(1)用PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用在其名称后面附加字母的引脚，例如"_A"、"_B"或"_C"来表示组成员资格。对于SSIE接口，针对每个组测量电特性的AC部分。

Parameter			Symbol	目标规格		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	t_O	80	—	ns	Figure 2.54
		Slave	t_I	80	—	ns	
	高电平低电平	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	上升时间下降时间	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	

Table 2.35 SSIE timing (2 of 2)

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" , "_B" or "_C" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification Min.	Target specification Max.	Unit	Comments
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	Input set up time	Master	t_{SR}	12	—	ns	Figure 2.56, Figure 2.57
		Slave		12	—	ns	
	Input hold time	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.56, Figure 2.57
	Output delay time from SSILRCK0/ SSIFS0 change	Slave	t_{DTRW}	—	20	ns	Figure 2.58[*1]
GTIOC2A, AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 2.55
	High level/ low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA0 pin.

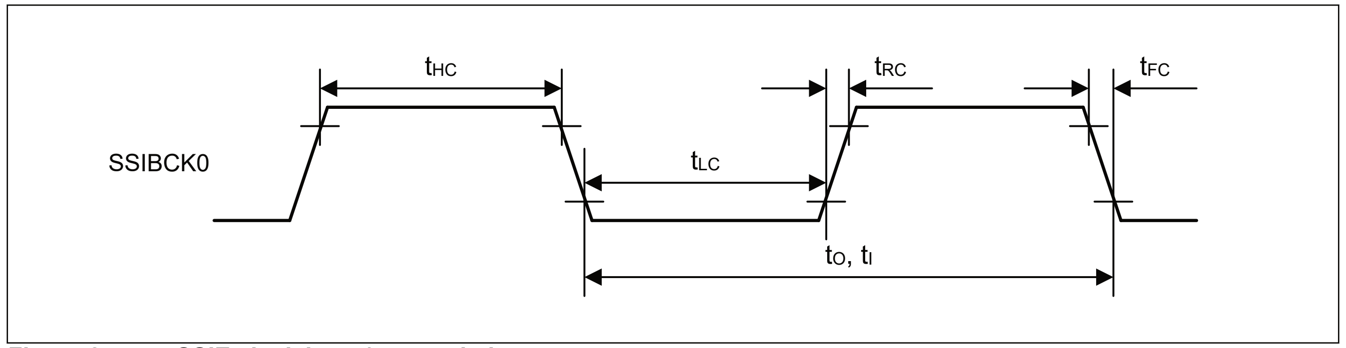


Figure 2.54 SSIE clock input/output timing

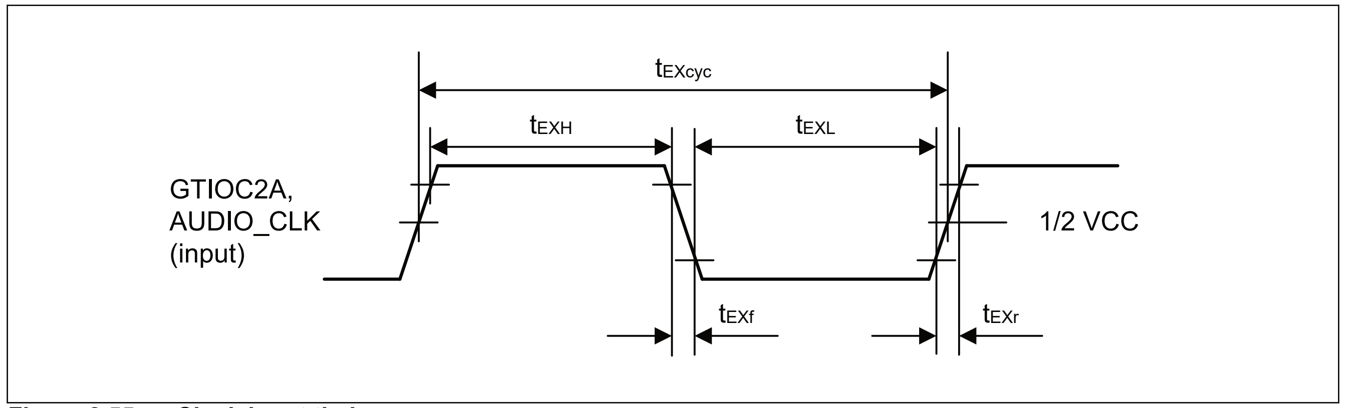


Figure 2.55 Clock input timing

Table 2.35 SSIE计时(2/2)

(1)用PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用在其名称后面附加字母的引脚，例如"_A"、"_B"或"_C"来表示组成员资格。对于SSIE接口，针对每个组测量电特性的AC部分。

Parameter			Symbol	目标规格 Min.	目标规格 Max.	Unit	Comments
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	输入设置时间	Master	t_{SR}	12	—	ns	Figure 2.56, Figure 2.57
		Slave		12	—	ns	
	输入保持时间	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	输出延迟时间	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.56, Figure 2.57
	从SSILRCK0输出延迟时间 SSIFS0 change	Slave	t_{DTRW}	—	20	ns	Figure 2.58[*1]
GTIOC2A, AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 2.55
	高电平低电平		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

注1。对于从模式传输，SSIE有一条路径，通过该路径，从SSILRCK0SSIFS0引脚输入的信号用于生成传输数据，并将传输数据逻辑输出到SSITXD0或SSIDATA0引脚。

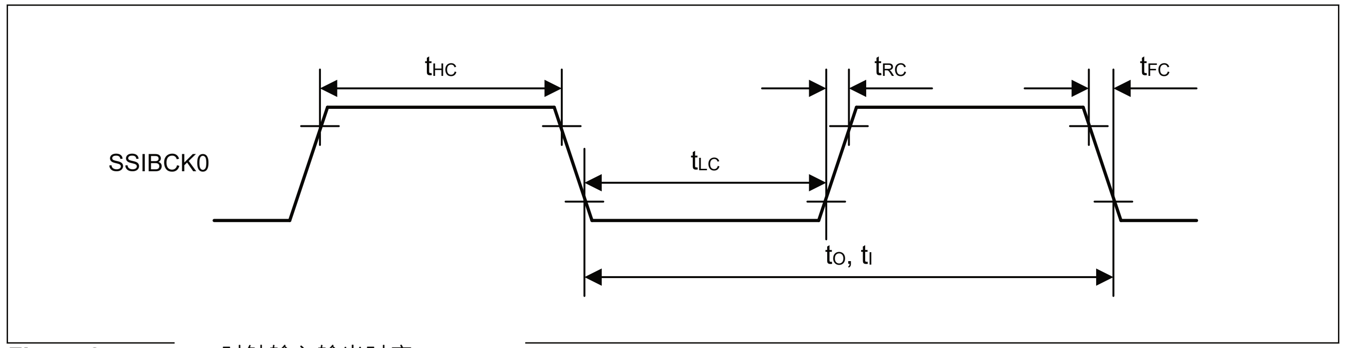


Figure 2.54 SSIE时钟输入输出时序

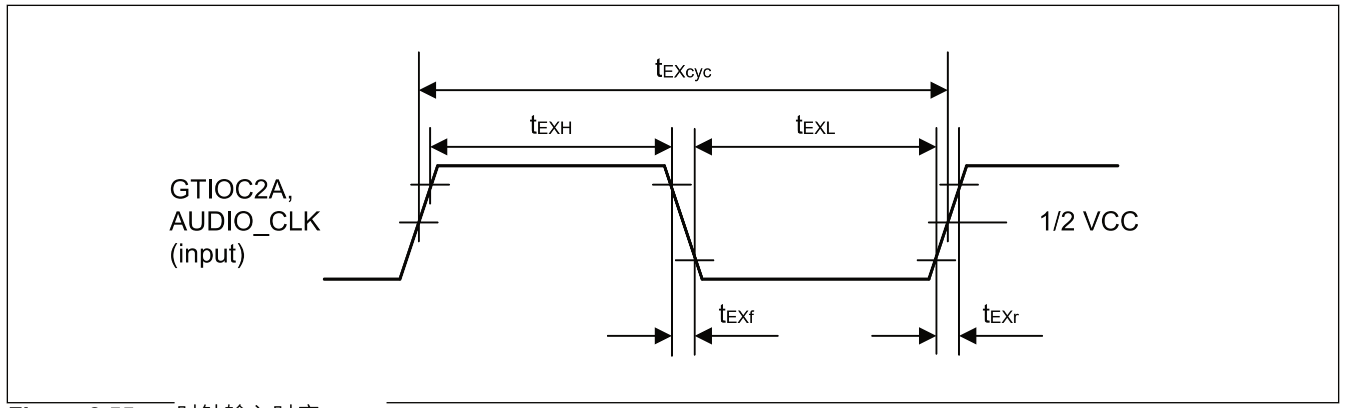


Figure 2.55 时钟输入时序

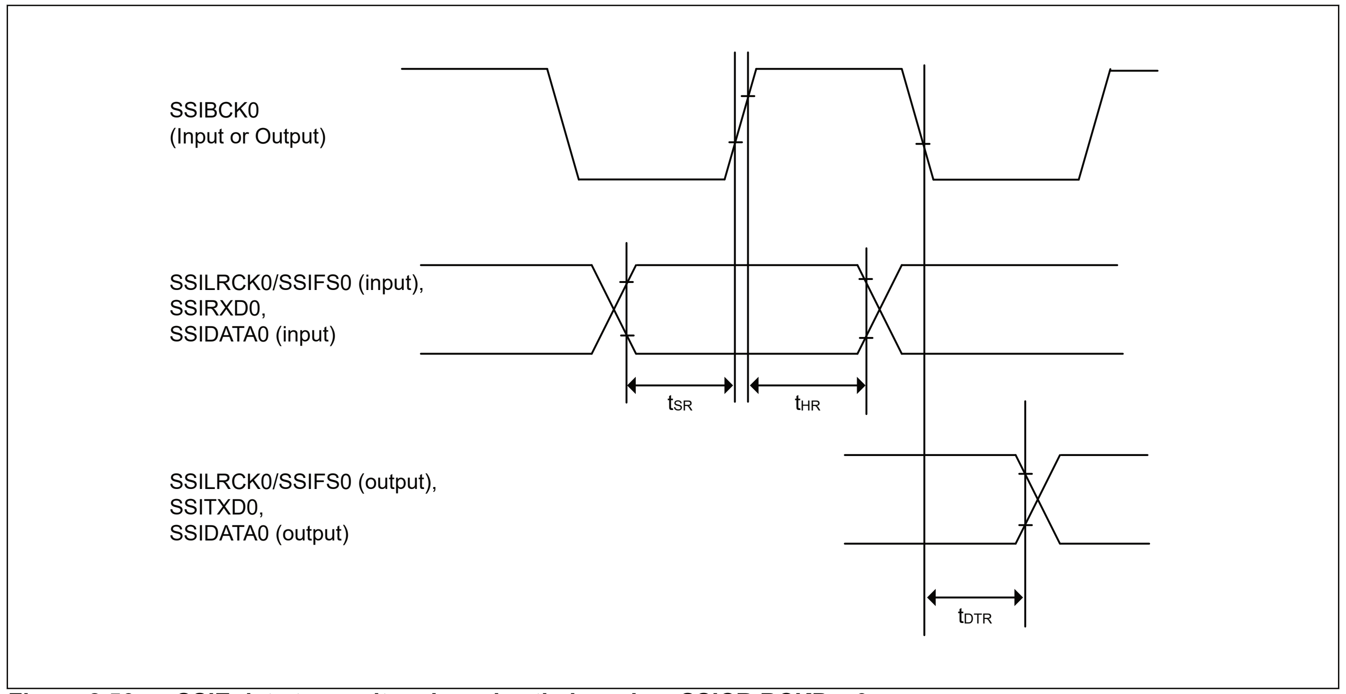


Figure 2.56 SSIE data transmit and receive timing when SSICR.BCKP = 0

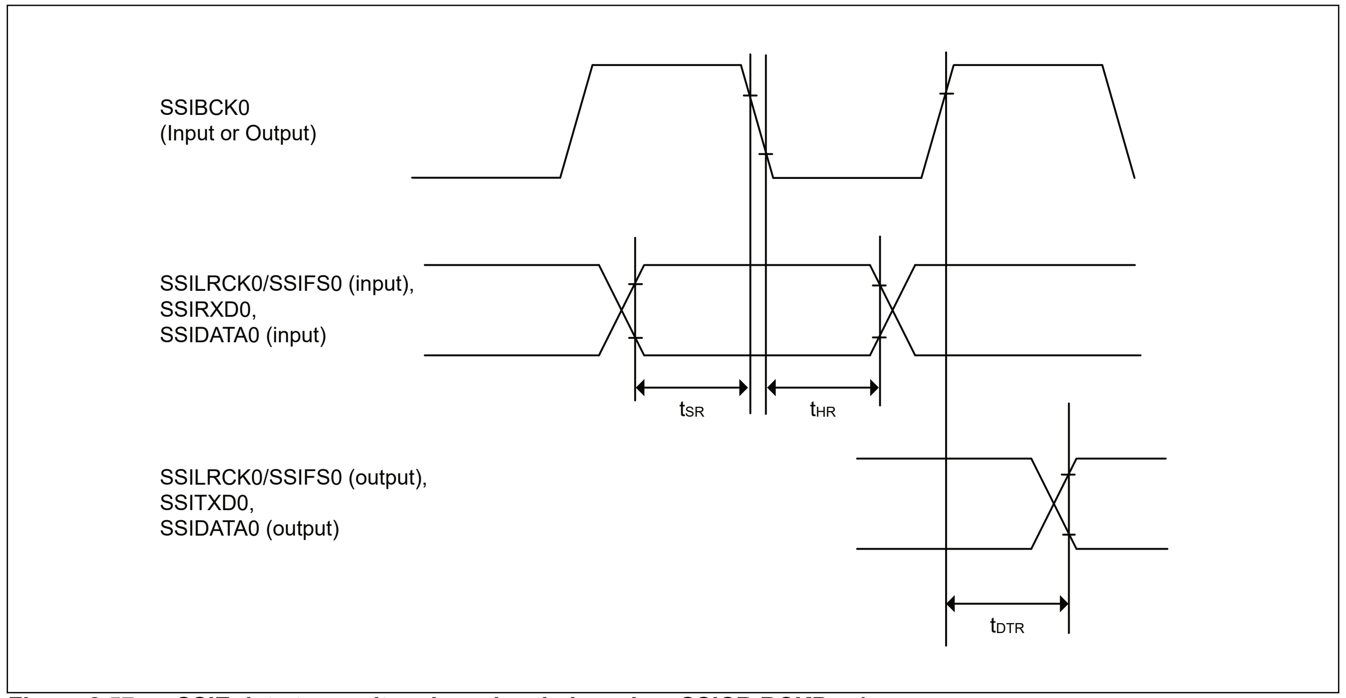


Figure 2.57 SSIE data transmit and receive timing when SSICR.BCKP = 1

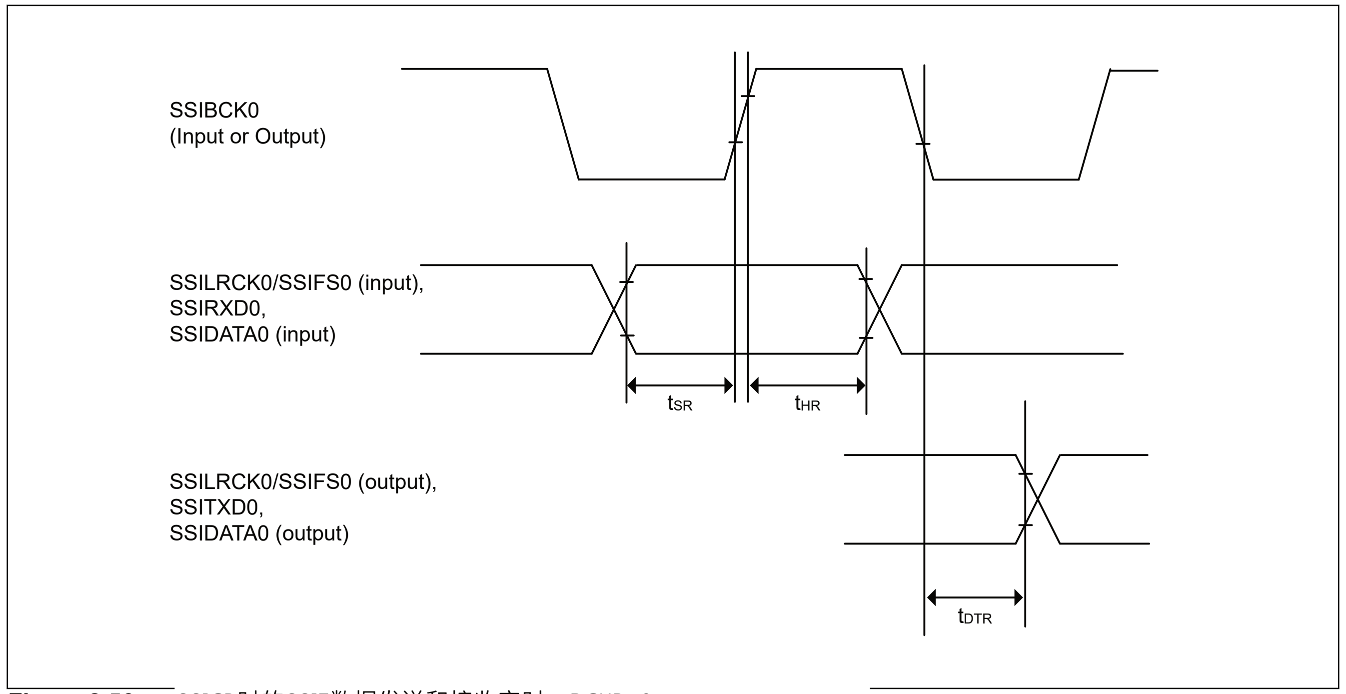


Figure 2.56 SSICR时的SSIE数据发送和接收定时。BCKP=0

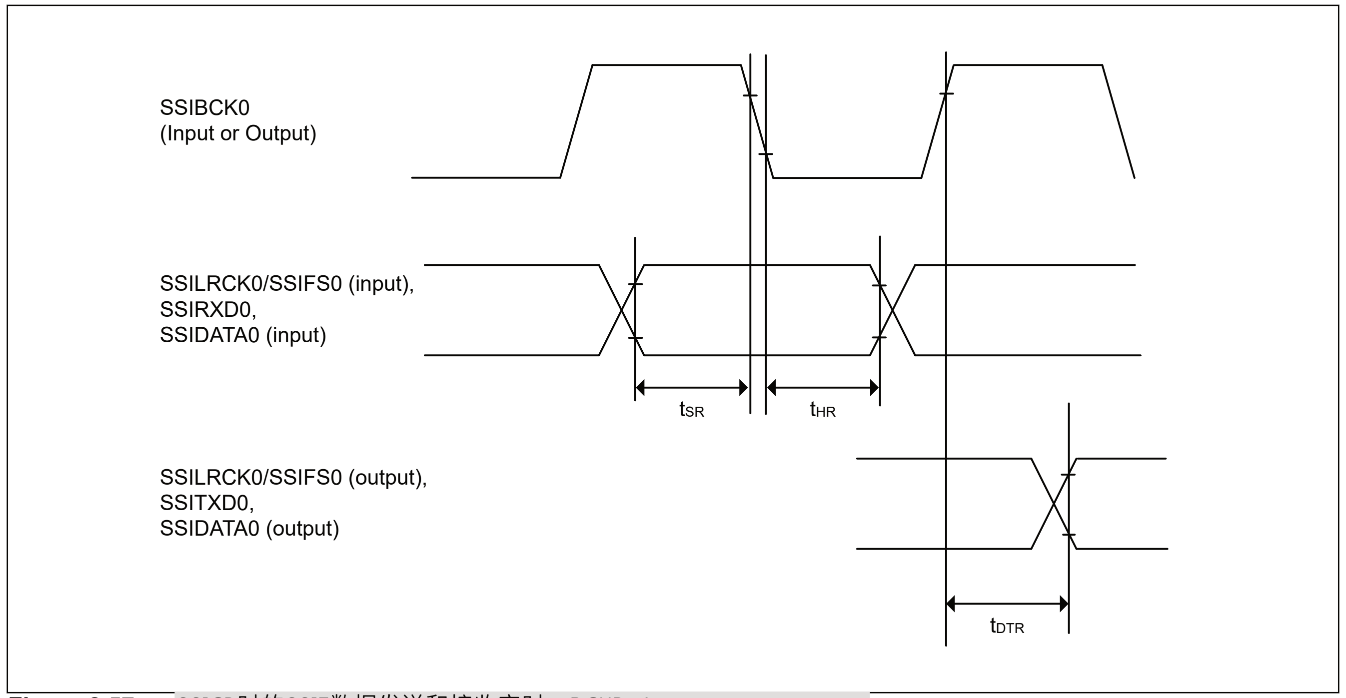
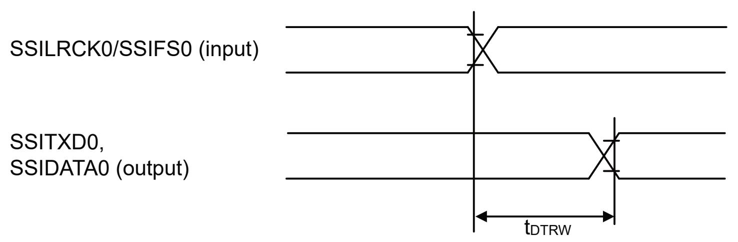


Figure 2.57 SSICR时的SSIE数据发送和接收定时。BCKP=1



MSB bit output delay after SSILRCK0/SSIFS0 change for slave transmitter when DEL = 1, SDTA = 0 or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0] in SSICR.

Figure 2.58 SSIE data output delay after SSILRCK0/SSIFS0 change

2.3.13 CANFD Timing

Table 2.36 CANFD interface timing

Parameter	Symbol	CAN-FD Min	CAN-FD Max	Unit	Test conditions
Internal delay time	t_{node}	—	75	ns	Figure 2.59
Transmission rate		—	5	Mbps	

Note: $t_{node} = t_{output} + t_{input}$

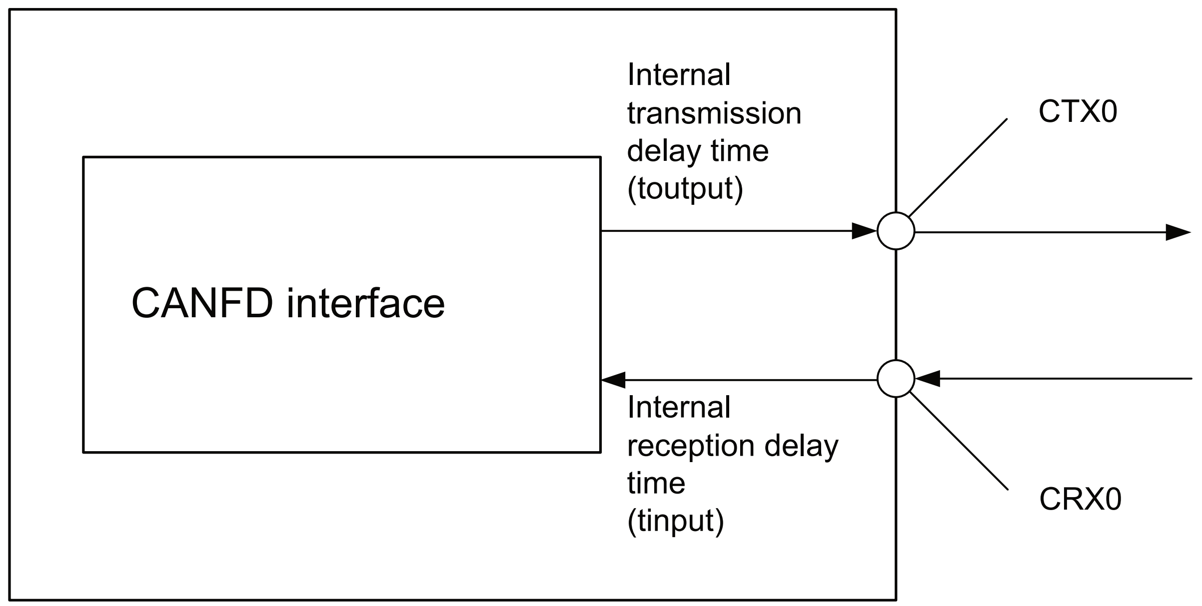
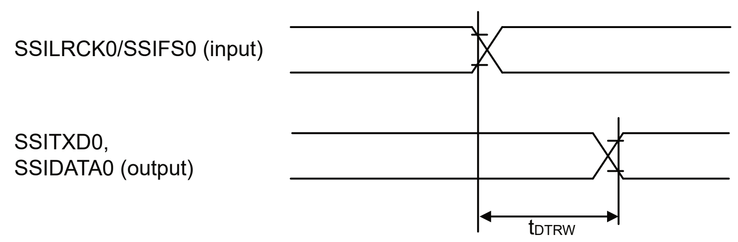


Figure 2.59 CANFD interface condition



SSILRCK0SSIFS0后的MSB位输出延迟在SSICR中当DEL=1、SDTA=0或DEL=1、SDTA=1、SWL[2:0]=DWL[2:0]时为从发射机改变。

Figure 2.58 Ssilrck0SSIFS0改变后的SSIE数据输出延迟

2.3.13 CANFD Timing

Table 2.36 CANFD接口定时

Parameter	Symbol	CAN-FD Min	CAN-FD Max	Unit	测试条件
内部延迟时间	t_{node}	—	75	ns	Figure 2.59
传输速率		—	5	Mbps	

Note: t节点=t输出+t输入

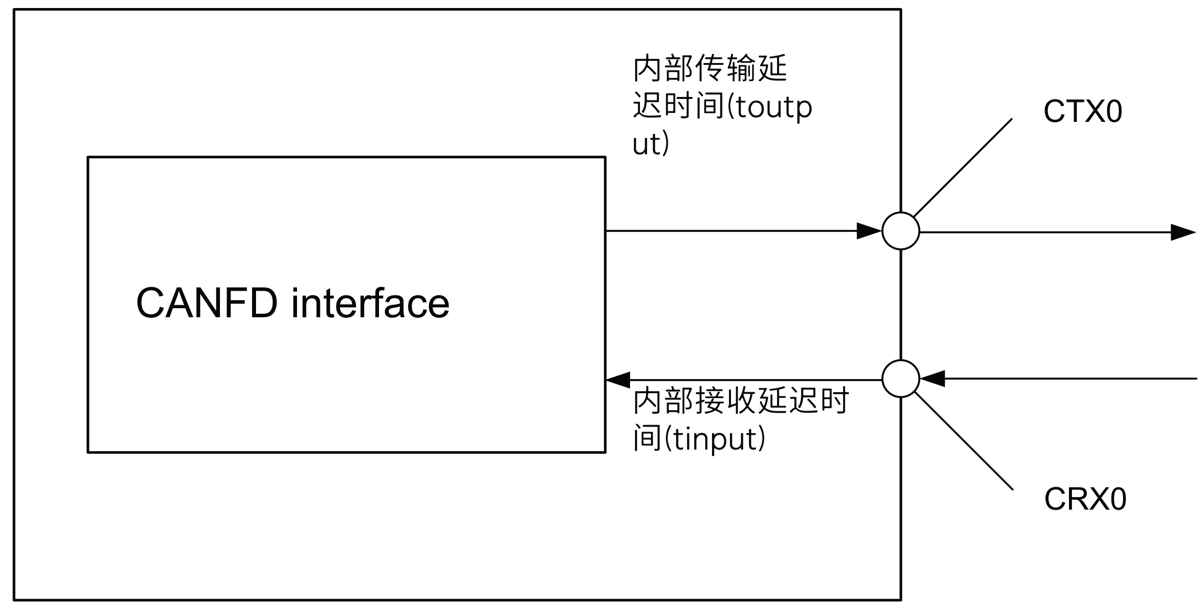


Figure 2.59 CANFD接口条件

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.37 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.60
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception

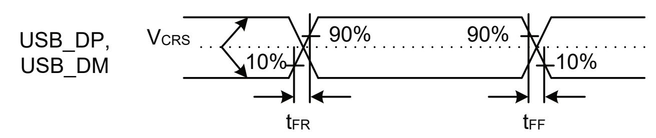


Figure 2.60 USB_DP and USB_DM output timing in full-speed mode

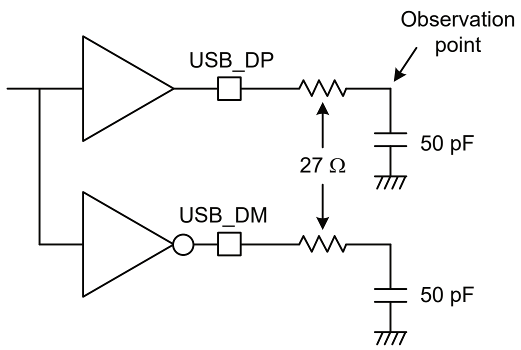


Figure 2.61 Test circuit in full-speed mode

2.4 USB特性

2.4.1 USBFS Timing

Table 2.37 USBFS全速特性（USB_DP和USB_DM引脚特性）

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	—	—	V	—
	输入低电压	V_{IL}	—	—	0.8	V	—
	差分输入灵敏度	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	—	2.5	V	—
输出特性	输出高压	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	输出低电压	V_{OL}	0.0	—	0.3	V	IOL=2毫安
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.60
	上升时间	t_{LR}	4	—	20	ns	
	秋季时间	t_{LF}	4	—	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
上拉和下拉特性	器件控制器模式下的DM上拉电阻	R_{pu}	0.900	—	1.575	kΩ	空闲状态期间
			1.425	—	3.090	kΩ	在传输和接收期间

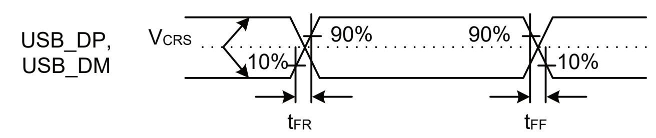


Figure 2.60 全速模式下的USB_DP和USB_DM输出时序

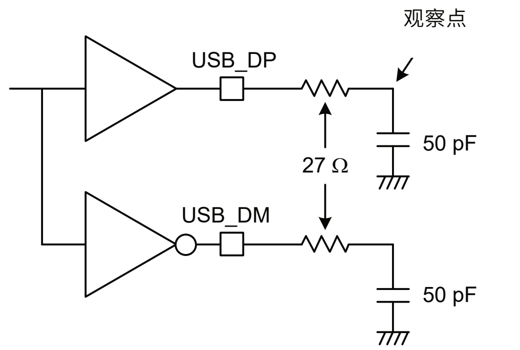


Figure 2.61 全速模式下的测试电路

2.5 ADC12 Characteristics

Table 2.38 A/D conversion characteristics for unit 0

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision high-speed channels (AN000 to AN002, AN007)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	μs	Sampling in 13 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN004 to AN006, AN008, AN011 to AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	μs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN016)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	μs	Sampling in 33 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.39 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	μs	—

2.5 ADC12 Characteristics

Table 2.38 A单位0的D转换特性

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	最大单位		测试条件
Frequency			1	—	50	MHz	—
模拟输入电容			—	—	30	pF	—
量化误差			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
高精度高速通道（AN000至AN002、AN007）	转换时间*1 (operation at PCLKC = 50 MHz)	允许信号源阻抗最大。= 1kΩ	0.52 (0.26)*2	—	—	μs	13个州的抽样
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对准确度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度正常速度通道（AN004至AN006、AN008、AN011至AN013）	转换时间*1 (Operation at PCLKC = 50 MHz)	允许信号源阻抗最大。= 1kΩ	0.92 (0.66)*2	—	—	μs	33个州的抽样
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对准确度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN016)	转换时间*1 (Operation at PCLKC = 50 MHz)	允许信号源阻抗最大。= 1kΩ	0.92 (0.66)*2	—	—	μs	33个州的抽样
	偏移误差		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	绝对准确度		—	±2.0	±7.5	LSB	—
	DNL微分非线性误差		—	±0.5	±4.5	LSB	—
	INL积分非线性误差		—	±1.0	±5.5	LSB	—

Note: 这些规格值适用于D转换期间无法访问外部总线时。如果在D转换期间发生访问，则值可能不在指定的范围内。使用12位AD转换器时，不允许使用PORT0作为数字输出。

该特性适用于AVCC0、AVSS0、VREFH0、VREFL0和12位AD转换器输入电压稳定时。
注1。转换时间包括采样和比较时间。为测试条件指示采样状态的数量。注2。括号中的值表示采样时间。

Table 2.39 AD内部基准电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部基准电压	1.13	1.18	1.23	V	—
采样时间	4.15	—	—	μs	—

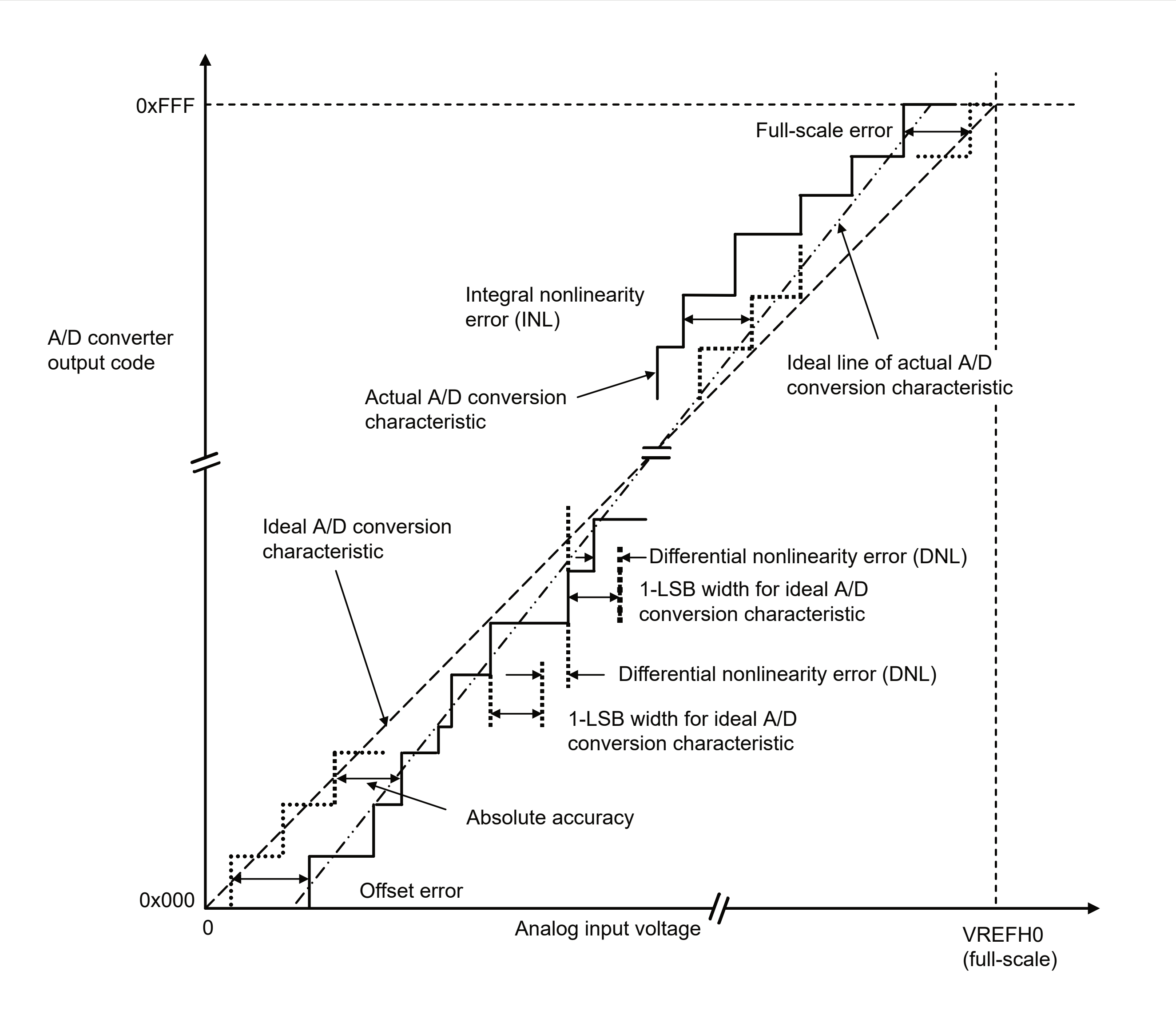


Figure 2.62 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

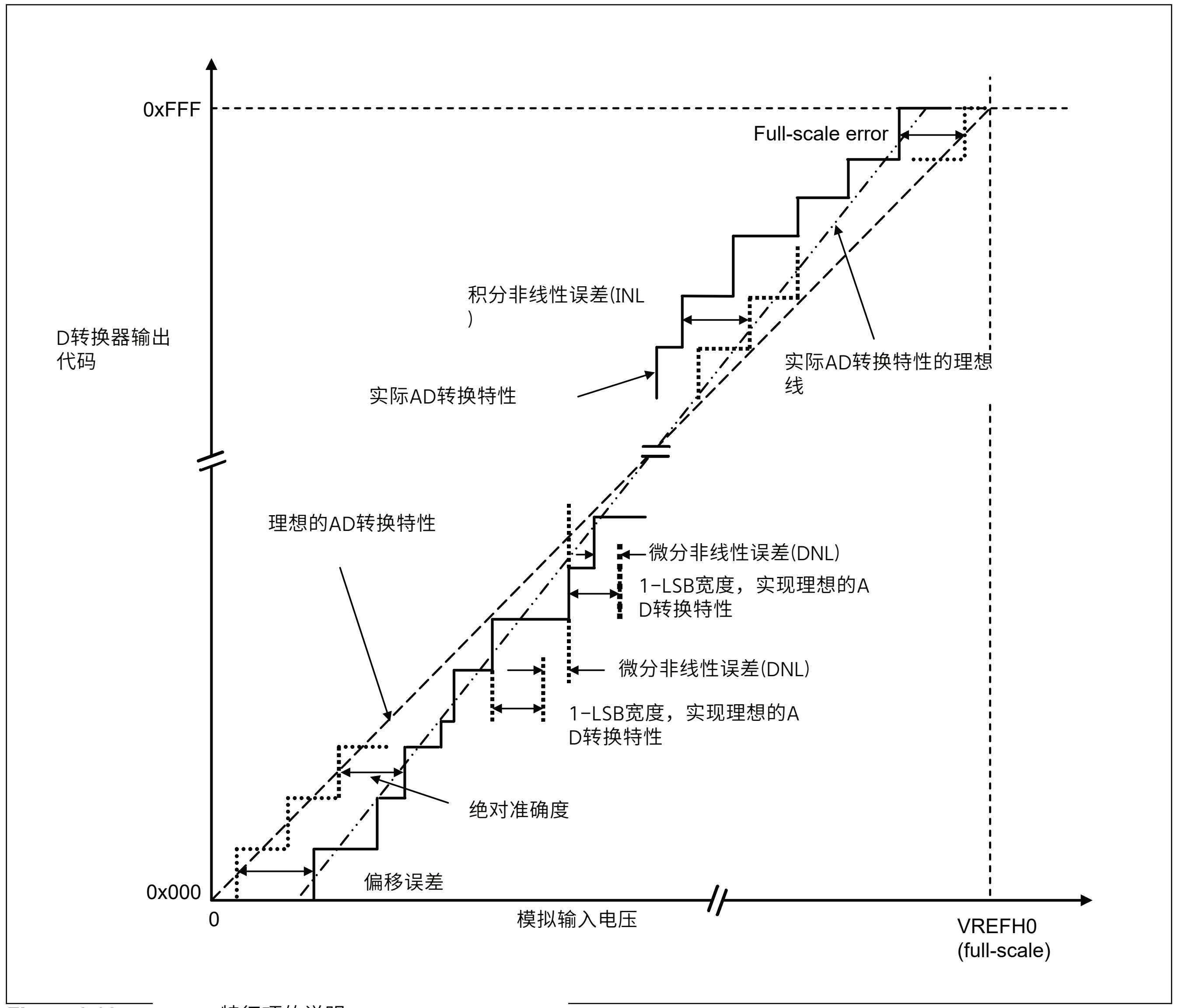


Figure 2.62 ADC12特征项的说明

绝对准确度

绝对精度是基于理论AD转换特性的输出码与实际AD转换结果之间的差值。在测量绝对精度时，将能够满足基于理论AD转换特性输出相等代码的期望的模拟输入电压的宽度（1-LSB宽度）的中点处的电压用作模拟输入电压。例如，如果使用12位分辨率并且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且0mV，0.75mV和1.5mV用作模拟输入电压。如果模拟输入电压为6mV，则±5LSB的绝对精度意味着实际的AD转换结果在0x003至0x00d范围内，但从理论AD转换特性可以预期输出代码为0x008。

积分非线性误差(INL)

积分非线性误差是当测量的偏移和满量程误差归零时理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码宽度之间的差值。

偏移误差

偏移误差为理想第一输出码与实际第一输出码的跳变点之差。

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.40 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	μs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	μs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

2.7 TSN Characteristics

Table 2.41 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	μs	—
Sampling time	—	4.15	—	—	μs	—

2.8 OSC Stop Detect Characteristics

Table 2.42 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.63

Full-scale error

满量程误差是理想的最后输出码和实际的最后输出码的过渡点之间的差。

2.6 DAC12 Characteristics

Table 2.40 Da转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	—	—	12	Bits	—
无输出放大器					
绝对准确度	—	—	±24	LSB	电阻负载2MΩ
INL	—	±2.0	±8.0	LSB	电阻负载2MΩ
DNL	—	±1.0	±2.0	LSB	—
输出阻抗	—	8.5	—	kΩ	—
转换时间	—	—	3	μs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	—	VREFH	V	—
带输出放大器					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
转换时间	—	—	4.0	μs	—
电阻负载	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
输出电压范围	0.2	—	VREFH – 0.2	V	—

2.7 TSN Characteristics

Table 2.41 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	—	—	± 1.0	—	°C	—
温度斜率	—	—	4.0	—	mV/°C	—
输出电压（25°C时）	—	—	1.24	—	V	—
温度传感器启动时间	t_{START}	—	—	30	μs	—
采样时间	—	4.15	—	—	μs	—

2.8 Osc停止检测特性

Table 2.42 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	—	—	1	ms	Figure 2.63

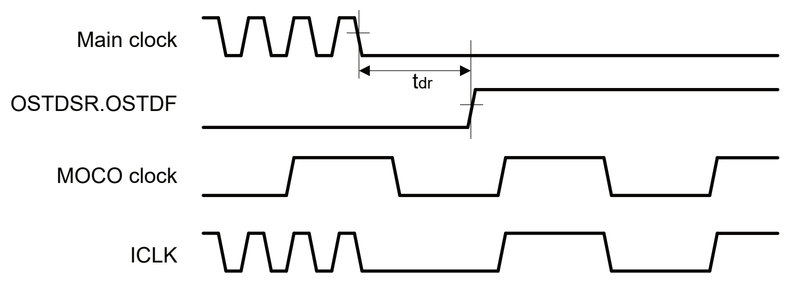


Figure 2.63 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.43 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.64
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.65
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.66
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.67
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 2.64
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 2.65
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 2.66
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 2.67
Minimum VCC down time*1			t_{VOFF}	200	—	—	μs	Figure 2.64, Figure 2.65
Response delay			t_{det}	—	—	200	μs	Figure 2.65 to Figure 2.67
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	μs	Figure 2.66, Figure 2.67
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

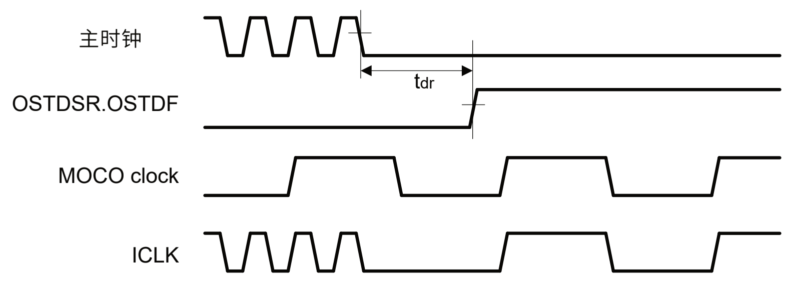


Figure 2.63 振荡停止检测定时

2.9 POR和LVD特性

Table 2.43 上电复位电路及电压检测电路特性(1)

Parameter			Symbol	Min	Typ	Max	联合国	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.64
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	电压检测电路(LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.65
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路(LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.66
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路(LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.67
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
内部复位时间	上电复位时间		t_{POR}	—	4.5	—	ms	Figure 2.64
	LVD0复位时间		t_{LVD0}	—	0.51	—		Figure 2.65
	LVD1复位时间		t_{LVD1}	—	0.38	—		Figure 2.66
	LVD2复位时间		t_{LVD2}	—	0.38	—		Figure 2.67
最小vcc停机时间*1			t_{VOFF}	200	—	—	μs	Figure 2.64, Figure 2.65
响应延迟			t_{det}	—	—	200	μs	图2.65至 Figure 2.67
LVD操作稳定时间（启用LVD后）			$t_{d(E-A)}$	—	—	10	μs	Figure 2.66, Figure 2.67
滞后宽度(LVD1和LVD2)			V_{LVH}	—	70	—	mV	

注1。最小vcc停机时间表示VCC低于电压检测电平Vpor、vdet0的最小值的时间 Vdet1，和Vdet2为POR和LVD。

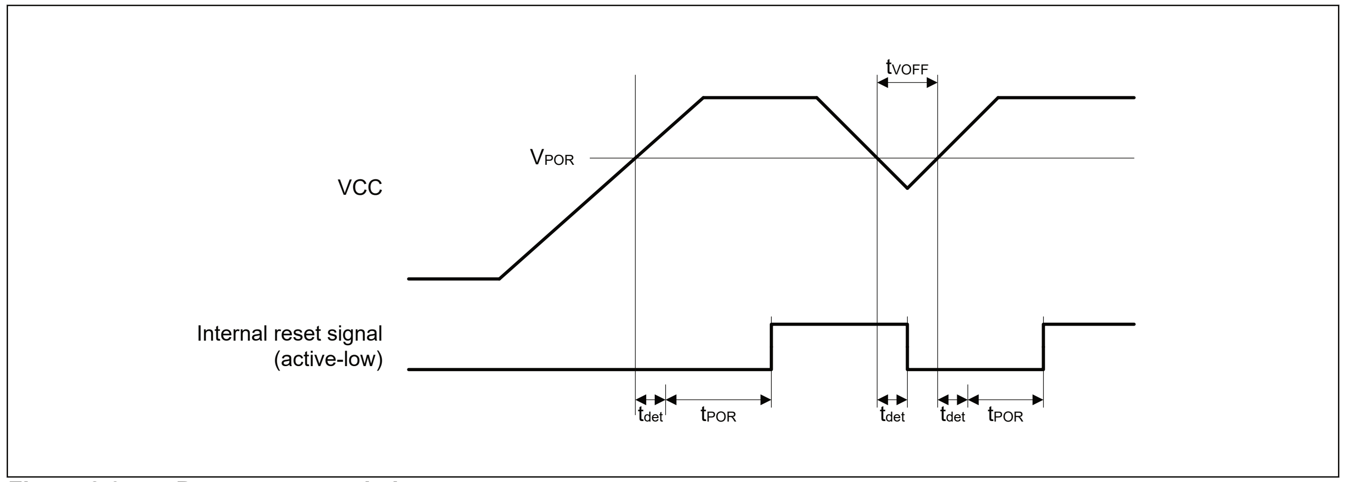


Figure 2.64 Power-on reset timing

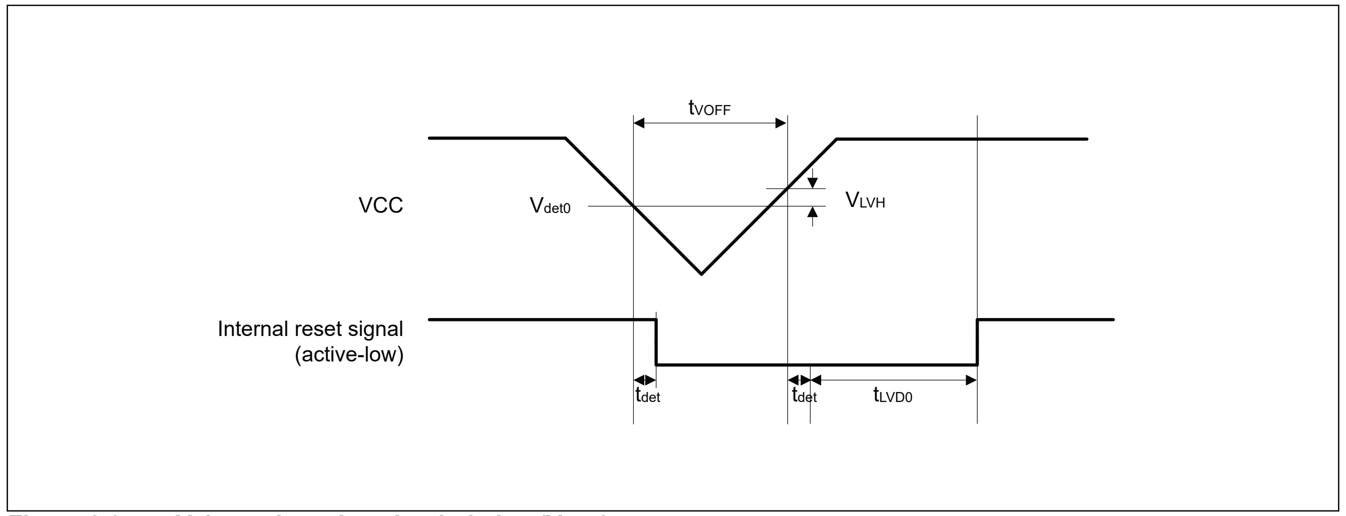


Figure 2.65 Voltage detection circuit timing (V_{det0})

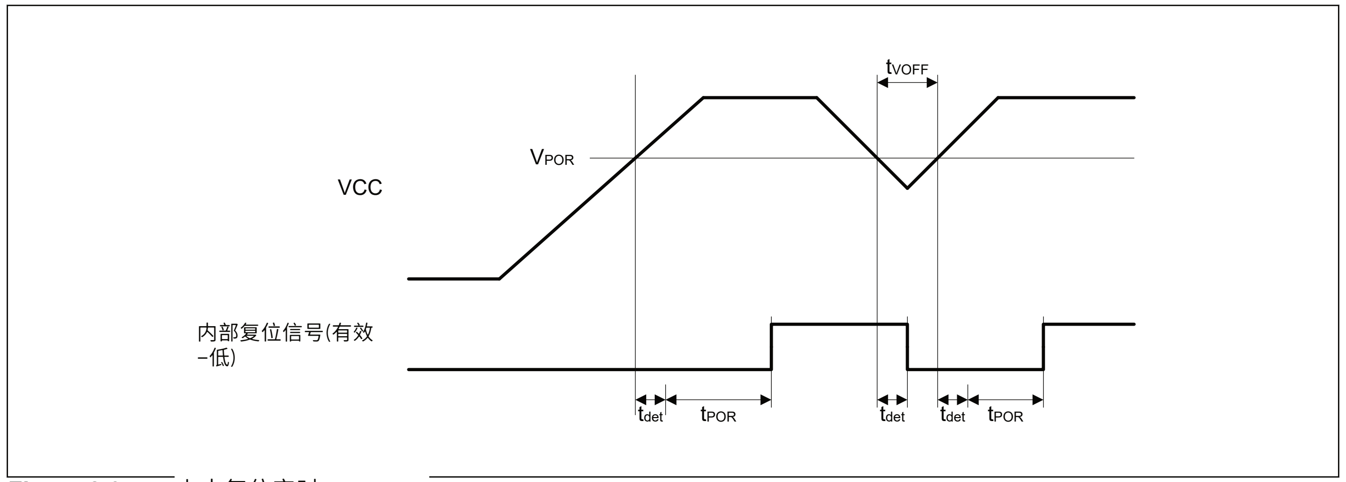


Figure 2.64 上电复位定时

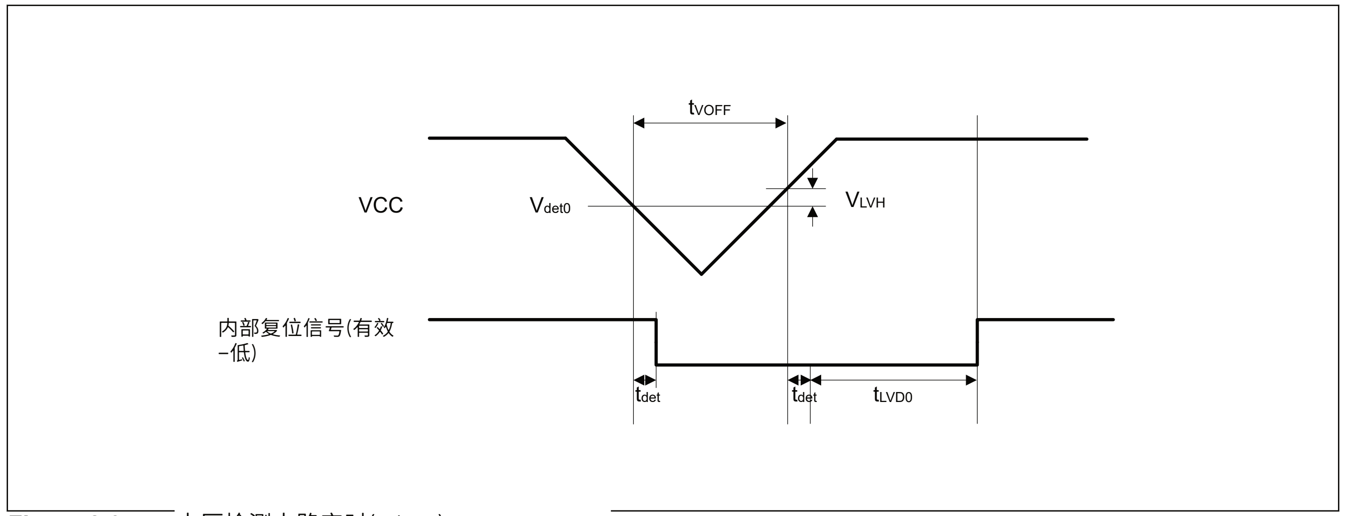


Figure 2.65 电压检测电路定时(vdet0)

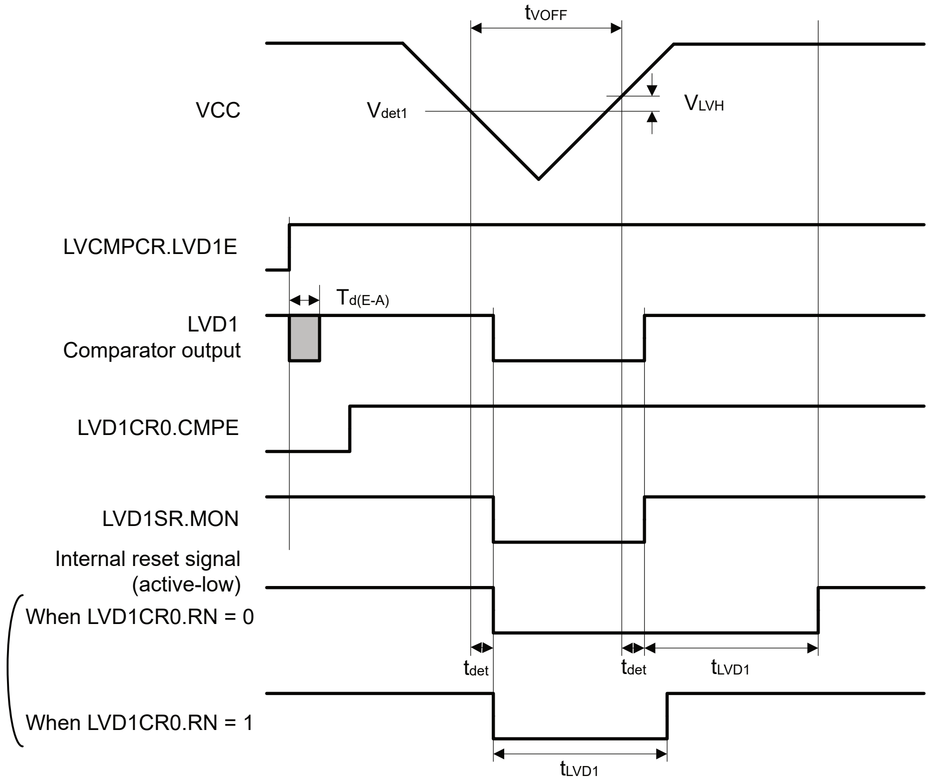


Figure 2.66 Voltage detection circuit timing (V_{det1})

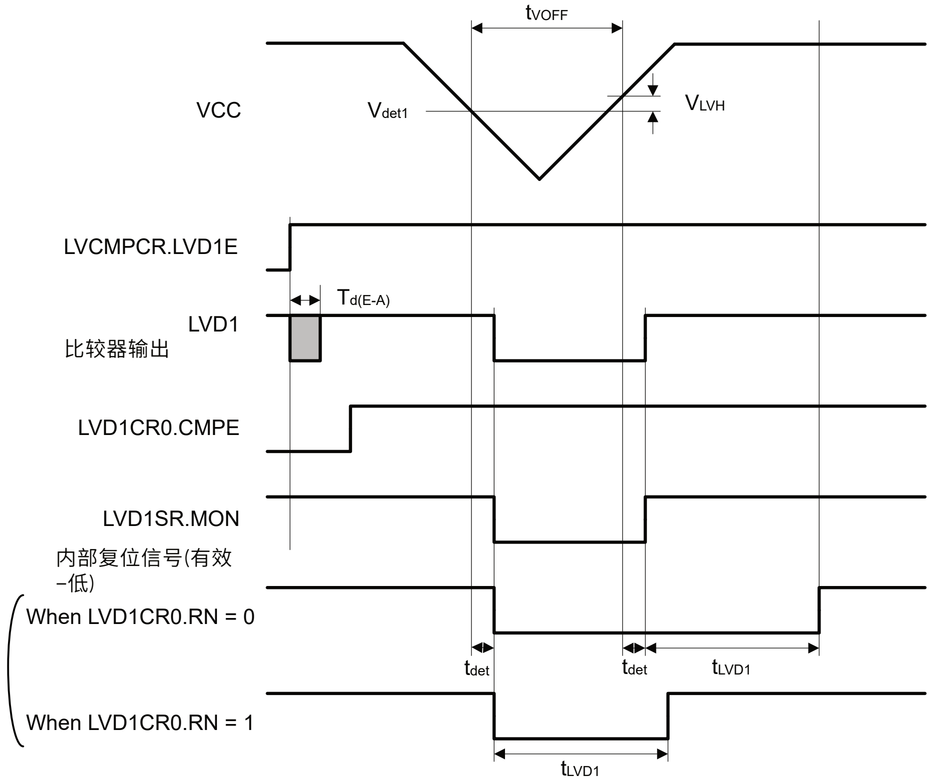


Figure 2.66 电压检测电路定时(vdet1)

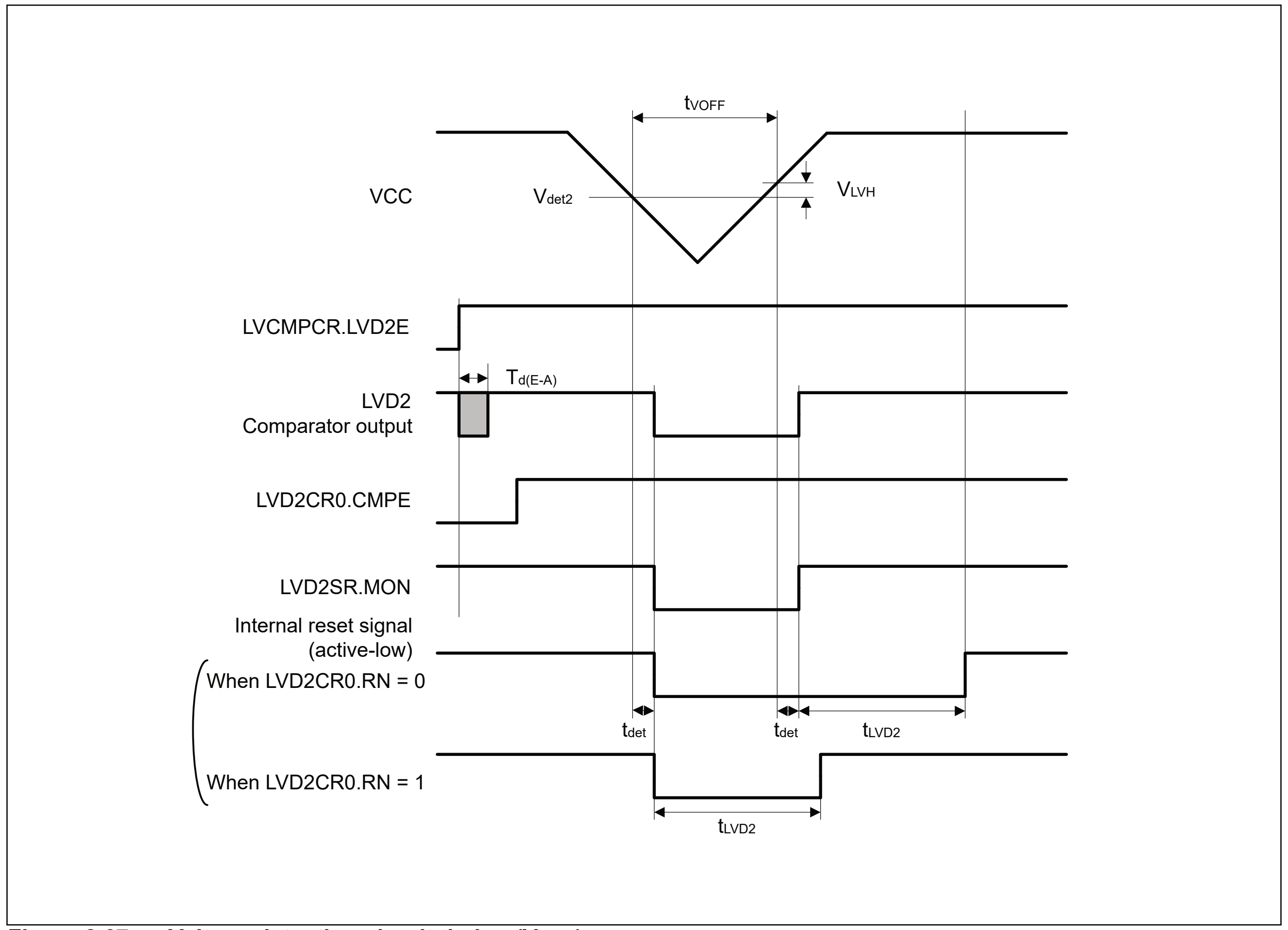


Figure 2.67 Voltage detection circuit timing (V_{det2})

2.10 Flash Memory Characteristics

2.10.1 Code Flash Memory Characteristics

Table 2.44 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

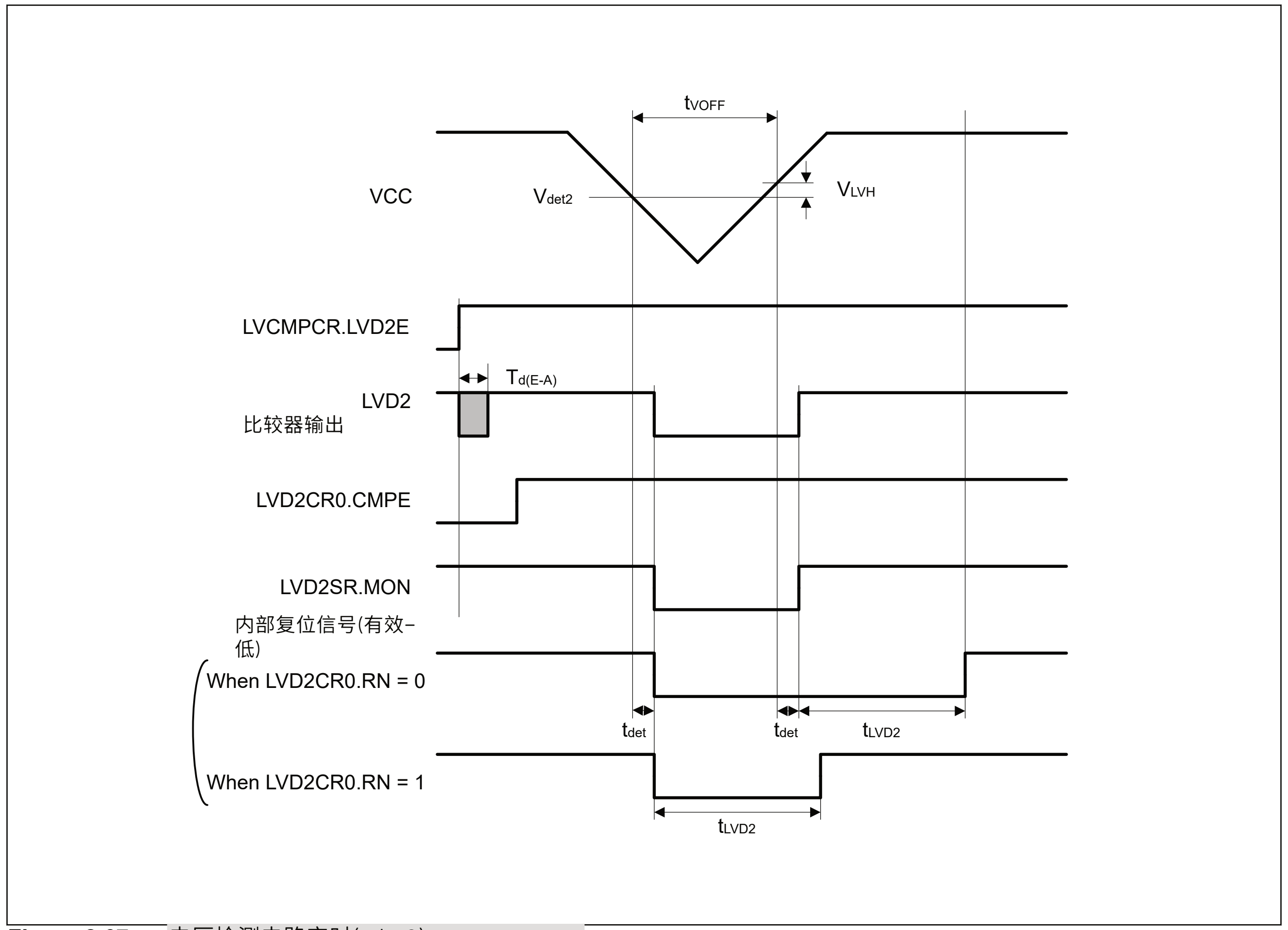


Figure 2.67 电压检测电路定时(vdet2)

2.10 闪存特性

2.10.1 代码闪存特性

Table 2.44 代码闪存特性（1/2）

条件：程序或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	Typ*6	Max	Min	Typ*6	Max		
编程时间NPEC≤10 0次	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
编程时间NPEC>10 0次	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
擦除时间 NPEC≤100次	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	

Table 2.44 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

		FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz				
Parameter	Symbol	Min	Typ*6	Max	Min	Typ*6	Max	Unit	Test conditions
Suspend delay during programming	t_{SPD}	—	—	264	—	—	120	μs	
Programming resume time	t_{PRT}	—	—	110	—	—	50	μs	
First suspend delay during erasure in suspend priority mode	t_{SESD1}	—	—	216	—	—	120	μs	
Second suspend delay during erasure in suspend priority mode	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode	t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode	t_{REST2}	—	—	144	—	—	80	μs	
Erasing resume time during erasure in erasure priority mode	t_{REET}	—	—	144	—	—	80	μs	
Forced stop command	t_{FD}	—	—	32	—	—	20	μs	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

Table 2.44 代码闪存特性（2/2）

条件：程序或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

		FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz				
Parameter	Symbol	Min	Typ*6	Max	Min	Typ*6	Max	Unit	测试条件
编程期间暂停延迟	t_{SPD}	—	—	264	—	—	120	μs	
编程恢复时间	t_{PRT}	—	—	110	—	—	50	μs	
在挂起优先级模式下擦除期间的第一挂起延迟	t_{SESD1}	—	—	216	—	—	120	μs	
挂起优先级模式下擦除期间的第二挂起延迟	t_{SESD2}	—	—	1.7	—	—	1.7	ms	
在擦除优先模式下擦除期间挂起延迟	t_{SEED}	—	—	1.7	—	—	1.7	ms	
在挂起优先模式下的擦除期间首次擦除恢复时间*5	t_{REST1}	—	—	1.7	—	—	1.7	ms	
挂起优先级模式下擦除期间的第二次擦除恢复时间	t_{REST2}	—	—	144	—	—	80	μs	
擦除优先模式下的擦除期间擦除恢复时间	t_{REET}	—	—	144	—	—	80	μs	
强制停止命令	t_{FD}	—	—	32	—	—	20	μs	
数据保持时间*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围是从1到最小值。注2。这表示在指定范围内执行重编程时特性的最小值。

注3。该结果是从可靠性测试中获得的。
注4。重编程擦除周期是每个块的擦除次数。当重编程擦除周期为n次（n=10 000)时，可以对每个块执行n次擦除。例如，当对8-KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为一。但是，在一次擦除时多次编程相同的地址是不启用的。禁止复盖。注5。恢复时间包括重新应用在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。

注6。Vcc=3.3V和室温下的参考值。

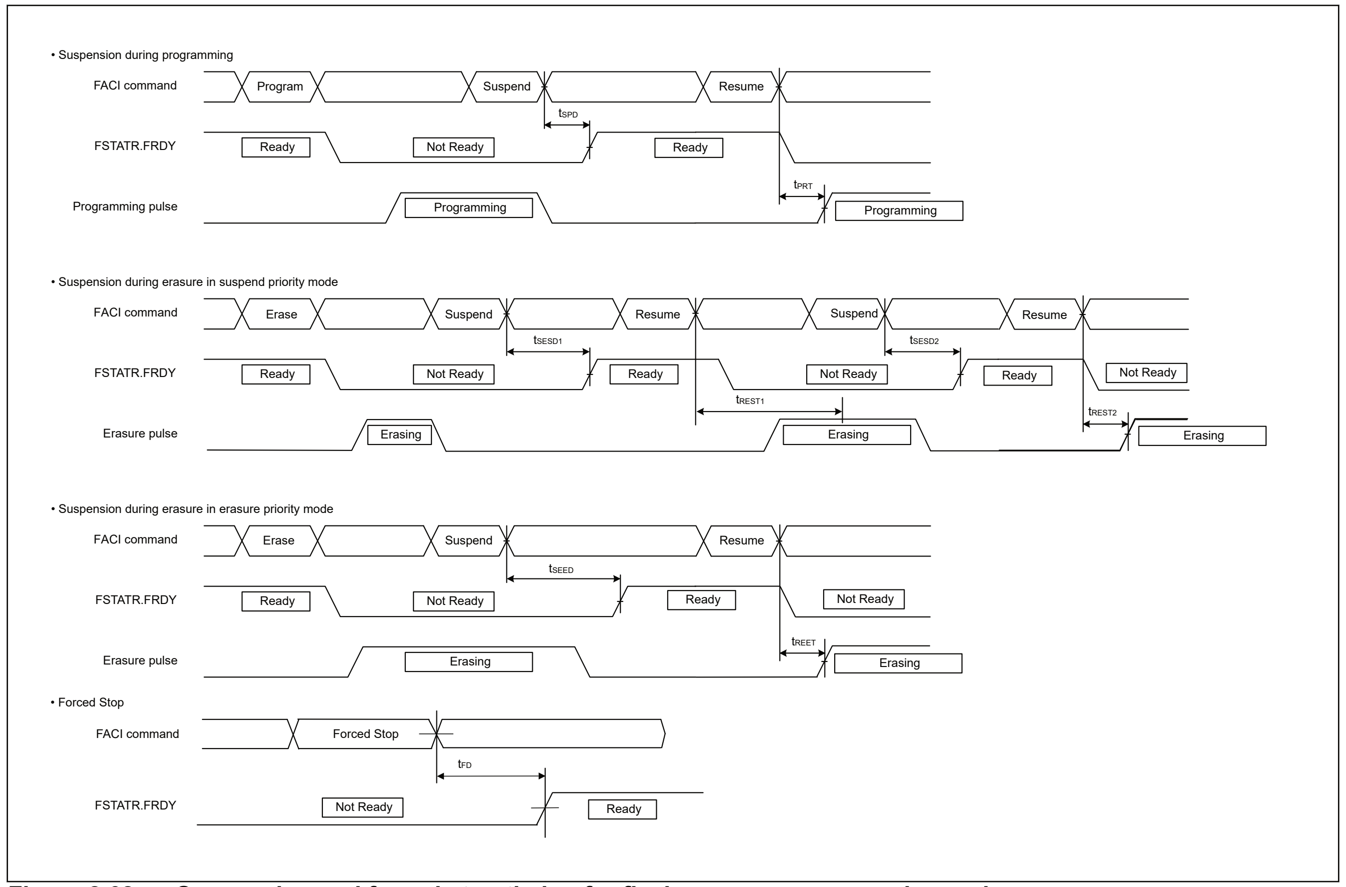


Figure 2.68 Suspension and forced stop timing for flash memory programming and erasure

2.10.2 Data Flash Memory Characteristics

Table 2.45 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	μs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	μs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	μs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	μs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

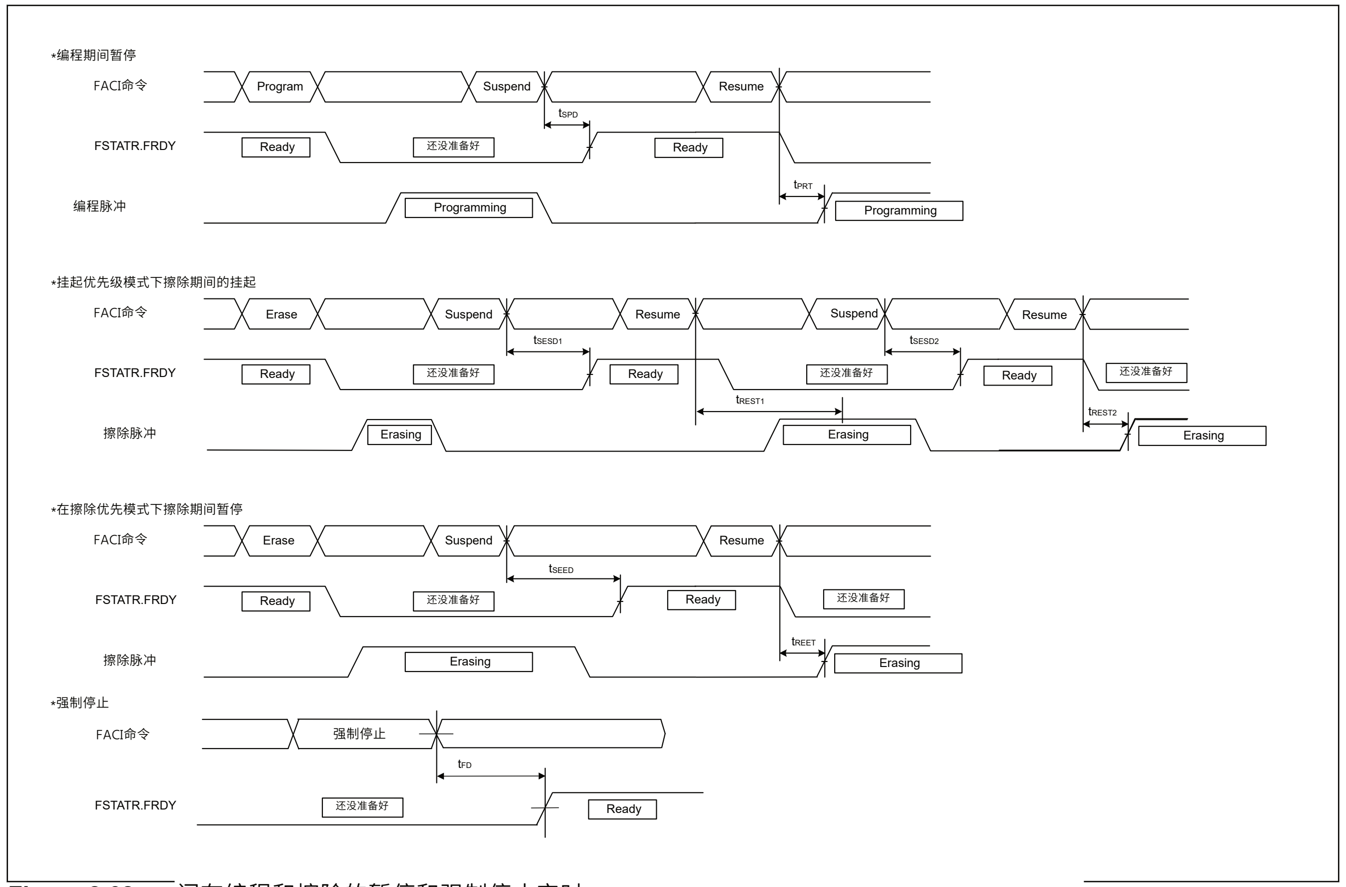


Figure 2.68 闪存编程和擦除的暂停和强制停止定时

2.10.2 数据闪存特性

Table 2.45 数据闪存特性（1/2）

条件：程序或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	Typ*6最大最小			Typ*6	Max		
编程时间	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
擦除时间	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
空白检查时间	4-byte	t_{DBC4}	—	—	84	—	—	30	μs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
编程期间暂停延迟	4-byte	t_{DSPD}	—	—	264	—	—	120	μs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
编程恢复时间		t_{DPRT}	—	—	110	—	—	50	μs	
挂起优先级模式下擦除期间的第一挂起延迟	64-byte	t_{DSESD1}	—	—	216	—	—	120	μs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

Table 2.45 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	μs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	μs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	μs	
Forced stop command		t_{FD}	—	—	32	—	—	20	μs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

2.10.3 Option Setting Memory Characteristics

Table 2.46 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

Table 2.45 数据闪存特性（2/2）

条件：程序或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	Typ*6最大最小			Typ*6	Max		
挂起优先级模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
在挂起优先模式下的擦除期间首次擦除恢复时间*5		t_{DREST1}	—	—	300	—	—	300	μs	
在挂起优先级模式下擦除期间的第二次擦除恢复时间在挂起优先级模式下擦除期间的第二次擦除恢复时间		t_{DREST2}	—	—	126	—	—	70	μs	
擦除优先模式下的擦除期间擦除恢复时间		t_{DREET}	—	—	126	—	—	70	μs	
强制停止命令		t_{FD}	—	—	32	—	—	20	μs	
数据保持时间*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

注1。重编程擦除周期是每个块的擦除次数。当重编程擦除周期为n次（n=125 000)时，可对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期被计为一。但是，在一次擦除时多次编程相同的地址是不启用的。禁止复盖。注2。这是保证重新编程后所有特性的最小次数。保证范围是从1到最小值。注3。这表示在指定范围内执行重编程时特性的最小值。

注4。该结果是从可靠性测试中获得的。
注5。恢复时间包括重新应用在暂停时被切断的擦除脉冲（最多一个完整脉冲）的时间。
注6。Vcc=3.3V和室温下的参考值。

2.10.3 选项设置内存特性

Table 2.46 选项设置内存特性

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
编程时间NOPC≤100次	t_{OP}	—	83	309	—	45	162	ms	
编程时间NOPC>100次	t_{OP}	—	100	371	—	55	195	ms	
重编程周期	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
数据保持时间*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1。这是保证重新编程后所有特性的最小次数。保证范围是从1到最小值。注2。这表示在指定范围内执行重编程时特性的最小值。

注3。该结果是从可靠性测试中获得的。
注4。Vcc=3.3V和室温下的参考值。

2.11 Serial Wire Debug (SWD)

Table 2.47 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 2.69
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 2.70
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

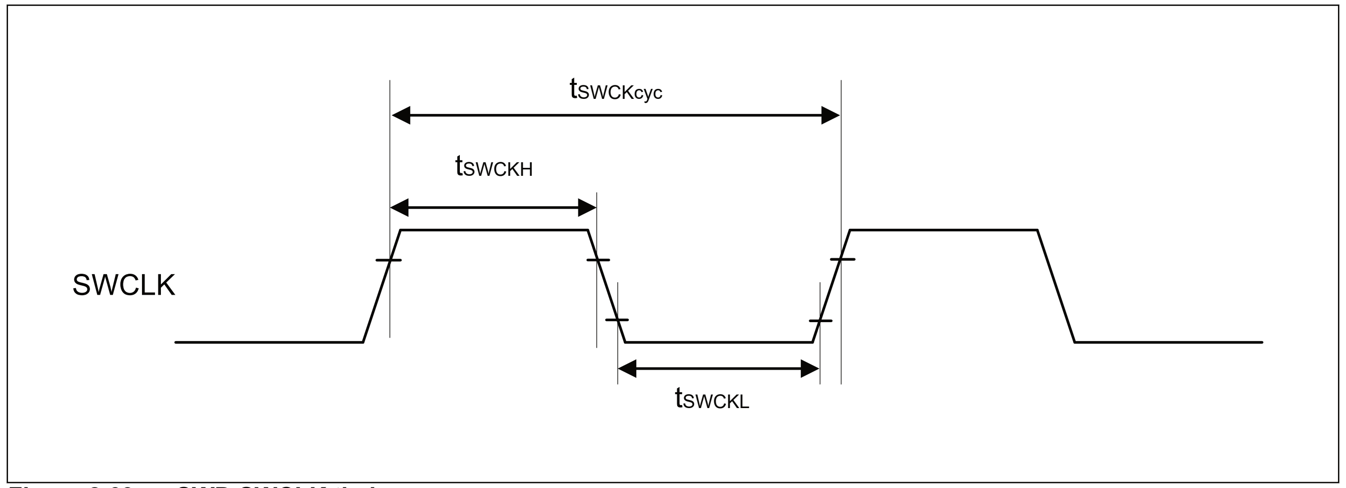


Figure 2.69 SWD SWCLK timing

2.11 串行线调试(SWD)

Table 2.47 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	—	—	ns	Figure 2.69
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	8	—	—	ns	Figure 2.70
SWDIO保持时间	t_{SWDH}	8	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	28	ns	

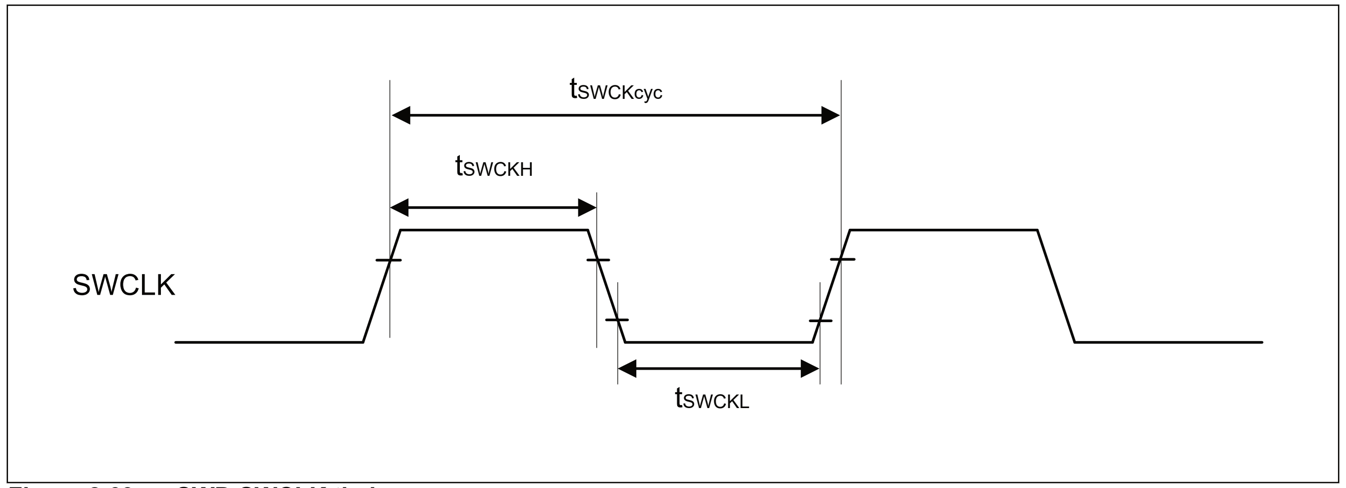


Figure 2.69 SWD SWCLK timing

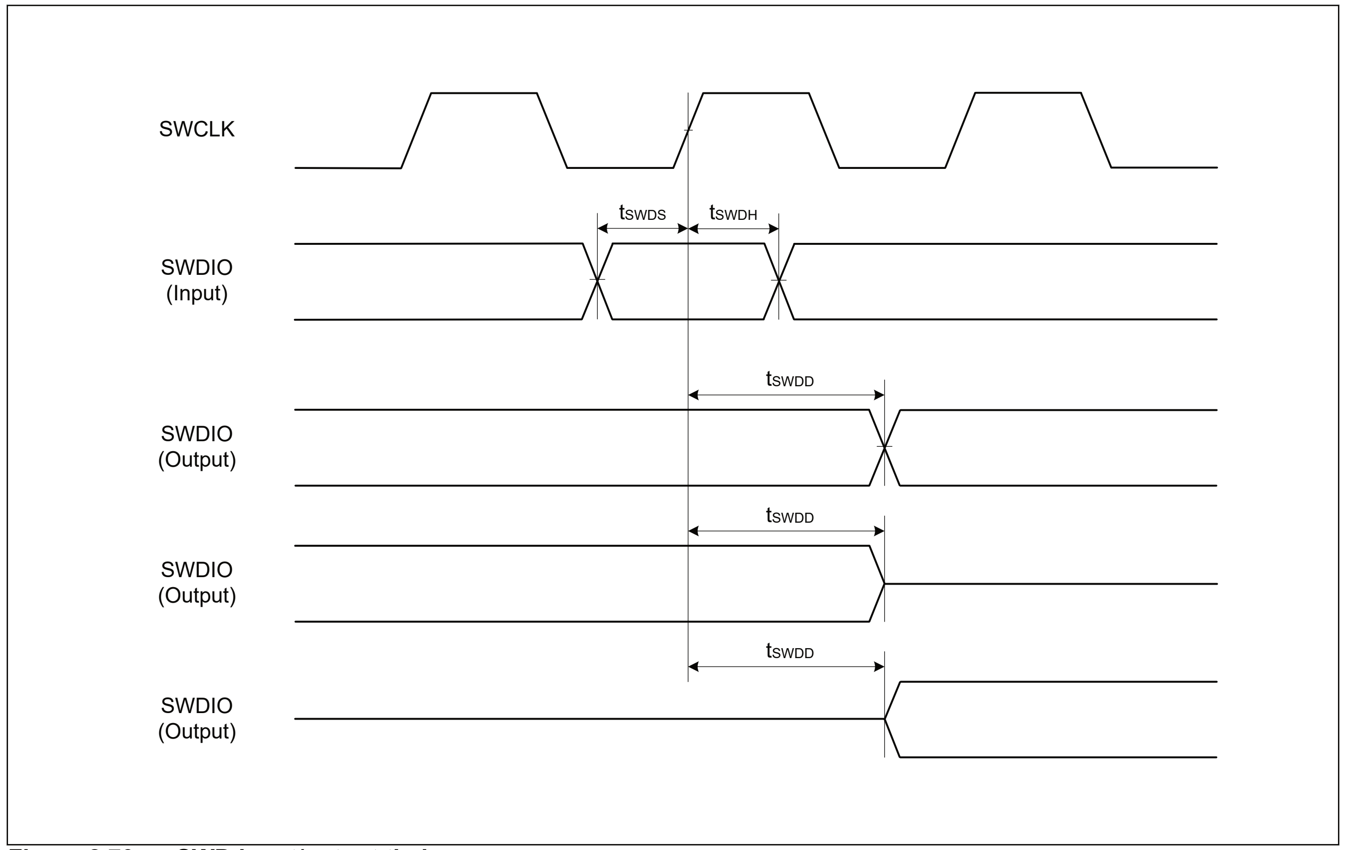


Figure 2.70 SWD input/output timing

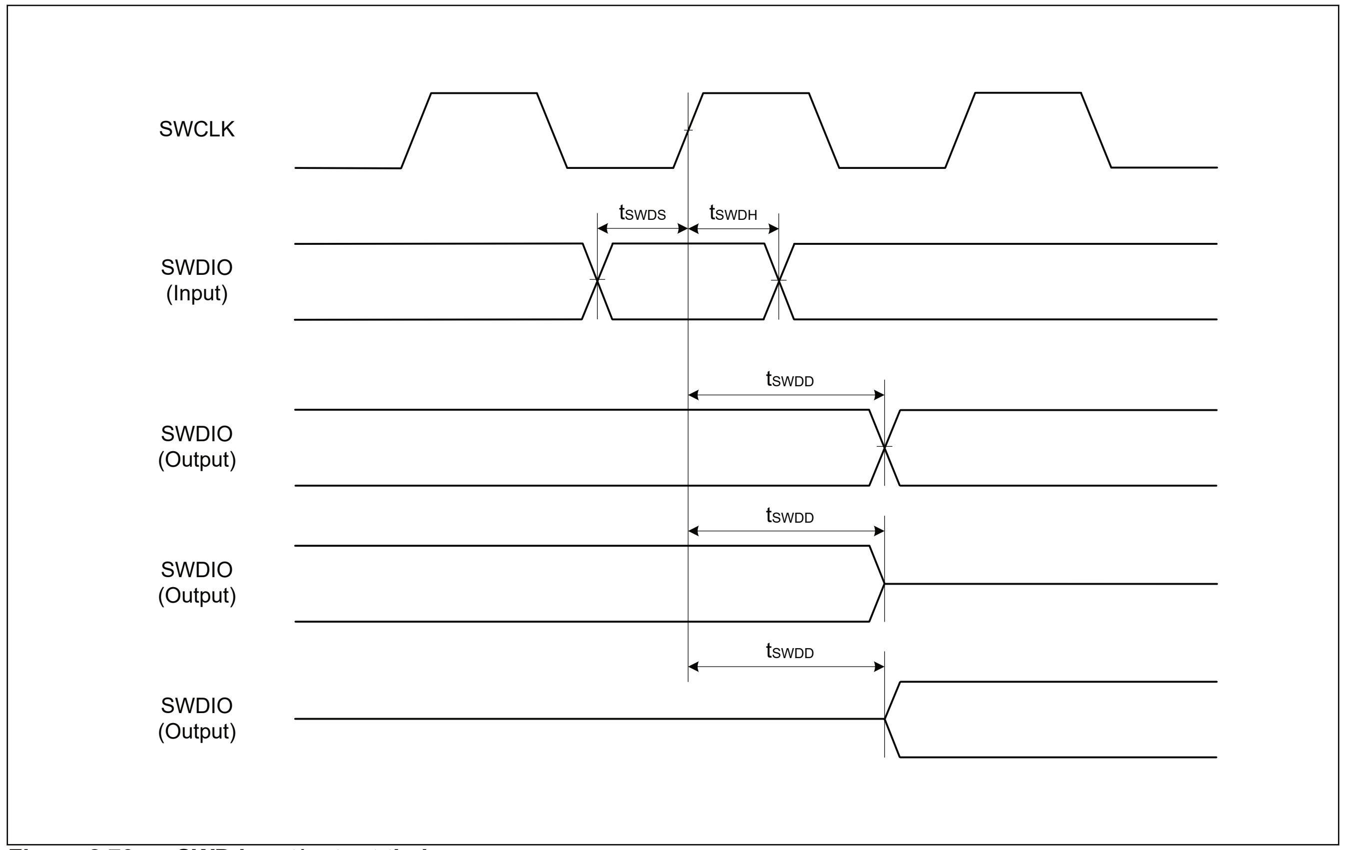


Figure 2.70 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1[*1]
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
	AGTIOn (n = 1)	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
USBFS	USB_VBUS	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O[*4]	Keep[*3]	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
	RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input pin.

Appendix 1. 每种处理模式下的端口状态

Function	引脚功能	Reset	软件待机模式	深度软件待机模式	软件待机模式取消后（返回启动模式）	
					IOKEEP = 0	IOKEEP = 1[*1]
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
	AGTIOn (n = 1)	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	Hi-Z	Keep-O[*2]	Keep	Hi-Z	Keep
USBFS	USB_VBUS	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O[*4]	Keep[*3]	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Keep-O[*2]	Keep[*3]	Hi-Z	Keep
	RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[丹输出(DAOE=1)]Da输出保留	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O：输出引脚保留其以前的值。输入引脚进入高阻抗。
保持：引脚状态在软件待机模式期间保留。

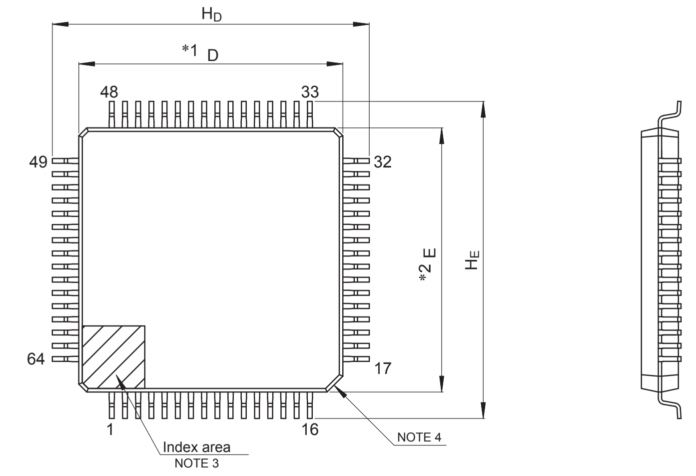
注1。保留IO端口状态，直到DPSBYCR。Iokeep位清零为0。
注2。如果该引脚被指定为软件待机消除源，而它被用作外部中断引脚，则使能输入。
注3。如果将引脚指定为深度软件待机取消源，则启用输入。
注4。引脚用作输入引脚时使能输入。

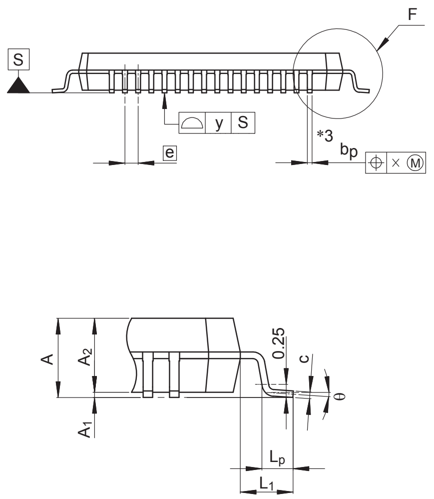
Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm





Detail F

NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

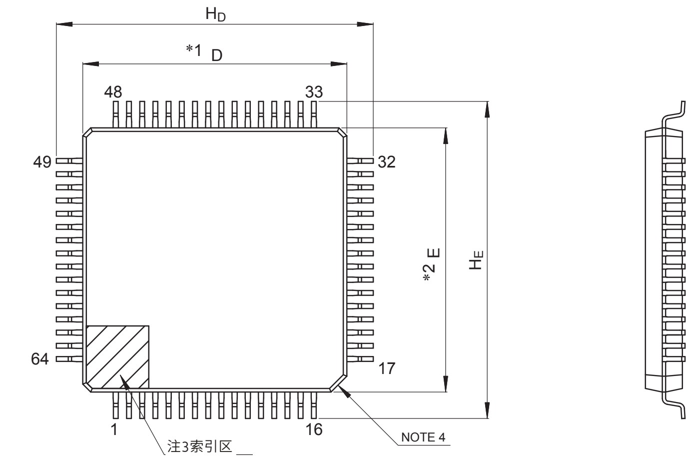
Figure 2.1 LQFP 64-pin

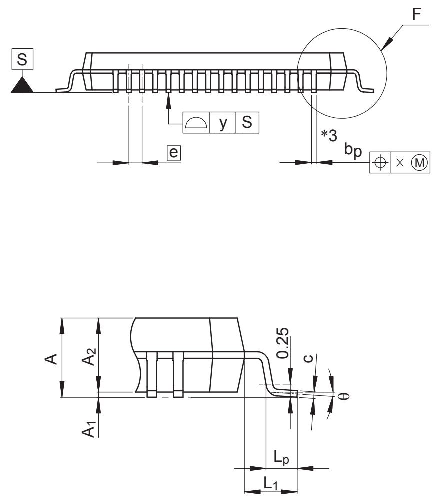
Appendix 2. 包装尺寸

有关最新版本的软件包尺寸或安装的信息显示在瑞萨的"软件包"中电子公司网站。

JEITA套餐代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm





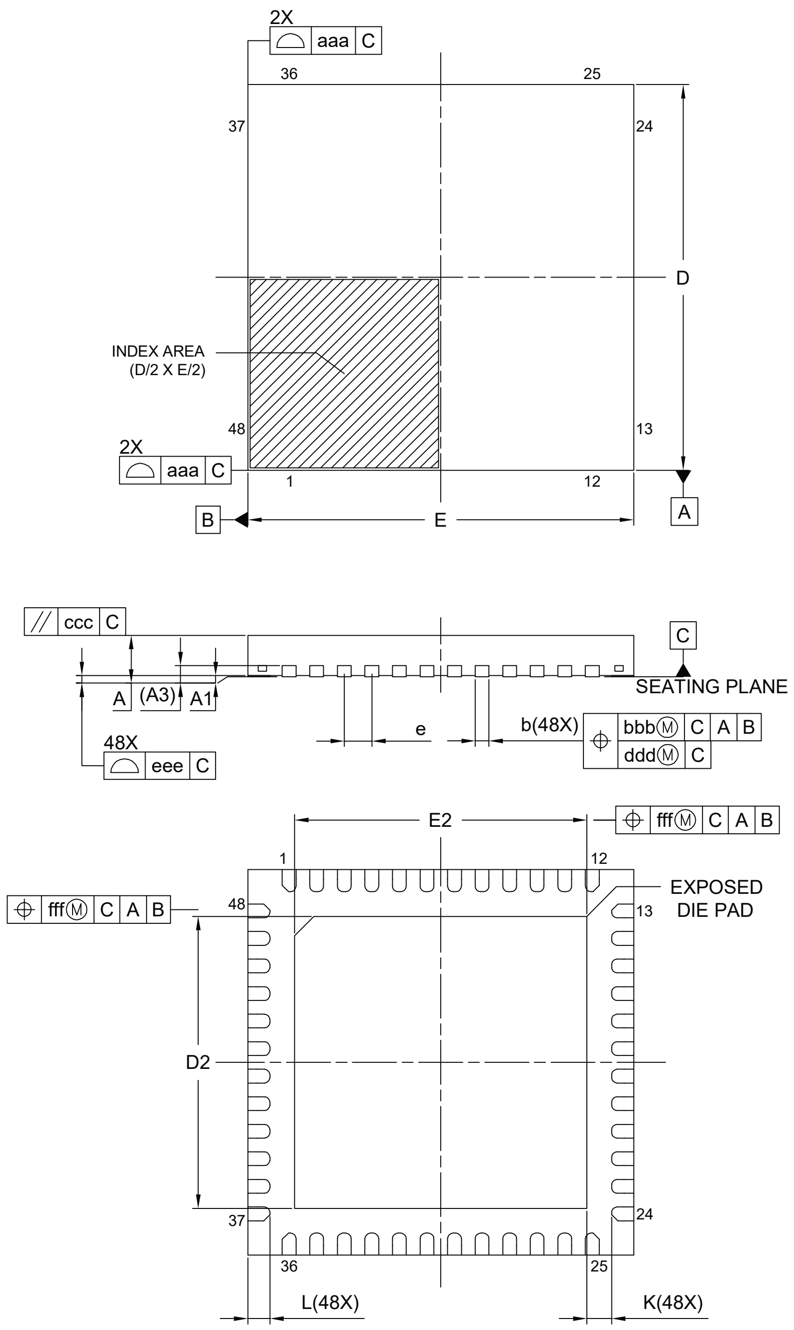
Detail F

注）1．尺寸"*1"和"*2"不包括模具闪光。2.尺寸"*3"不包括修剪偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于影线区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.1 LQFP 64-pin

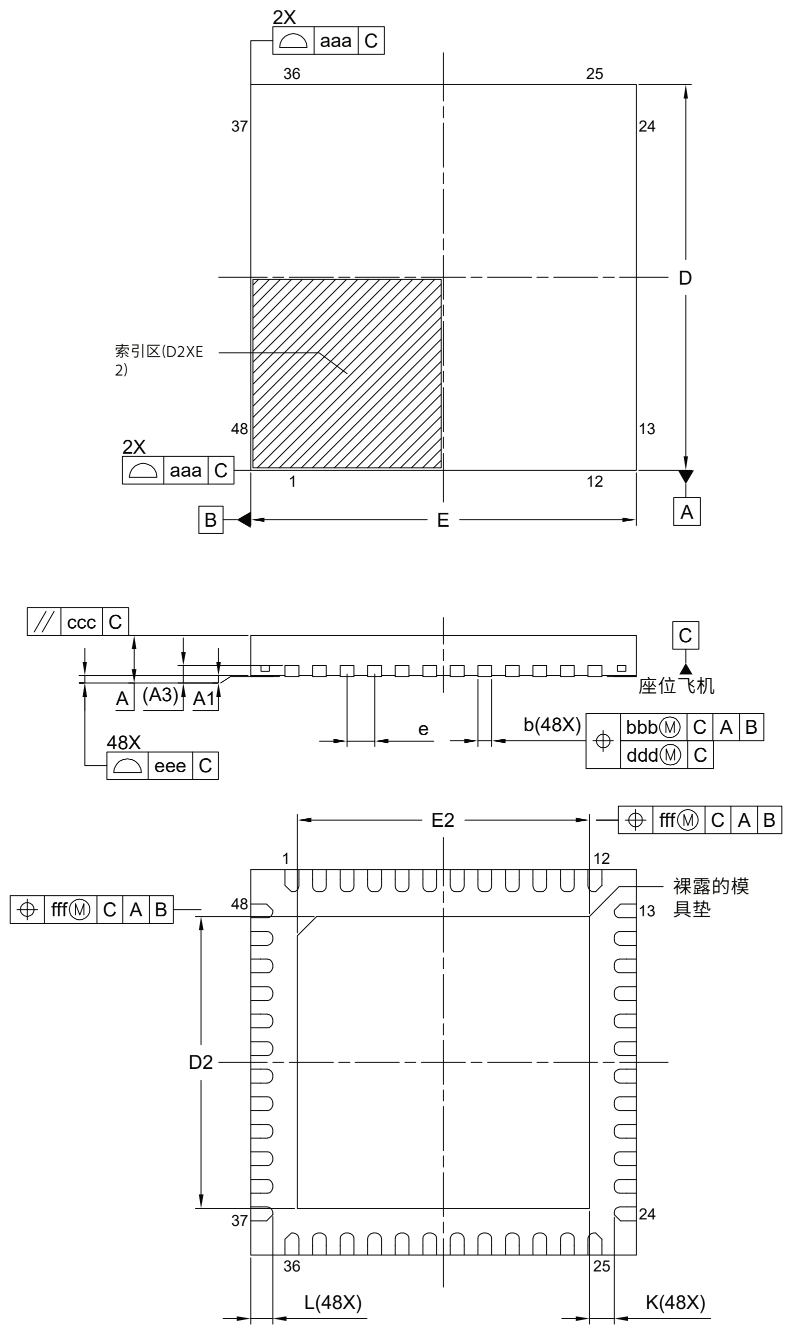
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.2 QFN 48-pin

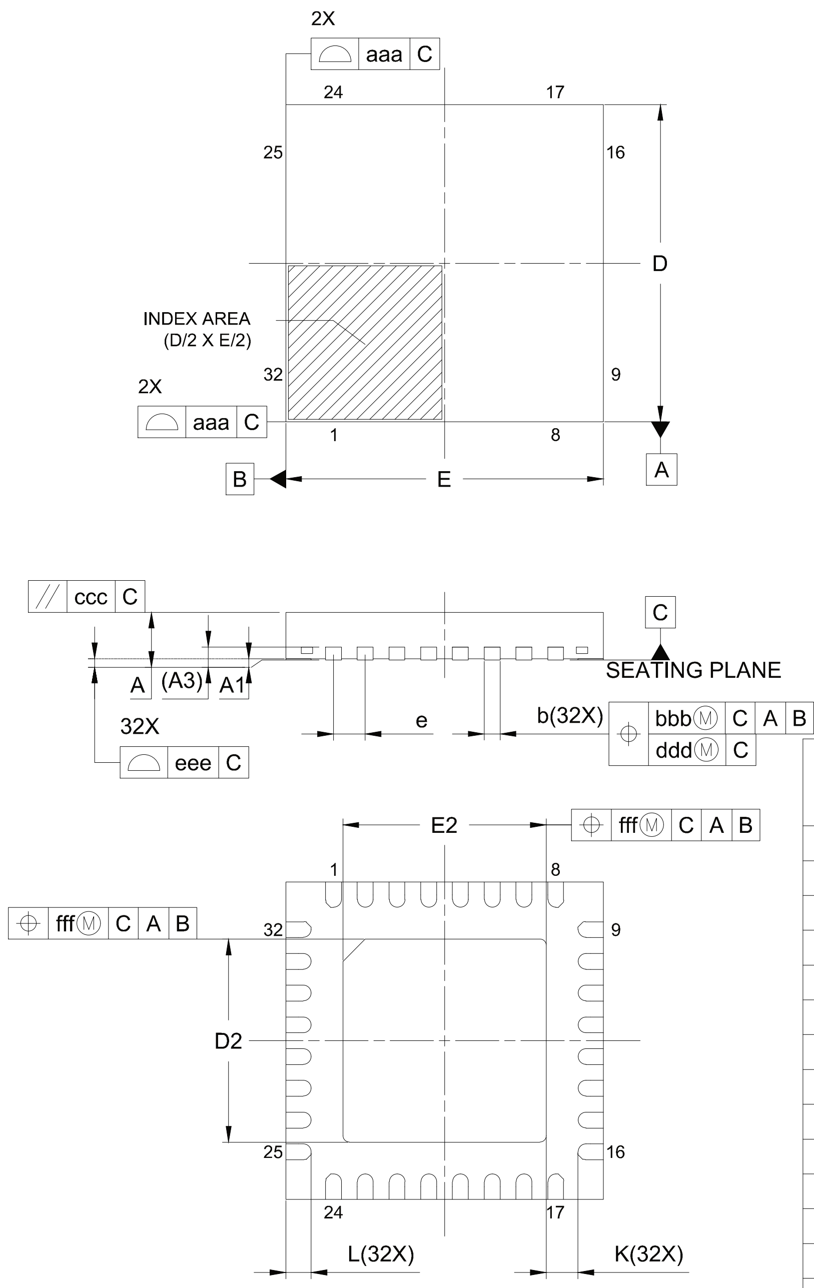
JEITA套餐代码	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	尺寸以毫米为单位		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.2 QFN 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06

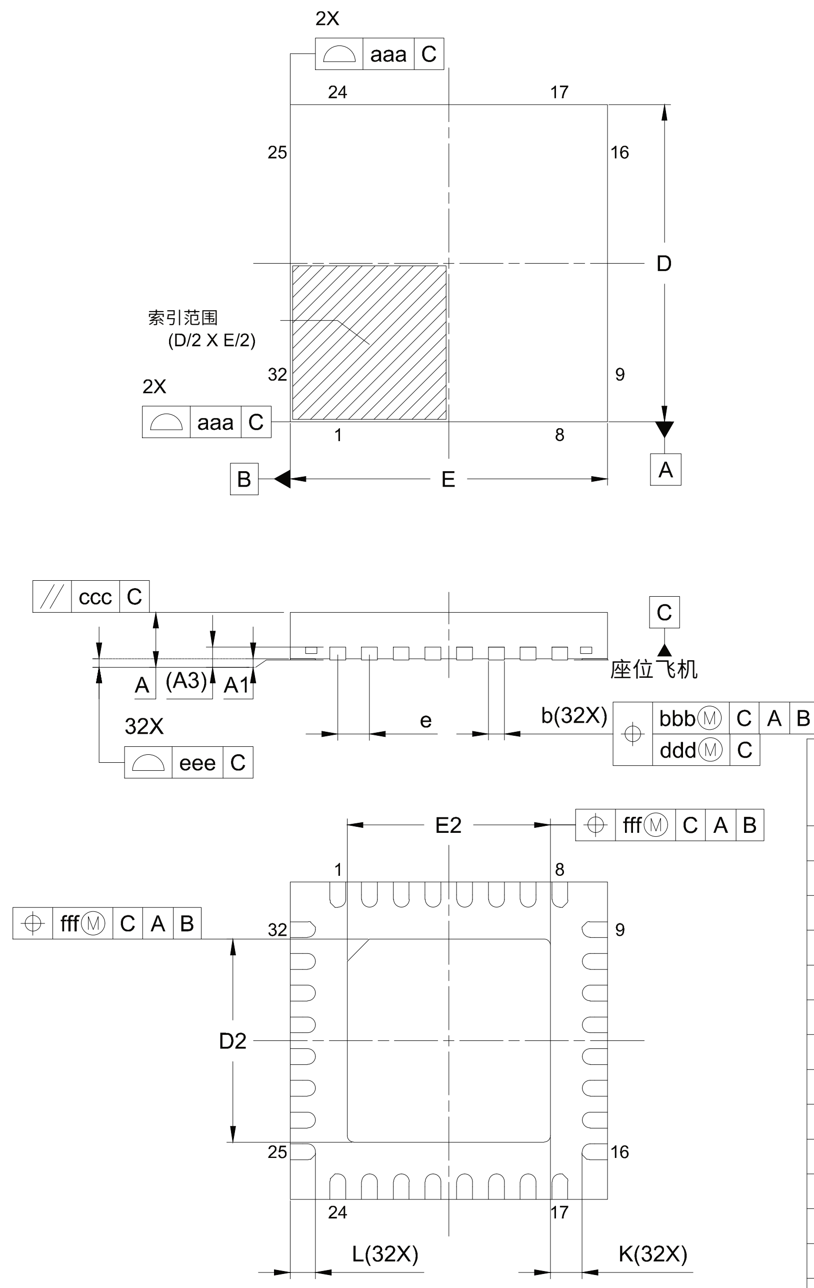


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.3 QFN 32-pin

瑞萨电子有限公司

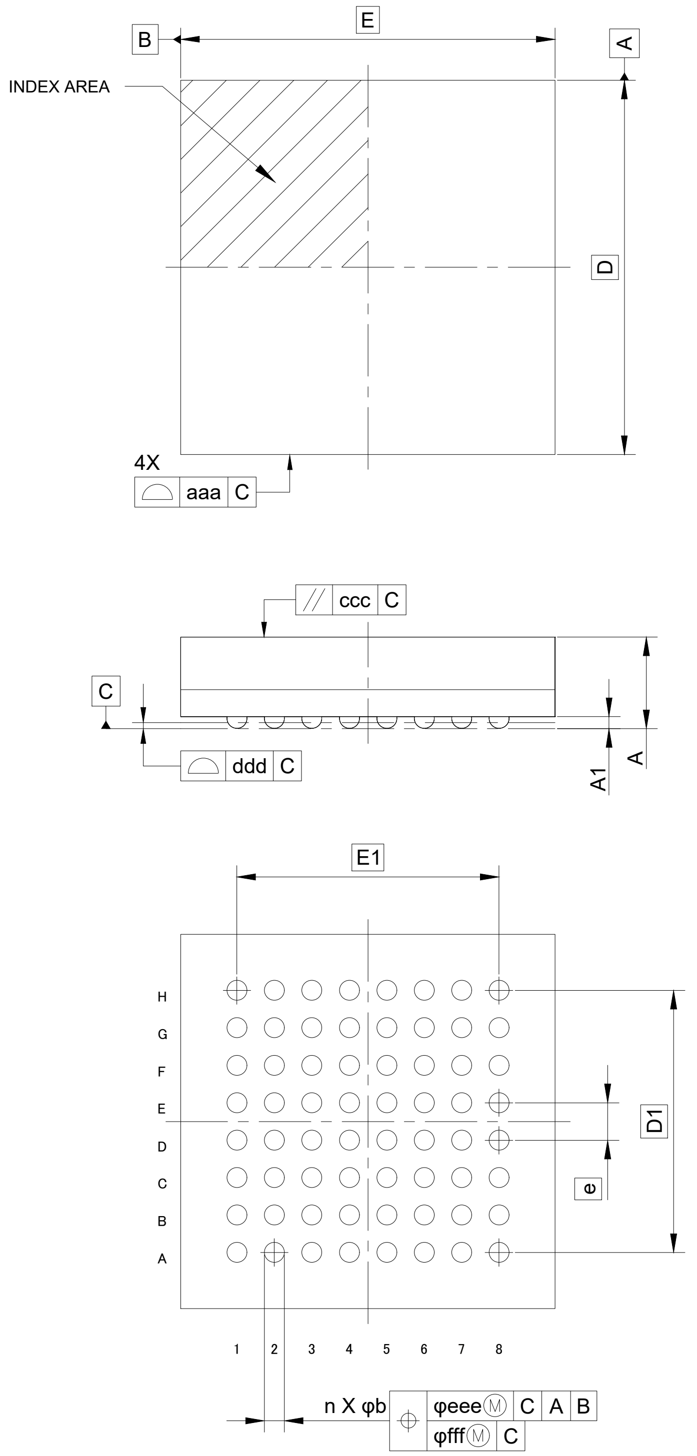
JEITA套餐代码	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	尺寸以毫米为单位		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 2.3 QFN 32-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA64-5x5-0.50	PLBG0064KB-A	0.06

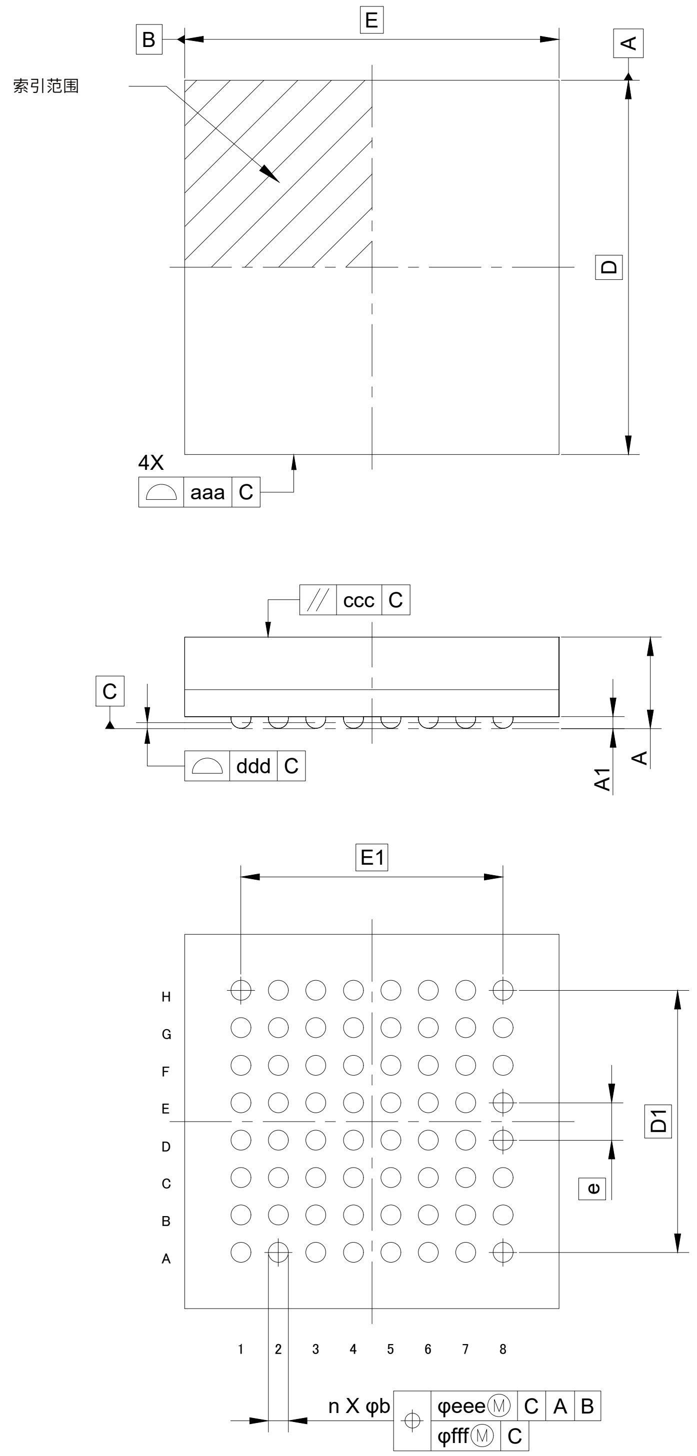


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	5.00	—
E	—	5.00	—
D1	—	3.50	—
E1	—	3.50	—
A	—	—	1.29
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	64	—

Figure 2.4 BGA 64-pin

外形图

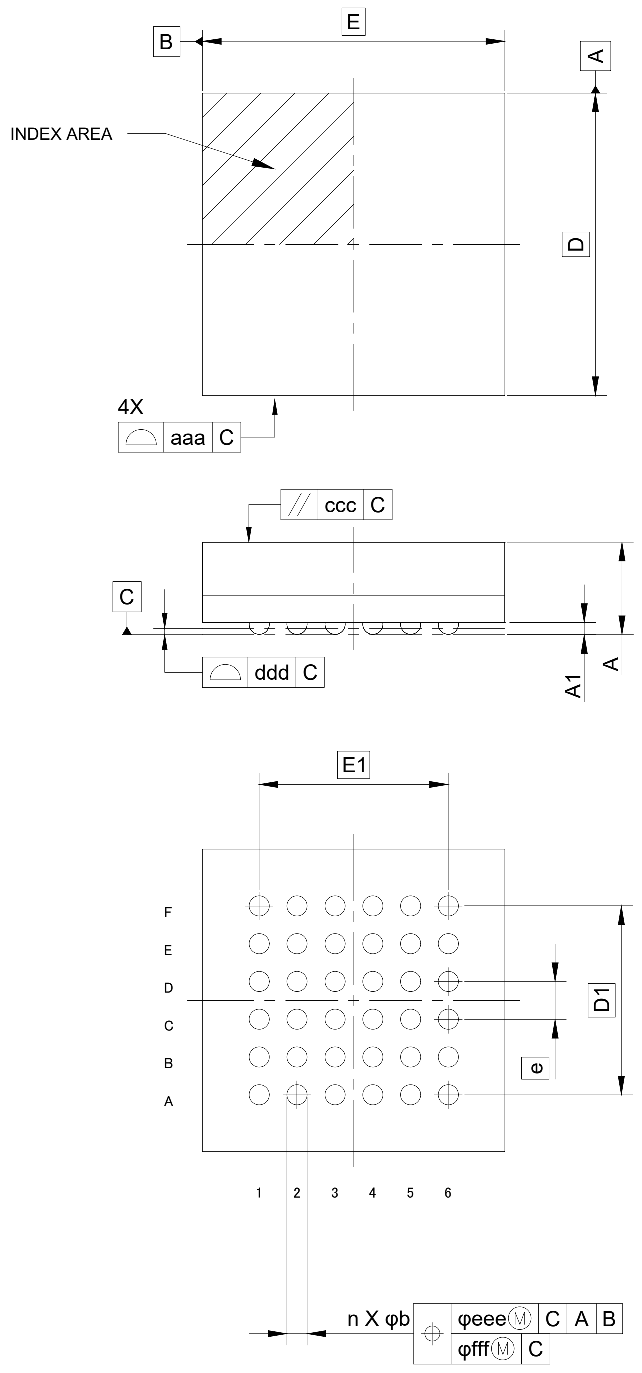
JEITA套餐代码	RENESAS code	MASS(TYP.)[g]
P-LFBGA64-5x5-0.50	PLBG0064KB-A	0.06



Reference Symbol	尺寸以毫米为单位		
	Min.	Nom.	Max.
D	—	5.00	—
E	—	5.00	—
D1	—	3.50	—
E1	—	3.50	—
A	—	—	1.29
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	64	—

Figure 2.4 BGA 64-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA36-4x4-0.50	PLBG0036KA-A	0.04

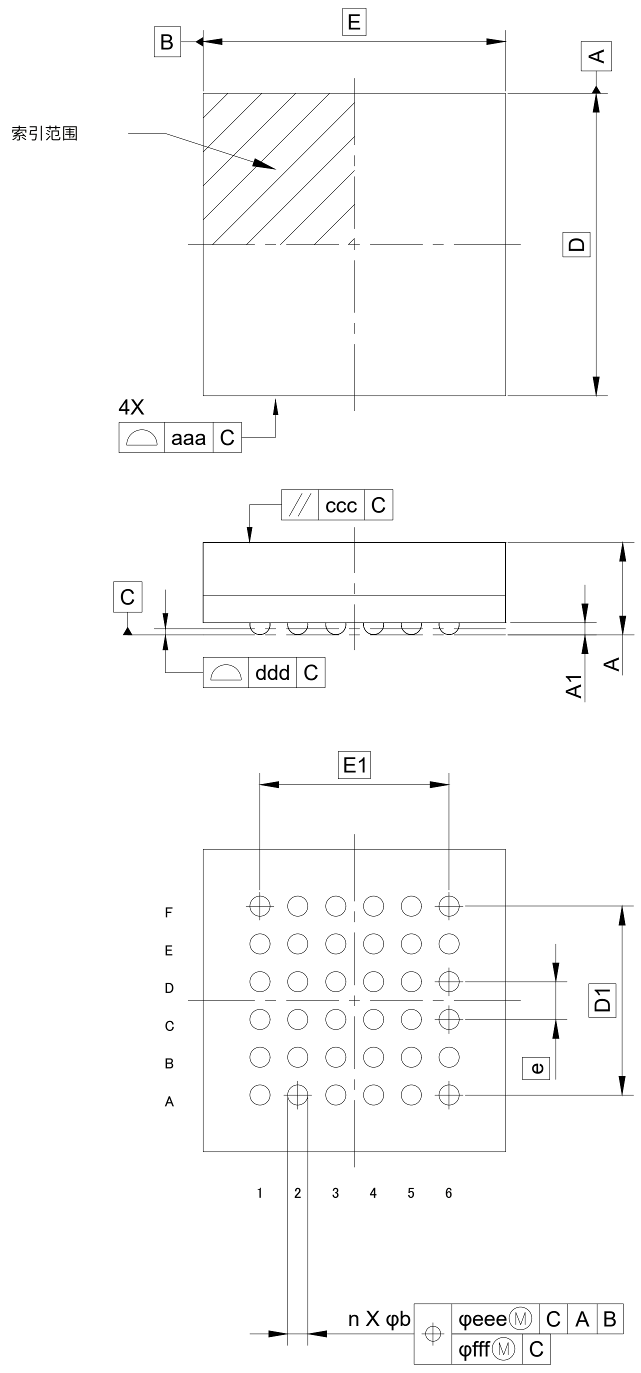


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	4.00	—
E	—	4.00	—
D1	—	2.50	—
E1	—	2.50	—
A	—	—	1.29
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	36	—

Figure 2.5 BGA 36-pin

外形图

JEITA套餐代码	RENESAS code	MASS(TYP.)[g]
P-LFBGA36-4x4-0.50	PLBG0036KA-A	0.04



Reference Symbol	尺寸以毫米为单位		
	Min.	Nom.	Max.
D	—	4.00	—
E	—	4.00	—
D1	—	2.50	—
E1	—	2.50	—
A	—	—	1.29
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	36	—

Figure 2.5 BGA 36-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x400_1B000
FCACHE	Flash Cache	0x400_1C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PORT5	Port 5 Control Registers	0x4008_00A0
PORT8	Port 8 Control Registers	0x4008_0100
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
RTC	Realtime Clock	0x4008_3000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000

Appendix 3. I/O Registers

本附录按功能描述IO寄存器地址和访问周期。

3.1 外围基地址

本节提供本手册中描述的外围设备的基本地址.表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外围基地址(1/2)

Name	Description	基地址
RMPU	瑞萨存储器保护单元	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	总线控制	0x4000_3000
DMAC0	直接内存访问控制器0	0x4000_5000
DMAC1	直接存储器存取控制器1	0x4000_5040
DMAC2	直接存储器存取控制器2	0x4000_5080
DMAC3	直接存储器存取控制器3	0x4000_50C0
DMAC4	直接存储器存取控制器4	0x4000_5100
DMAC5	直接存储器存取控制器5	0x4000_5140
DMAC6	直接存储器存取控制器6	0x4000_5180
DMAC7	直接存储器存取控制器7	0x4000_51C0
DMA	DMAC模块激活	0x4000_5200
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU系统安全控制单元	0x4000_8000
DBG	调试功能	0x400_1B000
FCACHE	闪存缓存	0x400_1C100
SYSC	系统控制	0x4001_E000
PORT0	端口0控制寄存器	0x4008_0000
PORT1	端口1控制寄存器	0x4008_0020
PORT2	端口2控制寄存器	0x4008_0040
PORT3	端口3控制寄存器	0x4008_0060
PORT4	端口4控制寄存器	0x4008_0080
PORT5	端口5控制寄存器	0x4008_00A0
PORT8	端口8控制寄存器	0x4008_0100
PFS	Pmn引脚功能控制寄存器	0x4008_0800
ELC	事件链接控制器	0x4008_2000
RTC	实时时钟	0x4008_3000
IWDT	独立看门狗定时器	0x4008_3200
WDT	看门狗定时器	0x4008_3400
CAC	时钟频率精度测量电路	0x4008_3600
MSTP	模块停止控制A、B、C、D	0x4008_4000
POEG	用于GPT的端口输出使能模块	0x4008_A000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
USBFS	USB 2.0 FS Module	0x4009_0000
SSIE0	Serial Sound Interface Enhanced (SSIE)	0x4009_D000
CEC	Consumer Electronics Control	0x400A_C000
CANFD	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
SPI1	Serial Peripheral Interface 1	0x4011_A100
I3C	I3C Bus Interface	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	General PWM 16-Bit Timer 0 (16-bit Enhanced High Resolution)	0x4016_9000
GPT16E1	General PWM 16-Bit Timer 1 (16-bit Enhanced High Resolution)	0x4016_9100
GPT16E2	General PWM 16-Bit Timer 2 (16-bit Enhanced High Resolution)	0x4016_9200
GPT16E3	General PWM 16-Bit Timer 3 (16-bit Enhanced High Resolution)	0x4016_9300
GPT16E4	General PWM 16-Bit Timer 4 (16-bit Enhanced High Resolution)	0x4016_9400
GPT16E5	General PWM 16-Bit Timer 5 (16-bit Enhanced High Resolution)	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000
QSPI	Quad-SPI	0x6400_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.

Table 3.1 外围基地址(2/2)

Name	Description	基地址
USBFS	USB2.0FS模块	0x4009_0000
SSIE0	串行声音接口增强(SSIE)	0x4009_D000
CEC	消费电子控制	0x400A_C000
CANFD	CANFD模块控制	0x400B_0000
PSCU	外围安全控制单元	0x400E_0000
AGT0	低功耗异步通用定时器0	0x400E_8000
AGT1	低功耗异步通用定时器1	0x400E_8100
TSN	温度传感器	0x400F_3000
CRC	CRC Calculator	0x4010_8000
DOC	数据运算电路	0x4010_9000
SCI0	串行通信接口0	0x4011_8000
SCI9	串行通信接口9	0x4011_8900
SPI0	串行外设接口0	0x4011_A000
SPI1	串行外设接口1	0x4011_A100
I3C	I3C总线接口	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	通用PWM16位定时器0（16位增强高分辨率）	0x4016_9000
GPT16E1	通用PWM16位定时器1（16位增强高分辨率）	0x4016_9100
GPT16E2	通用PWM16位定时器2（16位增强高分辨率）	0x4016_9200
GPT16E3	通用PWM16位定时器3（16位增强高分辨率）	0x4016_9300
GPT16E4	通用PWM16位定时器4（16位增强高分辨率）	0x4016_9400
GPT16E5	通用PWM16位定时器5（16位增强高分辨率）	0x4016_9500
GPT_OPS	输出相位切换控制器	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	数据闪	0x407F_C000
FACI	Flash应用程序命令接口	0x407F_E000
QSPI	Quad-SPI	0x6400_0000

Note: Name=外设名称
描述=外围功能
Baseaddress=最低预留地址或外设使用的地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

●寄存器按相关模块分组。

●访问周期数表示基于指定参考时钟的周期数。

●在内部IO区域，不得访问未分配给寄存器的保留地址，否则无法保证操作。

●IO访问周期数取决于内部外设总线的总线周期、划分的时钟同步周期和每个模块的等待周期。划分的时钟同步周期取决于ICLK和PCLK之间的频率比。

●当ICLK的频率等于PCLK时，分频时钟同步周期数始终不变。

- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK[*1]		Cycle Unit	
Peripherals	From	To	Read	Write	Read	Write		Related function
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, RTC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	Module Stop Control
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable Module for GPT
USBFS	0x4009_0000	0x4009_03FF	6	5	3 to 6	3 to 5	PCLKB	USB 2.0 FS Module
USBFS	0x4009_0400	0x4009_04FF	4	3	1 to 4	1 to 3	PCLKB	USB 2.0 FS Module
SSIE0	0x4009_2000	0x4009_FFFF	5	4	2 to 5	2 to 4	PCLKB	SD Host Interface 0, Serial Sound Interface Enhanced, Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit
CEC	0x400A_C000	0x400A_CFFF	4	3	1 to 3	1 to 3	PCLKB	Consumer Electronics Control
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit

●当ICLK的频率大于PCLK时，将至少1个PCLK周期加到划分的时钟同步周期数中。

●写访问周期数表示非缓冲写访问获得的周期数。

Note: 这适用于从CPU访问与从外部存储器获取指令或从其他总线主控器（如DTC或DMAC）访问总线不冲突的周期数。

Table 3.2 访问周期(1/3)

	Address		访问周期数					
			ICLK = PCLK		ICLK > PCLK[*1]		Cycle Unit	
Peripherals	From	To	Read	Write	Read	Write		相关功能
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	瑞萨存储器保护单元，TrustZone过滤器 SRAM控制，总线控制，直接存储器访问控制器n，DMAC模块激活，DTC控制寄存器 中断控制器
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU系统安全控制单元，调试功能，闪存缓存
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	系统控制
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	系统控制
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	端口N控制寄存器，Pmn引脚功能控制 Register
ELC, RTC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	事件链接控制器 实时时钟，独立的看门狗定时器，看门狗定时器，时钟频率 Accuracy 测量电路
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	模块停止控制
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	端口输出使能 GPT模块
USBFS	0x4009_0000	0x4009_03FF	6	5	3 to 6	3 to 5	PCLKB	USB2.0FS模块
USBFS	0x4009_0400	0x4009_04FF	4	3	1 to 4	1 to 3	PCLKB	USB2.0FS模块
SSIE0	0x4009_2000	0x4009_FFFF	5	4	2 to 5	2 to 4	PCLKB	SD主机接口0 串行声音接口 增强的，增强的 集成电路n 集成电路间0唤醒单元
CEC	0x400A_C000	0x400A_CFFF	4	3	1 to 3	1 to 3	PCLKB	消费电子产品 Control
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	外围安全管制组
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	低功耗 Asynchronous 一般用途 Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	温度传感器
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC计算器，数据操作电路

Table 3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
SCIn	0x4011_8000	0x4011_8FFF	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Peripheral Interface n
I3C	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	I3C Bus Interface
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module
GPT16En, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter
QSPI	0x6400_0010	0x6400_0013	25 to *4	6 to *4	25 to *4	5 to *4	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *4	2 to 5	14 to *4	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table 3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Note 4. The access cycles depend on the QSPI bus cycles.

Table 3.2 访问周期(2的3)

Peripherals	Address		访问周期数					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	相关功能
	From	To	Read	Write	Read	Write		
SCIn	0x4011_8000	0x4011_8FFF	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	串行通信 Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	串行外设 Interface n
I3C	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	I3C总线接口
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module
GPT16En, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	通用PWM16位定时器n，输出相位开关控制器
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter
QSPI	0x6400_0010	0x6400_0013	25 to *4	6 to *4	25 to *4	5 to *4	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *4	2 to 5	14 to *4	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table 3.2 访问周期(3/3)

Peripherals	Address		访问周期数					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	相关功能
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	数据闪，闪应用程序命令 Interface

注1。如果PCLK或FCLK周期数是非整数（例如1.5），则最小值没有小数点，最大值向上舍入到小数点。例如，1.5到2。5为1比3。注2。当访问一个16位寄存器（FTDRHL，FRDRHL，FCR，FDR，LSR和CDR），访问是2个周期比所示的值

表3.2。当访问一个8位寄存器（包括FTDRH，FTDRL，FRDRH和FRDRL），访问周期如图所示
Table 3.2.

注3。当访问32位寄存器(SPDR)时，访问比表3.2中的值多2个周期。当访问8位或16位寄存器(SPDR_HA)时，访问周期如表3.2所示。注4。访问周期取决于QSPI总线周期。

Revision History

Revision 1.00 — September 26, 2022

Initial release

Revision 1.10 — February 28, 2023

Features:
- Updated the title of Security.

1. Overview:
- Updated Figure 1.1 Block diagram.
- Updated Table 1.11 I/O ports.
- Updated Figure 1.2 Part numbering scheme.
- Updated Table 1.13 Function Comparison.
- Updated Table 1.14 Pin functions.
- Updated Figure 1.4 Pin assignment for BGA 64-pin.
- Updated Figure 1.6 Pin assignment for BGA 36-pin

2. Electrical Characteristics:
- Updated Table 2.5 I/O I_{OH}, I_{OL}.
- Updated Table 2.6 I/O VOH, VOL, and other characteristics.
- Updated Table 2.34 I3C timing (push-pull timing parameters for SDR mode).
- Updated Table 2.37 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics).

Appendix 3. I/O Registers:
- Updated Table 3.2 Access cycles.

修订历史

修订版1.00—2022年9月26日

初始版本

修订版1.10—2023年2月28日

Features:
- 更新了安全性的标题。

1. Overview:
- 更新图1.1框图。
- 更新表1.11IO端口。
- 更新图1.2零件编号方案。
- 更新表1.13功能比较。
- 更新表1.14引脚功能。
- 更新图1.4Bga64引脚的引脚分配。
- 更新图1.6Bga36引脚的引脚分配

2. Electrical Characteristics:
- 更新表2.5IOIOH IOL.
- 更新表2.6IOVOH，VOL和其他特性。
- 更新表2.34I3C定时（SDR模式的推挽定时参数）。
- 更新表2.37USBFS全速特性（USB_DP和USB_DM引脚特性）。

Appendix 3. I/O Registers:
- 更新表3.2访问周期。

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

处理微处理单元和微控制器的一般注意事项
单位产品

以下使用说明适用于瑞萨电子的所有微处理单元和微控制器单元产品。有关
本文档涵盖的产品，请参阅本文档的相关部分以及为产品发布的任何技术更新。

1. 防止静电放电(ESD)的预防措施
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的工作性能。步骤
   必须采取尽可能停止静电的产生，并在发生时迅速消散。环境控制必须是
   足够了。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。
   半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试及
   包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体 半导体
   设备不得徒手触摸。对于安装有半导体器件的印刷电路板必须采取类似的预防措施。
2. 开机处理
   产品的状态在供电时未定义。在LSI内部电路的状态是不确定的和状态
   在供电时，寄存器设置和引脚未定义。在复位信号施加到外部复位的成品中
   引脚，引脚的状态不保证从电源供应到复位过程完成。以类似的方式，引脚的状态
   在一个由片上电源复位功能复位的产品不能保证从供电的时间，直到功率达到
   指定重置的级别。
3. 在断电状态下输入信号
   器件断电时请勿输入信号或iO上拉电源。输入这样的信号或IO产生的电流注入
   上拉电源可能导致故障，此时在设备中通过的异常电流可能导致内部退化
   元素。按照产品文档中所述的关断状态下输入信号指南。
4. 处理未使用的引脚
   按照手册中处理未使用的引脚给出的指示处理未使用的引脚。CMOS产品的输入引脚是
   一般处于高阻抗状态。在操作与未使用的引脚在开路状态下，额外的电磁噪声在附近感应
   在LSI中，一个相关的直通电流在内部流动，由于错误地将引脚状态识别为输入信号而发生故障
   成为可能。
5. 时钟信号
   在施加复位之后，只有在工作时钟信号变得稳定之后才释放复位线。程中切换时钟信号时
   执行，等到目标时钟信号稳定。当用外部谐振器或从外部振荡器产生时钟信号时
   在复位期间，确保复位线只有在时钟信号完全稳定后才被释放。此外，当切换到时钟信号
   用外部谐振器或由外部振荡器在程序执行进行时产生，等到目标时钟信号稳定。
6. 输入引脚电压施加波形
   由于输入噪声或反射波而产生的波形失真可能导致故障。如果CMOS器件的输入停留在VIL之间的区域
   （马克斯。）和VIH（Min。例如，由于噪声，设备可能发生故障。注意防止颤动噪音进入设备时，
   输入电平是固定的，并且还在输入电平通过VIL(Max.）和VIH（Min。).
7. 禁止访问保留地址
   禁止访问保留地址。保留的地址是为将来可能的功能扩展而提供的。不要访问这些
   不能保证地址作为LSI的正确操作。
8. 产品之间的差异
   在从一个产品更改为另一个产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。
   同一组中但具有不同部件号的微处理单元或微控制器单元产品的特性可能在条款上有所不同
   内部存储器容量、布局模式和其他影响电气特性范围的因素，如特性值
   工作裕度、抗噪声能力和辐射噪声量。更改为具有不同部件号的产品时，实施系统-
   定产品的评价试验。

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