

Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 64-KB code flash memory, 8-KB SRAM, 12-bit A/D Converter, Security and Safety features.

Features

- **Arm Cortex-M23 Core**
 - Armv8-M architecture
 - Maximum operating frequency: 48 MHz
 - Arm Memory Protection Unit (Arm MPU) with 8 regions
 - Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
 - CoreSight Debug Port: SW-DP
- **Memory**
 - Up to 64-KB code flash memory
 - 2-KB data flash memory (100,000 program/erase (P/E) cycles)
 - 8-KB SRAM
 - Memory protection units
 - 128-bit unique ID
- **Connectivity**
 - Serial Communications Interface (SCI) × 1
 - Asynchronous interfaces
 - 8-bit clock synchronous interface
 - Simple IIC
 - Simple SPI
 - Smart card interface
 - Serial Peripheral Interface (SPI) × 1
 - I3C bus interface (I3C) × 1
- **Analog**
 - 12-bit A/D Converter (ADC12)
 - Temperature Sensor (TSN)
- **Timers**
 - General PWM Timer 16-bit (GPT16) × 6
 - Low Power Asynchronous General Purpose Timer (AGTW) × 2
 - Watchdog Timer (WDT)
- **Safety**
 - SRAM parity error check
 - Flash area protection
 - ADC self-diagnosis function
 - Clock Frequency Accuracy Measurement Circuit (CAC)
 - Cyclic Redundancy Check (CRC) calculator
 - Data Operation Circuit (DOC)
 - Port Output Enable for GPT (POEG)
 - Independent Watchdog Timer (IWDT)
 - GPIO readback level detection
 - Register write protection
 - Illegal memory access detection
- **Security and Encryption**
 - AES128/256
 - True Random Number Generator (TRNG)
- **System and Power Management**
 - Low power modes
 - Event Link Controller (ELC)
 - Data Transfer Controller (DTC)
 - Key Interrupt Function (KINT)
 - Power-on reset
 - Low Voltage Detection (LVD) with voltage settings
- **Multiple Clock Sources**
 - High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
 - Middle-speed on-chip oscillator (MOCO) (8 MHz)
 - Low-speed on-chip oscillator (LOCO) (32.768 kHz)
 - Clock trim function for HOCO/MOCO/LOCO
 - IWDT-dedicated on-chip oscillator (15 kHz)
 - Clock out support
- **Up to 20 pins for general I/O ports**
 - 5-V tolerance, open drain, input pull-up
- **Operating Voltage**
 - VCC: 1.6 to 5.5 V
- **Operating Temperature and Packages**
 - Ta = -40°C to +85°C
 - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)
 - Ta = -40°C to +105°C
 - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)
 - Ta = -40°C to +125°C
 - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 20-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
 - 16-pin WLCSP (1.84 mm × 1.87 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm[®]-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex[®]-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 64-KB code flash memory
- 8-KB SRAM
- 12-bit A/D Converter (ADC12)
- Security features

1.1 Function Outline

Table 1.1 Arm core

| Feature | Functional description |
|---------------------|---|
| Arm Cortex-M23 core | <ul style="list-style-type: none"> • Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: <ul style="list-style-type: none"> – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): <ul style="list-style-type: none"> – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: <ul style="list-style-type: none"> – Driven by SYSTICCLK (LOCO) or ICLK |

Table 1.2 Memory

| Feature | Functional description |
|-----------------------|--|
| Code flash memory | Maximum 64-KB of code flash memory. |
| Data flash memory | 2-KB of data flash memory. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. |
| SRAM | On-chip high-speed SRAM with parity bit. |

Table 1.3 System (1 of 2)

| Feature | Functional description |
|-----------------------------|--|
| Operating modes | Two operating modes: <ul style="list-style-type: none"> • Single-chip mode • SCI boot mode |
| Resets | The MCU provides 12 resets (RES pin reset, power-on reset, independent watchdog timer reset, watchdog timer reset, voltage monitor 0/1/2 resets, SRAM parity error reset, bus master/slave MPU error resets, CPU stack pointer error reset, software reset). |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. |
| Clocks | <ul style="list-style-type: none"> • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support |

Table 1.3 System (2 of 2)

| Feature | Functional description |
|--|--|
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. |
| Key Interrupt Function (KINT) | The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins. |
| Low power modes | Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. |
| Register write protection | The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). |
| Memory Protection Unit (MPU) | The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided. |
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. |

Table 1.4 Event link

| Feature | Functional description |
|-----------------------------|--|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. |

Table 1.5 Direct memory access

| Feature | Functional description |
|--------------------------------|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. |

Table 1.6 Timers

| Feature | Functional description |
|---|--|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. |
| Port Output Enable for GPT (POEG) | The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state |
| Low power Asynchronous General Purpose Timer (AGTW) | The low power Asynchronous General Purpose Timer (AGTW) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. |

Table 1.7 Communication interfaces

| Feature | Functional description |
|---------------------------------------|--|
| Serial Communications Interface (SCI) | <p>The Serial Communications Interface (SCI) × 1 channel has asynchronous and synchronous serial interface:</p> <ul style="list-style-type: none"> • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface <p>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. The data transfer speed can be configured independently using an on-chip baud rate generator.</p> |
| I3C bus interface (I3C) | The I3C bus interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C. |
| Serial Peripheral Interface (SPI) | The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. |

Table 1.8 Analog

| Feature | Functional description |
|------------------------------|--|
| 12-bit A/D Converter (ADC12) | A 12-bit successive approximation A/D converter is provided. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. |
| Temperature Sensor (TSN) | The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application. |

Table 1.9 Data processing

| Feature | Functional description |
|--|--|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. |

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

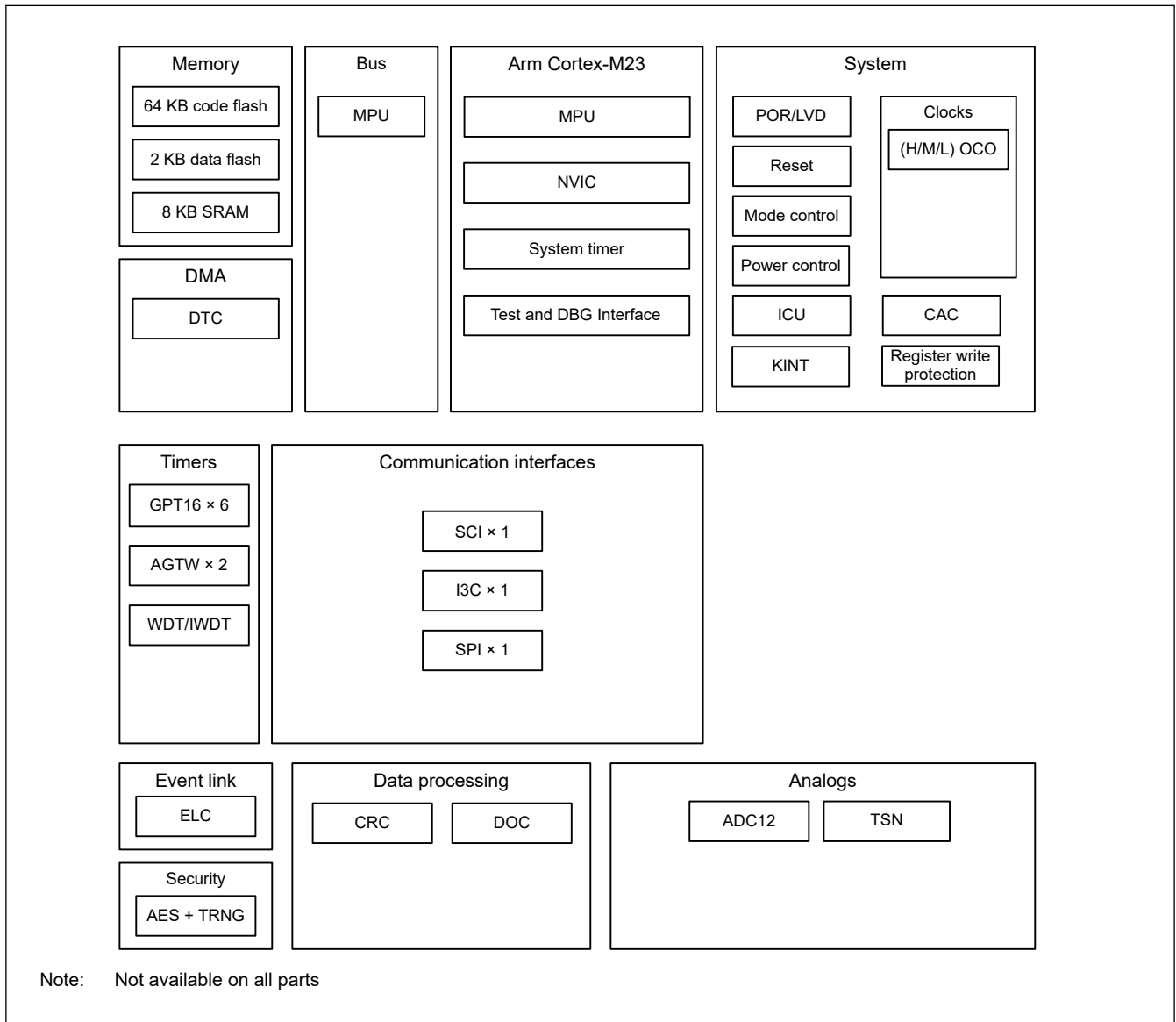


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.10 shows a list of products.

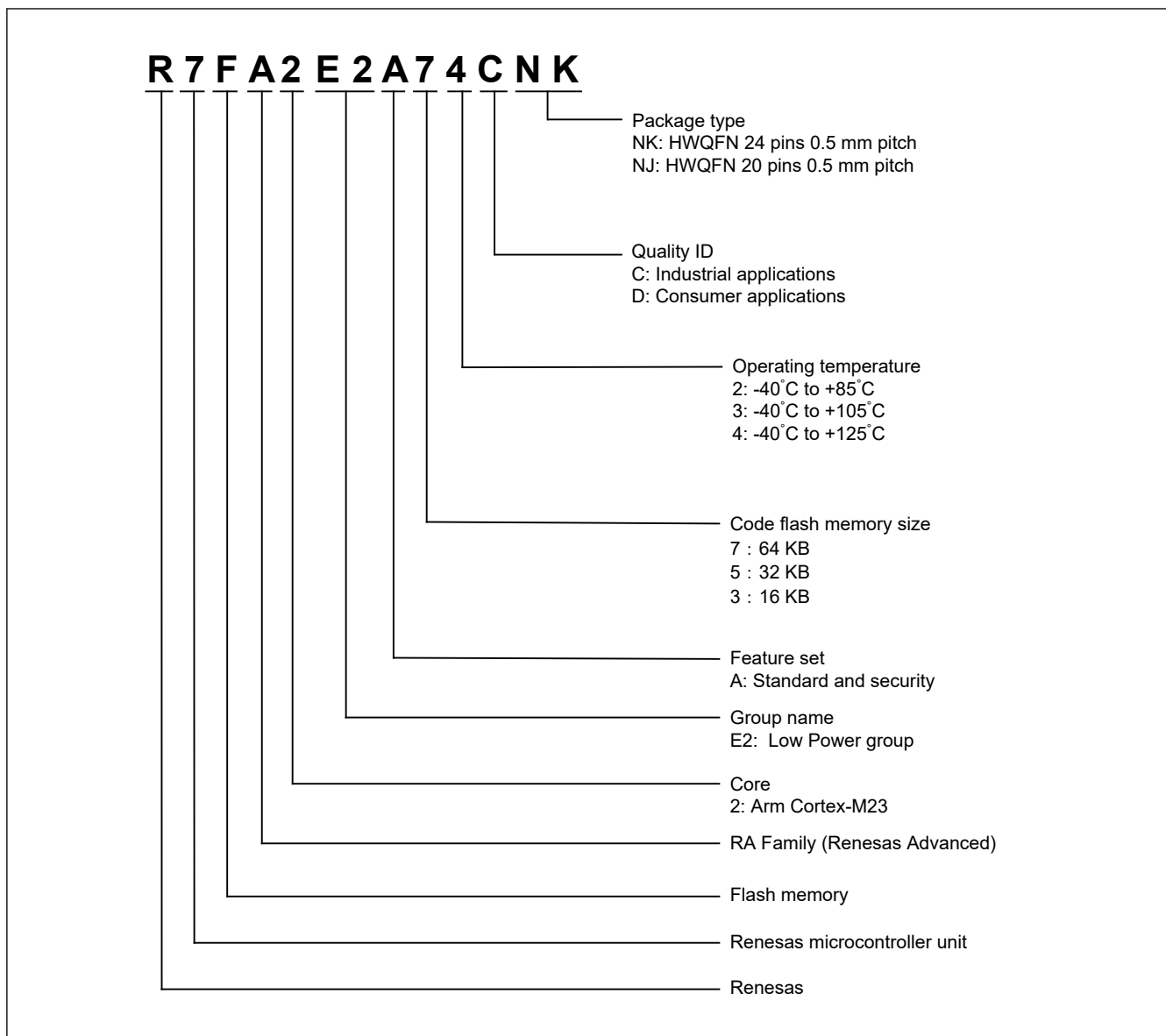


Figure 1.2 Part numbering scheme

Table 1.10 Product list (1 of 2)

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---------------------|--------------|------------|------------|------|-----------------------|
| R7FA2E2A74CNK | PWQN0024KG-A | 64 | 2 | 8 | -40 to +125°C |
| R7FA2E2A74CNJ | PWQN0020KC-A | | | | |
| R7FA2E2A73CNK | PWQN0024KG-A | 64 | 2 | 8 | -40 to +105°C |
| R7FA2E2A73CNJ | PWQN0020KC-A | | | | |
| R7FA2E2A72DNK | PWQN0024KG-A | 64 | 2 | 8 | -40 to +85°C |
| R7FA2E2A72DNJ | PWQN0020KC-A | | | | |

Table 1.10 Product list (2 of 2)

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---------------------|--------------|------------|------------|------|-----------------------|
| R7FA2E2A54CNK | PWQN0024KG-A | 32 | 2 | 8 | -40 to +125°C |
| R7FA2E2A54CNJ | PWQN0020KC-A | | | | -40 to +105°C |
| R7FA2E2A53CNK | PWQN0024KG-A | | | | -40 to +85°C |
| R7FA2E2A53CNJ | PWQN0020KC-A | | | | |
| R7FA2E2A52DNK | PWQN0024KG-A | | | | |
| R7FA2E2A52DNJ | PWQN0020KC-A | | | | |
| R7FA2E2A34CNK | PWQN0024KG-A | 16 | 2 | 8 | -40 to +125°C |
| R7FA2E2A34CNJ | PWQN0020KC-A | | | | -40 to +105°C |
| R7FA2E2A33CNK | PWQN0024KG-A | | | | -40 to +85°C |
| R7FA2E2A33CNJ | PWQN0020KC-A | | | | |
| R7FA2E2A32DNK | PWQN0024KG-A | | | | |
| R7FA2E2A32DNJ | PWQN0020KC-A | | | | |

1.4 Function Comparison

Table 1.11 Function Comparison

| Parts number | | R7FA2E2A74CNK R7FA2E2A73CNK R7FA2E2A72DNK | R7FA2E2A54CNK R7FA2E2A53CNK R7FA2E2A52DNK | R7FA2E2A34CNK R7FA2E2A33CNK R7FA2E2A32DNK | R7FA2E2A74CNJ R7FA2E2A73CNJ R7FA2E2A72DNJ | R7FA2E2A54CNJ R7FA2E2A53CNJ R7FA2E2A52DNJ | R7FA2E2A34CNJ R7FA2E2A33CNJ R7FA2E2A32DNJ |
|-------------------|-----------|---|---|---|---|---|---|
| Pin count | | 24 | | | 20 | | |
| Package | | HWQFN | | | HWQFN | | |
| Code flash memory | | 64 KB | 32 KB | 16 KB | 64 KB | 32 KB | 16 KB |
| Data flash memory | | 2 KB | | | 2 KB | | |
| SRAM(Parity) | | 8 KB | | | 8 KB | | |
| System | CPU clock | 48 MHz | | | 48 MHz | | |
| | ICU | Yes | | | Yes | | |
| | KINT | 4 | | | 4 | | |
| Event control | ELC | Yes | | | Yes | | |
| DMA | DTC | Yes | | | Yes | | |
| Timers | GPT16 | 6 (PWM outputs: 12) | | | 6 (PWM outputs: 11) | | |
| | AGTW | 2 | | | 2 | | |
| | WDT/IWDT | Yes | | | Yes | | |
| Communication | SCI | 1 | | | 1 | | |
| | I3C | 1 | | | 1 | | |
| | SPI | 1 | | | 1 | | |
| Analog | ADC12 | 8 | | | 7 | | |
| | TSN | Yes | | | Yes | | |
| Data processing | CRC | Yes | | | Yes | | |
| | DOC | Yes | | | Yes | | |
| Security | | AES & TRNG | | | AES & TRNG | | |

1.5 Pin Functions

Table 1.12 Pin functions (1 of 2)

| Function | Signal | I/O | Description |
|------------------------|--|--------|--|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- μ F capacitor. Place the capacitor close to the pin. |
| | VCL | I/O | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| Clock | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| On-chip debug | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ7 | Input | Maskable interrupt request pins |
| GPT | GTETRGA, GTETRGB | Input | External trigger input pins |
| | GTIOcNA (n = 4 to 9), GTIOcNB (n = 4 to 9) | I/O | Input capture, output compare, or PWM output pins |
| | GTOUUP | Output | 3-phase PWM output for BLDC motor control (positive U phase) |
| | GTOULO | Output | 3-phase PWM output for BLDC motor control (negative U phase) |
| | GTOVUP | Output | 3-phase PWM output for BLDC motor control (positive V phase) |
| | GTOVLO | Output | 3-phase PWM output for BLDC motor control (negative V phase) |
| | GTOUWP | Output | 3-phase PWM output for BLDC motor control (positive W phase) |
| | GTOWLO | Output | 3-phase PWM output for BLDC motor control (negative W phase) |
| AGTW | AGTEE0, AGTEE1 | Input | External event input enable signals |
| | AGTIO0, AGTIO1 | I/O | External event input and pulse output pins |
| | AGTO0, AGTO1 | Output | Pulse output pins |
| | AGTOA0, AGTOA1 | Output | Output compare match A output pins |
| | AGTOB0, AGTOB1 | Output | Output compare match B output pins |

Table 1.12 Pin functions (2 of 2)

| Function | Signal | I/O | Description |
|---------------------|--|--------|---|
| SCI | SCKn (n = 9) | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXDn (n = 9) | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXDn (n = 9) | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTS _n _RTS _n (n = 9) | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low. |
| | SCLn (n = 9) | I/O | Input/output pins for the IIC clock (simple IIC mode) |
| | SDAn (n = 9) | I/O | Input/output pins for the IIC data (simple IIC mode) |
| | SCKn (n = 9) | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISO _n (n = 9) | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSI _n (n = 9) | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| | SS _n (n = 9) | Input | Chip-select input pins (simple SPI mode), active-low |
| I3C | SCLn (n = 0) | I/O | Input/output pins for the clock |
| | SDAn (n = 0) | I/O | Input/output pins for data |
| SPI | RSPCKA | I/O | Clock input/output pin |
| | SSLA0 | I/O | Input or output pin for slave selection |
| | MOSIA | I/O | Input or output pins for data output from the master |
| | MISOA | I/O | Input or output pins for data output from the slave |
| Analog power supply | VREFH0 | Input | Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12. |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12. |
| ADC12 | AN005, AN006, AN009, AN010, AN019 to AN022 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADTRG0 | Input | Input pin for the external trigger signals that start the A/D conversion, active-low. |
| KINT | KR00 to KR03 | Input | Key interrupt input pins |
| I/O ports | P010, P011, P014, P015 | I/O | General-purpose input/output pins |
| | P100 to P103, P108 to P112 | I/O | General-purpose input/output pins |
| | P200 | Input | General-purpose input pin |
| | P201, P205 | I/O | General-purpose input/output pins |
| | P300 | I/O | General-purpose input/output pins |
| | P400, P401 | I/O | General-purpose input/output pins |
| | P914 | I/O | General-purpose input/output pins |

1.6 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments from the top view.

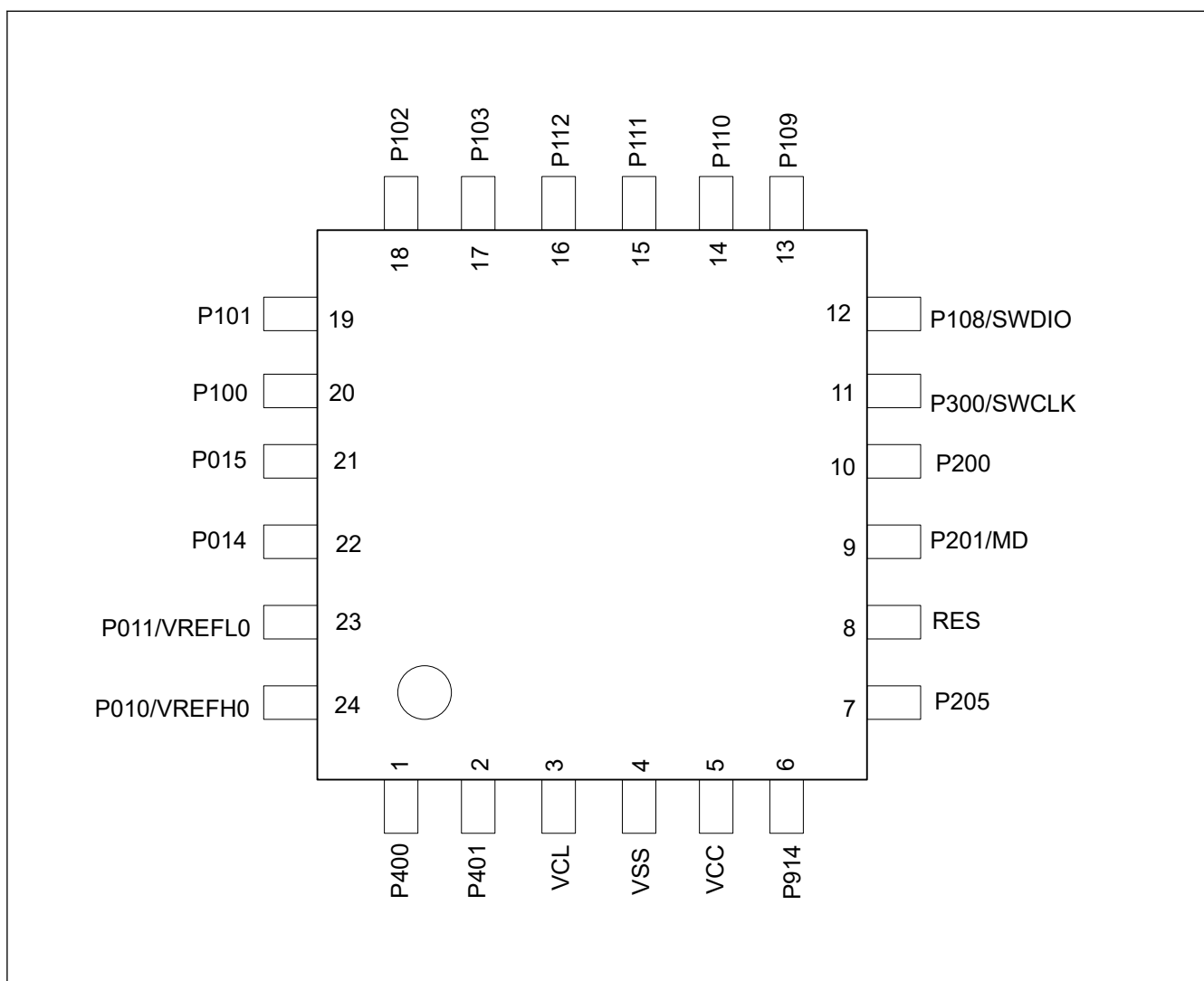


Figure 1.3 Pin assignment for HWQFN 24-pin (top view)

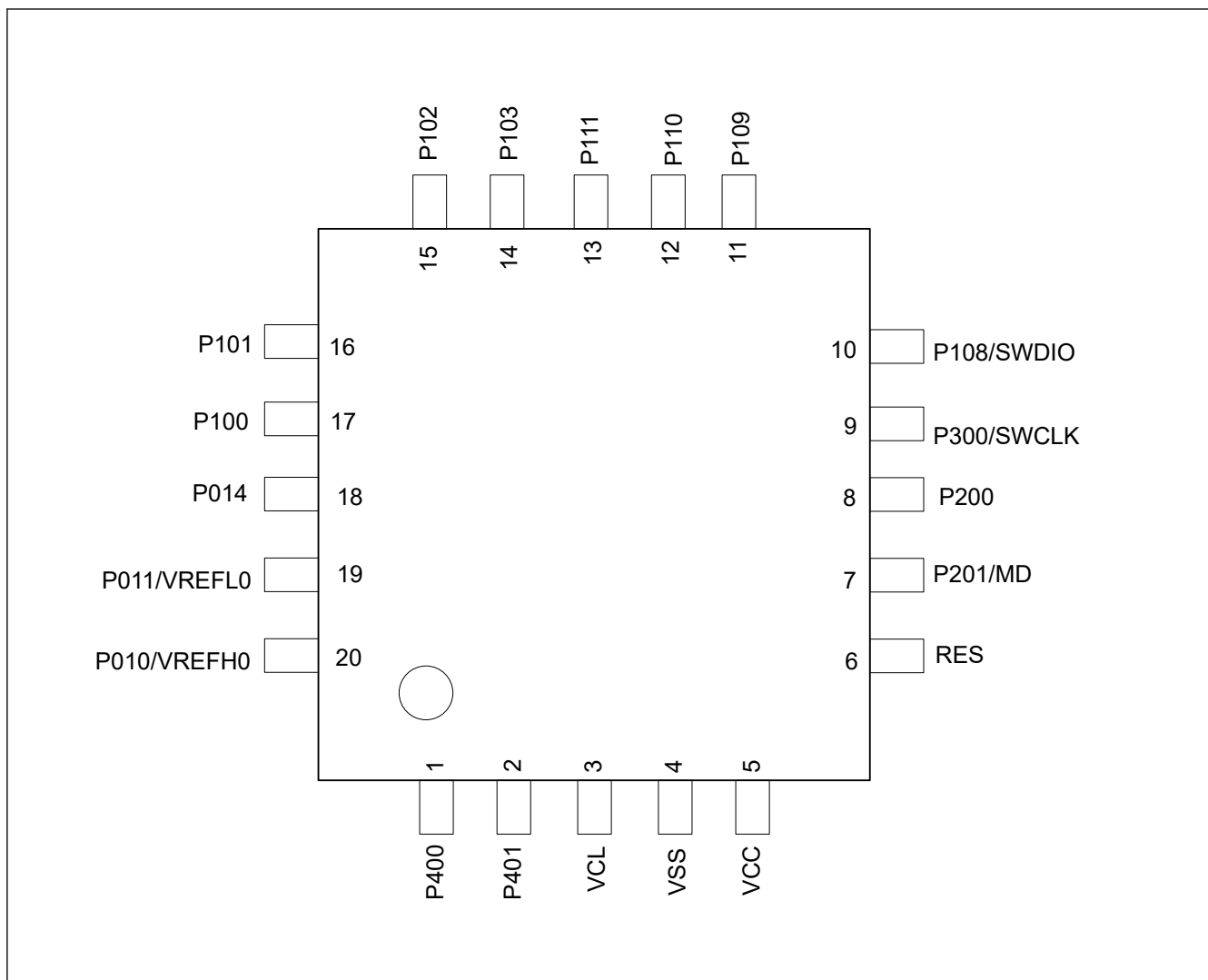


Figure 1.4 Pin assignment for HWQFN 20-pin (top view)

| | | | | | |
|---|----------------|----------------|---------|------|---|
| | A | B | C | D | |
| 4 | P103 | P101 | P100 | P400 | 4 |
| 3 | P110 | P102 | VCL | P401 | 3 |
| 2 | P109 | P200 | VCC | VSS | 2 |
| 1 | P108/ SWDIO | P300/ SWCLK | P201/MD | RES | 1 |
| | A | B | C | D | |

Figure 1.5 Pin assignment for WLCSP 16-pin (top view, pad side down)

1.7 Pin Lists

Table 1.13 Pin list

| Pin number | | | Power, System, Clock, Debug, CAC | I/O ports | Timers | | | Communication interfaces | | | | Analogs | HMI |
|--------------|--------------|--------------|----------------------------------|-----------|----------|---------------|-----------|-------------------------------|-------------------------------|--------|----------|--------------------|--------------------|
| HWQFN 24-pin | HWQFN 20-pin | WLCSP 16-pin | | | AGTW | GPT_OPS, PDEG | GPT | SCI9 | SCI9 | I3C | SPI | ADC | Interrupt |
| 1 | 1 | D4 | CACREF_C | P400 | AGTIO1_C | — | GTIOC9A_A | SCK9_D | TXD9_F/ MOSI9_F/ SDA9_F | SCL0_A | — | — | IRQ0_A/ KRM02_A |
| 2 | 2 | D3 | — | P401 | AGTEE1_A | GTETRG_A_B | GTIOC9B_A | CTS9_RTS9_F/ SS9_F | RxD9_F/ MISO9_F/ SCL9_F | SDA0_A | — | — | IRQ5/KRM03_A |
| 3 | 3 | C3 | — | VCL | — | — | — | — | — | — | — | — | — |
| 4 | 4 | D2 | VSS | — | — | — | — | — | — | — | — | — | — |
| 5 | 5 | C2 | VCC | — | — | — | — | — | — | — | — | — | — |
| 6 | — | — | — | P914 | AGTOA1_A | GTETRGB_F | — | RxD9_J/ MISO9_J/ SCL9_J | SCK9_H | — | — | — | IRQ2_C/ KRM00_A |
| 7 | — | — | CLKOUT_A | P205 | AGTO1 | — | — | TXD9_I/ MOSI9_I/ SDA9_I | CTS9_RTS9_A/ SS9_A | — | — | — | IRQ1/KRM01_A |
| 8 | 6 | D1 | RES# | — | — | — | — | — | — | — | — | — | — |
| 9 | 7 | C1 | MD | P201 | — | — | — | — | — | — | — | — | — |
| 10 | 8 | B2 | — | P200 | — | — | — | — | — | — | — | — | NMI |
| 11 | 9 | B1 | SWCLK | P300 | AGTOB1_A | GTOUUP_C | GTIOC7A_C | RXD9_H/ MISO9_H/ SCL9_H | SCK9_G | — | RSPCKA_C | — | IRQ0_C |
| 12 | 10 | A1 | SWDIO | P108 | AGTOA1_B | GTOULO_C | GTIOC7B_C | TXD9_H/ MOSI9_H/ SDA9_H | CTS9_RTS9_B/ SS9_B | — | MOSIA_C | — | IRQ5_C |
| 13 | 11 | A2 | CLKOUT_B | P109 | AGTO1_A | GTOVUP_A | GTIOC4A_A | SCK9_F | TXD9_B/ MOSI9_B/ SDA9_B | — | MISOA_C | — | IRQ7_C/ KRM01_B |
| 14 | 12 | A3 | — | P110 | AGTOA0_A | GTOVLO_A | GTIOC4B_A | CTS9_RTS9_H/ SS9_H | RXD9_B/ MISO9_B/ SCL9_B | — | SSLA0_C | — | IRQ3_A/ KRM00_B |
| 15 | 13 | — | — | P111 | AGTOA0 | — | GTIOC6A_A | RXD9_G/ MISO9_G/ SCL9_G | SCK9_B | — | — | — | IRQ4_A/ KRM03_B |
| 16 | — | — | — | P112 | AGTOB0 | — | GTIOC6B_A | TXD9_J/ MOSI9_J/ SDA9_J | CTS9_RTS9_I/ SS9_I | — | — | — | IRQ1_C/ KRM02_B |
| 17 | 14 | A4 | — | P103 | AGTOB0_B | GTOVUP_A | GTIOC5A_A | CTS9_RTS9_E/ SS9_E | RxD9_I/ MISO9_I/ SCL9_I | — | SSLA0_A | AN019 | IRQ6_C/KRM03 |
| 18 | 15 | B3 | — | P102 | AGTO0 | GTOVLO_A | GTIOC5B_A | SCK9_C | TXD9_G/ MOSI9_G/ SDA9_G | — | RSPCKA_A | AN020/ ADTRG0_A | IRQ4_C/KRM02 |
| 19 | 16 | B4 | — | P101 | AGTEE0 | GTETRGB_A | GTIOC8A_A | TXD9_E/ MOSI9_E/ SDA9_E | CTS9_RTS9_G/ SS9_G | — | MOSIA_A | AN021 | IRQ1_A/KRM01 |
| 20 | 17 | C4 | — | P100 | AGTIO0_A | GTETRG_A | GTIOC8B_A | RxD9_E/ MISO9_E/ SCL9_E | SCK9_E | — | MISOA_A | AN022 | IRQ2_A/KRM00 |
| 21 | — | — | — | P015 | — | — | — | — | — | — | — | AN010 | IRQ7_A |
| 22 | 18 | — | — | P014 | — | — | — | — | — | — | — | AN009 | — |
| 23 | 19 | — | VREFL0 | P011 | — | — | — | — | — | — | — | AN006 | — |
| 24 | 20 | — | VREFH0 | P010 | — | — | — | — | — | — | — | AN005 | — |

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E, _F, _G, _H, _I, and _J. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics (Applicable for QFN24 and QFN20 only)

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$$VCC^{*1} = 1.6 \text{ to } 5.5 \text{ V}, VREFH0 = 1.6 \text{ V to } VCC$$

$$VSS = VREFL0 = 0 \text{ V}, T_a = T_{opr}$$

Note 1. The typical condition is set to $VCC = 3.3 \text{ V}$.

Figure 2.1 shows the timing conditions.

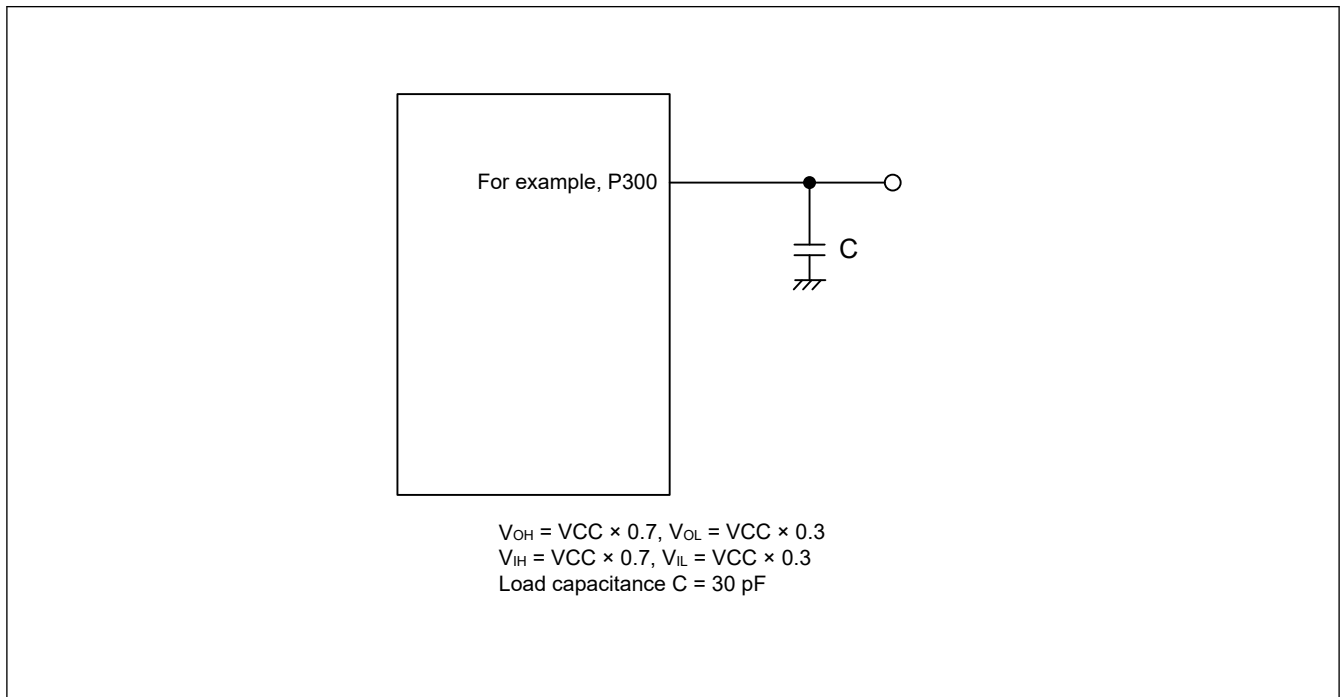


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

| Parameter | Symbol | Value | Unit | |
|---|---------------------------------|--|-------------------|---|
| Power supply voltage | VCC | -0.5 to +6.5 | V | |
| Input voltage | 5V-tolerant ports ^{*1} | V_{in} | -0.3 to +6.5 | V |
| | Others | V_{in} | -0.3 to VCC + 0.3 | V |
| Reference power supply voltage | VREFH0 | -0.3 to +6.5 | V | |
| Analog input voltage | V_{AN} | -0.3 to VCC + 0.3 | V | |
| Operating temperature ^{*2 *3 *4} | T_{opr} | -40 to +85 -40 to +105 -40 to +125 | °C | |
| Storage temperature | T_{stg} | -55 to +140 | °C | |

Note 1. Ports P400 and P401 are 5V-tolerant.

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 2. See [section 2.2.1. Tj/Ta Definition](#).

Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +125°C. Derating is the systematic reduction of load for improved reliability.

Note 4. The upper limit of the operating temperature is 85°C, 105°C or 125°C, depending on the product.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- VCC and VSS: about 0.1 μF
- VREFH0 and VREFL0: about 0.1 μF

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 μF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

| Parameter | Symbol | Min | Typ | Max | Unit | |
|------------------------------|--------|------------------------------|-----|-----|------|---|
| Power supply voltages | VCC | 1.6 | — | 5.5 | V | |
| | VSS | — | 0 | — | V | |
| Analog power supply voltages | VREFH0 | When used as ADC12 Reference | 1.6 | — | VCC | V |
| | VREFL0 | | — | 0 | — | V |

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +125°C

| Parameter | Symbol | Typ | Max*1 | Unit | Test conditions |
|----------------------------------|--------|-----|-------|------|-------------------------------------|
| Permissible junction temperature | Tj | — | 140 | °C | High-speed mode |
| | | | 125 | | Middle-speed mode |
| | | | 105 | | Low-speed mode Subosc-speed mode |

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

Note 1. The upper limit of operating temperature is 85°C, 105°C or 125°C depending on the product. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C, If the part number shows the operation temperature at 105°C, then the maximum value of Tj is 125°C, otherwise it is 140°C.

2.2.2 I/O V_{IH} , V_{IL} **Table 2.4** I/O V_{IH} , V_{IL}

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|--|----------|------------------|-----|------------------|------|--------------------|
| Schmitt trigger input voltage | I3C (except for SMBus)* ¹ | V_{IH} | $VCC \times 0.7$ | — | 5.8 | V | — |
| | | V_{IL} | — | — | $VCC \times 0.3$ | | |
| | RES, NMI Other peripheral input pins excluding I3C | V_{IH} | $VCC \times 0.8$ | — | — | | |
| | | V_{IL} | — | — | $VCC \times 0.2$ | | |
| Input voltage (except for Schmitt trigger input pin) | I3C (SMBus)* ² | V_{IH} | 2.2 | — | — | V | VCC = 3.6 to 5.5 V |
| | | V_{IH} | 2.0 | — | — | | VCC = 2.7 to 3.6 V |
| | | V_{IL} | — | — | 0.8 | | VCC = 3.6 to 5.5 V |
| | | V_{IL} | — | — | 0.5 | | VCC = 2.7 to 3.6 V |
| | 5V-tolerant ports* ³ | V_{IH} | $VCC \times 0.8$ | — | 5.8 | | — |
| | | V_{IL} | — | — | $VCC \times 0.2$ | | |
| | Input ports pins | V_{IH} | $VCC \times 0.8$ | — | — | | |
| | | V_{IL} | — | — | $VCC \times 0.2$ | | |

Note 1. SCL0_A, SDA0_A (total 2 pins)

Note 2. SCL0_A, SDA0_A (total 2 pins)

Note 3. P400, P401 (total 2 pins)

2.2.3 I/O I_{OH} , I_{OL} **Table 2.5** I/O I_{OH} , I_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------------------------|----------|-----|-----|------|------|-----------------|
| Permissible output current (max value per pin) | Ports P010, P011, P014, P015 | I_{OH} | — | — | -4.0 | mA | |
| | | I_{OL} | — | — | 8.0 | mA | |
| | Ports P400, P401 | I_{OH} | — | — | -8.0 | mA | |
| | | I_{OL} | — | — | 15.0 | mA | |
| | Other output pins* ¹ | I_{OH} | — | — | -4.0 | mA | |
| | | I_{OL} | — | — | 20.0 | mA | |

Table 2.5 I/O I_{OH} , I_{OL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|------------------------------------|----------------------|-----|-----|--------------------|------|--------------------|
| Permissible output current (max value total pins) ^{*1} | Total of ports P400, P401 | $\Sigma I_{OH(max)}$ | — | — | -16 | mA | VCC = 2.7 to 5.5 V |
| | | | — | — | -2 | | VCC = 1.8 to 2.7 V |
| | | | — | — | -1 | | VCC = 1.6 to 1.8 V |
| | | $\Sigma I_{OL(max)}$ | — | — | 30 | | VCC = 2.7 to 5.5 V |
| | | | — | — | 1.2 | | VCC = 1.8 to 2.7 V |
| | | | — | — | 0.6 | | VCC = 1.6 to 1.8 V |
| | Total of ports P010,P011,P014,P015 | $\Sigma I_{OH(max)}$ | — | — | -16 | mA | VCC = 2.7 to 5.5 V |
| | | | — | — | -4 | | VCC = 1.8 to 2.7 V |
| | | | — | — | -2 | | VCC = 1.6 to 1.8 V |
| | | $\Sigma I_{OL(max)}$ | — | — | 32 | | VCC = 2.7 to 5.5 V |
| | | | — | — | 2.4 | | VCC = 1.8 to 2.7 V |
| | | | — | — | 1.2 | | VCC = 1.6 to 1.8 V |
| | Total of other output ports | $\Sigma I_{OH(max)}$ | — | — | -30 | mA | VCC = 2.7 to 5.5 V |
| | | | — | — | -12 | | VCC = 1.8 to 2.7 V |
| | | | — | — | -6 | | VCC = 1.6 to 1.8 V |
| $\Sigma I_{OL(max)}$ | | — | — | 50 | VCC = 2.7 to 5.5 V | | |
| | | — | — | 9 | VCC = 1.8 to 2.7 V | | |
| | | — | — | 4.5 | VCC = 1.6 to 1.8 V | | |
| Total of all output pin | $\Sigma I_{OH(max)}$ | — | — | -30 | mA | — | |
| | $\Sigma I_{OL(max)}$ | — | — | 80 | | — | |

Note 1. Specification under conditions where the duty factor $\leq 70\%$.The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$ <Example> Where n = 80% and $I_{OH} = -30.0$ mATotal output current of pins = $(-30.0 \times 0.7)/(80 \times 0.01) \cong -26.2$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in [Table 2.5](#).

2.2.4 I/O V_{OH} , V_{OL} , and Other Characteristics

Table 2.6 I/O V_{OH} , V_{OL} (1)

Conditions: VCC = 4.0 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--|----------|------------|-----|--------------------|------|--------------------|
| Output voltage | Ports P400, P401 | V_{OH} | VCC - 0.27 | — | — | V | $I_{OH} = -3.0$ mA |
| | | V_{OH} | VCC - 0.8 | — | — | | $I_{OH} = -8.0$ mA |
| | Output pins except for P400 and P401 ^{*1} | V_{OH} | VCC - 0.8 | — | — | | $I_{OH} = -4.0$ mA |
| | Ports P400, P401 | V_{OL} | — | — | 0.27 | | $I_{OL} = 3.0$ mA |
| | | V_{OL} | — | — | 0.4 | | $I_{OL} = 9.0$ mA |
| | | V_{OL} | — | — | 0.8 | | $I_{OL} = 15.0$ mA |
| | P010, P011, P014, P015 | V_{OL} | — | — | 0.8 | | $I_{OL} = 8.0$ mA |
| Output pins except for P010, P011, P014, P015, P400 and P401 ^{*1} | V_{OL} | — | — | 1.2 | $I_{OL} = 20.0$ mA | | |

Note 1. Except for Port P200 which is input port.

Table 2.7 I/O V_{OH} , V_{OL} (2)

Conditions: $V_{CC} = 2.7$ to 4.0 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--|--|----------|-----------------|-----|-------------------|-----------------|--------------------|
| Output voltage | Ports P400, P401 | V_{OH} | $V_{CC} - 0.27$ | — | — | V | $I_{OH} = -3.0$ mA |
| | | V_{OH} | $V_{CC} - 0.8$ | — | — | | $I_{OH} = -8.0$ mA |
| | Output pins except for P400 and P401*1 | V_{OH} | $V_{CC} - 0.8$ | — | — | | $I_{OH} = -4.0$ mA |
| | Ports P400, P401 | V_{OL} | — | — | 0.27 | | $I_{OL} = 3.0$ mA |
| | | | | | 0.4 | | $I_{OL} = 9.0$ mA |
| | | | | | 0.8 | | $I_{OL} = 15$ mA |
| Output pins except for P400 and P401*1 | V_{OL} | — | — | 0.8 | $I_{OL} = 8.0$ mA | | |

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH} , V_{OL} (3)

Conditions: $V_{CC} = 1.6$ to 2.7 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|----------------|---------------|----------|----------------|-----|------|-----------------|---|
| Output voltage | Output pins*1 | V_{OH} | $V_{CC} - 0.5$ | — | — | V | $I_{OH} = -1.0$ mA $V_{CC} = 1.8$ to 2.7 V |
| | | V_{OH} | $V_{CC} - 0.5$ | — | — | | $I_{OH} = -0.5$ mA $V_{CC} = 1.6$ to 1.8 V |
| | Output pins*1 | V_{OL} | — | — | 0.4 | | $I_{OL} = 0.6$ mA $V_{CC} = 1.8$ to 2.7 V |
| | | | | | 0.4 | | $I_{OL} = 0.3$ mA $V_{CC} = 1.6$ to 1.8 V |

Note 1. Except for Ports P200 which is input port.

Table 2.9 I/O other characteristics

Conditions: $V_{CC} = 1.6$ to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|-------------|-----|-----|------|-----------------|---|
| Input leakage current | RES, port P200 | $ I_{in} $ | — | — | 1.0 | μ A | $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| Three-state leakage current (off state) | 5V-tolerant ports*1 | $ I_{TSI} $ | — | — | 10 | μ A | $V_{in} = 0$ V $V_{in} = 5.8$ V |
| | Other ports (except for P200 and 5V-tolerant ports) | | — | — | 1.0 | | $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| Input pull-up resistor | All ports (except for P200) | R_U | 10 | 20 | 100 | k Ω | $V_{in} = 0$ V |
| Input capacitance | P200 | C_{in} | — | — | 30 | pF | $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ$ C |
| | Other input pins | | — | — | 15 | | |

Note 1. P400 and P401 (total 2 pins)

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | | Symbol | Typ ^{*10} | Max | Unit | Test Conditions | |
|------------------------------|---|-------------|--|---------------|--------------------|------|------|-----------------|--------|
| Supply current ^{*1} | High-speed mode ^{*2} | Normal mode | All peripheral clocks disabled, CoreMark code executing from flash ^{*5} | ICLK = 48 MHz | I _{CC} | 3.90 | — | mA | *7 *11 |
| | | | | ICLK = 32 MHz | | 2.85 | — | | *7 |
| | | | | ICLK = 16 MHz | | 1.75 | — | | |
| | | | | ICLK = 8 MHz | | 1.20 | — | | |
| | | | All peripheral clocks enabled, code executing from flash ^{*5} | ICLK = 48 MHz | | — | 10.5 | | *9 *11 |
| | | Sleep mode | All peripheral clocks disabled ^{*5} | ICLK = 48 MHz | 1.00 | — | *7 | | |
| | | | | ICLK = 32 MHz | 0.85 | — | *7 | | |
| | | | | ICLK = 16 MHz | 0.65 | — | | | |
| | | | | ICLK = 8 MHz | 0.60 | — | | | |
| | | | All peripheral clocks enabled ^{*5} | ICLK = 48 MHz | 3.90 | — | *9 | | |
| | | | ICLK = 32 MHz | 3.50 | — | *8 | | | |
| | | | ICLK = 16 MHz | 2.00 | — | | | | |
| | | | ICLK = 8 MHz | 1.20 | — | | | | |
| | Increase during BGO operation ^{*6} | | | | | 2.05 | — | | — |

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | | | Symbol | Typ ^{*10} | Max | Unit | Test Conditions | | | | |
|---|--|--|--|---|--|--|-----------------|------|-----------------|------|-----|----|----|
| Supply current ^{*1} | Middle-speed mode ^{*2} | Normal mode | All peripheral clocks disabled, CoreMark code executing from flash ^{*5} | ICLK = 24 MHz | I _{CC} | 2.15 | — | mA | *7 | | | | |
| | | | | ICLK = 4 MHz | | 0.80 | — | | | | | | |
| | | | All peripheral clocks enabled, code executing from flash ^{*5} | ICLK = 24 MHz | | — | 7.0 | | | *8 | | | |
| | | Sleep mode | All peripheral clocks disabled ^{*5} | ICLK = 24 MHz | | 0.70 | — | | *7 | | | | |
| | | | | ICLK = 4 MHz | | 0.55 | — | | | | | | |
| | | | All peripheral clocks enabled ^{*5} | ICLK = 24 MHz | | 2.70 | — | | *8 | | | | |
| | | | | ICLK = 4 MHz | | 0.85 | — | | | | | | |
| | | | Increase during BGO operation ^{*6} | | | | | | 1.85 | — | | — | |
| | | | Low-speed mode ^{*3} | Normal mode | | All peripheral clocks disabled, CoreMark code executing from flash ^{*5} | ICLK = 2 MHz | | I _{CC} | 0.30 | — | mA | *7 |
| | ICLK = 2 MHz | — | | | 2.0 | | *8 | | | | | | |
| | All peripheral clocks enabled, code executing from flash ^{*5} | ICLK = 2 MHz | | | 0.11 | — | *7 | | | | | | |
| | Sleep mode | All peripheral clocks disabled ^{*5} | | ICLK = 2 MHz | 0.30 | — | *8 | | | | | | |
| | | | | All peripheral clocks enabled ^{*5} | ICLK = 2 MHz | — | 150 | *8 | | | | | |
| | | Subosc-speed mode ^{*4} | | Normal mode | All peripheral clocks enabled, code executing from flash ^{*5} | ICLK = 32.768 kHz | I _{CC} | | | — | 150 | | μA |
| | Sleep mode | | All peripheral clocks disabled ^{*5} | | | ICLK = 32.768 kHz | | | 1.00 | — | | | |
| All peripheral clocks enabled ^{*5} | | | | ICLK = 32.768 kHz | 3.65 | — | | *8 | | | | | |

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.

Note 2. The clock source is HOCO.

Note 3. The clock source is MOCO.

Note 4. The clock source is LOCO.

Note 5. This does not include BGO operation.

Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Note 7. PCLKB and PCLKD are set to divided by 64.

Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.

Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.

Note 10. VCC = 3.3 V.

Note 11. The prefetch buffer is operating.

Table 2.11 Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | | Symbol | Typ*3 | Max | Unit | Test conditions | |
|------------------|-------------------------|-------------------------|---|------------------------|-----------------|------|------|-----------------|---|
| Supply current*1 | Software Standby mode*2 | Peripheral modules stop | All SRAMs (0x2000_4000 to 0x2000_5FFF) are on | T _a = 25°C | I _{CC} | 0.2 | 1.3 | μA | — |
| | | | | T _a = 55°C | | 0.4 | 3.7 | | |
| | | | | T _a = 85°C | | 1.35 | 12 | | |
| | | | | T _a = 105°C | | 3.05 | 42 | | |
| | | | | T _a = 125°C | | 6.00 | 85 | | |
| | | | Only 4 KB SRAM (0x2000_4000 to 0x2000_4FFF) is on | T _a = 25°C | | 0.2 | 1.3 | | |
| | | | | T _a = 55°C | | 0.4 | 3.7 | | |
| | | | | T _a = 85°C | | 1.30 | 12 | | |
| | | | | T _a = 105°C | | 2.85 | 42 | | |
| | | | | T _a = 125°C | | 5.85 | 85 | | |

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.

Note 2. The IWDT and LVD are not operating.

Note 3. VCC = 3.3 V.

Table 2.12 Operating and standby current (3)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--|--------------------|-----|-----|------|------|------------------------|
| Analog power supply current | During 12-bit A/D conversion (at high-speed A/D conversion mode) | I _{VCCAD} | — | — | 1.44 | mA | — |
| | During 12-bit A/D conversion (at low-power A/D conversion mode) | | — | — | 0.78 | mA | — |
| | Waiting for 12-bit A/D conversion (all units)*1 | | — | — | 1.0 | μA | — |
| Reference power supply current | During 12-bit A/D conversion | I _{REFH0} | — | — | 120 | μA | — |
| | Waiting for 12-bit A/D conversion | | — | — | 60 | μA | T _a = 105°C |
| | | | — | — | 120 | μA | T _a = 125°C |
| Temperature Sensor (TSN) operating current | | I _{TNS} | — | 95 | — | μA | — |

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = 0 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------|---|--------|------|-----|-----|------|-----------------|
| Power-on VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.02 | — | 2 | ms/V | — |
| | Voltage monitor 0 reset enabled at startup*1 *2 | | | | — | | |
| | SCI boot mode*2 | | | | 2 | | |

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When the VCC change exceeds $VCC \pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--------------|-----|-----|-----|------|---|
| Allowable ripple frequency | $f_{r(VCC)}$ | — | — | 10 | kHz | Figure 2.2 $V_r(VCC) \leq VCC \times 0.2$ |
| | | — | — | 1 | MHz | Figure 2.2 $V_r(VCC) \leq VCC \times 0.08$ |
| | | — | — | 10 | MHz | Figure 2.2 $V_r(VCC) \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$ | 1.0 | — | — | ms/V | When VCC change exceeds $VCC \pm 10\%$ |

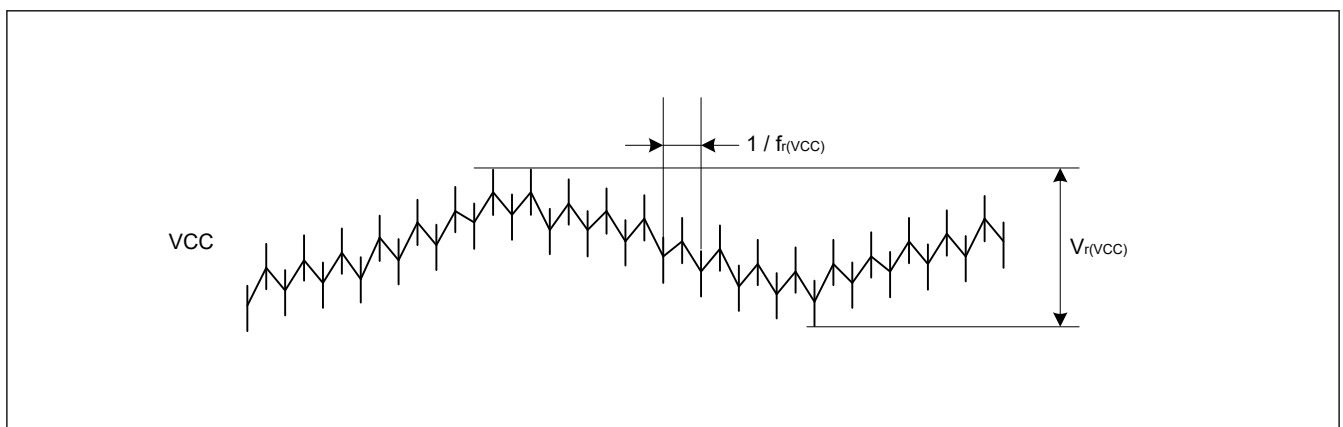


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.15 Operation frequency in high-speed operating mode

Conditions: VCC = 1.8 to 5.5 V

| Parameter | Symbol | Min | Typ | Max ^{*4} | Unit |
|---------------------|---|--------------|-----|-------------------|------|
| Operation frequency | System clock (ICLK) ^{*1*2} | 1.8 to 5.5 V | f | 0.032768 | MHz |
| | Peripheral module clock (PCLKB) | 1.8 to 5.5 V | — | — | |
| | Peripheral module clock (PCLKD) ^{*3} | 1.8 to 5.5 V | — | — | |

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of ICLK must be $\pm 1.0\%$ during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.

Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.19](#).

Table 2.16 Operation frequency in middle-speed mode

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max ^{*4} | Unit |
|---------------------|---|--------------|--------|----------|-----|-------------------|------|
| Operation frequency | System clock (ICLK) ^{*1*2} | 1.8 to 5.5 V | f | 0.032768 | — | 24 | MHz |
| | | 1.6 to 1.8 V | | 0.032768 | — | 4 | |
| | Peripheral module clock (PCLKB) | 1.8 to 5.5 V | | — | — | 24 | |
| | | 1.6 to 1.8 V | | — | — | 4 | |
| | Peripheral module clock (PCLKD) ^{*3} | 1.8 to 5.5 V | | — | — | 24 | |
| | | 1.6 to 1.8 V | | — | — | 4 | |

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of ICLK must be $\pm 1.0\%$ while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.

Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.19](#).

Table 2.17 Operation frequency in low-speed mode

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max ^{*4} | Unit |
|---------------------|---|--------------|--------|----------|-----|-------------------|------|
| Operation frequency | System clock (ICLK) ^{*1*2} | 1.6 to 5.5 V | f | 0.032768 | — | 2 | MHz |
| | Peripheral module clock (PCLKB) | 1.6 to 5.5 V | | — | — | 2 | |
| | Peripheral module clock (PCLKD) ^{*3} | 1.6 to 5.5 V | | — | — | 2 | |

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.

Note 2. The frequency accuracy of ICLK must be $\pm 1.0\%$ while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.

Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see [Table 2.19](#).

Table 2.18 Operation frequency in Subosc-speed mode

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---------------------|---|--------------|--------|---------|--------|---------|------|
| Operation frequency | System clock (ICLK) ^{*1} | 1.6 to 5.5 V | f | 27.8528 | 32.768 | 37.6832 | kHz |
| | Peripheral module clock (PCLKB) | 1.6 to 5.5 V | | — | — | 37.6832 | |
| | Peripheral module clock (PCLKD) ^{*2} | 1.6 to 5.5 V | | — | — | 37.6832 | |

Note 1. Programming and erasing the flash memory is not possible.

Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.19 Clock timing (1 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--------------------|---------|--------|---------|------|----------------------------|
| LOCO clock oscillation frequency | f _{LOCO} | 27.8528 | 32.768 | 37.6832 | kHz | — |
| LOCO clock oscillation stabilization time | t _{LOCO} | — | — | 100 | μs | Figure 2.3 |
| IWDT-dedicated clock oscillation frequency | f _{ILOCO} | 12.75 | 15 | 17.25 | kHz | — |
| MOCO clock oscillation frequency | f _{MOCO} | 6.8 | 8 | 9.2 | MHz | — |
| MOCO clock oscillation stabilization time | t _{MOCO} | — | — | 1 | μs | — |

Table 2.19 Clock timing (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--|-------|-----|-------|------|--------------------------------------|
| HOCO clock oscillation frequency*3 | f _{HOCO24} | 23.76 | 24 | 24.24 | MHz | Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 |
| | f _{HOCO32} | 31.68 | 32 | 32.32 | | Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 |
| | f _{HOCO48} | 47.52 | 48 | 48.48 | | Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 |
| | f _{HOCO64} | 63.36 | 64 | 64.64 | | Ta = -40 to 125°C 1.6 ≤ VCC ≤ 5.5 |
| HOCO clock oscillation stabilization time*1 *2 | t _{HOCO24} t _{HOCO32} t _{HOCO48} t _{HOCO64} | — | 6.7 | 7.7 | μs | Figure 2.4 |

Note 1. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.

Note 2. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

Note 3. Accuracy at production test.

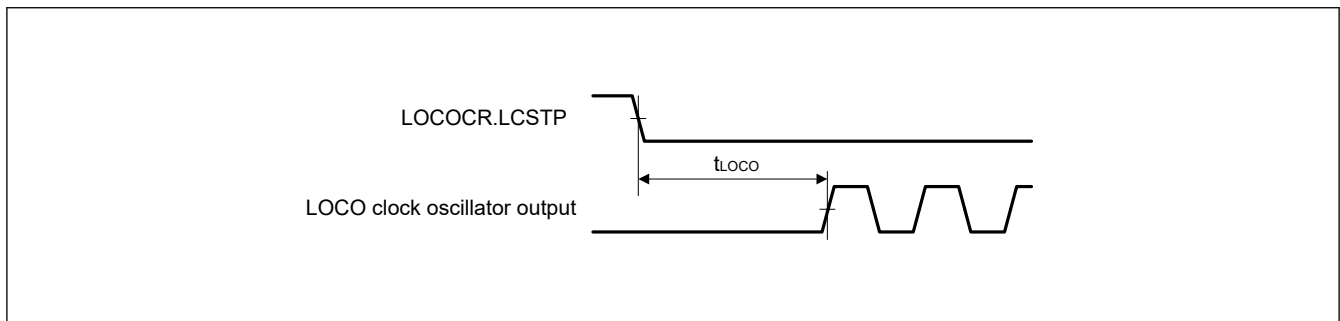


Figure 2.3 LOCO clock oscillation start timing

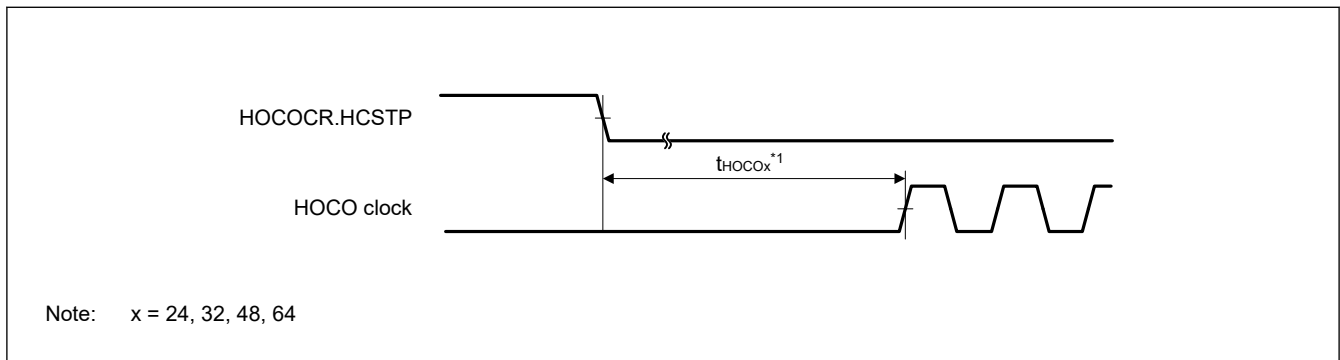


Figure 2.4 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

2.3.3 Reset Timing

Table 2.20 Reset timing (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|-----------------|--------------------|-----|-----|-----|------|-----------------|
| RES pulse width | At power-on | t _{RESWP} | 10 | — | — | ms | Figure 2.5 |
| | Not at power-on | t _{RESW} | 30 | — | — | μs | Figure 2.6 |
| Wait time after RES cancellation (at power-on) | LVD0 enabled*1 | t _{RESWT} | — | 0.9 | — | ms | Figure 2.5 |
| | LVD0 disabled*2 | | — | 0.2 | — | | |

Table 2.20 Reset timing (2 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|-----------------------------|--------------|-----|------|-----|------|-----------------|
| Wait time after RES cancellation (during powered-on state) | LVD0 enabled ^{*1} | t_{RESWT2} | — | 0.9 | — | ms | Figure 2.6 |
| | LVD0 disabled ^{*2} | | — | 0.2 | — | | |
| Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset) | LVD0 enabled ^{*1} | t_{RESWT3} | — | 0.9 | — | ms | Figure 2.7 |
| | LVD0 disabled ^{*2} | | — | 0.15 | — | | |

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

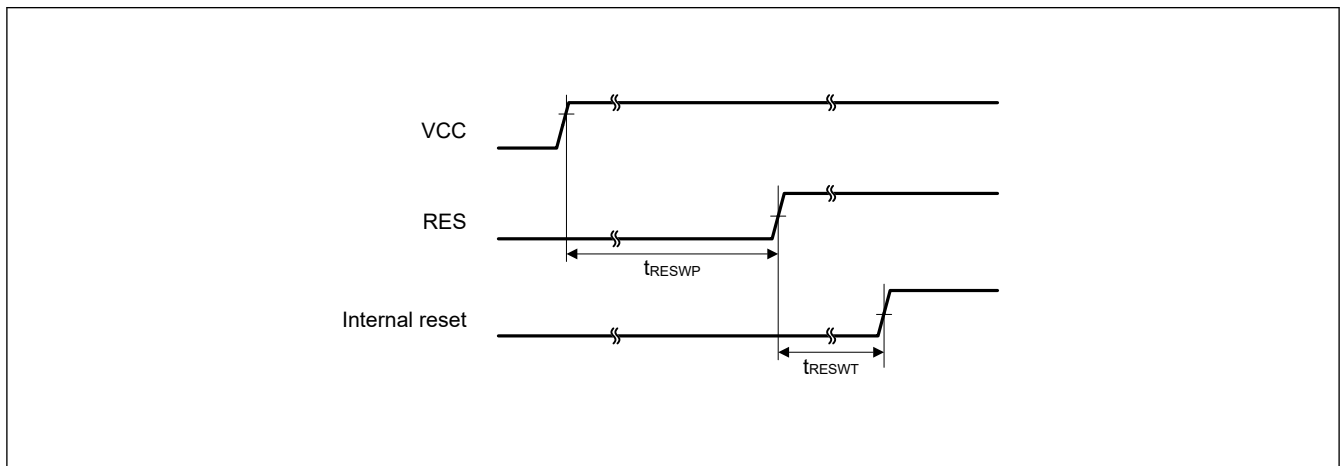


Figure 2.5 Reset input timing at power-on

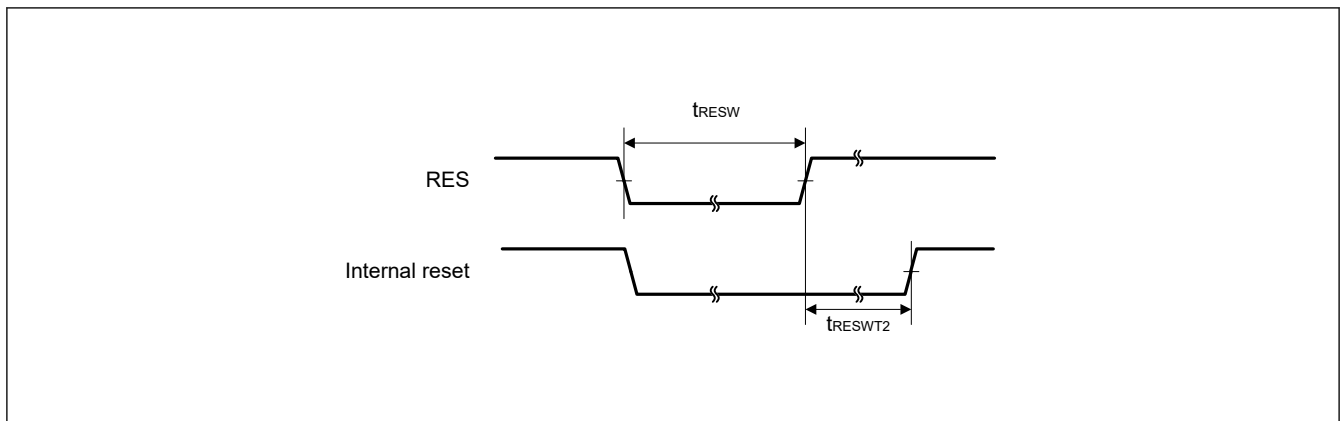


Figure 2.6 Reset input timing (1)

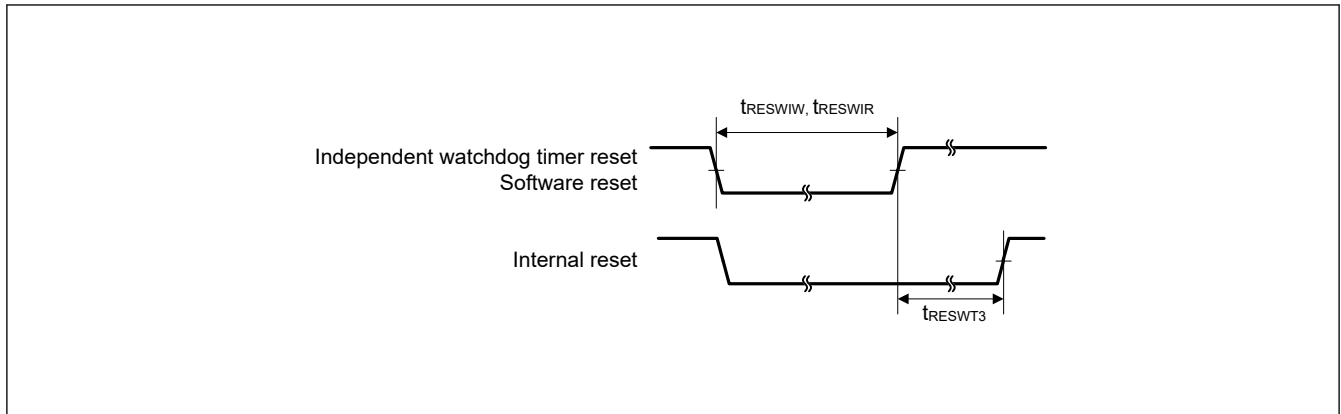


Figure 2.7 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.21 Timing of recovery from low power modes (1)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--|-----------------|--|--------------------|-----|-----|------|-----------------|------------|
| Recovery time from Software Standby mode ^{*1} | High-speed mode | System clock source is HOCO (HOCO clock is 32 MHz) ^{*2} | t _{SBYHO} | — | 7.4 | 9.1 | μs | Figure 2.8 |
| | | System clock source is HOCO (HOCO clock is 48 MHz) ^{*3} | t _{SBYHO} | — | 7.3 | 8.9 | μs | |
| | | System clock source is HOCO (HOCO clock is 64 MHz) ^{*2} | t _{SBYHO} | — | 7.4 | 9.1 | μs | |
| | | System clock source is MOCO (8 MHz) | t _{SBYMO} | — | 4 | 5 | μs | |

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The system clock is 32 MHz.

Note 3. The system clock is 48 MHz.

Table 2.22 Timing of recovery from low power modes (2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|--|-------------------|---|----------------------|--------------------|------|------|-----------------|----|------------|
| Recovery time from Software Standby mode ^{*1} | Middle-speed mode | System clock source is HOCO ^{*2} | VCC = 1.8 V to 5.5 V | t _{SBYHO} | — | 7.7 | 9.4 | μs | Figure 2.8 |
| | | | VCC = 1.6 V to 1.8 V | — | 15.7 | 17.9 | μs | | |
| | | System clock source is MOCO (8 MHz) | VCC = 1.8 V to 5.5 V | t _{SBYMO} | — | 4 | 5 | μs | |
| | | | VCC = 1.6 V to 1.8 V | — | 7.2 | 9 | μs | | |

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The system clock is 24 MHz.

Table 2.23 Timing of recovery from low power modes (3)

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|----------------|-------------------------------------|-------------|-----|-----|-----|---------------|-----------------|
| Recovery time from Software Standby mode*1 | Low-speed mode | System clock source is MOCO (2 MHz) | t_{SBYMO} | — | 12 | 15 | μs | Figure 2.8 |

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Table 2.24 Timing of recovery from low power modes (4)

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|-------------------|--|-------------|-----|------|-----|------|-----------------|
| Recovery time from Software Standby mode | Subosc-speed mode | System clock source is LOCO (32.768 kHz) | t_{SBYLO} | — | 0.85 | 1.2 | ms | Figure 2.8 |

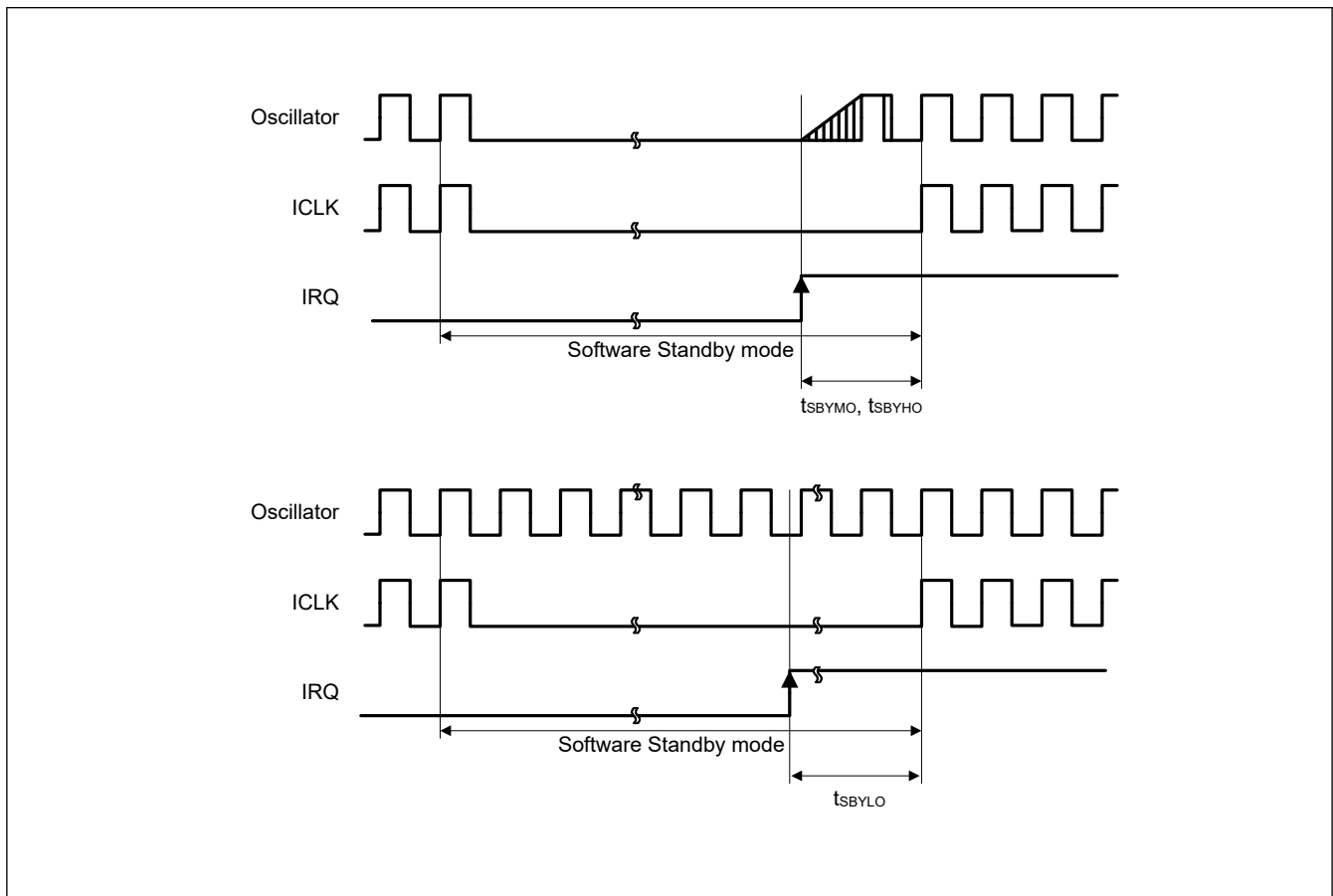


Figure 2.8 Software Standby mode cancellation timing

Table 2.25 Timing of recovery from low power modes (5) (1 of 2)

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|-----------|--------|-----|-----|---------------|------------|-----------------|
| Recovery time from Software Standby mode to Snooze mode | High-speed mode System clock source is HOCO | t_{SNZ} | — | 6.6 | 8.1 | μs | Figure 2.9 | |
| | Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V | t_{SNZ} | — | 6.7 | 8.2 | μs | | |

Table 2.25 Timing of recovery from low power modes (5) (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|-----------|-----|------|------|---------|-----------------|
| Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V | t_{SNZ} | — | 10.8 | 12.9 | μs | |
| Low-speed mode System clock source is MOCO (2 MHz) | t_{SNZ} | — | 6.7 | 8.0 | μs | |

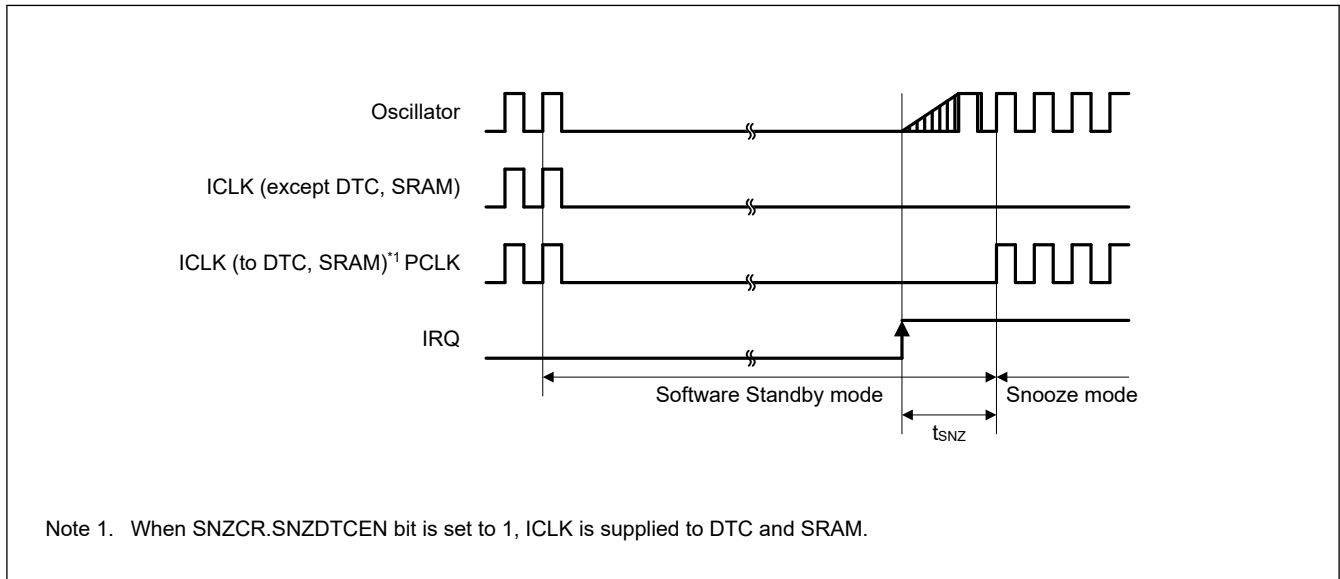


Figure 2.9 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.26 NMI and IRQ noise filter

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|-----------------|------------|-----------------------------|-----|-----|------|-----------------------------|----------------------------------|
| NMI pulse width | t_{NMIW} | 200 | — | — | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5^{*2}$ | — | — | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | t_{IRQW} | 200 | — | — | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5^{*3}$ | — | — | | | $t_{IRQCK} \times 3 > 200$ ns |

- Note: 200 ns minimum in Software Standby mode.
- Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
- Note 1. t_{Pcyc} indicates the PCLKB cycle.
- Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
- Note 3. t_{IRQCK} indicates the cycle of the IRQ_i digital filter sampling clock (i = 0 to 7).

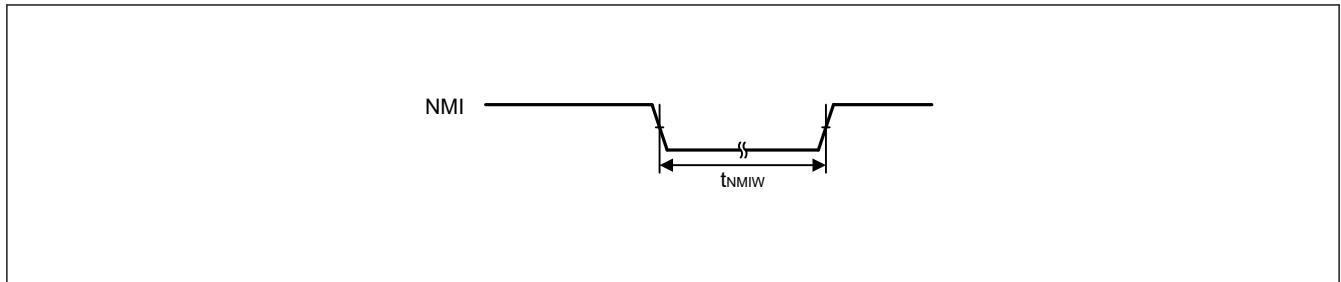


Figure 2.10 NMI interrupt input timing

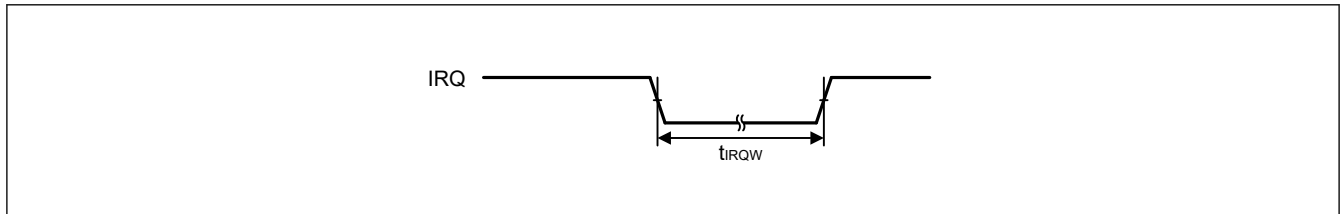


Figure 2.11 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGTW, KINT, and ADC12 Trigger Timing

Table 2.27 I/O Ports, POEG, GPT, AGTW, KINT, and ADC12 trigger timing

| Parameter | | Symbol | Min | Max | Unit | Test conditions | |
|---|--|--|-----------------|------|------------|-----------------|-------------|
| I/O Ports | Input data pulse width | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | t_{PRW} | 2 | — | t_{Pcyc} | Figure 2.12 |
| | | $2.4\text{ V} \leq V_{CC} < 2.7\text{ V}$ | | 3 | | | |
| | | $1.6\text{ V} \leq V_{CC} < 2.4\text{ V}$ | | 4 | | | |
| POEG | POEG input trigger pulse width | t_{POEW} | 3 | — | t_{Pcyc} | Figure 2.13 | |
| GPT | Input capture pulse width | Single edge | t_{GTICW} | 1.5 | — | t_{PDcyc} | Figure 2.14 |
| | | Dual edge | | 2.5 | | | |
| AGTW | AGTIO, AGTEE input cycle | $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | t_{ACYC}^{*1} | 250 | — | ns | Figure 2.15 |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | | 2000 | | ns | |
| | AGTIO, AGTEE input high-level width, low-level width | $1.8\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | t_{ACKWH} | 100 | — | ns | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | t_{ACKWL} | 800 | — | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | t_{ACYC2} | 62.5 | — | ns | Figure 2.15 |
| | | $2.4\text{ V} \leq V_{CC} < 2.7\text{ V}$ | | 125 | | ns | |
| $1.8\text{ V} \leq V_{CC} < 2.4\text{ V}$ | | 250 | | ns | | | |
| $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | | 500 | | ns | | | |
| ADC12 | 12-bit A/D converter trigger input pulse width | t_{TRGW} | 1.5 | — | t_{Pcyc} | Figure 2.16 | |
| KINT | KRn (n = 00 to 03) pulse width | t_{KR} | 250 | — | ns | Figure 2.17 | |

Note 1. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc} : PCLKB cycle) < t_{ACYC} .

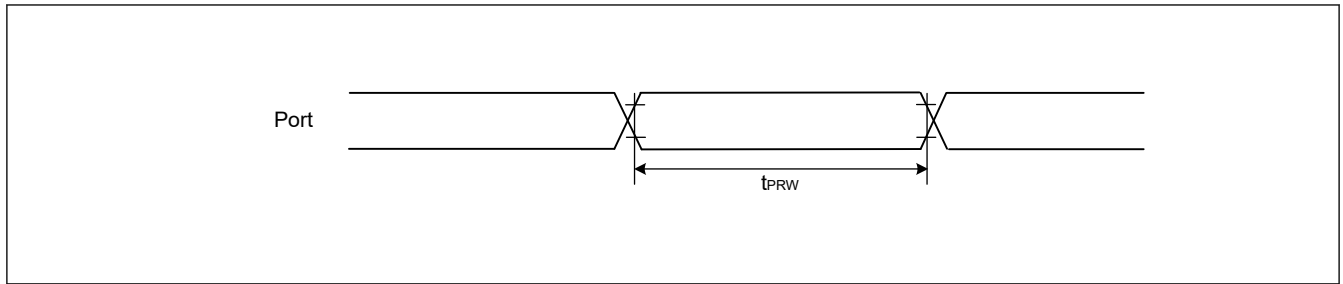


Figure 2.12 I/O ports input timing

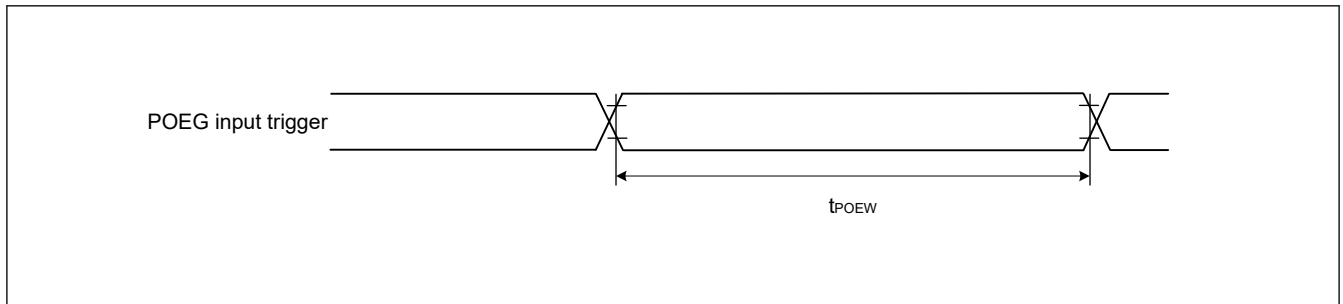


Figure 2.13 POEG input trigger timing

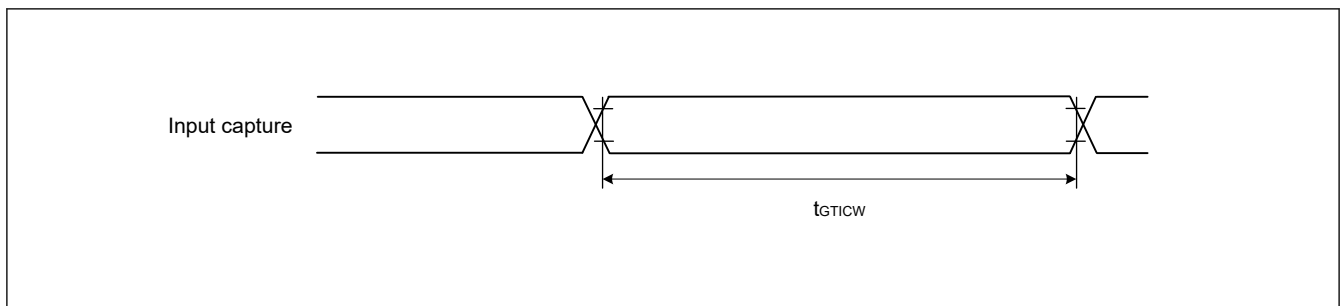


Figure 2.14 GPT input capture timing

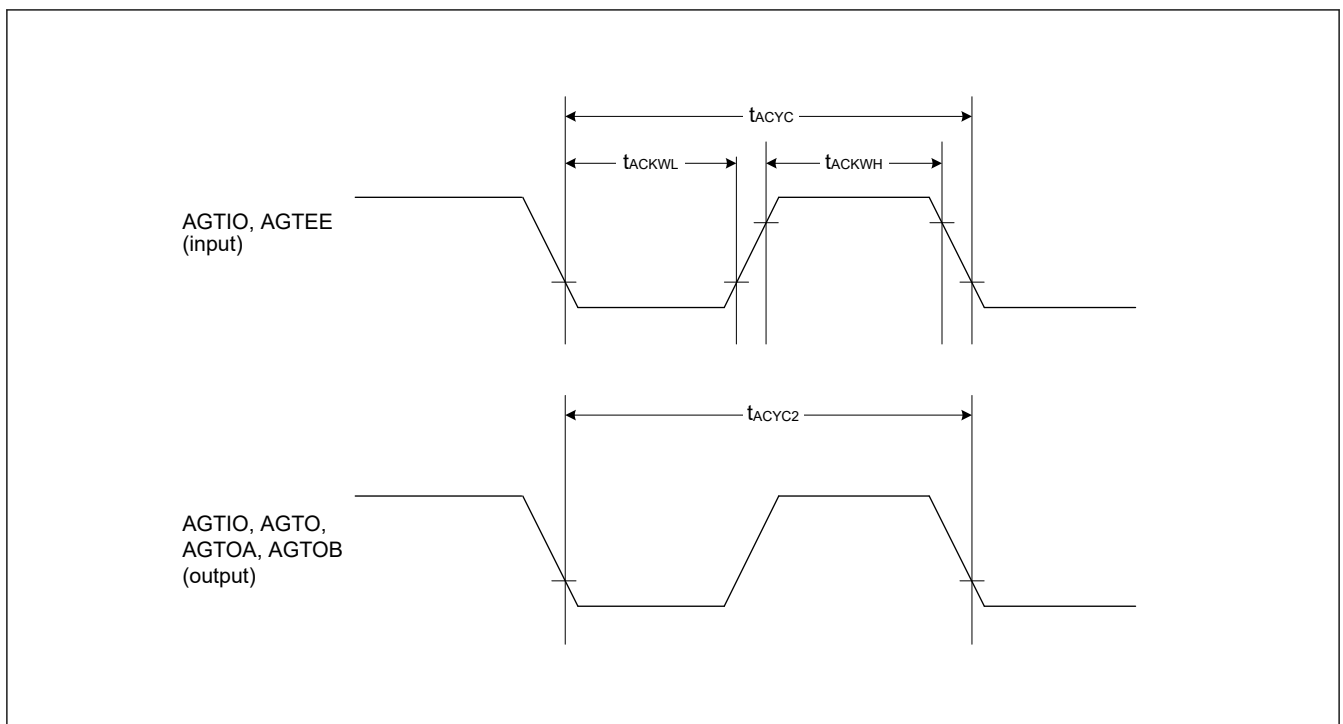


Figure 2.15 AGTW I/O timing

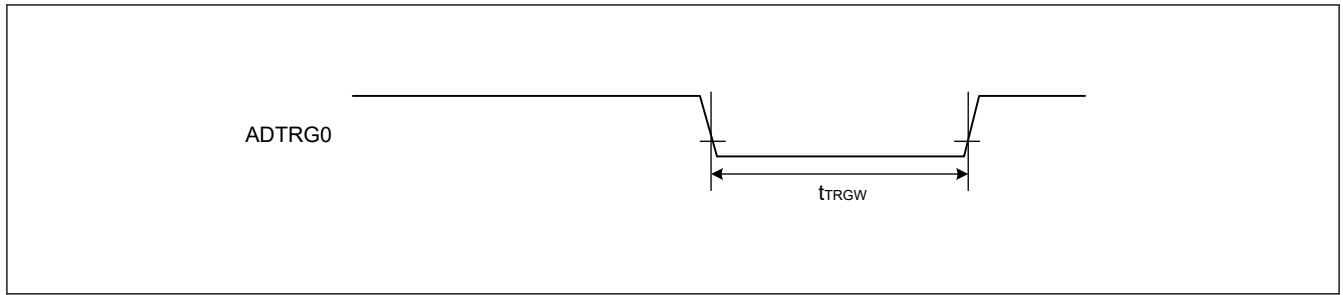


Figure 2.16 ADC12 trigger input timing

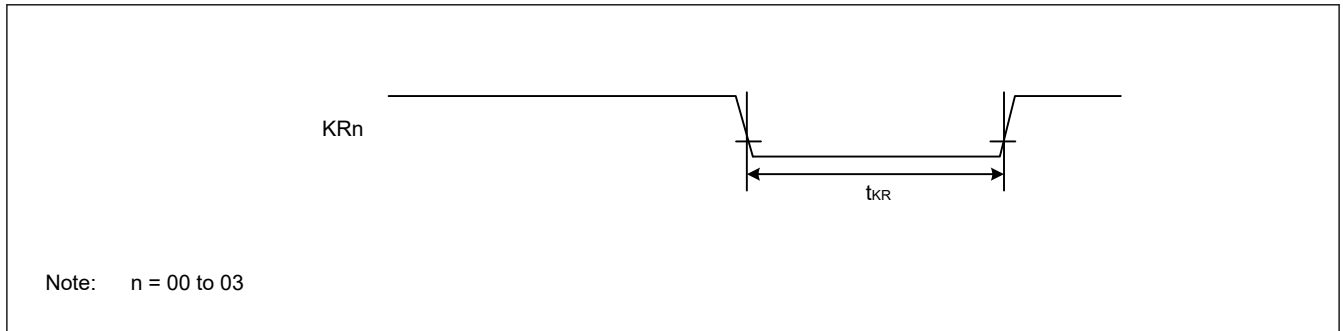


Figure 2.17 Key interrupt input timing

2.3.7 CAC Timing

Table 2.28 CAC timing

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------|--------------------------|---------|-----------------------------------|--|-----|------|-----------------|
| CAC | CACREF input pulse width | tCACREF | $t_{Pcyc}^{*1} \leq t_{CAC}^{*2}$ | — | — | ns | — |
| | | | $t_{Pcyc}^{*1} > t_{CAC}^{*2}$ | $4.5 \times t_{CAC} + 3 \times t_{Pcyc}$ | — | — | |

Note 1. tPcyc: PCLKB cycle.

Note 2. tCAC: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.29 SCI timing (1)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | | Symbol | Min | Max | Unit | Test conditions | |
|---|-------------------------|-------------------|--|-------------------|-------------------|-----|-------------------|-----------------|-------------------|
| SCI | Input clock cycle | Asynchronous | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{Scyc} | 125 | — | ns | Figure 2.18 | |
| | | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 250 | — | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 500 | — | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 1000 | — | | | |
| | | Clock synchronous | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | 187.5 | — | | | |
| | | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 375 | — | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 750 | — | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 1500 | — | | | |
| | Input clock pulse width | | | | t_{SCKW} | 0.4 | 0.6 | | t_{Scyc} |
| | Input clock rise time | | | | t_{SCKr} | — | 20 | | ns |
| | Input clock fall time | | | | t_{SCKf} | — | 20 | | ns |
| | Output clock cycle | Asynchronous | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{Scyc} | 187.5 | — | ns | | |
| | | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 375 | — | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 750 | — | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 1500 | — | | | |
| | | Clock synchronous | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | 125 | — | | | |
| $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | | 250 | | — | | | | |
| $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | | 500 | | — | | | | |
| $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | | 1000 | | — | | | | |
| Output clock pulse width | | | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | | |
| Output clock rise time | | | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{SCKr} | — | 20 | ns | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | — | 30 | | | |
| Output clock fall time | | | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{SCKf} | — | 20 | ns | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | — | 30 | | | |
| Transmit data delay time (master) | Clock synchronous | | | t_{TXD} | — | 40 | ns | | |
| | | | | | — | 45 | | | |
| Transmit data delay time (slave) | Clock synchronous | | | t_{TXD} | — | 55 | ns | | |
| | | | | | — | 60 | | | |
| | | | | | — | 100 | | | |
| | | | | | — | 125 | | | |
| Receive data setup time (master) | Clock synchronous | | | t_{RXS} | 45 | — | ns | | |
| | | | | | 55 | — | | | |
| | | | | | 90 | — | | | |
| | | | | | 110 | — | | | |
| Receive data setup time (slave) | Clock synchronous | | | t_{RXS} | 40 | — | ns | | |
| | | | | | 45 | — | | | |
| Receive data hold time (master) | Clock synchronous | | | | t_{RXH} | 5 | — | ns | |
| Receive data hold time (slave) | Clock synchronous | | | | t_{RXH} | 40 | — | ns | |

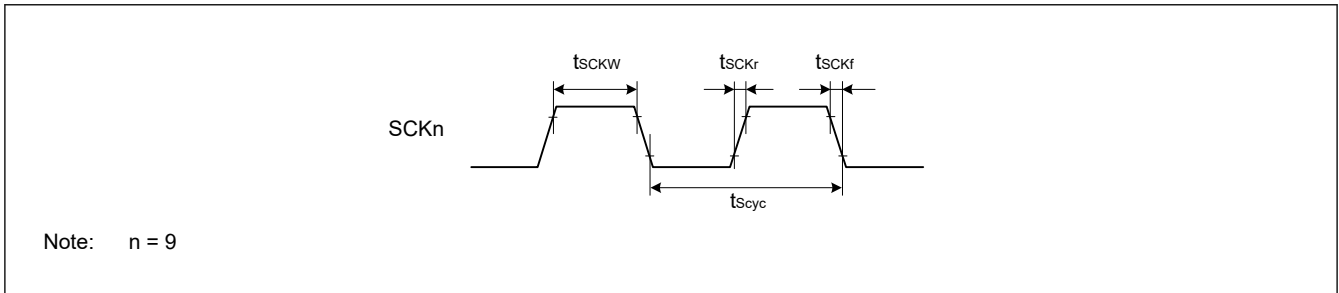


Figure 2.18 SCK clock input timing

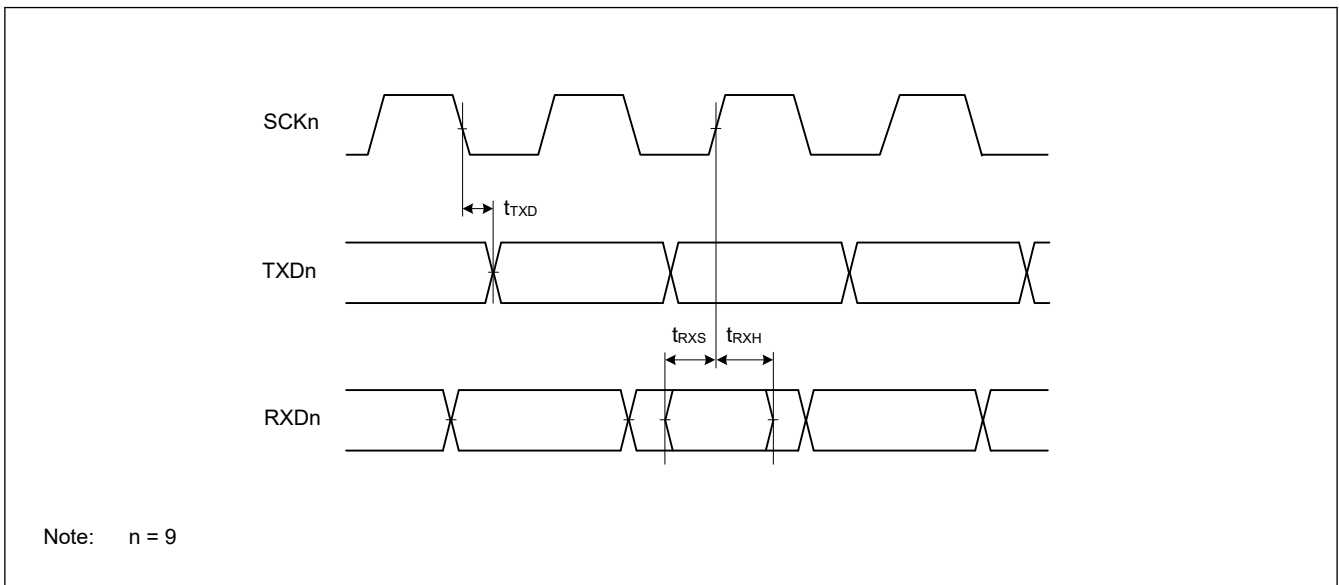


Figure 2.19 SCI input/output timing in clock synchronous mode

Table 2.30 SCI timing (2) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions | | | | |
|---|--|--|--------------------|--|--------------------------------|--------------------|----------------------------|-----|-----|--------------------|--|
| Simple SPI | SCK clock cycle output (master) | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{SPcyc} | 125 | — | ns | Figure 2.20 | | | | |
| | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 250 | — | | | | | | |
| | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 500 | — | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 1000 | — | | | | | | |
| | SCK clock cycle input (slave) | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | 187.5 | — | | | | | | |
| | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 375 | — | | | | | | |
| | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 750 | — | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 1500 | — | | | | | | |
| | SCK clock high pulse width | | | | t_{SPCKWH} | | | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock low pulse width | | | | t_{SPCKWL} | | | 0.4 | 0.6 | t_{SPcyc} | |
| SCK clock rise and fall time | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | t_{SPCKr} | — | 20 | ns | | | | | |
| | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | t_{SPCKf} | — | 30 | | | | | | |
| Data input setup time | Master | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{SU} | 45 | — | ns | Figure 2.21 to Figure 2.24 | | | | |
| | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 55 | — | | | | | | |
| | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | 80 | — | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | 110 | — | | | | | | |
| | Slave | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | 40 | — | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | 45 | — | | | | | | |
| Data input hold time | Master | | t_{H} | 33.3 | — | ns | | | | | |
| | Slave | | | 40 | — | | | | | | |
| SS input setup time | | | t_{LEAD} | 1 | — | t_{SPcyc} | | | | | |
| SS input hold time | | | t_{LAG} | 1 | — | t_{SPcyc} | | | | | |
| Data output delay time | Master | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{OD} | — | 40 | ns | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | — | 50 | | | | | | |
| | Slave | $2.4\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | | — | 65 | | | | | | |
| | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | — | 100 | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | — | 125 | | | | | | |
| Data output hold time | Master | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | t_{OH} | -10 | — | ns | | | | | |
| | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | | -20 | — | | | | | | |
| | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | | -30 | — | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | -40 | — | | | | | | |
| | Slave | | | | -10 | | | — | | | |
| | Data rise and fall time | Master | | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | $t_{\text{Dr}}, t_{\text{Df}}$ | | | — | 20 | ns | |
| $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | | | — | 30 | | | | | | | |
| Slave | | $1.8\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | — | 20 | | | | | | | |
| | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | — | 30 | | | | | | | |

Table 2.30 SCI timing (2) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Max | Unit*1 | Test conditions | |
|------------|---------------------------|---------------------|-------------------------|-----|-------------------|-----------------|-------------------|
| Simple SPI | Slave access time | 2.4 V ≤ VCC ≤ 5.5 V | — | 6 | t _{Pcyc} | Figure 2.24 | |
| | | 1.8 V ≤ VCC < 2.4 V | 24 MHz ≤ PCLKB ≤ 32 MHz | — | | | 7 |
| | | | PCLKB < 24 MHz | — | | | 6 |
| | | 1.6 V ≤ VCC < 1.8 V | — | 6 | | | |
| | Slave output release time | 2.4 V ≤ VCC ≤ 5.5 V | t _{REL} | — | 6 | | t _{Pcyc} |
| | | 1.8 V ≤ VCC < 2.4 V | 24 MHz ≤ PCLKB ≤ 32 MHz | — | 7 | | |
| | | | PCLKB < 24 MHz | — | 6 | | |
| | | 1.6 V ≤ VCC < 1.8 V | — | 6 | | | |

Note 1. t_{Pcyc}: PCLKB cycle.

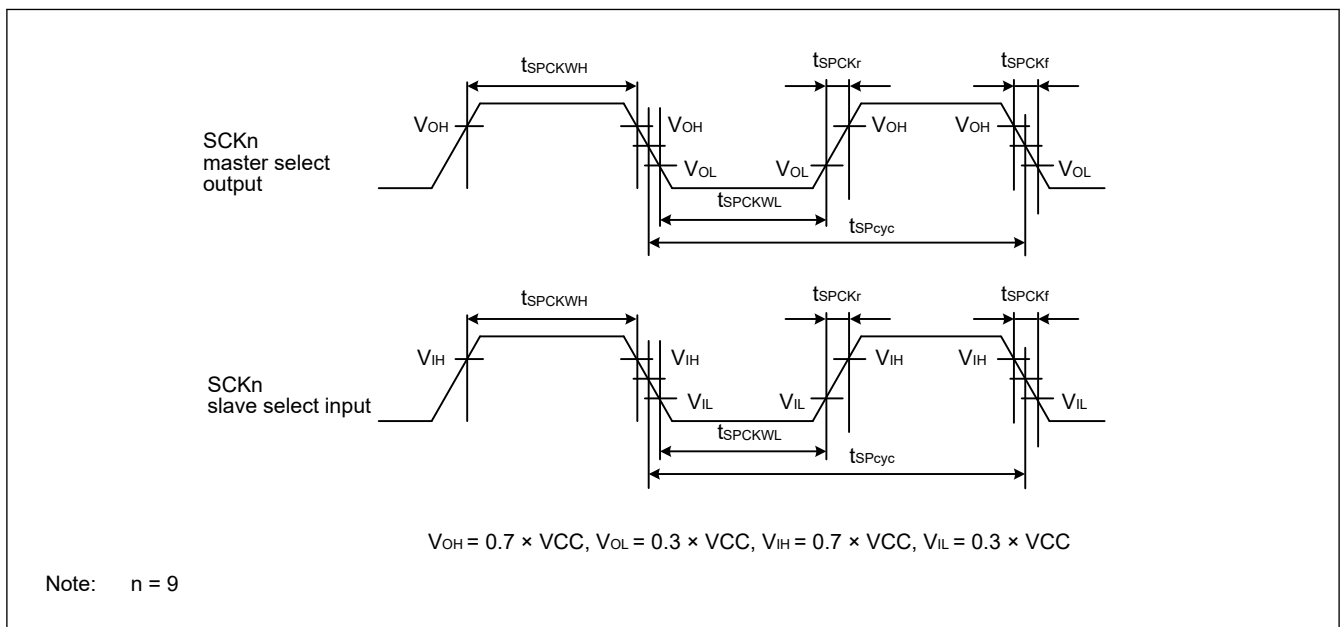


Figure 2.20 SCI simple SPI mode clock timing

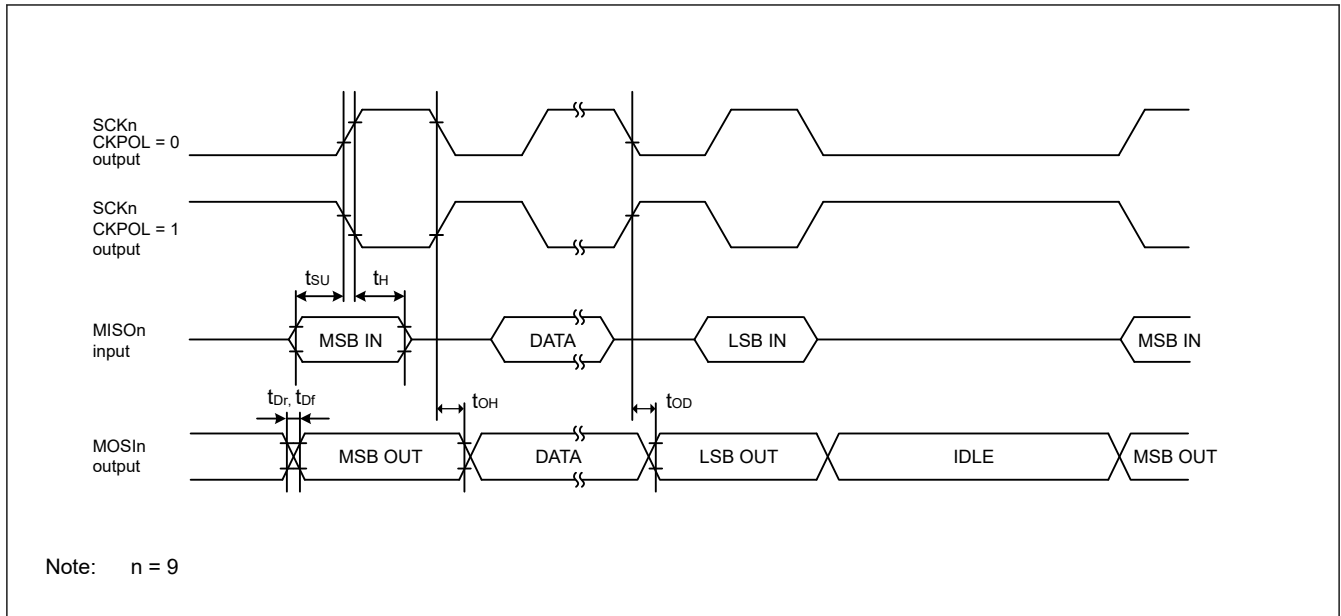


Figure 2.21 SCI simple SPI mode timing (master, CKPH = 1)

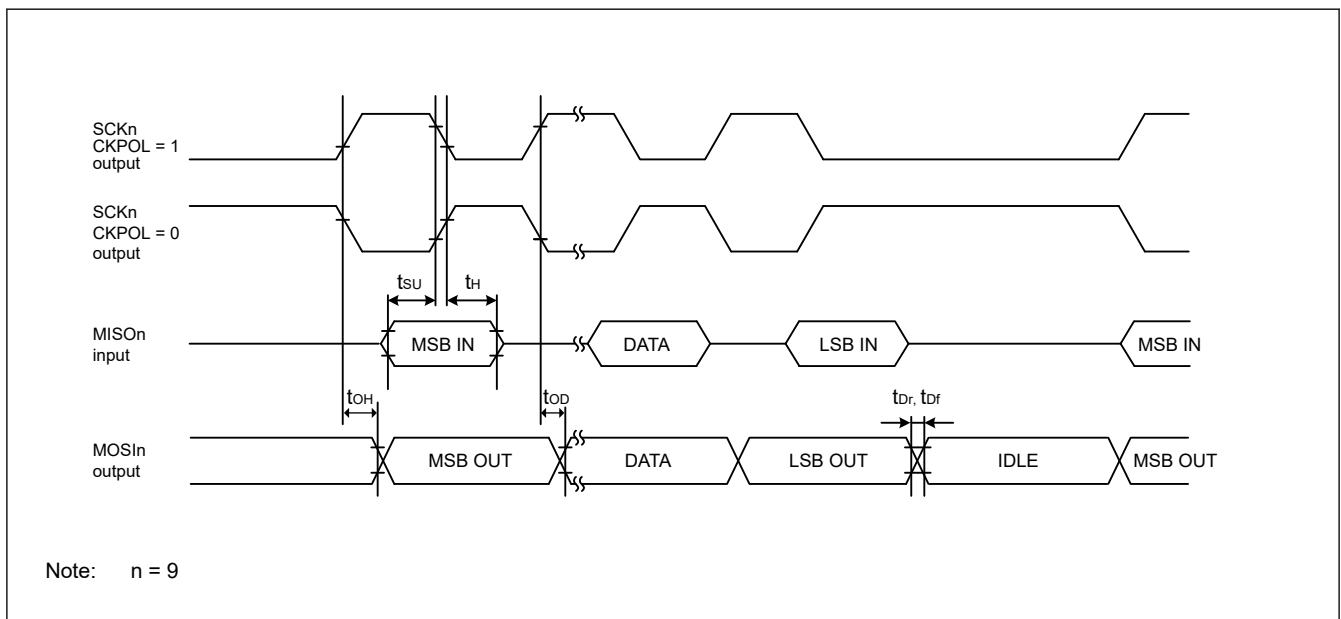


Figure 2.22 SCI simple SPI mode timing (master, CKPH = 0)

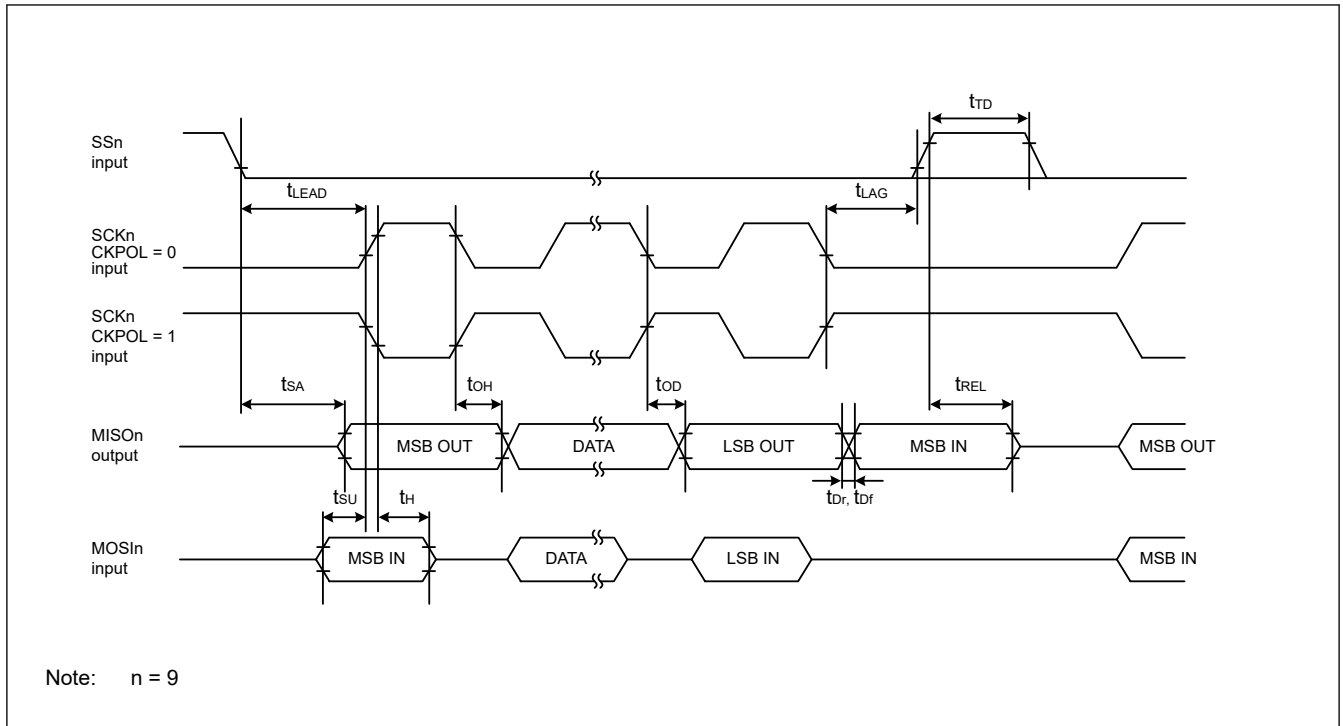


Figure 2.23 SCI simple SPI mode timing (slave, CKPH = 1)

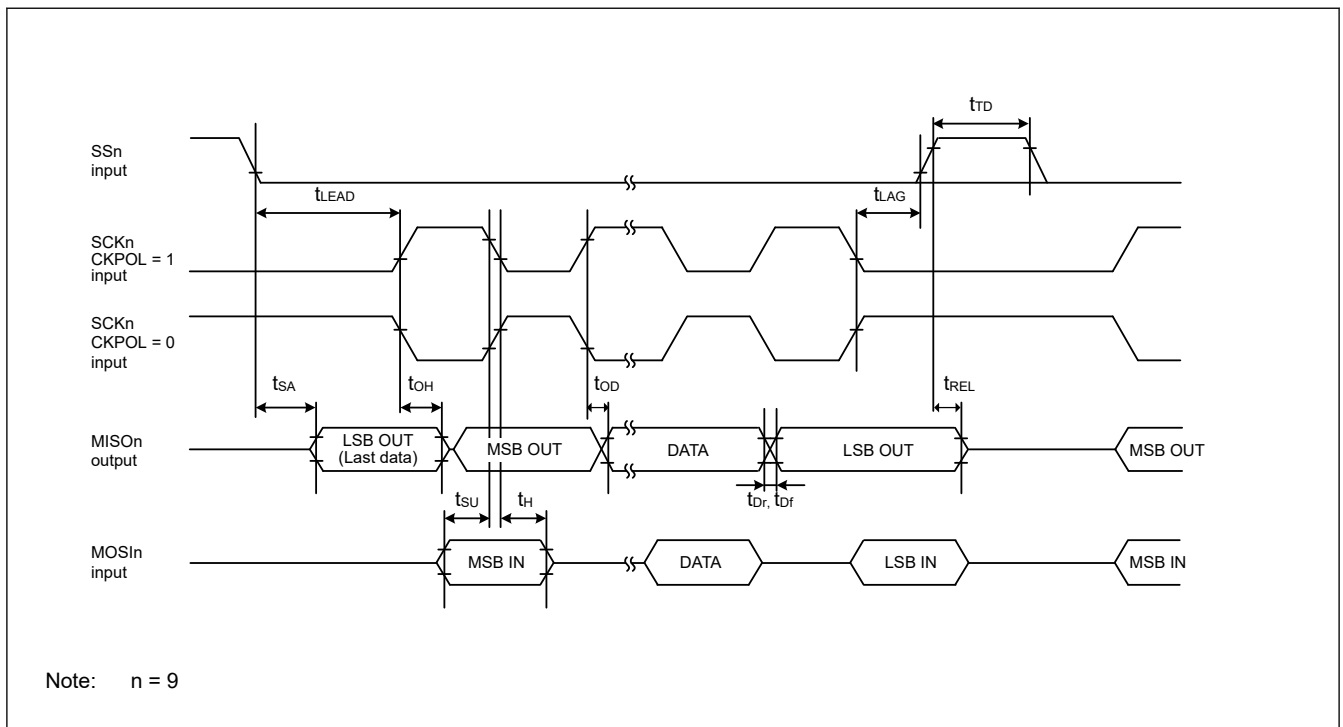


Figure 2.24 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.31 SCI timing (3)

Conditions: VCC = 2.7 to 5.5 V

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|----------------------------|------------------------------------|------------|-----|----------------------------|-----------------|-------------|
| Simple IIC (Standard mode) | SDA input rise time | t_{Sr} | — | 1000 | ns | Figure 2.25 |
| | SDA input fall time | t_{Sf} | — | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}^{*1}$ | ns | |
| | Data input setup time | t_{SDAS} | 250 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF | |
| Simple IIC (Fast mode) | SDA input rise time | t_{Sr} | — | 300 | ns | Figure 2.25 |
| | SDA input fall time | t_{Sf} | — | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}^{*1}$ | ns | |
| | Data input setup time | t_{SDAS} | 100 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF | |

Note 1. t_{IICcyc} : Clock cycle selected by the SMR.CKS[1:0] bits.

Note 2. C_b indicates the total capacity of the bus line.

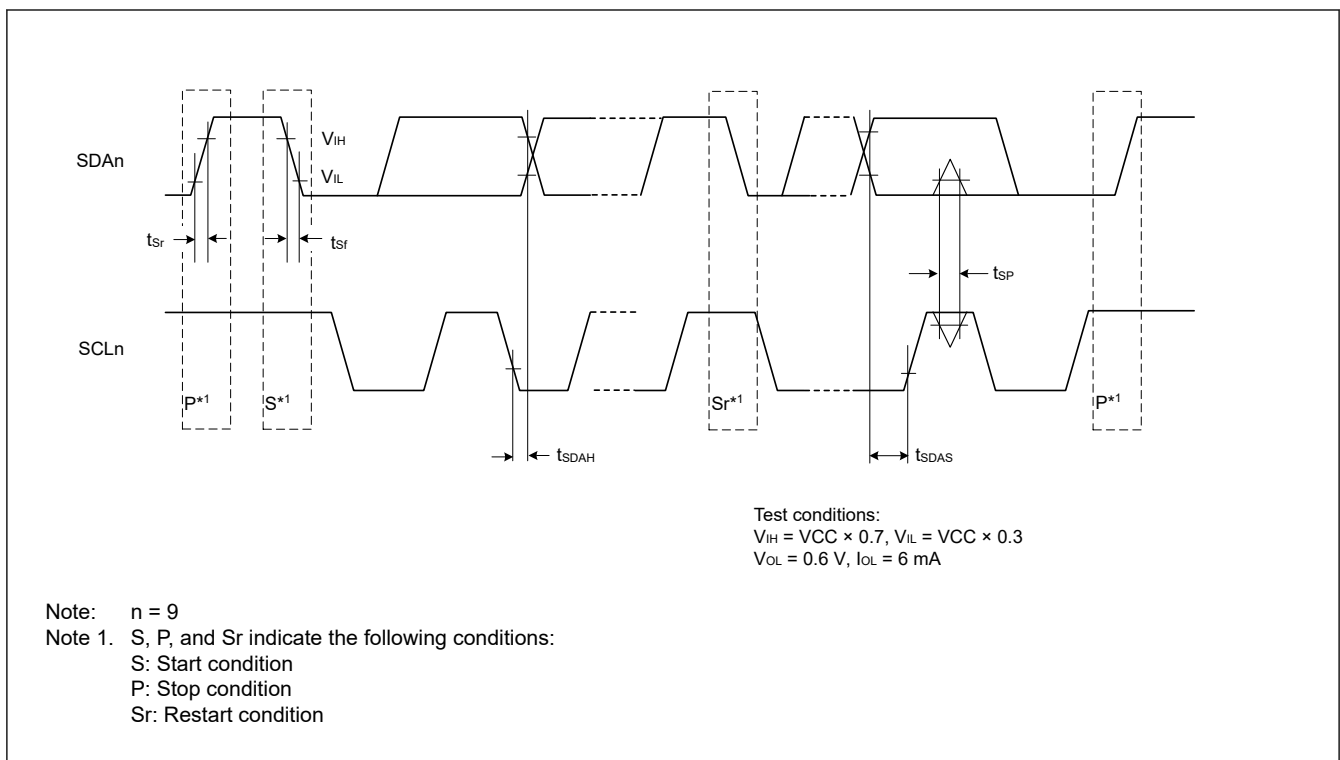


Figure 2.25 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.32 SPI timing (1 of 3)

| Parameter | | | | Symbol | Min | Max | Unit*1 | Test conditions |
|--------------------------------|------------------------------|---------------------|--|---------------------|---|-----|--------|--------------------------|
| SPI | RSPCK clock cycle | Master | 2.7 V ≤ VCC ≤ 5.5 V | t _{SPcyc} | 62.5 | — | ns | Figure 2.26 C = 30 pF |
| | | | 2.4 V ≤ VCC < 2.7 V | | 125 | — | | |
| | | | 1.8 V ≤ VCC < 2.4 V | | 250 | — | | |
| | | | 1.6 V ≤ VCC < 1.8 V | | 500 | — | | |
| | | Slave | 2.7 V ≤ VCC ≤ 5.5 V | | 187.5 | — | | |
| | | | 2.4 V ≤ VCC < 2.7 V | | 375 | — | | |
| | | | 1.8 V ≤ VCC < 2.4 V | | 750 | — | | |
| | | | 1.6 V ≤ VCC < 1.8 V | | 1500 | — | | |
| | RSPCK clock high pulse width | Master | | t _{SPCKWH} | (t _{SPcyc} - t _{SPCKr} - t _{SPCKf}) / 2 - 3 | — | ns | |
| | | Slave | | | | | | |
| | RSPCK clock low pulse width | Master | | t _{SPCKWL} | (t _{SPcyc} - t _{SPCKr} - t _{SPCKf}) / 2 - 3 | — | ns | |
| | | Slave | | | | | | |
| RSPCK clock rise and fall time | Output | 2.7 V ≤ VCC ≤ 5.5 V | t _{SPCKr} , t _{SPCKf} | — | 10 | ns | | |
| | | 2.4 V ≤ VCC < 2.7 V | | — | 15 | | | |
| | | 1.8 V ≤ VCC ≤ 2.4 V | | — | 20 | | | |
| | | 1.6 V ≤ VCC < 1.8 V | | — | 30 | | | |
| | Input | — | — | 1 | μs | | | |

Table 2.32 SPI timing (2 of 3)

| Parameter | | | | Symbol | Min | Max | Unit*1 | Test conditions | | |
|------------------------------------|------------------------|-------------------------------|---------------------|--|--|--|--------|-----------------|---|--|
| SPI | Data input setup time | Master | 2.7 V ≤ VCC ≤ 5.5 V | | t _{SU} | 10 | — | ns | Figure 2.27 to Figure 2.32 C = 30 pF | |
| | | | 2.4 V ≤ VCC < 2.7 V | 16 MHz < PCLKB ≤ 32 MHz | | 30 | — | | | |
| | | | | PCLKB ≤ 16 MHz | | 10 | — | | | |
| | | | 1.8 V ≤ VCC < 2.4 V | 16 MHz < PCLKB ≤ 32 MHz | | 55 | — | | | |
| | | | | 8 MHz < PCLKB ≤ 16 MHz | | 30 | — | | | |
| | | | | PCLKB ≤ 8 MHz | | 10 | — | | | |
| | | 1.6 V ≤ VCC < 1.8 V | | 10 | — | | | | | |
| | | Slave | 2.4 V ≤ VCC ≤ 5.5 V | | 10 | — | | | | |
| | | | 1.8 V ≤ VCC < 2.4 V | | 15 | — | | | | |
| | 1.6 V ≤ VCC < 1.8 V | | 20 | — | | | | | | |
| | Data input hold time | Master (RSPCK is PCLKB/2) | | t _{HF} | 0 | — | ns | | | |
| | | Master (RSPCK is not PCLKB/2) | | t _H | t _{Pcyc} | — | | | | |
| Slave | | t _H | 20 | — | | | | | | |
| SPI | SSL setup time | Master | 1.8 V ≤ VCC ≤ 5.5 V | | t _{LEAD} | -30 + N × t _{SPcyc} ^{*2} | — | ns | | |
| | | | 1.6 V ≤ VCC < 1.8 V | | | -50 + N × t _{SPcyc} ^{*2} | — | | | |
| | | Slave | | 6 × t _{Pcyc} | | — | ns | | | |
| | SSL hold time | Master | | t _{LAG} | -30 + N × t _{SPcyc} ^{*3} | — | ns | | | |
| | | Slave | | 6 × t _{Pcyc} | — | ns | | | | |
| | Data output delay time | Master | 2.7 V ≤ VCC ≤ 5.5 V | | t _{OD} | — | 14 | ns | | |
| 2.4 V ≤ VCC < 2.7 V | | | — | 20 | | | | | | |
| 1.8 V ≤ VCC < 2.4 V | | | — | 25 | | | | | | |
| 1.6 V ≤ VCC < 1.8 V | | | — | 30 | | | | | | |
| Slave | | 2.7 V ≤ VCC ≤ 5.5 V | | — | | 50 | | | | |
| | | 2.4 V ≤ VCC < 2.7 V | | — | | 60 | | | | |
| | | 1.8 V ≤ VCC < 2.4 V | | — | | 85 | | | | |
| | | 1.6 V ≤ VCC < 1.8 V | | — | | 110 | | | | |
| Data output hold time | Master | | t _{OH} | 0 | — | ns | | | | |
| | Slave | | | 0 | — | | | | | |
| Successive transmission delay time | Master | | t _{TD} | t _{SPcyc} + 2 × t _{Pcyc} | 8 × t _{SPcyc} + 2 × t _{Pcyc} | ns | | | | |
| | Slave | | | 6 × t _{Pcyc} | — | | | | | |

Table 2.32 SPI timing (3 of 3)

| Parameter | | Symbol | Min | Max | Unit*1 | Test conditions | | | |
|---------------------------|----------------------------------|------------------|--|--|----------------------------------|----------------------------------|---|----|--|
| SPI | MOSI and MISO rise and fall time | Output | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | — | 10 | ns | Figure 2.27 to Figure 2.32 C = 30 pF | | |
| | | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | — | 15 | | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | — | 20 | | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | — | 30 | | | | |
| | | Input | | — | 1 | μs | | | |
| | SSL rise and fall time | Output | $t_{\text{SSLr}}, t_{\text{SSLf}}$ | $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | — | 10 | | ns | |
| | | | $2.4\text{ V} \leq \text{VCC} < 2.7\text{ V}$ | — | 15 | | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | — | 20 | | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | — | 30 | | | | |
| | | Input | | — | 1 | μs | | | |
| | Slave access time | | t_{SA} | $2.4\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 100$ | | ns | Figure 2.31 and Figure 2.32 C = 30 pF |
| | | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 140$ | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 180$ | | | | |
| Slave output release time | | t_{REL} | $2.4\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 100$ | ns | | | |
| | | | $1.8\text{ V} \leq \text{VCC} < 2.4\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 140$ | | | | |
| | | | $1.6\text{ V} \leq \text{VCC} < 1.8\text{ V}$ | — | $2 \times t_{\text{Pcyc}} + 180$ | | | | |

Note 1. t_{Pcyc} : PCLKB cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

Note 3. N is set as an integer from 1 to 8 by the SSLND register.

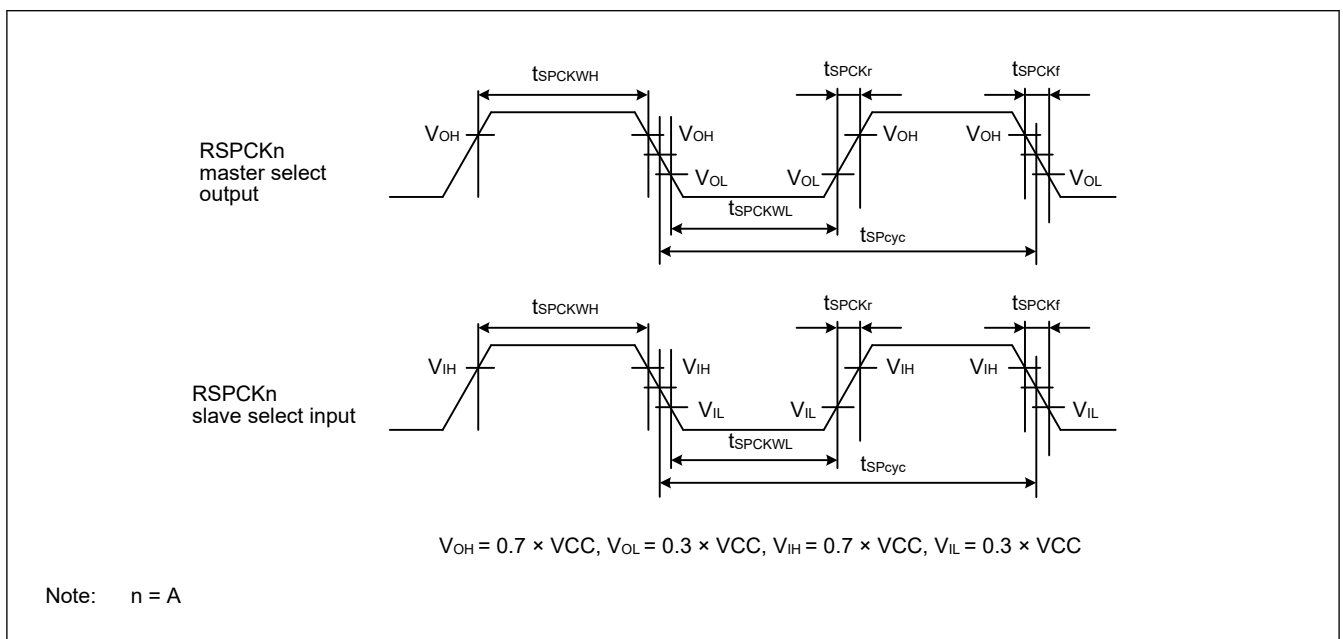


Figure 2.26 SPI clock timing

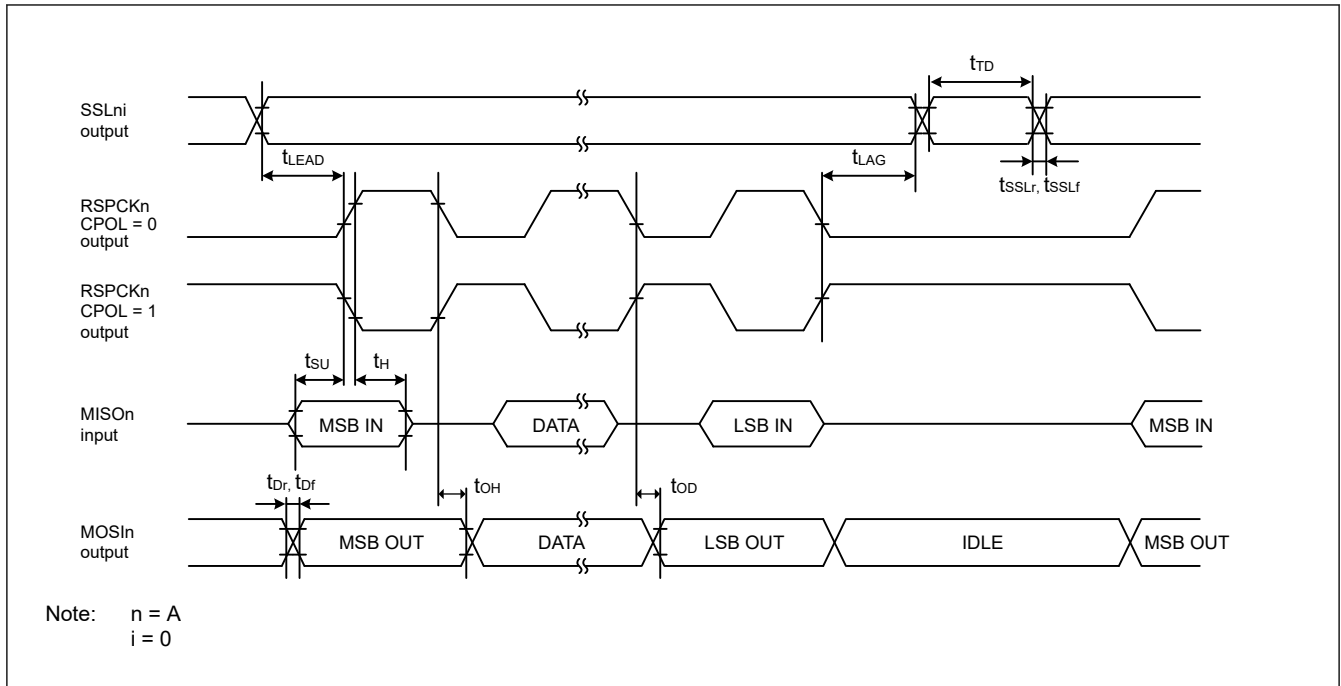


Figure 2.27 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

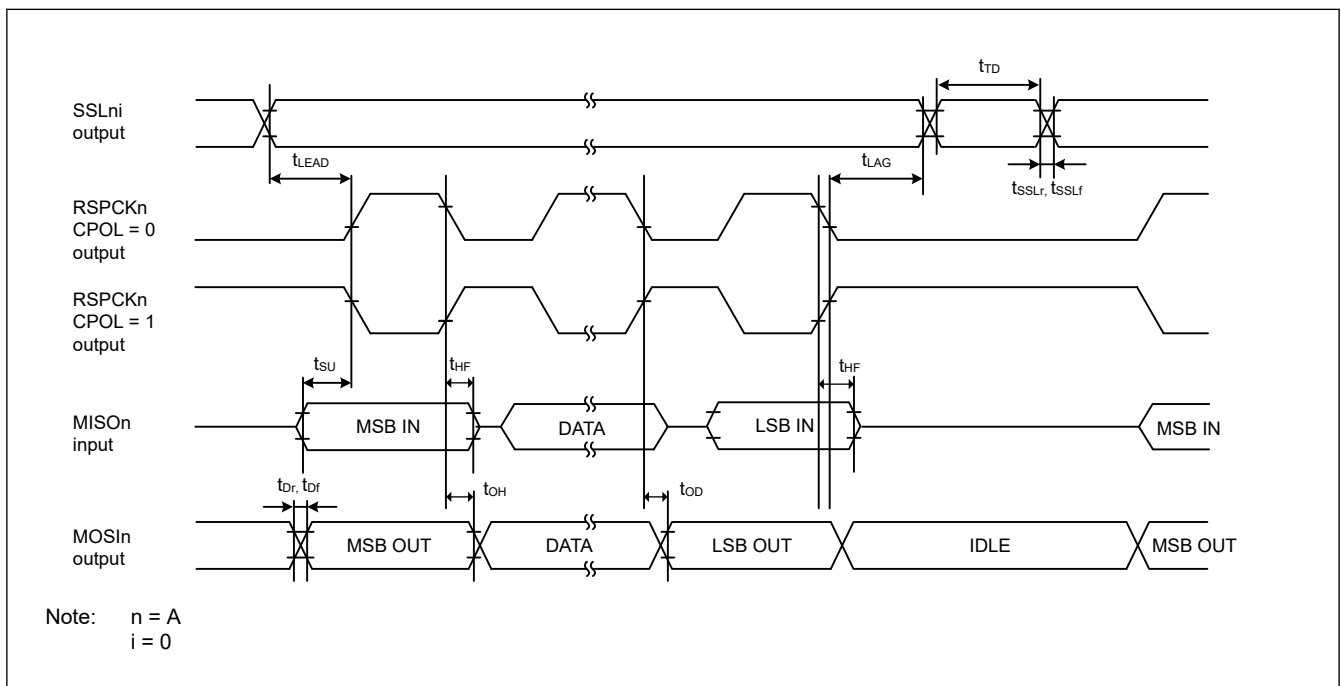


Figure 2.28 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

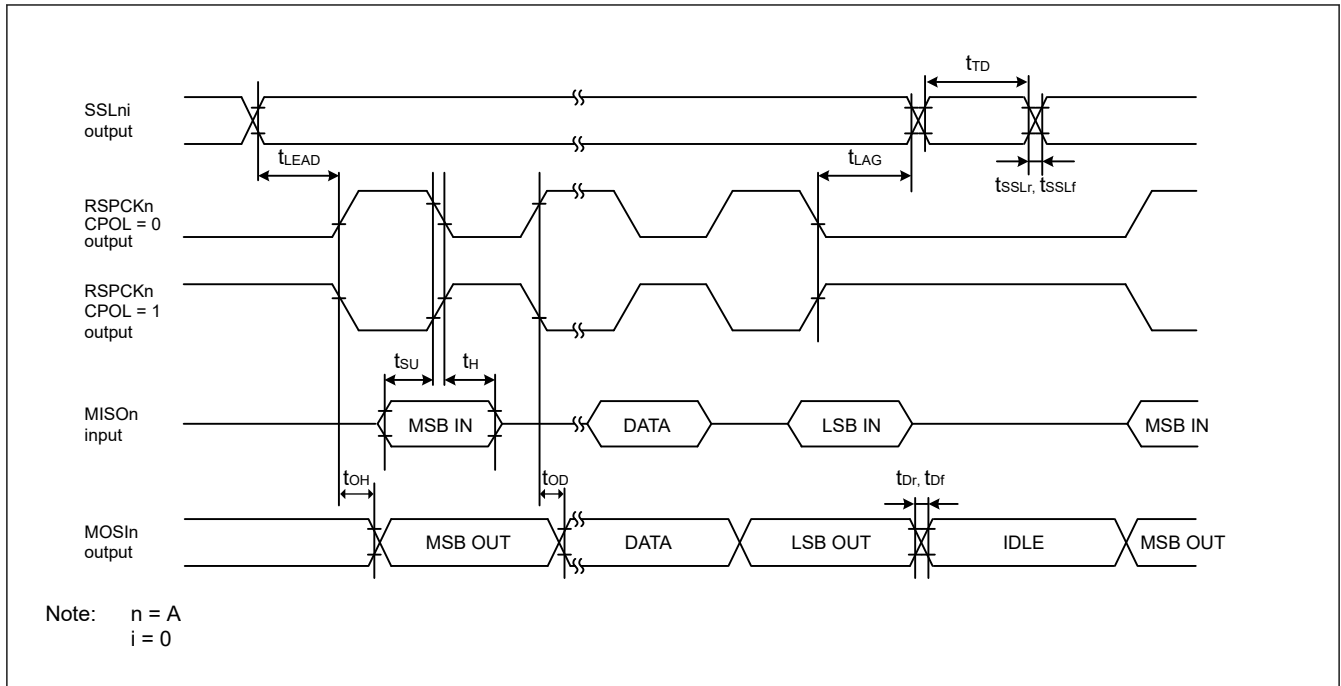


Figure 2.29 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

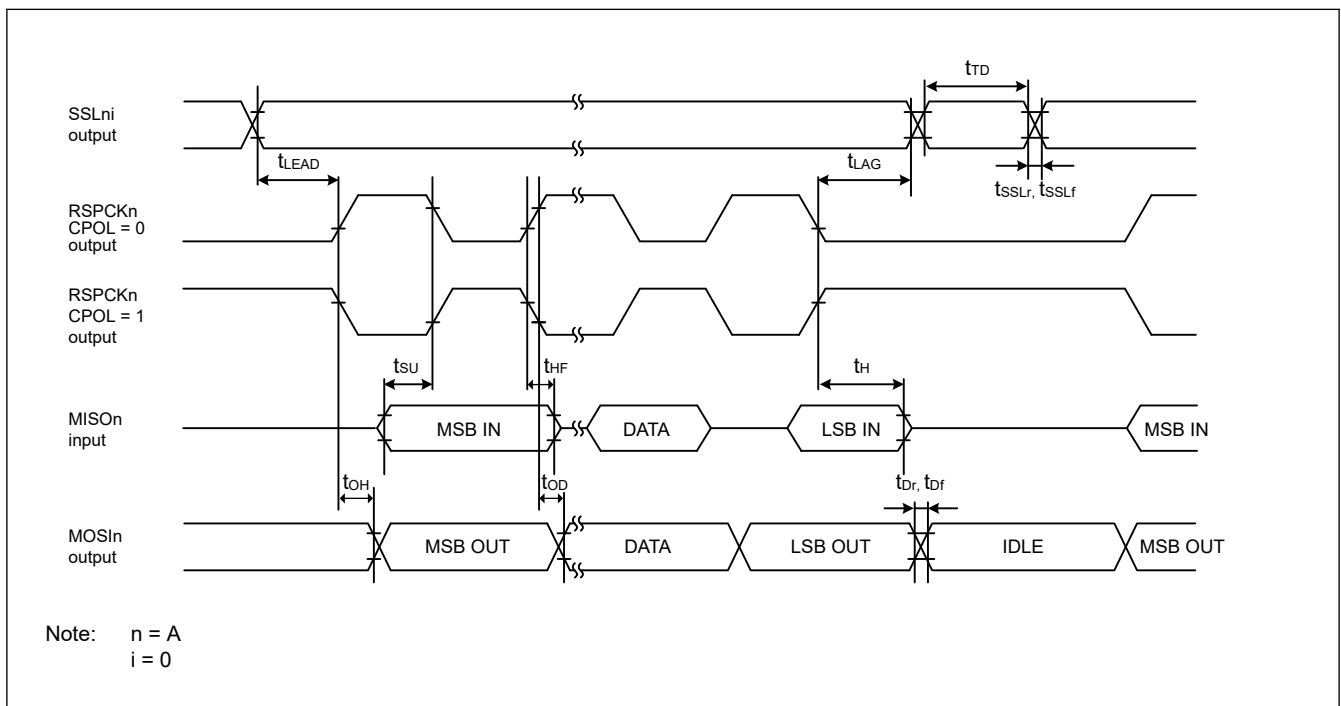


Figure 2.30 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

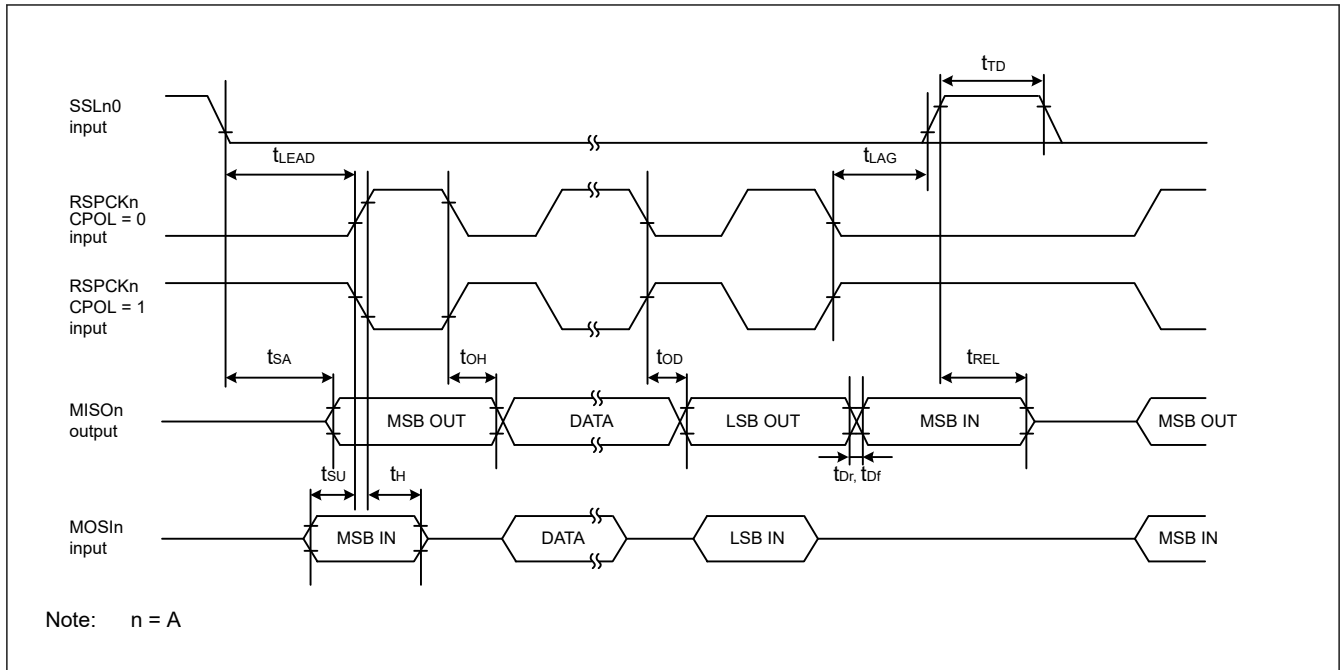


Figure 2.31 SPI timing (slave, CPHA = 0)

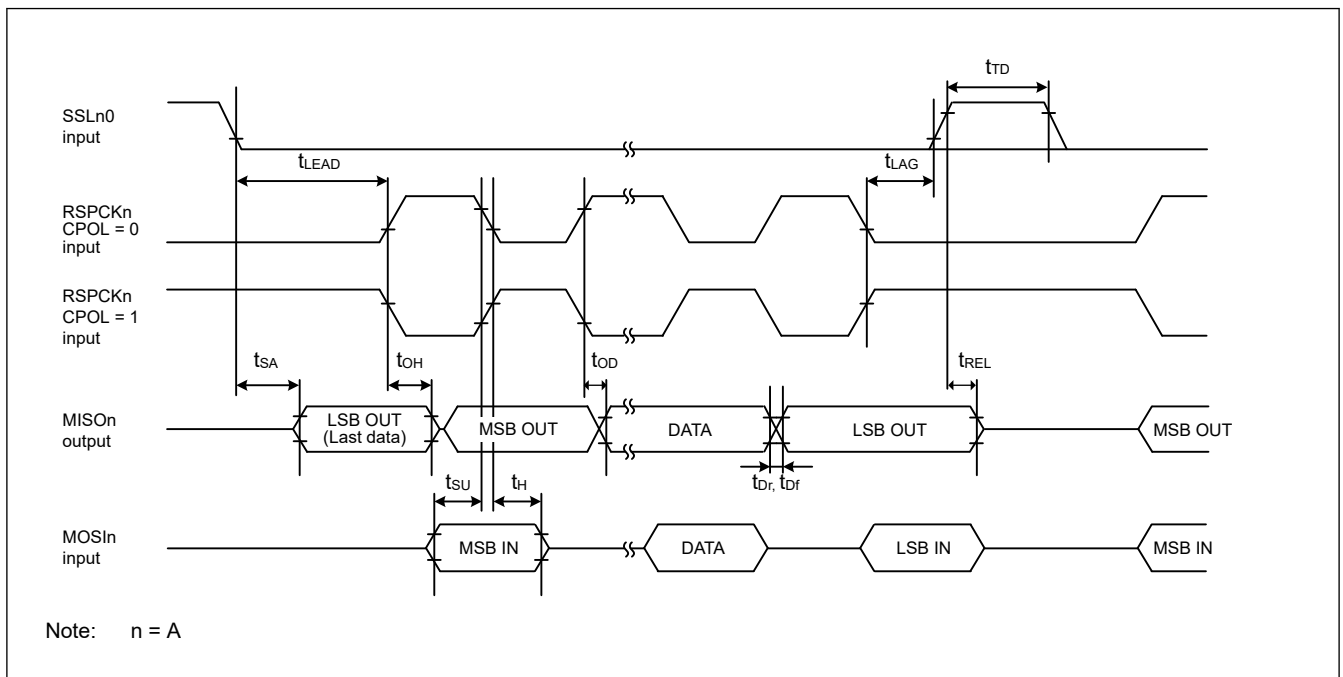


Figure 2.32 SPI timing (slave, CPHA = 1)

2.3.10 I3C Timing

Table 2.33 IIC timing

Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions |
|----------------------------|---|-------------------|---|------------------------------|------|-----------------|
| IIC (standard mode, SMBus) | SCL cycle time | t _{SCL} | 6 (40) × t _{IICcyc} + 4 × t _{Pcyc} + 1300 | — | ns | Figure 2.33 |
| | SCL high pulse width | t _{SCLH} | 3 (20) × t _{IICcyc} + 2 × t _{Pcyc} + 300 | — | ns | |
| | SCL low pulse width | t _{SCLL} | 3 (20) × t _{IICcyc} + 2 × t _{Pcyc} + 800 | — | ns | |
| | SCL, SDA rise time | t _{Sr} | — | 1000 | ns | |
| | SCL, SDA fall time | t _{Sf} | — | 300 | ns | |
| | SCL, SDA spike pulse removal time | t _{SP} | 0 | 1 (16) × t _{IICcyc} | ns | |
| | SDA bus free time | t _{BUF} | 3 (20) × t _{IICcyc} + 300 | — | ns | |
| | Hold time for START condition | t _{STAH} | t _{IICcyc} + 300 | — | ns | |
| | Setup time for repeated START condition | t _{STAS} | 1000 | — | ns | |
| | Setup time for STOP condition | t _{STOS} | 1000 | — | ns | |
| | Data setup time | t _{SDAS} | t _{IICcyc} + 50 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |
| IIC (Fast mode) | SCL cycle time | t _{SCL} | 6 (40) × t _{IICcyc} + 4 × t _{Pcyc} + 600 | — | ns | Figure 2.33 |
| | SCL high pulse width | t _{SCLH} | 3 (20) × t _{IICcyc} + 2 × t _{Pcyc} + 300 | — | ns | |
| | SCL low pulse width | t _{SCLL} | 3 (20) × t _{IICcyc} + 2 × t _{Pcyc} + 300 | — | ns | |
| | SCL, SDA rise time | t _{Sr} | — | 300 | ns | |
| | SCL, SDA fall time | t _{Sf} | — | 300 | ns | |
| | SCL, SDA spike pulse removal time | t _{SP} | 0 | 1 (16) × t _{IICcyc} | ns | |
| | SDA bus free time | t _{BUF} | 3 (20) × t _{IICcyc} + 300 | — | ns | |
| | Hold time for START condition | t _{STAH} | t _{IICcyc} + 300 | — | ns | |
| | Setup time for repeated START condition | t _{STAS} | 300 | — | ns | |
| | Setup time for STOP condition | t _{STOS} | 300 | — | ns | |
| | Data setup time | t _{SDAS} | t _{IICcyc} + 50 | — | ns | |
| | Data hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with DNFE.DNFE set to 1.

Table 2.34 IIC timing (Fast-mode+)

Conditions: VCC = 2.7 to 5.5 V

| Parameter | Symbol | Min*1 | Max | Unit | Test conditions | |
|---------------------|---|------------|--|----------------------------|-----------------|-------------|
| IIC (Fast-mode+) | SCL cycle time | t_{SCL} | $6 (40) \times t_{IICcyc} + 4 \times t_{Pcyc} + 240$ | — | ns | Figure 2.33 |
| | SCL high pulse width | t_{SCLH} | $3 (20) \times t_{IICcyc} + 2 \times t_{Pcyc} + 120$ | — | ns | |
| | SCL low pulse width | t_{SCLL} | $3 (20) \times t_{IICcyc} + 2 \times t_{Pcyc} + 120$ | — | ns | |
| | SCL, SDA rise time | t_{Sr} | — | 120 | ns | |
| | SCL, SDA fall time | t_{Sf} | — | 120 | ns | |
| | SCL, SDA spike pulse removal time | t_{SP} | — | $1 (16) \times t_{IICcyc}$ | ns | |
| | SDA bus free time | t_{BUF} | $3 (20) \times t_{IICcyc} + 120$ | — | ns | |
| | Hold time for START condition | t_{STAH} | $t_{IICcyc} + 135$ | — | ns | |
| | Setup time for repeated START condition | t_{STAS} | 260 | — | ns | |
| | Setup time for STOP condition | t_{STOS} | 260 | — | ns | |
| | Data setup time | t_{SDAS} | 50 | — | ns | |
| | Data hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b | — | 550 | pF | |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKD cycle.

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.

Table 2.35 IIC timing (HS mode)

Conditions: VCC = 2.7 to 5.5 V

| Parameter | | Symbol | Cb = 100 pF | | Cb = 400 pF | | Unit | Test conditions |
|--------------------------|---|--------------------|--|-----------------------------|--|-----------------------------|------|-----------------|
| | | | Min*1 | Max | Min*1 | Max | | |
| IIC(HS mode) | SCL cycle time | t _{SCL} | 330 (+ 10 × t _{IICcyc}) when PCLKD = 64 MHz 390 (+ 10 × t _{IICcyc}) when PCLKD = 48 MHz | — | 500 (+ 10 × t _{IICcyc}) when PCLKD = 64 MHz *2 560 (+ 10 × t _{IICcyc}) when PCLKD = 48 MHz | — | ns | Figure 2.33 |
| | SCL high pulse width | t _{SCLH} | 125 (+ 5 × t _{IICcyc}) when PCLKD = 64 MHz 155 (+ 5 × t _{IICcyc}) when PCLKD = 48 MHz | — | 140 (+ 5 × t _{IICcyc}) when PCLKD = 64 MHz 170 (+ 5 × t _{IICcyc}) when PCLKD = 48 MHz | — | ns | |
| | SCL low pulse width | t _{SCLL} | 205 (+ 5 × t _{IICcyc}) when PCLKD = 64 MHz 230 (+ 5 × t _{IICcyc}) when PCLKD = 48 MHz | — | 320 (+ 5 × t _{IICcyc}) when PCLKD = 64 MHz 350 (+ 5 × t _{IICcyc}) when PCLKD = 48 MHz | — | ns | |
| | SCL rise time | t _{Sr} | — | 40 | — | 80 | ns | |
| | SCL rise time after a repeated START condition and after an acknowledge bit | t _{Sr} | — | 80 | — | 160 | ns | |
| | SCL fall time | t _{Sf} | — | 40 | — | 80 | ns | |
| | SDA fall time | t _{Sf} | — | 80 | — | 160 | ns | |
| | SDA fall time | t _{Sf} | — | 80 | — | 160 | ns | |
| | SCL, SDA spike pulse removal time | t _{SP} | 0 | 1 (4) × t _{IICcyc} | 0 | 1 (4) × t _{IICcyc} | ns | |
| | Hold time for START condition | t _{STA H} | t _{IICcyc} + 135 | — | t _{IICcyc} + 135 | — | ns | |
| | Setup time for repeated START condition | t _{STA S} | 160 | — | 160 | — | ns | |
| | Setup time for STOP condition | t _{STO S} | 160 | — | 160 | — | ns | |
| | Data setup time | t _{SDA S} | 10 | — | 10 | — | ns | |
| | Data hold time | t _{SDA H} | 0 | 80 | 0 | 150 | ns | |
| SCL, SDA capacitive load | C _b | — | 100 | — | 400 | pF | | |

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKD cycle.

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 1111b while the digital filter is enabled with INCTL.DNFE set to 1.

Note 2. The maximum SCL clock frequency is 1.7MHz.

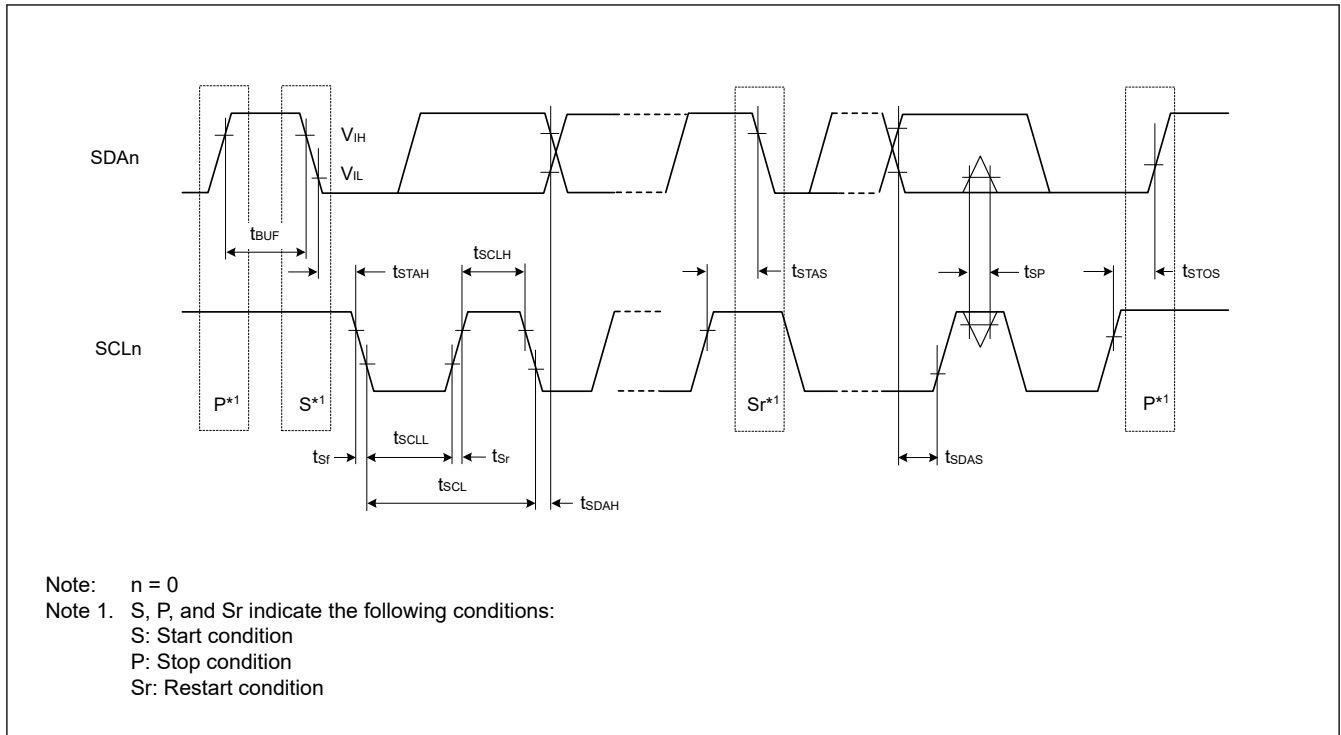


Figure 2.33 I²C bus interface input/output timing

Table 2.36 I³C timing (Open Drain Timing Parameters)

Conditions: VCC = 2.97 to 3.63 V

| Parameter | Symbol | Timing Diagram | Min | Max | Units | Notes |
|--|------------------------|----------------|---|-------------------|---------|-------|
| SCL Clock Low Period | t _{LOW_OD} | Figure 2.36 | 200 | — | ns | 1, 2 |
| | t _{DIG_OD_L} | Figure 2.36 | t _{LOW_ODmin} + t _{fDA_ODmin} | — | ns | — |
| SDA Signal Fall Time | t _{fDA_OD} | Figure 2.36 | t _{CF} | 33 | ns | — |
| SDA Data Setup Time Open Drain Mode | t _{SU_OD} | Figure 2.35 | 4 | — | ns | 1 |
| | | Figure 2.36 | | | | |
| Clock After START (S) Condition | t _{CAS} | Figure 2.36 | 38.4 | For ENTAS0: 1 μ | seconds | 5, 6 |
| | | | | For ENTAS1: 100 μ | | |
| | | | | For ENTAS2: 2 m | | |
| | | | | For ENTAS3: 50 m | | |
| Clock Before STOP (P) Condition | t _{CBP} | Figure 2.37 | t _{CASmin} | — | seconds | — |
| Current Master to Secondary Master Overlap time during handoff | t _{MMOverlap} | Figure 2.42 | t _{DIG_OD_Lmin} | — | ns | — |
| Bus Available Condition | t _{AVAIL} | — | 1 | — | μs | 7 |
| Bus Idle Condition | t _{IDLE} | — | 1 | — | ms | — |
| Time Interval Where New Master Not Driving SDA Low | t _{MMLock} | Figure 2.42 | t _{AVAILmin} | — | μs | — |

- Note:
1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}.
 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above V_{IH}.
 3. On a Legacy Bus where I²C Devices need to see Start.
 4. Slaves that do not support the optional ENTAS_x CCCs shall use the t_{CAS} Max value shown for ENTAS3
 5. On a Mixed Bus with Fm Legacy I²C Devices, t_{AVAIL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.37 I3C timing (Push-Pull Timing Parameters for SDR)

| Parameter | Symbol | Timing Diagram | Min | Max | Units | Notes |
|---|------------------------|----------------|--|--|-------|-------|
| SCL Clock Frequency | f_{SCL} | — | 0.01 | 4.6 (when PCLKD = 64 M) 3.4 (when PCLKD = 48 M) | M Hz | 1 |
| SCL Clock Low Period | t_{LOW} | Figure 2.34 | 80 (when PCLKD = 64 M) 104 (when PCLKD = 48 M) | — | ns | — |
| | t_{DIG_L} | Figure 2.34 | 88 (when PCLKD = 64 M) 112 (when PCLKD = 48 M) | — | ns | 2,4 |
| SCL Clock High Period | t_{HIGH} | Figure 2.34 | 112 (when PCLKD = 64 M) 148 (when PCLKD = 48 M) | — | ns | — |
| | t_{DIG_H} | Figure 2.34 | 120 (when PCLKD = 64 M) 156 (when PCLKD = 48 M) | — | ns | 2 |
| Clock in to Data Out for Slave | t_{SCO} | Figure 2.39 | — | 42 | ns | — |
| SCL Clock Rise Time | t_{CR} | Figure 2.34 | — | $150 * 1 / f_{SCL}$ (capped at 60) | ns | — |
| SCL Clock Fall Time | t_{CF} | Figure 2.34 | — | $150 * 1 / f_{SCL}$ (capped at 60) | ns | — |
| SDA Signal Data Hold in Push-Pull Mode | Master t_{HD_PP} | Figure 2.38 | $t_{CR} + 3$ and $t_{CF} + 3$ | — | — | 4 |
| | Slave t_{HD_PP} | Figure 2.40 | 0 | — | — | — |
| SDA Signal Data Setup in Push-Pull Mode | t_{SU_PP} | Figure 2.38 | 4 | N/A | ns | — |
| | | Figure 2.39 | | | | |
| Clock After Repeated START (Sr) | t_{CASr} | Figure 2.41 | t_{CASmin} | N/A | ns | — |
| Clock Before Repeated START (Sr) | t_{CBSr} | Figure 2.41 | t_{CASmin} | N/A | ns | — |
| Capacitive Load per Bus Line (SDA/SCL) | C_b | — | — | 50 | pF | — |

Note: 1. $f_{SCL} = 1 / (t_{DIG_L} + t_{DIG_H})$

- t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 2.34)
- As both edges are used, the hold time must be satisfied for the respective edges, for example, $t_{CF} + 3$ for falling edge clocks, and $t_{CR} + 3$ for rising edge clocks.

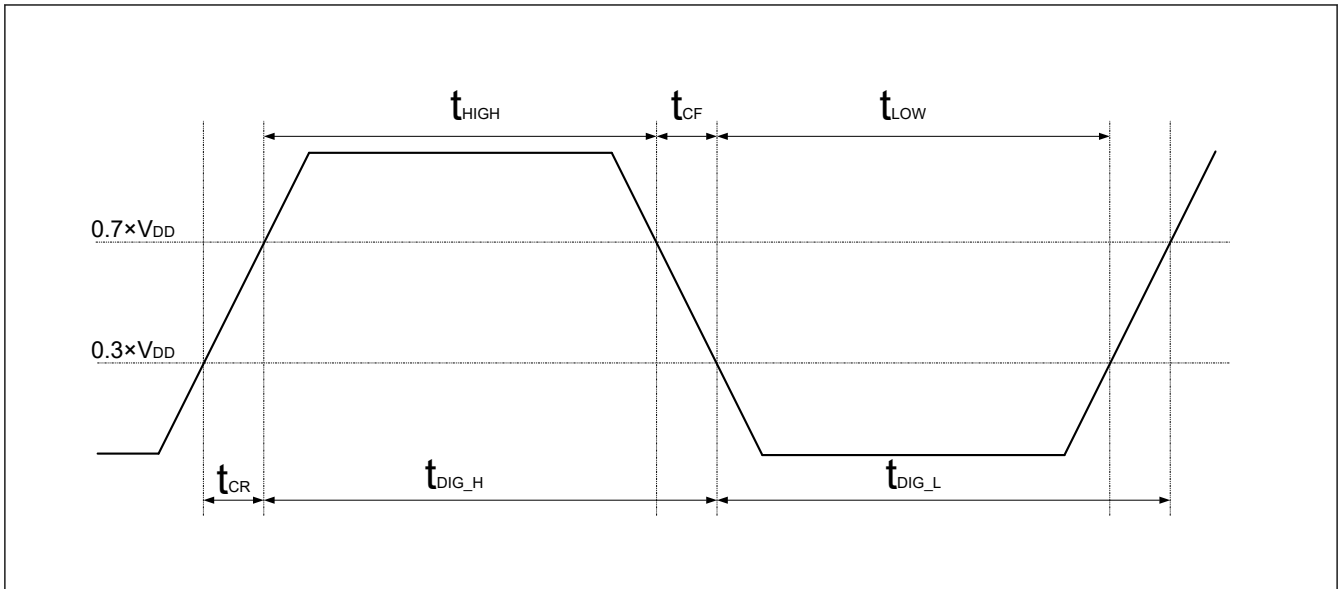


Figure 2.34 t_{DIG_H} and t_{DIG_L}

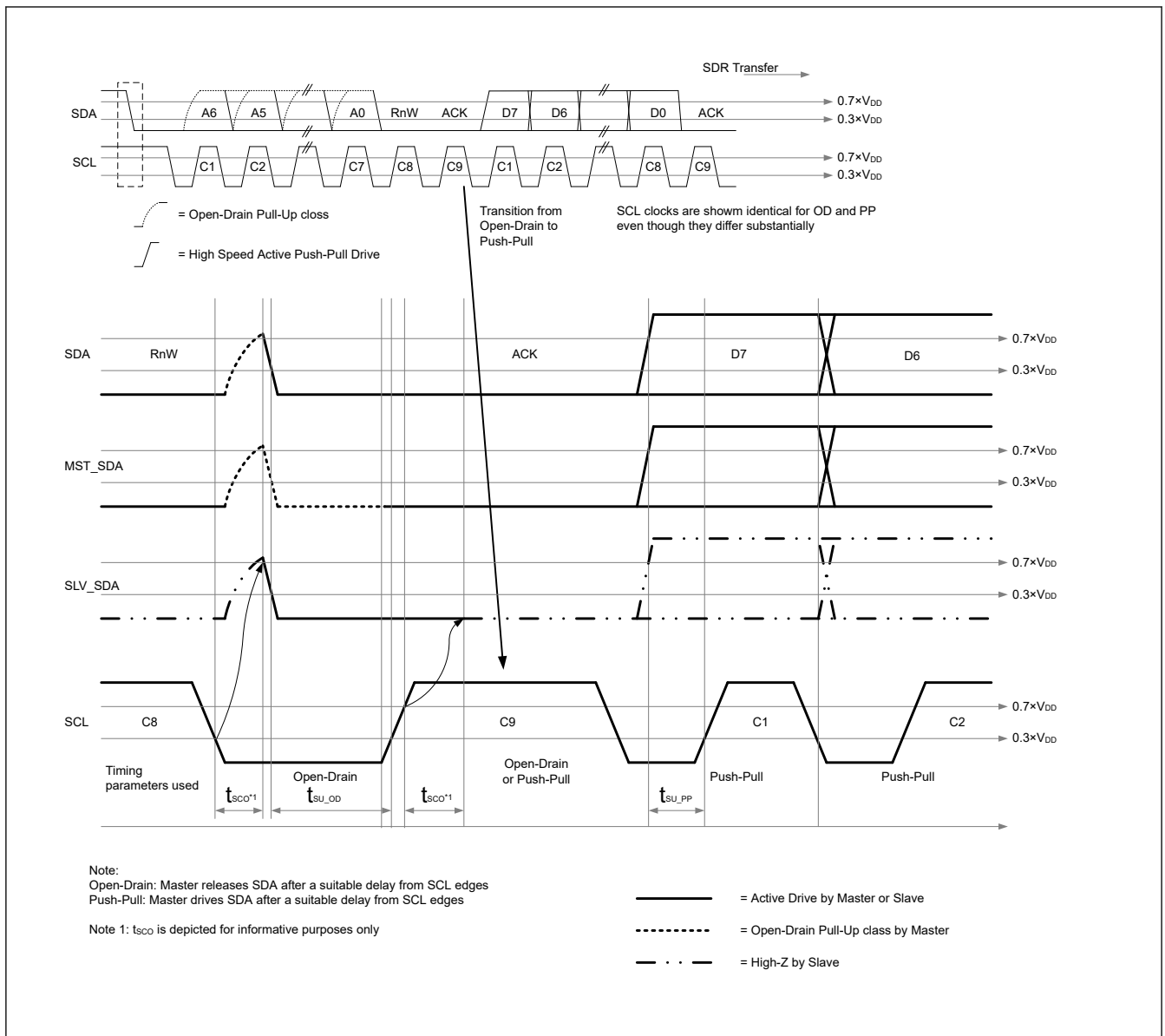


Figure 2.35 I3C Data Transfer – ACK by Slave

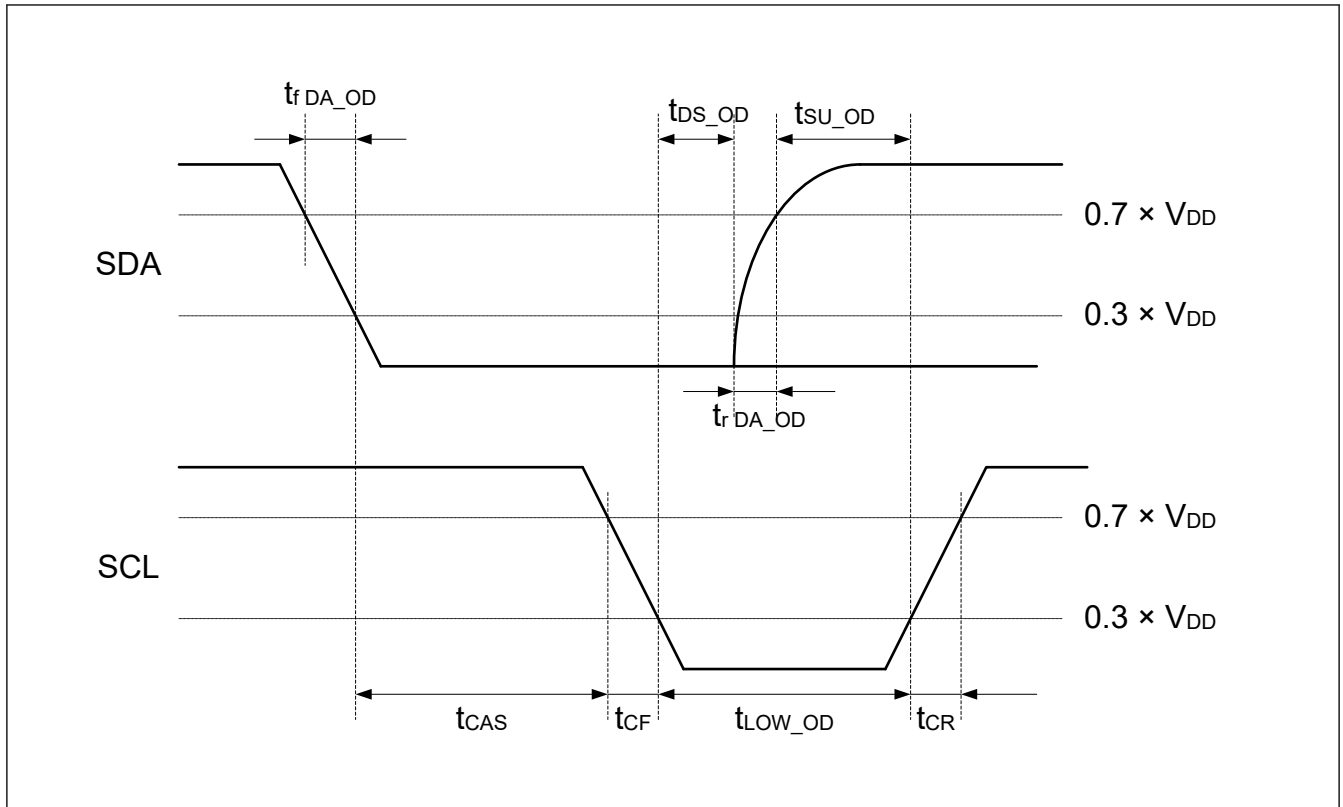


Figure 2.36 I3C START condition Timing

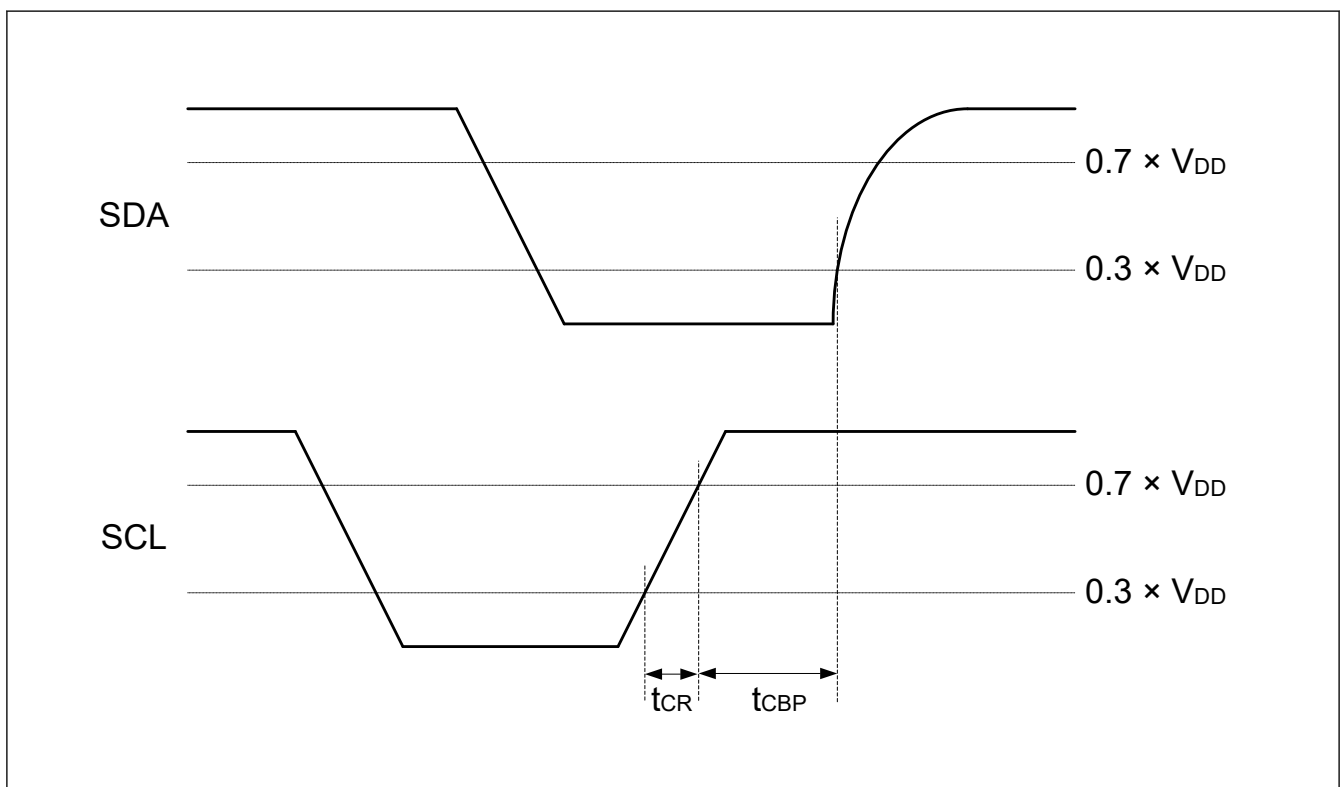


Figure 2.37 I3C STOP condition Timing

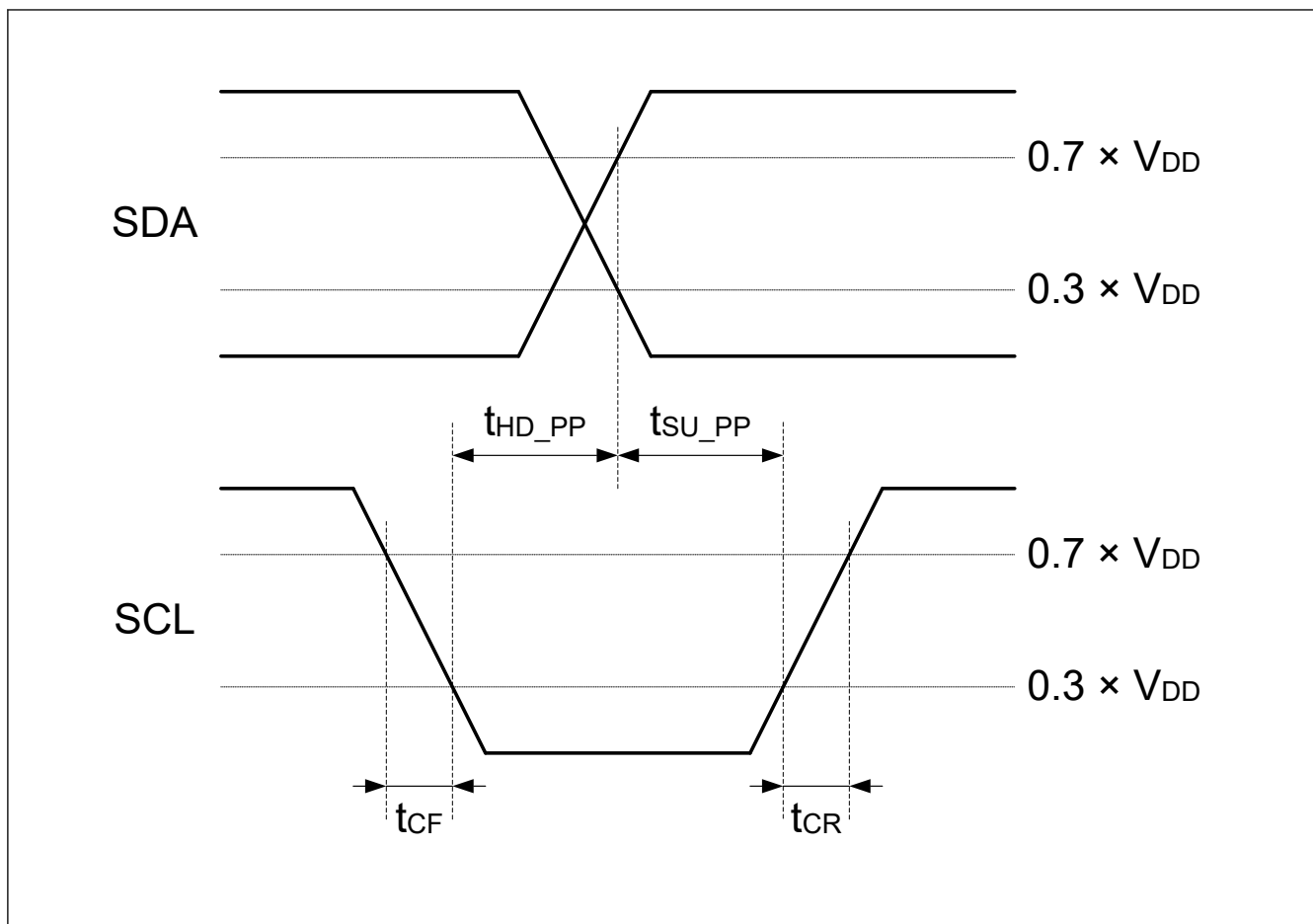


Figure 2.38 I3C Master Out Timing

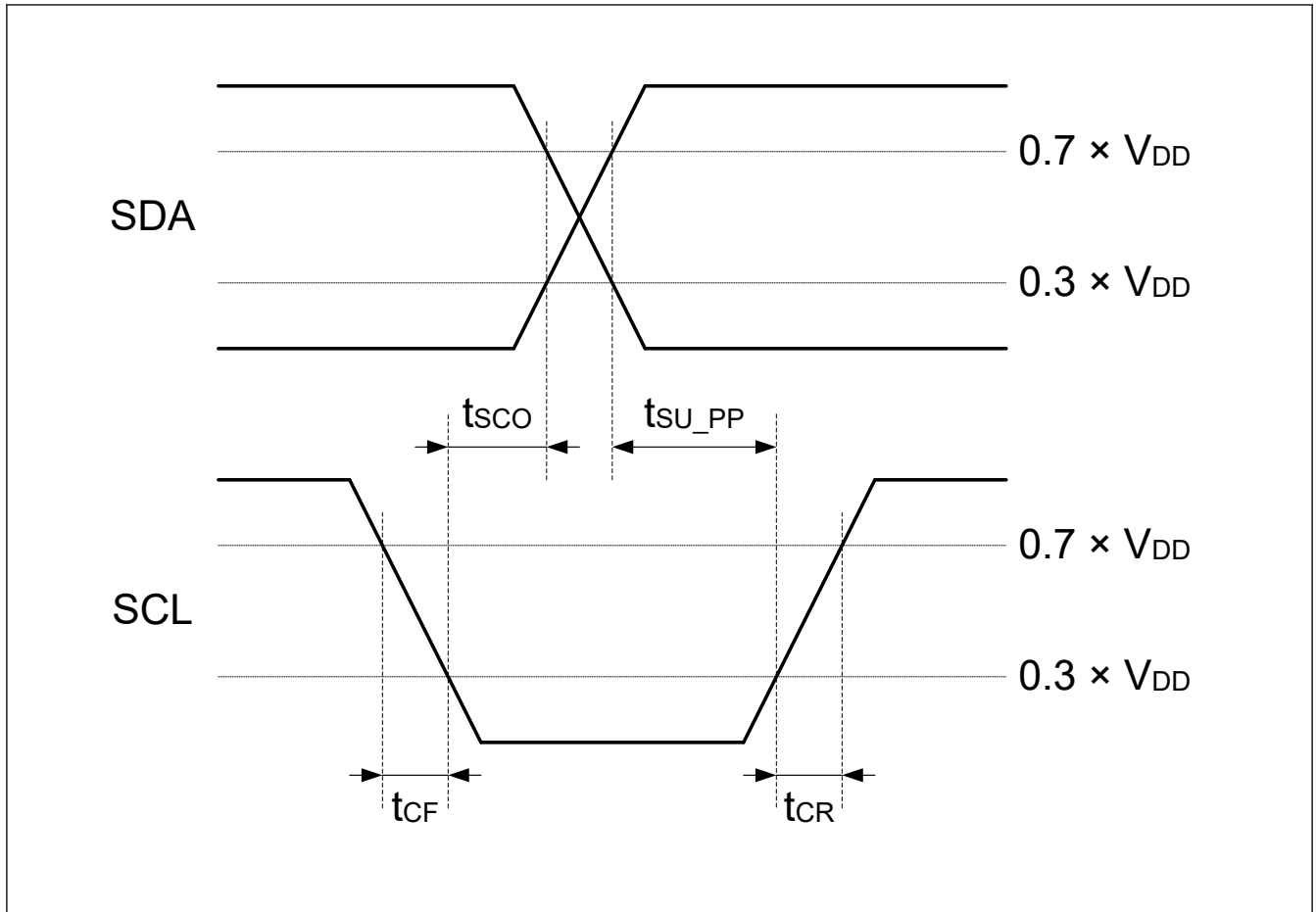


Figure 2.39 I3C Slave Out Timing

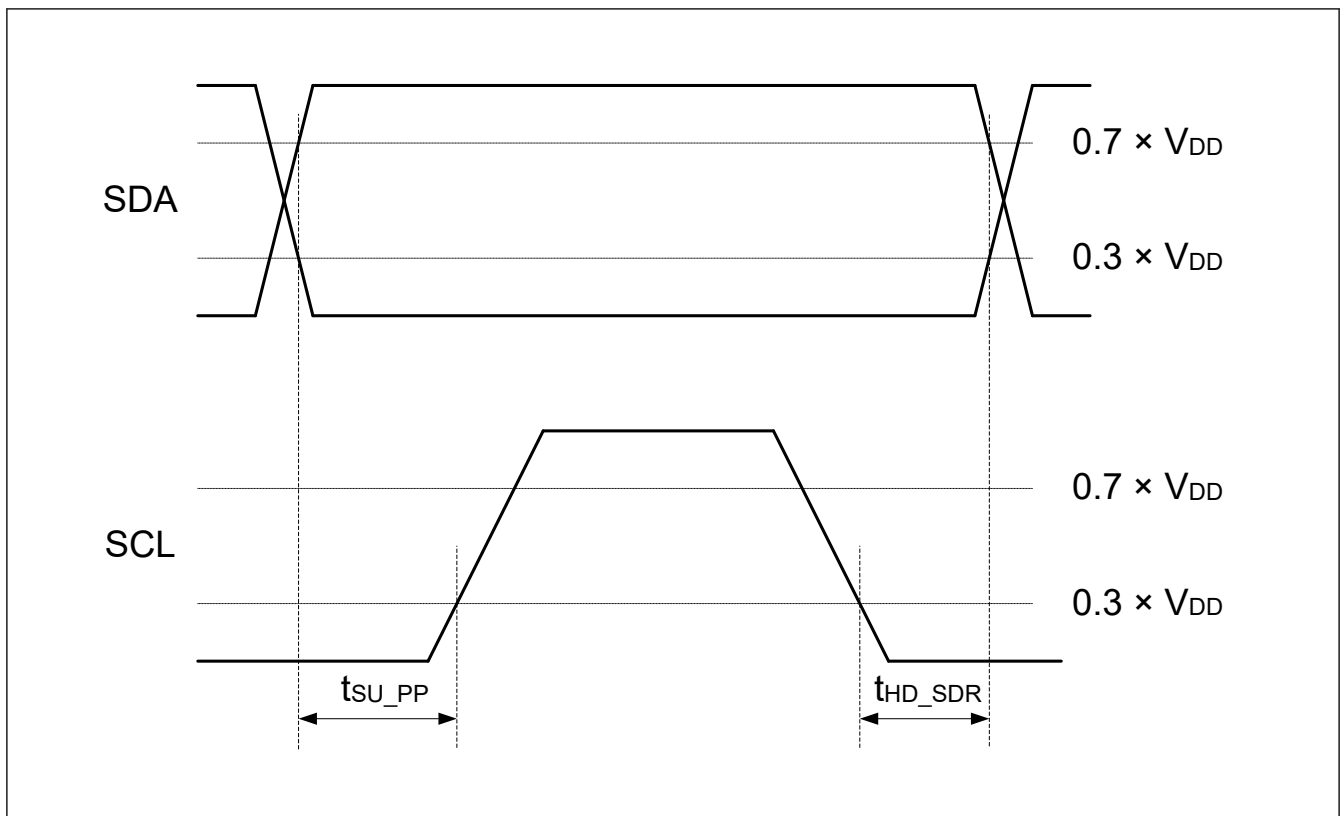


Figure 2.40 Master SDR Timing

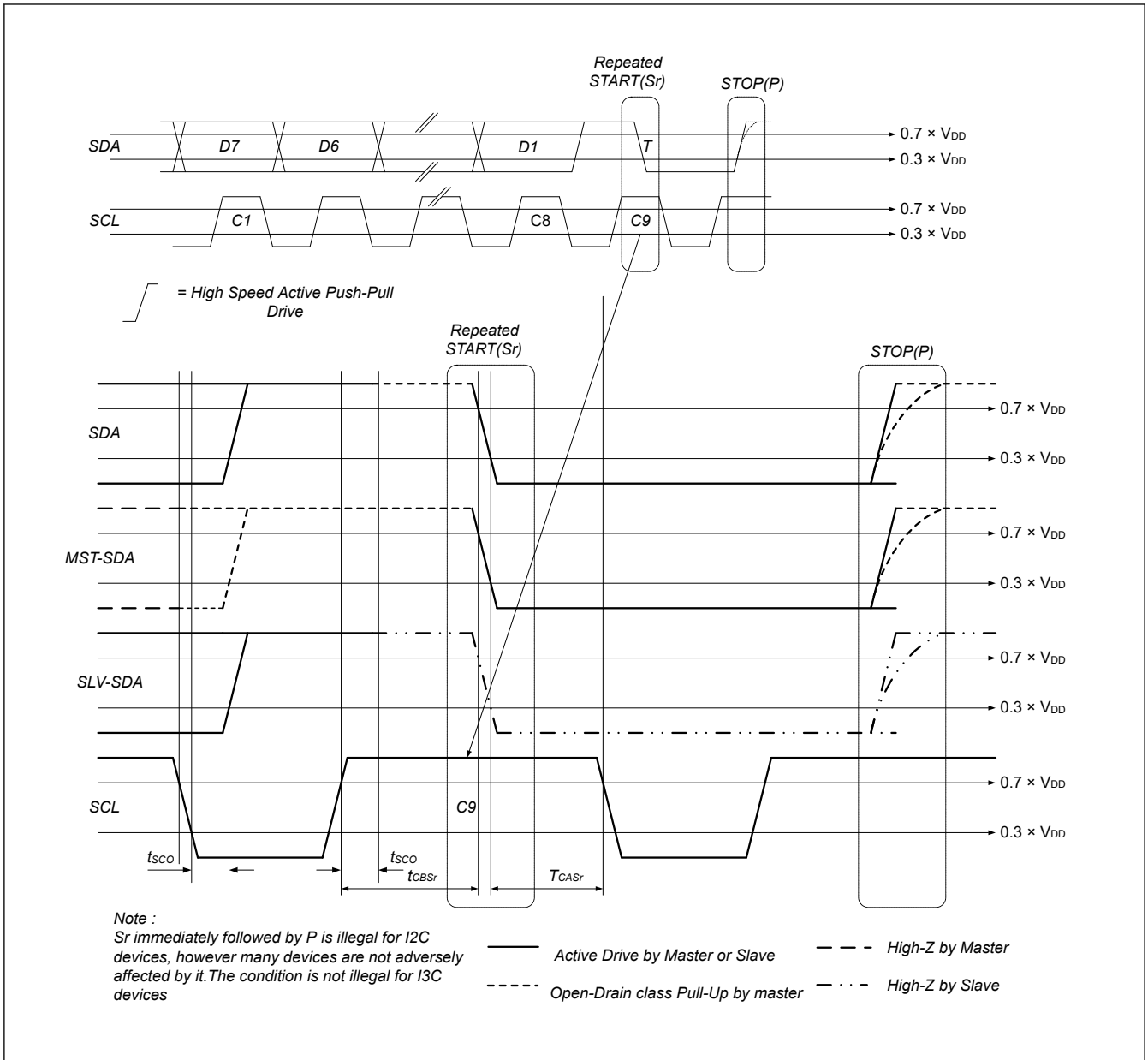


Figure 2.41 T-Bit When Master Ends Read with Repeated START and STOP

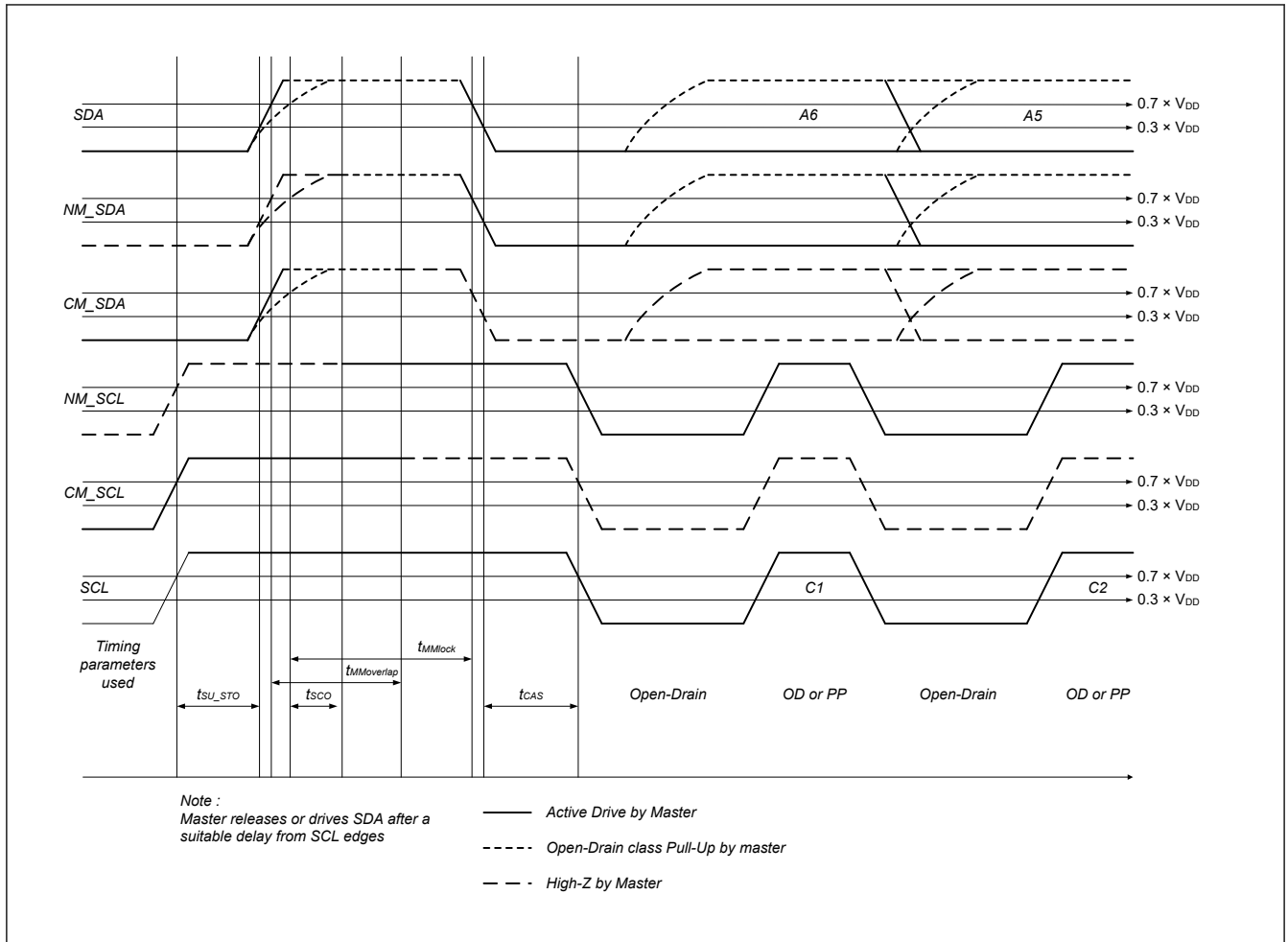


Figure 2.42 I3C Timing

2.3.11 CLKOUT Timing

Table 2.38 CLKOUT timing

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|-------------------------------|-----------|--|------|------|-----------------|-------------|
| CLKOUT pin output cycle | t_{Cyc} | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 62.5 | — | ns | Figure 2.43 |
| | | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | 125 | — | | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | 250 | — | | |
| CLKOUT pin high pulse width*1 | t_{CH} | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 15 | — | ns | |
| | | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | 30 | — | | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | 150 | — | | |
| CLKOUT pin low pulse width*1 | t_{CL} | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 15 | — | ns | |
| | | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | 30 | — | | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | 150 | — | | |
| CLKOUT pin output rise time | t_{Cr} | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | — | 12 | ns | |
| | | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | — | 25 | | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | — | 50 | | |
| CLKOUT pin output fall time | t_{Cf} | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | — | 12 | ns | |
| | | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | — | 25 | | |
| | | $1.6\text{ V} \leq V_{CC} < 1.8\text{ V}$ | — | 50 | | |

Note 1. When MOCO is selected as the clock output source (the CKOCR.CKOSSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

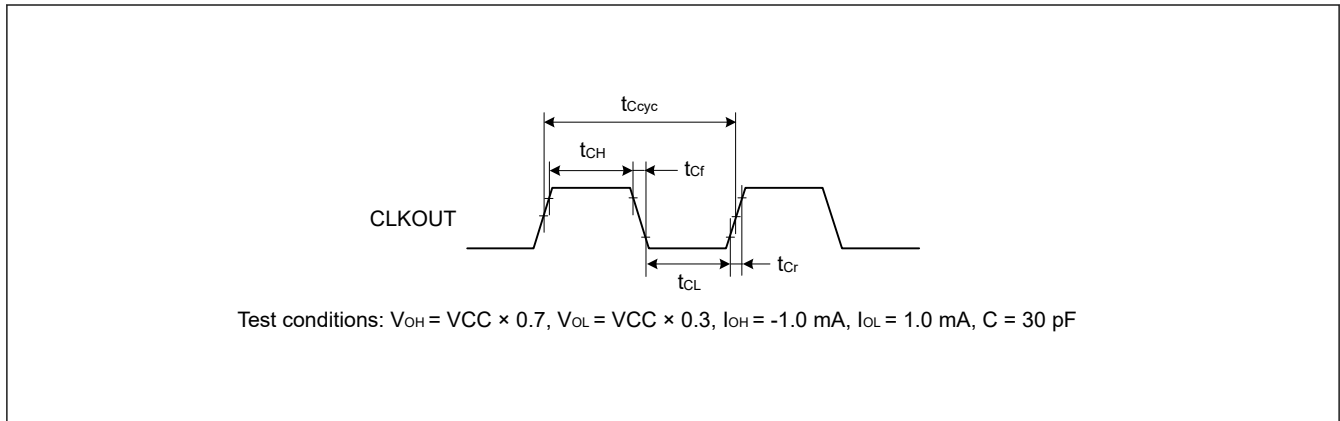


Figure 2.43 CLKOUT output timing

2.4 ADC12 Characteristics

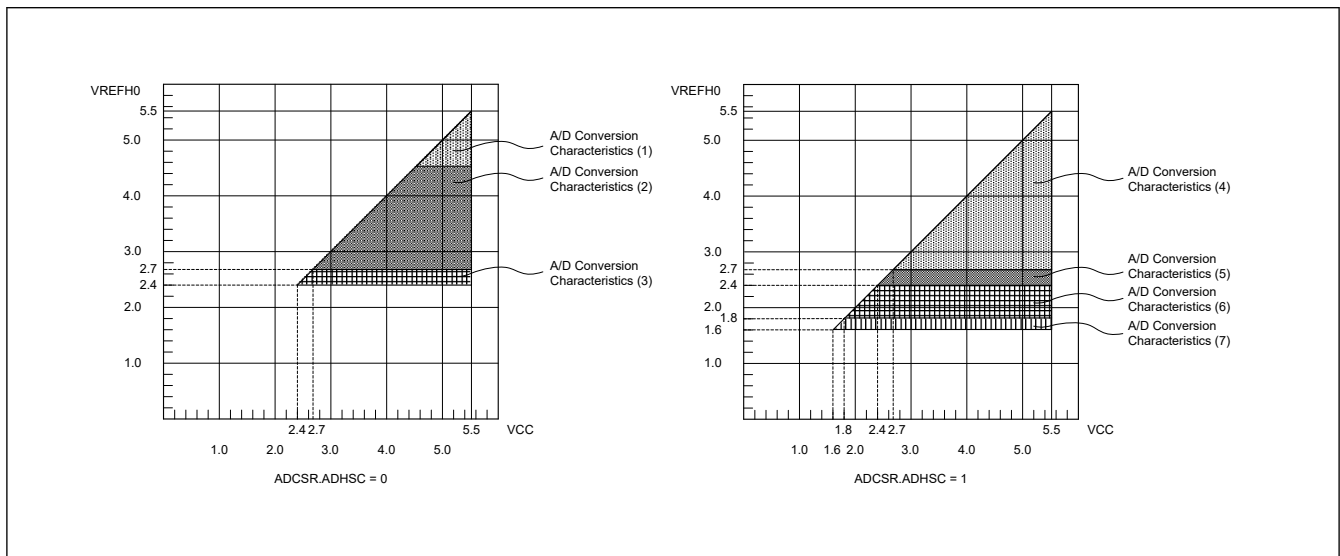


Figure 2.44 VCC to VREFH0 voltage range

Table 2.39 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: $V_{CC} = V_{REFH0} = 4.5 \text{ to } 5.5 \text{ V}^5$, $V_{SS} = V_{REFL0} = 0 \text{ V}$
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | Min | Typ | Max | Unit | Test conditions |
|----------------------------|-----|-----|------------|------------|--------------------------|
| PCLKD (ADCLK) frequency | 1 | — | 64 | MHz | ADACSR.ADSAC = 0 |
| | | | 48 | MHz | ADACSR.ADSAC = 1 |
| Analog input capacitance*2 | Cs | — | 9^{*3} | pF | High-precision channel |
| | | | 10^{*3} | pF | Normal-precision channel |
| Analog input resistance | Rs | — | 1.3^{*3} | k Ω | High-precision channel |
| | | | 5.0^{*3} | k Ω | Normal-precision channel |
| Analog input voltage range | Ain | 0 | VREFH0 | V | — |
| Resolution | — | — | 12 | Bit | — |

Table 2.39 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 4.5 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|--|--|-------------------------------|------|------|------|--|
| Conversion time* ¹ (Operation at PCLKD = 64 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.70 (0.211) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0 |
| | | 1.34 (0.852) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x36 ADACSR.ADSAC = 0 |
| Conversion time* ¹ (Operation at PCLKD = 48 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.67 (0.219) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 1.29 (0.844) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1 |
| Offset error | | — | ±1.0 | ±5 | LSB | High-precision channel |
| | | | | ±6 | LSB | Other than specified |
| Full-scale error | | — | ±1.0 | ±5 | LSB | High-precision channel |
| | | | | ±6 | LSB | Other than specified |
| Quantization error | | — | ±0.5 | — | LSB | — |
| Absolute accuracy | | — | ±2.5 | ±5.5 | LSB | High-precision channel |
| | | | | ±8.5 | LSB | Other than specified |
| DNL differential nonlinearity error | | — | ±1.0 | — | LSB | — |
| INL integral nonlinearity error | | — | ±1.5 | ±3.0 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).

Note 3. Reference data.

Note 4. () lists sampling time.

Note 5. When VREFH0 < VCC, the MAX. values are as follows.

Absolute accuracy/Offset error/Full-scale error:

For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.

INL integral non-linearity error:

For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.40 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|--|-----------------|-----|-----|-------------------|------|--------------------------|
| PCLKD (ADCLK) frequency | | 1 | — | 48 | MHz | — |
| Analog input capacitance* ² | Cs | — | — | 9 ^{*3} | pF | High-precision channel |
| | | — | — | 10 ^{*3} | pF | Normal-precision channel |
| Analog input resistance | Rs | — | — | 1.9 ^{*3} | kΩ | High-precision channel |
| | | — | — | 6.0 ^{*3} | kΩ | Normal-precision channel |
| Analog input voltage range | A _{in} | 0 | — | VREFH0 | V | — |
| Resolution | | — | — | 12 | Bit | — |

Table 2.40 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|--|--|-------------------------------|------|------|------|--|
| Conversion time ^{*1} (Operation at PCLKD = 48 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.67 (0.219) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 1.29 (0.844) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1 |
| Offset error | | — | ±1.0 | ±6.5 | LSB | High-precision channel |
| | | | | ±8 | LSB | Other than specified |
| Full-scale error | | — | ±1.0 | ±6.5 | LSB | High-precision channel |
| | | | | ±8 | LSB | Other than specified |
| Quantization error | | — | ±0.5 | — | LSB | — |
| Absolute accuracy | | — | ±2.5 | ±7 | LSB | High-precision channel |
| | | | | ±10 | LSB | Other than specified |
| DNL differential nonlinearity error | | — | ±1.0 | — | LSB | — |
| INL integral nonlinearity error | | — | ±1.5 | ±3.0 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).

Note 3. Reference data.

Note 4. () lists sampling time.

Note 5. When VREFH0 < VCC, the MAX. values are as follows.

Absolute accuracy/Offset error/Full-scale error:

For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.

INL integral non-linearity error:

For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.41 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|--|--|-------------------------------|-----|-------------------|------|--|
| PCLKD (ADCLK) frequency | | 1 | — | 32 | MHz | — |
| Analog input capacitance ^{*2} | Cs | — | — | 9 ^{*3} | pF | High-precision channel |
| | | — | — | 10 ^{*3} | pF | Normal-precision channel |
| Analog input resistance | Rs | — | — | 2.2 ^{*3} | kΩ | High-precision channel |
| | | — | — | 7.0 ^{*3} | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | — | VREFH0 | V | — |
| Resolution | | — | — | 12 | Bit | — |
| Conversion time ^{*1} (Operation at PCLKD = 32 MHz) | Permissible signal source impedance Max. = 1.3 kΩ | 1.00 (0.328) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 1.94 (1.266) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1 |

Table 2.41 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.4 to 5.5 V⁵, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | Min | | Max | Unit | Test conditions |
|-------------------------------------|-----|-------|------|------|------------------------|
| Offset error | — | ±1.0 | ±6.5 | LSB | High-precision channel |
| | | | ±8 | LSB | Other than specified |
| Full-scale error | — | ±1.0 | ±6.5 | LSB | High-precision channel |
| | | | ±8 | LSB | Other than specified |
| Quantization error | — | ±0.5 | — | LSB | — |
| Absolute accuracy | — | ±2.50 | ±7 | LSB | High-precision channel |
| | | | ±10 | LSB | Other than specified |
| DNL differential nonlinearity error | — | ±1.0 | — | LSB | — |
| INL integral nonlinearity error | — | ±1.5 | ±3.0 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).

Note 3. Reference data.

Note 4. () lists sampling time.

Note 5. When VREFH0 < VCC, the MAX. values are as follows.

Absolute accuracy/Offset error/Full-scale error:

For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.

INL integral non-linearity error:

For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.42 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V⁵, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | Min | Typ | Max | Unit | Test conditions | |
|--|--|----------------|--------|------|--------------------------|--|
| PCLKD (ADCLK) frequency | 1 | — | 24 | MHz | — | |
| Analog input capacitance*2 | Cs | — | 9*3 | pF | High-precision channel | |
| | | | 10*3 | pF | Normal-precision channel | |
| Analog input resistance | Rs | — | 1.9*3 | kΩ | High-precision channel | |
| | | | 6*3 | kΩ | Normal-precision channel | |
| Analog input voltage range | Ain | 0 | VREFH0 | V | — | |
| Resolution | — | — | 12 | Bit | — | |
| Conversion time*1 (Operation at PCLKD = 24 MHz) | Permissible signal source impedance Max. = 1.1 kΩ | 1.58 (0.438)*4 | — | — | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 2.0 (0.854)*4 | — | — | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1 |
| Offset error | — | ±1.25 | ±7 | LSB | High-precision channel | |
| | | | ±8.5 | LSB | Other than specified | |
| Full-scale error | — | ±1.25 | ±7 | LSB | High-precision channel | |
| | | | ±8.5 | LSB | Other than specified | |
| Quantization error | — | ±0.5 | — | LSB | — | |

Table 2.42 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = VREFH0 = 2.7 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | Min | Typ | Max | Unit | Test conditions |
|-------------------------------------|-----|-------|------|------|------------------------|
| Absolute accuracy | — | ±3.25 | ±8 | LSB | High-precision channel |
| | | | ±11 | LSB | Other than specified |
| DNL differential nonlinearity error | — | ±1.5 | — | LSB | — |
| INL integral nonlinearity error | — | ±1.75 | ±4.0 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).

Note 3. Reference data.

Note 4. () lists sampling time.

Note 5. When VREFH0 < VCC, the MAX. values are as follows.

Absolute accuracy/Offset error/Full-scale error:

For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.

INL integral non-linearity error:

For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.43 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 2.4 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | Min | Typ | Max | Unit | Test conditions | |
|--|--|-------------------|--------|------|--------------------------|--|
| PCLKD (ADCLK) frequency | 1 | — | 16 | MHz | — | |
| Analog input capacitance*2 | Cs | — | g*3 | pF | High-precision channel | |
| | | | 10*3 | pF | Normal-precision channel | |
| Analog input resistance | Rs | — | 2.2*3 | kΩ | High-precision channel | |
| | | | 7*3 | kΩ | Normal-precision channel | |
| Analog input voltage range | Ain | 0 | VREFH0 | V | — | |
| Resolution | — | — | 12 | Bit | — | |
| Conversion time*1 (Operation at PCLKD = 16 MHz) | Permissible signal source impedance Max. = 2.2 kΩ | 2.38 (0.656)*4 | — | — | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 3.0 (1.281)*4 | — | — | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1 |
| Offset error | — | ±1.25 | ±7 | LSB | High-precision channel | |
| | | | ±8.5 | LSB | Other than specified | |
| Full-scale error | — | ±1.25 | ±7 | LSB | High-precision channel | |
| | | | ±8.5 | LSB | Other than specified | |
| Quantization error | — | ±0.5 | — | LSB | — | |
| Absolute accuracy | — | ±3.25 | ±8 | LSB | High-precision channel | |
| | | | ±11 | LSB | Other than specified | |
| DNL differential nonlinearity error | — | ±1.5 | — | LSB | — | |
| INL integral nonlinearity error | — | ±1.75 | ±4.0 | LSB | — | |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

- Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
- Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).
- Note 3. Reference data.
- Note 4. () lists sampling time.
- Note 5. When VREFH0 < VCC, the MAX. values are as follows.
 Absolute accuracy/Offset error/Full-scale error:
 For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
 INL integral non-linearity error:
 For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.44 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 1.8 to 5.5 V⁵, VSS = VREFL0 = 0 V
 Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|--|-------------------------------|-------|------------------|------|--|
| PCLKD (ADCLK) frequency | | 1 | — | 8 | MHz | — |
| Analog input capacitance ^{*2} | Cs | — | — | 9 ^{*3} | pF | High-precision channel |
| | | — | — | 10 ^{*3} | pF | Normal-precision channel |
| Analog input resistance | Rs | — | — | 6 ^{*3} | kΩ | High-precision channel |
| | | — | — | 14 ^{*3} | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | — | VREFH0 | V | — |
| Resolution | | — | — | 12 | Bit | — |
| Conversion time ^{*1} (Operation at PCLKD = 8 MHz) | Permissible signal source impedance Max. = 5 kΩ | 4.75 (1.313) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 6.0 (2.563) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1 |
| Offset error | | — | ±1.25 | ±8.5 | LSB | High-precision channel |
| | | | | ±11 | LSB | Other than specified |
| Full-scale error | | — | ±1.5 | ±8.5 | LSB | High-precision channel |
| | | | | ±11 | LSB | Other than specified |
| Quantization error | | — | ±0.5 | — | LSB | — |
| Absolute accuracy | | — | ±3.75 | ±10.5 | LSB | High-precision channel |
| | | | | ±14.5 | LSB | Other than specified |
| DNL differential nonlinearity error | | — | ±2.0 | — | LSB | — |
| INL integral nonlinearity error | | — | ±2.25 | ±4.5 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

- Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
- Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).
- Note 3. Reference data.
- Note 4. () lists sampling time.
- Note 5. When VREFH0 < VCC, the MAX. values are as follows.
 Absolute accuracy/Offset error/Full-scale error:
 For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
 INL integral non-linearity error:
 For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.45 A/D conversion characteristics (7) in low-power A/D conversion mode

Conditions: VCC = VREFH0 = 1.6 to 5.5 V^{*5}, VSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|--|----------------------------|-------|------------------|------|--|
| PCLKD (ADCLK) frequency | | 1 | — | 4 | MHz | — |
| Analog input capacitance ^{*2} | Cs | — | — | 9 ^{*3} | pF | High-precision channel |
| | | — | — | 10 ^{*3} | pF | Normal-precision channel |
| Analog input resistance | Rs | — | — | 12 ^{*3} | kΩ | High-precision channel |
| | | — | — | 28 ^{*3} | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | — | VREFH0 | V | — |
| Resolution | | — | — | 12 | Bit | — |
| Conversion time ^{*1} (Operation at PCLKD = 4 MHz) | Permissible signal source impedance Max. = 9.9 kΩ | 9.5 (2.625) ^{*4} | — | — | μs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1 |
| | | 12.0 (5.125) ^{*4} | — | — | μs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1 |
| Offset error | | — | ±1.25 | ±8.5 | LSB | High-precision channel |
| | | | | ±11 | LSB | Other than specified |
| Full-scale error | | — | ±1.5 | ±8.5 | LSB | High-precision channel |
| | | | | ±11 | LSB | Other than specified |
| Quantization error | | — | ±0.5 | — | LSB | — |
| Absolute accuracy | | — | ±3.75 | ±10.5 | LSB | High-precision channel |
| | | | | ±14.5 | LSB | Other than specified |
| DNL differential nonlinearity error | | — | ±2.0 | — | LSB | — |
| INL integral nonlinearity error | | — | ±2.25 | ±4.5 | LSB | — |

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4. I/O VOH, VOL, and Other Characteristics](#).

Note 3. Reference data.

Note 4. () lists sampling time.

Note 5. When VREFH0 < VCC, the MAX. values are as follows.

Absolute accuracy/Offset error/Full-scale error:

For voltage difference between VCC and VREFH0, it should be added ±0.75 LSB/V to the Max spec.

INL integral non-linearity error:

For voltage difference between VCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.45 shows the equivalent circuit for analog input.

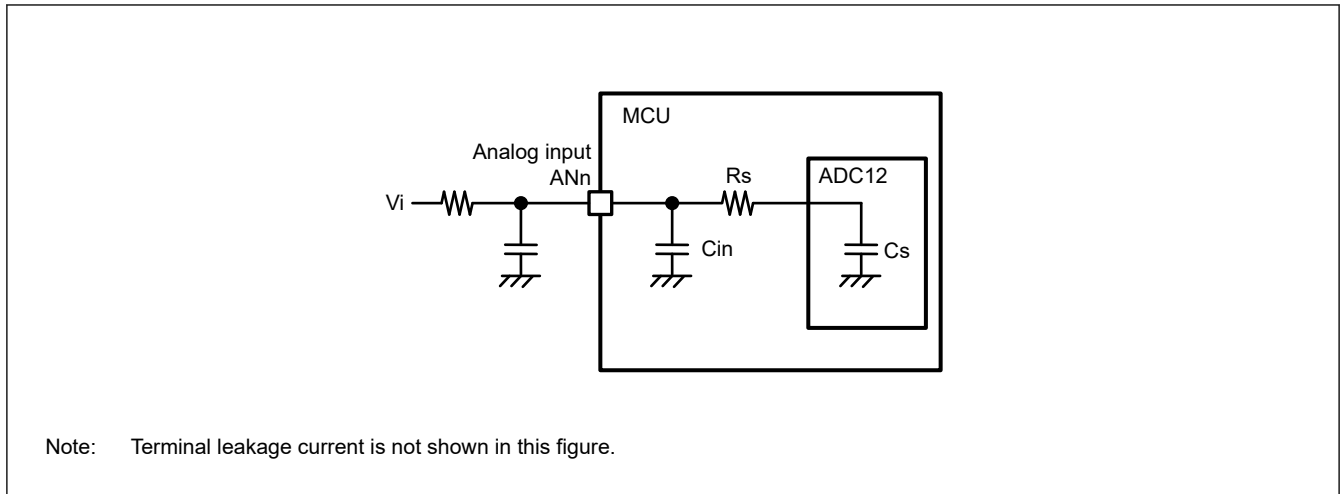


Figure 2.45 Equivalent circuit for analog input

Table 2.46 12-bit A/D converter channel classification

| Classification | Channel | Conditions | Remarks |
|--|----------------------------|--------------------|---|
| High-precision channel | AN005, AN006, AN009, AN010 | VCC = 1.6 to 5.5 V | Pins AN005, AN006, AN009, AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use. |
| Normal-precision channel | AN019 to AN022 | | |
| Internal reference voltage input channel | Internal reference voltage | VCC = 1.8 to 5.5 V | — |
| Temperature sensor input channel | Temperature sensor output | VCC = 1.8 to 5.5 V | — |

Table 2.47 A/D internal reference voltage characteristics

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*1

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--|------|------|------|------|-----------------|
| Internal reference voltage input channel*2 | 1.42 | 1.48 | 1.54 | V | — |
| PCLKD (ADCLK) frequency*3 | 1 | — | 2 | MHz | — |
| Sampling time*4 | 5.0 | — | — | μs | — |

Note 1. The internal reference voltage cannot be selected for input channels when VCC < 1.8 V.

Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.

Note 3. When the internal reference voltage is selected as the high-potential reference voltage.

Note 4. When the internal reference voltage is converted.

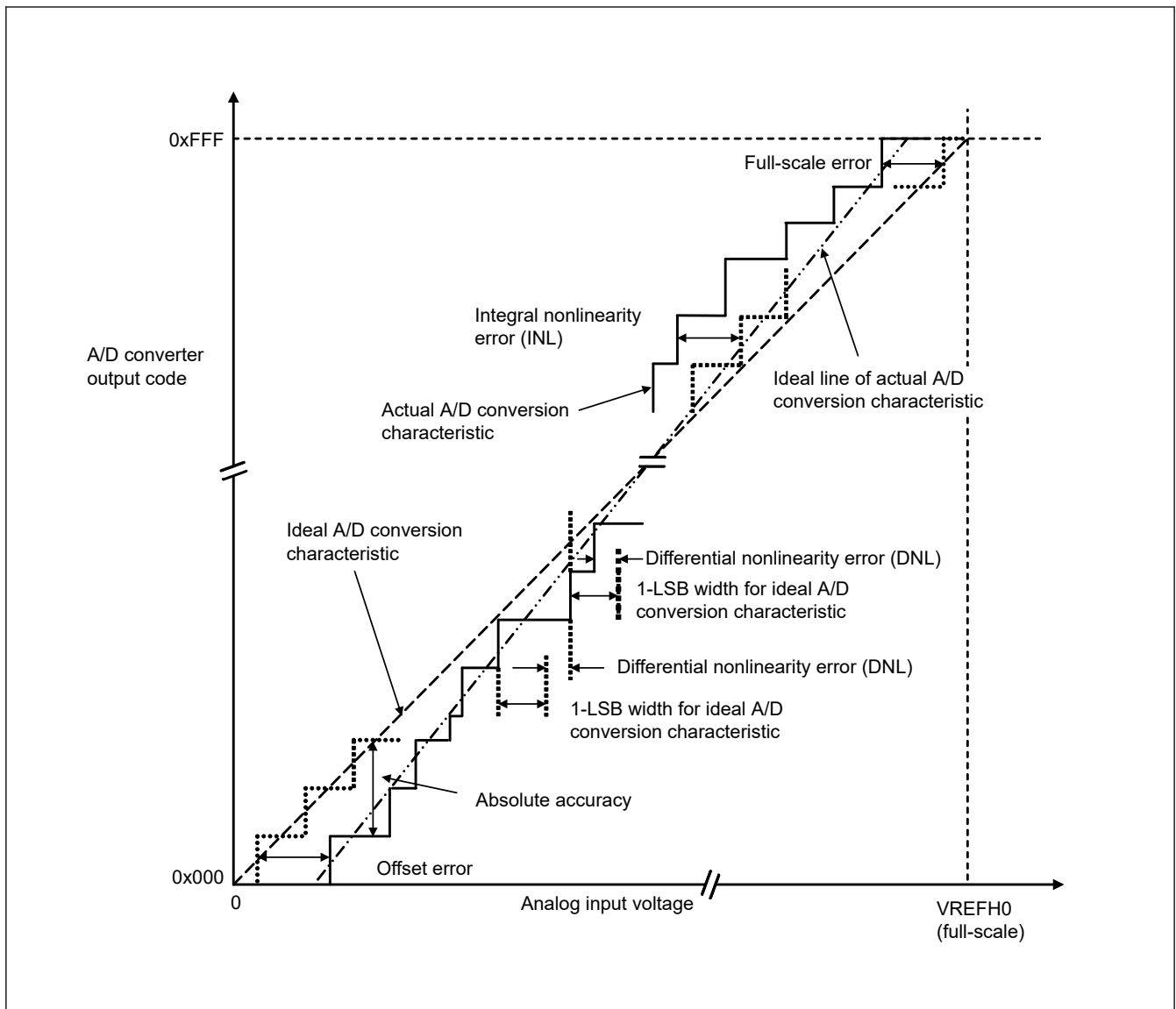


Figure 2.46 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072\text{ V}$, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ± 5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 TSN Characteristics**Table 2.48 TSN characteristics**

Conditions: VCC = 1.8 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|-------------------------------|--------------------|-----|-------|-----|-------|-----------------|
| Relative accuracy | — | — | ± 1.5 | — | °C | 2.4 V or above |
| | | — | ± 2.0 | — | °C | Below 2.4 V |
| Temperature slope | — | — | -3.3 | — | mV/°C | — |
| Output voltage (at 25°C) | — | — | 1.05 | — | V | VCC = 3.3 V |
| Temperature sensor start time | t _{START} | — | — | 5 | μs | — |
| Sampling time | — | 5 | — | — | μs | |

2.6 POR and LVD Characteristics**Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---------------------------|------------------------------------|------------------------|------------------------|------------------------|------|------|------|---|
| Voltage detection level*1 | Power-on reset (POR) | When power supply rise | V _{POR} | 1.47 | 1.51 | 1.55 | V | Figure 2.47 |
| | | When power supply fall | V _{PDR} | 1.46 | 1.50 | 1.54 | | Figure 2.48 |
| | Voltage detection circuit (LVD0)*2 | When power supply rise | V _{det0_0} | 3.74 | 3.91 | 4.06 | V | Figure 2.49 At falling edge VCC |
| | | | When power supply fall | | 3.68 | 3.85 | | |
| | | When power supply rise | V _{det0_1} | 2.73 | 2.9 | 3.01 | | |
| | | | | When power supply fall | 2.68 | 2.85 | | |
| | | When power supply rise | V _{det0_2} | 2.44 | 2.59 | 2.70 | | |
| | | | | When power supply fall | 2.38 | 2.53 | | |
| | | When power supply rise | V _{det0_3} | 1.83 | 1.95 | 2.07 | | |
| | | | | When power supply fall | 1.78 | 1.90 | | |
| | | When power supply rise | V _{det0_4} | 1.66 | 1.75 | 1.88 | | |
| | | | | When power supply fall | 1.60 | 1.69 | | |

Table 2.49 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|---------------------------|------------------------------------|------------------------|---------------------|------|------|------|-----------------|---------------------------------------|
| Voltage detection level*1 | Voltage detection circuit (LVD1)*3 | When power supply rise | V _{det1_0} | 4.23 | 4.39 | 4.55 | V | Figure 2.50 At falling edge VCC |
| | | When power supply fall | | 4.13 | 4.29 | 4.45 | | |
| | | When power supply rise | V _{det1_1} | 4.07 | 4.25 | 4.39 | | |
| | | When power supply fall | | 3.98 | 4.16 | 4.30 | | |
| | | When power supply rise | V _{det1_2} | 3.97 | 4.14 | 4.29 | | |
| | | When power supply fall | | 3.86 | 4.03 | 4.18 | | |
| | | When power supply rise | V _{det1_3} | 3.74 | 3.92 | 4.06 | | |
| | | When power supply fall | | 3.68 | 3.86 | 4.00 | | |
| | | When power supply rise | V _{det1_4} | 3.05 | 3.17 | 3.29 | | |
| | | When power supply fall | | 2.98 | 3.10 | 3.22 | | |
| | | When power supply rise | V _{det1_5} | 2.95 | 3.06 | 3.17 | | |
| | | When power supply fall | | 2.89 | 3.00 | 3.11 | | |
| | | When power supply rise | V _{det1_6} | 2.86 | 2.97 | 3.08 | | |
| | | When power supply fall | | 2.79 | 2.90 | 3.01 | | |
| | | When power supply rise | V _{det1_7} | 2.74 | 2.85 | 2.96 | | |
| | | When power supply fall | | 2.68 | 2.79 | 2.90 | | |
| Voltage detection level*1 | Voltage detection circuit (LVD1)*3 | When power supply rise | V _{det1_8} | 2.63 | 2.75 | 2.85 | V | Figure 2.50 At falling edge VCC |
| | | When power supply fall | | 2.58 | 2.68 | 2.78 | | |
| | | When power supply rise | V _{det1_9} | 2.54 | 2.64 | 2.75 | | |
| | | When power supply fall | | 2.48 | 2.58 | 2.68 | | |
| | | When power supply rise | V _{det1_A} | 2.43 | 2.53 | 2.63 | | |
| | | When power supply fall | | 2.38 | 2.48 | 2.58 | | |
| | | When power supply rise | V _{det1_B} | 2.16 | 2.26 | 2.36 | | |
| | | When power supply fall | | 2.10 | 2.20 | 2.30 | | |
| | | When power supply rise | V _{det1_C} | 1.88 | 2 | 2.09 | | |
| | | When power supply fall | | 1.84 | 1.96 | 2.05 | | |
| | | When power supply rise | V _{det1_D} | 1.78 | 1.9 | 1.99 | | |
| | | When power supply fall | | 1.74 | 1.86 | 1.95 | | |
| | | When power supply rise | V _{det1_E} | 1.67 | 1.79 | 1.88 | | |
| | | When power supply fall | | 1.63 | 1.75 | 1.84 | | |
| | | When power supply rise | V _{det1_F} | 1.65 | 1.7 | 1.78 | | |
| | | When power supply fall | | 1.60 | 1.65 | 1.73 | | |
| Voltage detection level*1 | Voltage detection circuit (LVD2)*4 | When power supply rise | V _{det2_0} | 4.20 | 4.40 | 4.57 | V | Figure 2.51 At falling edge VCC |
| | | When power supply fall | | 4.11 | 4.31 | 4.48 | | |
| | | When power supply rise | V _{det2_1} | 4.05 | 4.25 | 4.42 | | |
| | | When power supply fall | | 3.97 | 4.17 | 4.34 | | |
| | | When power supply rise | V _{det2_2} | 3.91 | 4.11 | 4.28 | | |
| | | When power supply fall | | 3.83 | 4.03 | 4.20 | | |
| | | When power supply rise | V _{det2_3} | 3.71 | 3.91 | 4.08 | | |
| | | When power supply fall | | 3.64 | 3.84 | 4.01 | | |

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0_#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol $V_{det1_#}$ denotes the value of the LVDLVLRLVD1LVL[4:0] bits.

Note 4. # in the symbol $V_{det2_#}$ denotes the value of the LVDLVLRLVD2LVL[2:0] bits.

Table 2.50 Power-on reset circuit and voltage detection circuit characteristics (2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|--|-----------------------------|----------------|-----|------|------|---|-----------------------------------|
| Wait time after power-on reset cancellation | LVD0: enable | t_{POR} | — | 4.3 | — | ms | — |
| | LVD0: disable | t_{POR} | — | 3.7 | — | ms | — |
| Wait time after voltage monitor 0, 1, 2 reset cancellation | LVD0: enable* ¹ | $t_{LVD0,1,2}$ | — | 1.4 | — | ms | — |
| | LVD0: disable* ² | $t_{LVD1,2}$ | — | 0.7 | — | ms | — |
| Power-on reset response delay time* ³ | t_{det} | — | — | 500 | — | μ s | Figure 2.47, Figure 2.48 |
| LVD0 response delay time* ³ | t_{det} | — | — | 500 | — | μ s | Figure 2.49 |
| LVD1 response delay time* ³ | t_{det} | — | — | 350 | — | μ s | Figure 2.50 |
| LVD2 response delay time* ³ | t_{det} | — | — | 600 | — | μ s | Figure 2.51 |
| Minimum VCC down time | $t_{V_{OFF}}$ | 500 | — | — | — | μ s | Figure 2.47, VCC = 1.0 V or above |
| Power-on reset enable time | t_W (POR) | 1 | — | — | — | ms | Figure 2.48, VCC = below 1.0 V |
| LVD1 operation stabilization time (after LVD1 is enabled) | T_d (E-A) | — | — | 300 | — | μ s | Figure 2.50 |
| LVD2 operation stabilization time (after LVD2 is enabled) | T_d (E-A) | — | — | 1200 | — | μ s | Figure 2.51 |
| Hysteresis width (POR) | V_{PORH} | — | 10 | — | — | mV | — |
| Hysteresis width (LVD0, LVD1 and LVD2) | V_{LVH} | — | 60 | — | mV | LVD0 selected | |
| | | — | 110 | — | | V_{det1_0} to V_{det1_2} selected | |
| | | — | 70 | — | | V_{det1_3} to V_{det1_9} selected | |
| | | — | 60 | — | | V_{det1_A} to V_{det1_B} selected | |
| | | — | 50 | — | | V_{det1_C} to V_{det1_F} selected | |
| | | — | 90 | — | | LVD2 selected | |

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

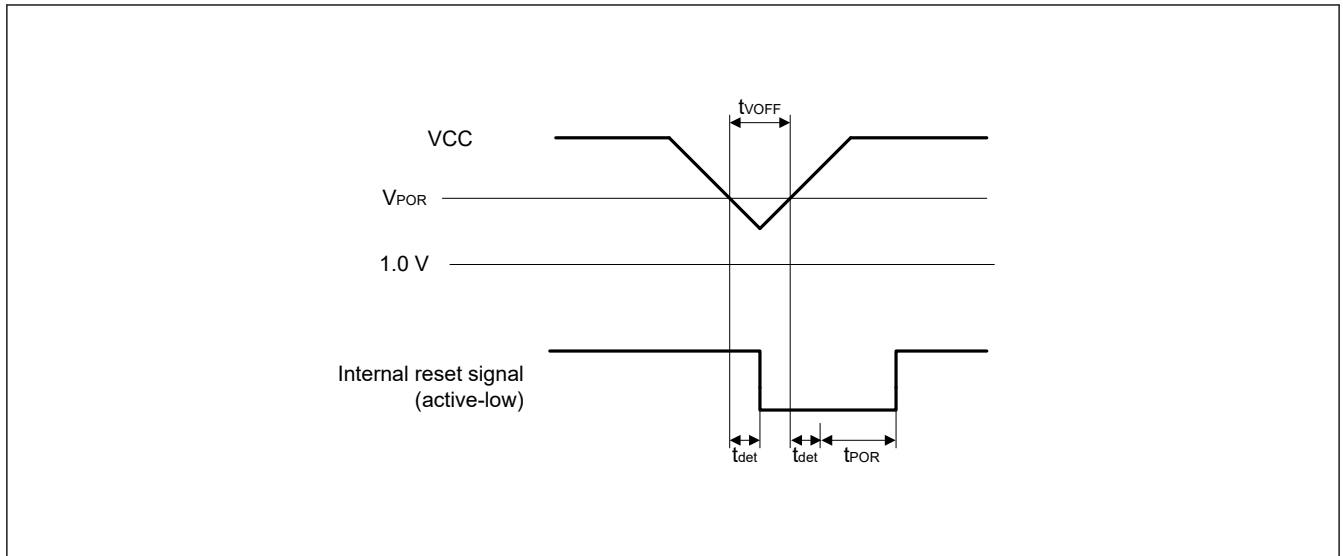
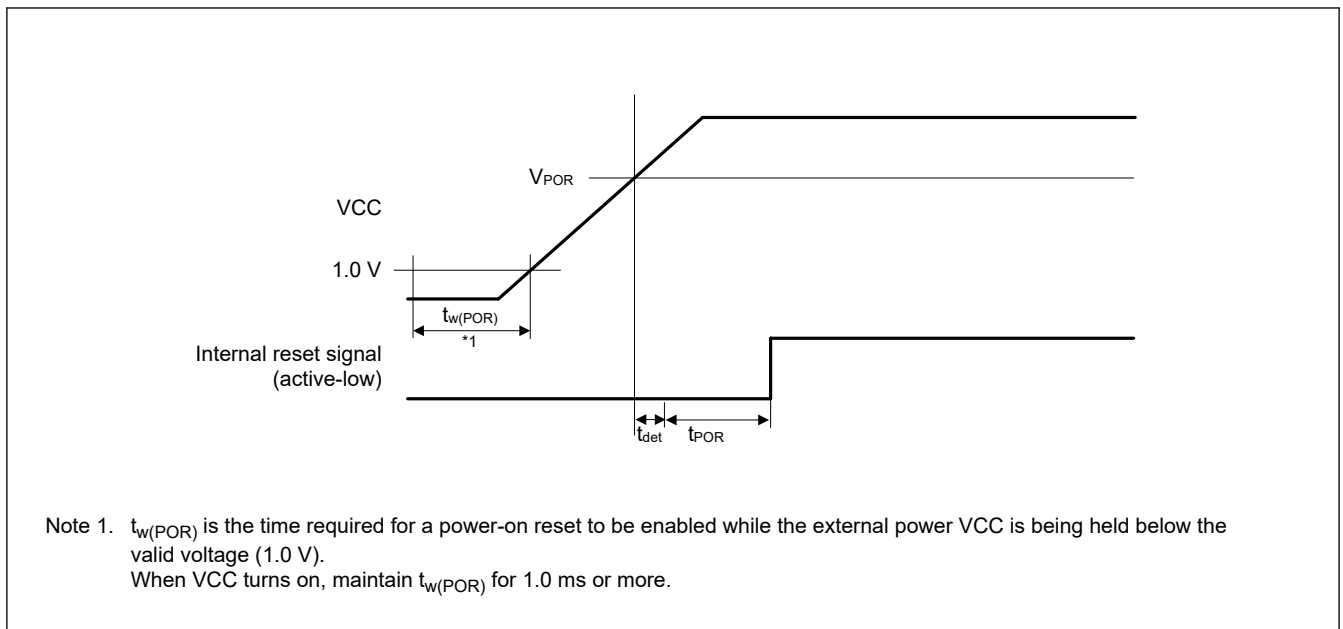


Figure 2.47 Voltage detection reset timing



Note 1. $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.48 Power-on reset timing

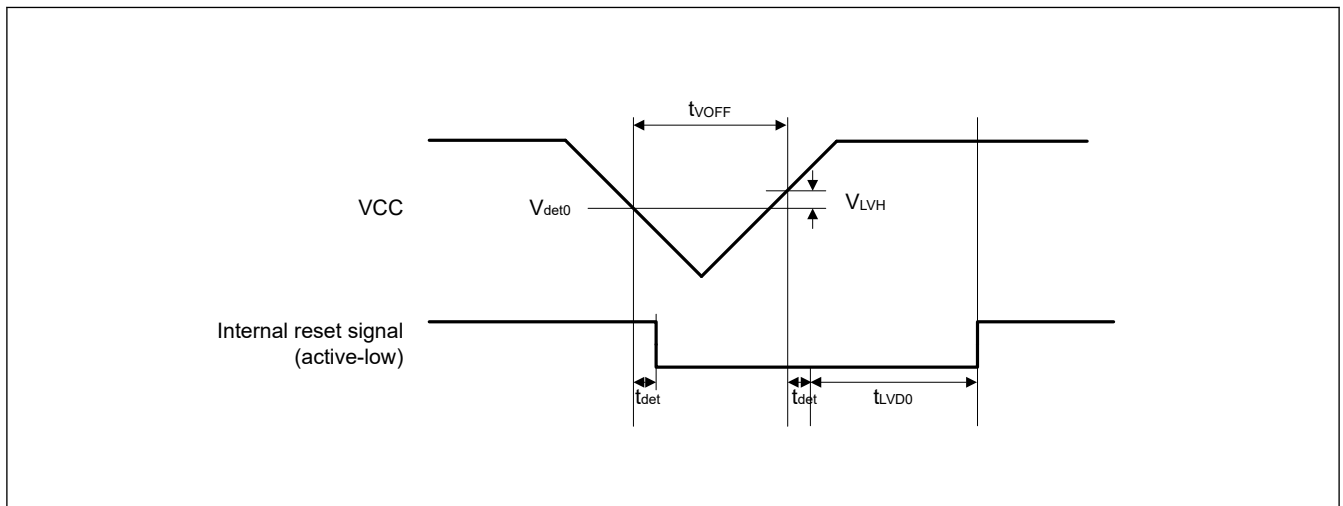


Figure 2.49 Voltage detection circuit timing (V_{det0})

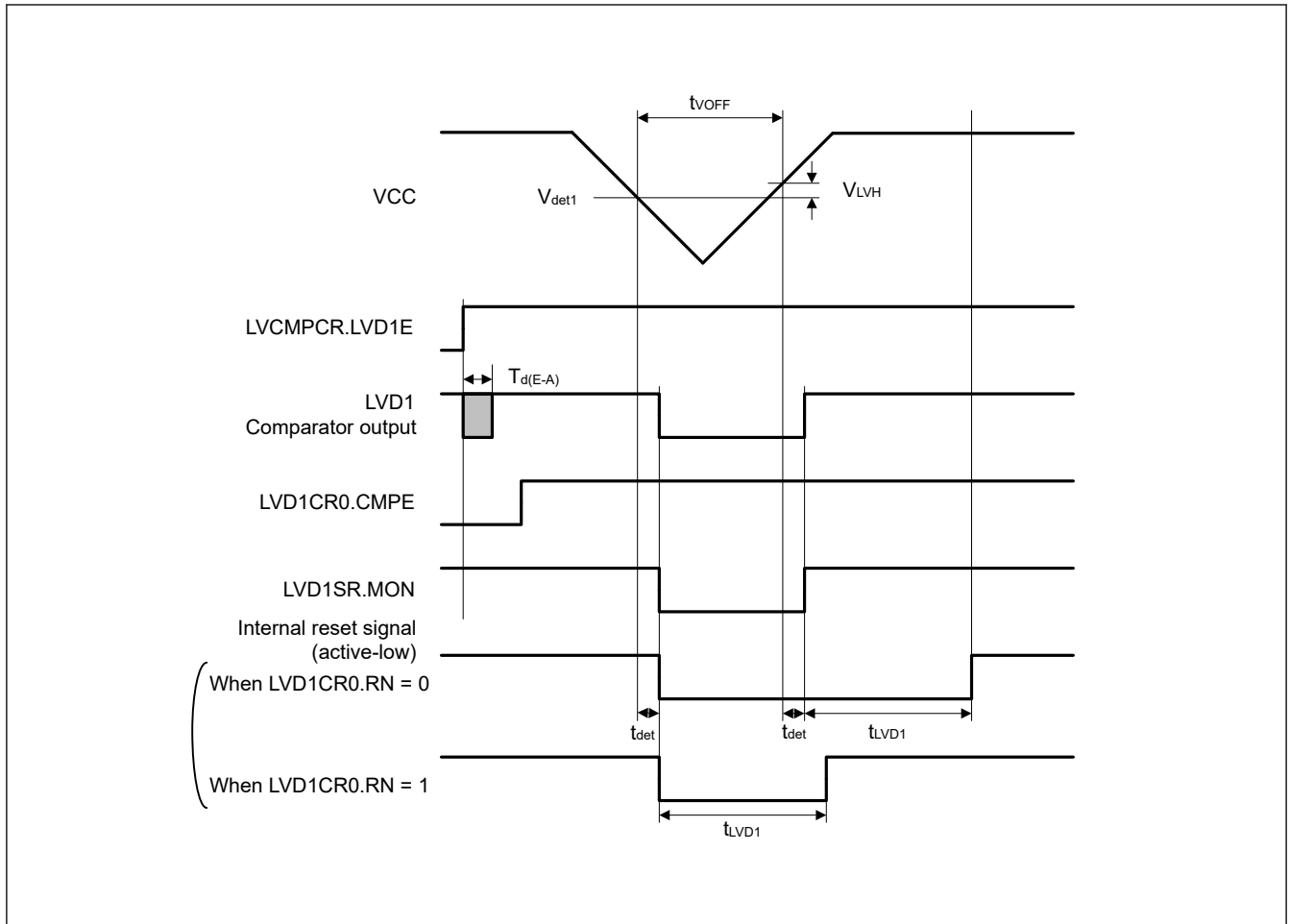


Figure 2.50 Voltage detection circuit timing (V_{det1})

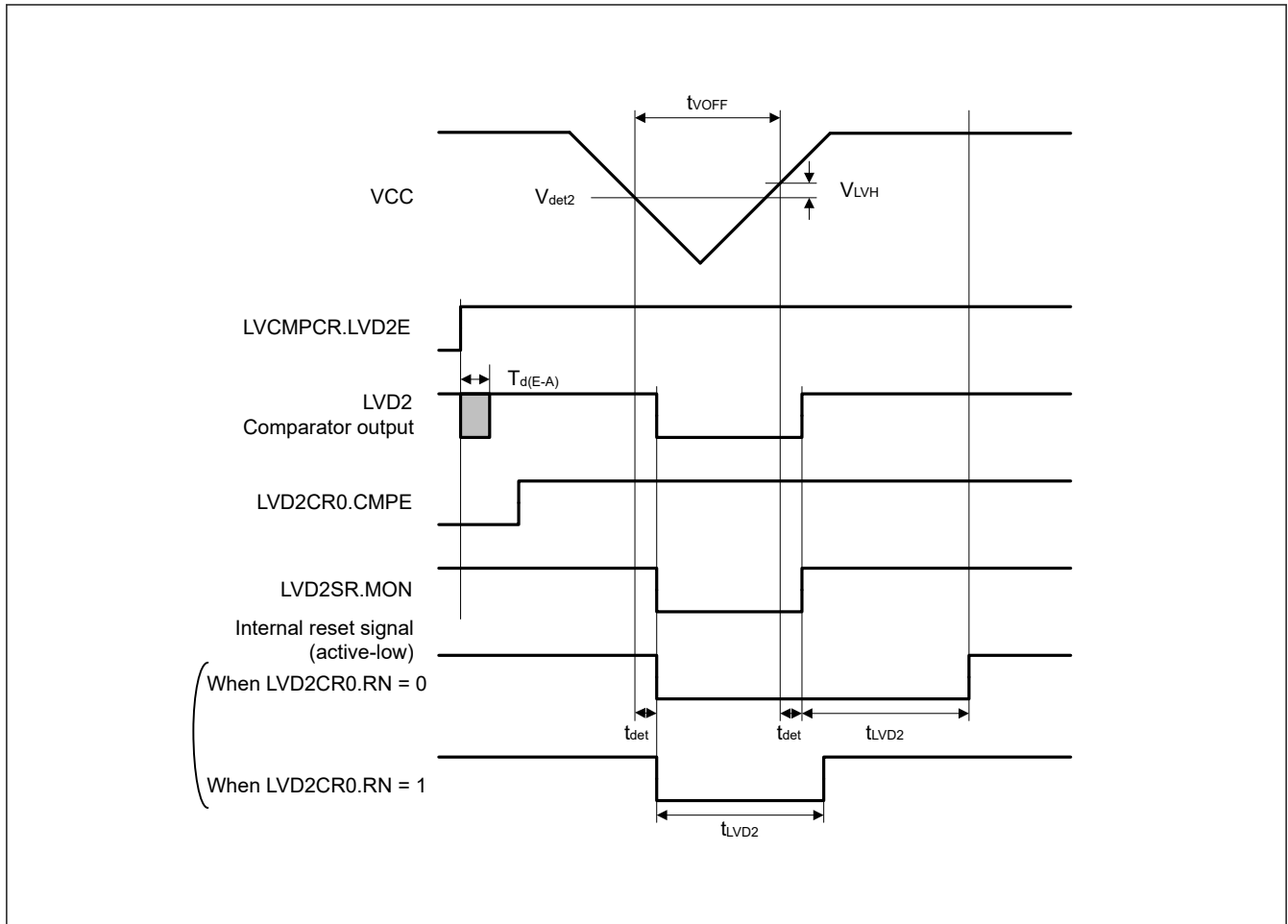


Figure 2.51 Voltage detection circuit timing (V_{det2})

2.7 Flash Memory Characteristics

2.7.1 Code Flash Memory Characteristics

Table 2.51 Code flash characteristics (1)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|-------------------------------|----------------------------|-----------|--------------|-----|-------|-----------------------|
| Reprogramming/erasure cycle*1 | N_{PEC} | 1000 | — | — | Times | — |
| Data hold time | After 1000 times N_{PEC} | t_{DRP} | 20^{*2} *3 | — | Year | $T_a = +105^{\circ}C$ |
| | | | 10 | — | | $T_a = +125^{\circ}C$ |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times ($n = 1,000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is target spec, may be changed after reliability testing.

Table 2.52 Code flash characteristics (2) (1 of 2)

High-speed operating mode
Conditions: $V_{CC} = 1.8$ to 5.5 V

| Parameter | Symbol | ICLK = 1 MHz | | | ICLK = 48 MHz | | | Unit | |
|------------------|--------|--------------|-----|-----|---------------|-----|-----|------|---------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 4-byte | t_{P4} | — | 86 | 732 | — | 34 | 321 | μs |

Table 2.52 Code flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

| Parameter | Symbol | ICLK = 1 MHz | | | ICLK = 48 MHz | | | Unit | |
|---|--------|---------------------|-----|------|---------------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Erase time | 2-KB | t _{E2K} | — | 12.5 | 355 | — | 5.6 | 215 | ms |
| Blank check time | 4-byte | t _{BC4} | — | — | 46.5 | — | — | 8.3 | μs |
| | 2-KB | t _{BC2K} | — | — | 3681 | — | — | 240 | μs |
| Erase suspended time | | t _{SED} | — | — | 22.3 | — | — | 10.5 | μs |
| Access window information program Start-up area selection and security setting time | | t _{AWSSAS} | — | 21.2 | 570 | — | 11.4 | 423 | ms |
| OCD/serial programmer ID setting time*1 | | t _{OSIS} | — | 84.7 | 2280 | — | 45.3 | 1690 | ms |
| Flash memory mode transition wait time 1 | | t _{DIS} | 2 | — | — | 2 | — | — | μs |
| Flash memory mode transition wait time 2 | | t _{MS} | 15 | — | — | 15 | — | — | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. Total time of four commands.

Table 2.53 Code flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = to 5.5 V, Ta = -40 to +85°C

| Parameter | Symbol | ICLK = 1 MHz | | | ICLK = MHz*2 | | | Unit | |
|---|--------|---------------------|-----|------|--------------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 4-byte | t _{P4} | — | 86 | 732 | — | 39 | 356 | μs |
| Erase time | 2-KB | t _{E2K} | — | 12.5 | 355 | — | 6.2 | 227 | ms |
| Blank check time | 4-byte | t _{BC4} | — | — | 46.5 | — | — | 11.3 | μs |
| | 2-KB | t _{BC2K} | — | — | 3681 | — | — | 534 | μs |
| Erase suspended time | | t _{SED} | — | — | 22.3 | — | — | 11.7 | μs |
| Access window information program Start-up area selection and security setting time | | t _{AWSSAS} | — | 21.2 | 570 | — | 12.2 | 435 | ms |
| OCD/serial programmer ID setting time*1 | | t _{OSIS} | — | 84.7 | 2280 | — | 48.7 | 1740 | ms |
| Flash memory mode transition wait time 1 | | t _{DIS} | 2 | — | — | 2 | — | — | μs |
| Flash memory mode transition wait time 2 | | t _{MS} | 15 | — | — | 15 | — | — | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. Total time of four commands.

Note 2. When 1.8 V ≤ VCC ≤ 5.5 V

Table 2.54 Code flash characteristics (4)

Low-speed operating mode

Conditions: VCC = 1.6 to 5.5 V, Ta = -40 to +85°C

| Parameter | Symbol | ICLK = 1 MHz | | | ICLK = 2 MHz | | | Unit | |
|---|--------|---------------------|-----|------|--------------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 4-byte | t _{P4} | — | 86 | 732 | — | 57 | 502 | μs |
| Erase time | 2-KB | t _{E2K} | — | 12.5 | 355 | — | 8.8 | 280 | ms |
| Blank check time | 4-byte | t _{BC4} | — | — | 46.5 | — | — | 23.3 | μs |
| | 2-KB | t _{BC2K} | — | — | 3681 | — | — | 1841 | μs |
| Erase suspended time | | t _{SED} | — | — | 22.3 | — | — | 16.2 | μs |
| Access window information program Start-up area selection and security setting time | | t _{AWSSAS} | — | 21.2 | 570 | — | 15.9 | 491 | ms |
| OCD/serial programmer ID setting time*1 | | t _{OSIS} | — | 84.7 | 2280 | — | 63.5 | 1964 | ms |
| Flash memory mode transition wait time 1 | | t _{DIS} | 2 | — | — | 2 | — | — | μs |
| Flash memory mode transition wait time 2 | | t _{MS} | 15 | — | — | 15 | — | — | μs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. Total time of four commands.

2.7.2 Data Flash Memory Characteristics

Table 2.55 Data flash characteristics (1)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions | |
|-----------------------------|---|-------------------|---------|-----|-------------|------------|-------------|
| Reprogramming/erase cycle*1 | N _{DPEC} | 100000 | 1000000 | — | Times | — | |
| Data hold time | After 10000 times of N _{DPEC} | t _{DDRP} | 20*2 *3 | — | — | Year | Ta = +105°C |
| | | | 10 | — | — | | Ta = +125°C |
| | After 100000 times of N _{DPEC} | 5*2 *3 | — | — | Ta = +105°C | | |
| | | — | 1*2 *3 | — | Ta = +25°C | | |

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are target spec, may changed after reliability testing.

Table 2.56 Data flash characteristics (2) (1 of 2)

High-speed operating mode

Conditions: VCC = 1.8 to 5.5 V

| Parameter | Symbol | ICLK = MHz | | | ICLK = 48 MHz | | | Unit | |
|------------------|--------|--------------------|-----|-----|---------------|-----|-----|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 1-byte | t _{DP1} | — | 45 | 404 | — | 34 | 321 | μs |
| Erase time | 1-KB | t _{DE1K} | — | 8.8 | 280 | — | 6.1 | 224 | ms |
| Blank check time | 1-byte | t _{DBC1} | — | — | 15.2 | — | — | 8.3 | μs |
| | 1-KB | t _{DBC1K} | — | — | 1832 | — | — | 466 | μs |

Table 2.56 Data flash characteristics (2) (2 of 2)

High-speed operating mode
Conditions: VCC = 1.8 to 5.5 V

| Parameter | Symbol | ICLK = MHz | | | ICLK = 48 MHz | | | Unit |
|-------------------------------|---------------------|------------|-----|------|---------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Suspended time during erasing | t _{DS} ED | — | — | 13.2 | — | — | 10.5 | μs |
| Data flash STOP recovery time | t _D STOP | 250 | — | — | 250 | — | — | ns |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.57 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = 1.8 to 5.5 V, Ta = -40 to +85°C

| Parameter | Symbol | ICLK = MHz | | | ICLK = MHz ^{*1} | | | Unit | |
|-------------------------------|---------------------|---------------------|-----|------|--------------------------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 1-byte | t _{DP} 1 | — | 45 | 404 | — | 39 | 356 | μs |
| Erase time | 1-KB | t _{DE} 1K | — | 8.8 | 280 | — | 7.3 | 248 | ms |
| Blank check time | 1-byte | t _{DBC} 1 | — | — | 15.2 | — | — | 11.3 | μs |
| | 1-KB | t _{DBC} 1K | — | — | 1.84 | — | — | 1.06 | ms |
| Suspended time during erasing | t _{DS} ED | — | — | 13.2 | — | — | 11.7 | μs | |
| Data flash STOP recovery time | t _D STOP | 250 | — | — | 250 | — | — | ns | |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. When 1.8 V ≤ VCC ≤ 5.5 V

Table 2.58 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = 1.6 to 5.5 V, Ta = -40 to +85°C

| Parameter | Symbol | ICLK = 1 MHz | | | ICLK = 2 MHz | | | Unit | |
|-------------------------------|---------------------|---------------------|-----|------|--------------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 1-byte | t _{DP} 1 | — | 86 | 732 | — | 57 | 502 | μs |
| Erase time | 1-KB | t _{DE} 1K | — | 19.7 | 504 | — | 12.4 | 354 | ms |
| Blank check time | 1-byte | t _{DBC} 1 | — | — | 46.5 | — | — | 23.3 | μs |
| | 1-KB | t _{DBC} 1K | — | — | 7.3 | — | — | 3.66 | ms |
| Suspended time during erasing | t _{DS} ED | — | — | 22.3 | — | — | 16.2 | μs | |
| Data flash STOP recovery time | t _D STOP | 250 | — | — | 250 | — | — | ns | |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.8 Serial Wire Debug (SWD)

Table 2.59 SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------|---------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 80 | — | — | ns | Figure 2.52 |
| SWCLK clock high pulse width | t_{SWCKH} | 35 | — | — | ns | |
| SWCLK clock low pulse width | t_{SWCKL} | 35 | — | — | ns | |
| SWCLK clock rise time | t_{SWCKr} | — | — | 5 | ns | |
| SWCLK clock fall time | t_{SWCKf} | — | — | 5 | ns | |
| SWDIO setup time | t_{SWDS} | 16 | — | — | ns | Figure 2.53 |
| SWDIO hold time | t_{SWDH} | 16 | — | — | ns | |
| SWDIO data delay time | t_{SWDD} | 2 | — | 70 | ns | |

Table 2.60 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------|---------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 250 | — | — | ns | Figure 2.52 |
| SWCLK clock high pulse width | t_{SWCKH} | 120 | — | — | ns | |
| SWCLK clock low pulse width | t_{SWCKL} | 120 | — | — | ns | |
| SWCLK clock rise time | t_{SWCKr} | — | — | 5 | ns | |
| SWCLK clock fall time | t_{SWCKf} | — | — | 5 | ns | |
| SWDIO setup time | t_{SWDS} | 50 | — | — | ns | Figure 2.53 |
| SWDIO hold time | t_{SWDH} | 50 | — | — | ns | |
| SWDIO data delay time | t_{SWDD} | 2 | — | 170 | ns | |

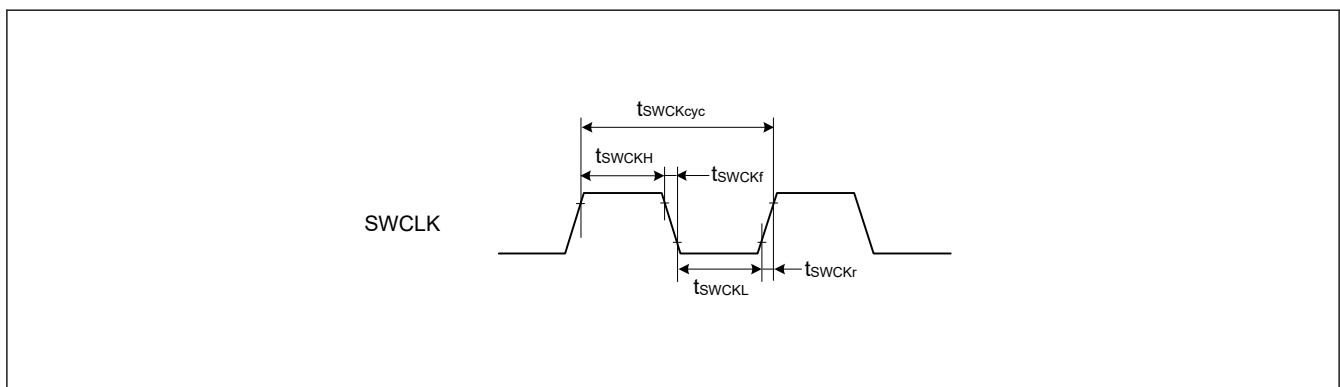


Figure 2.52 SWD SWCLK timing

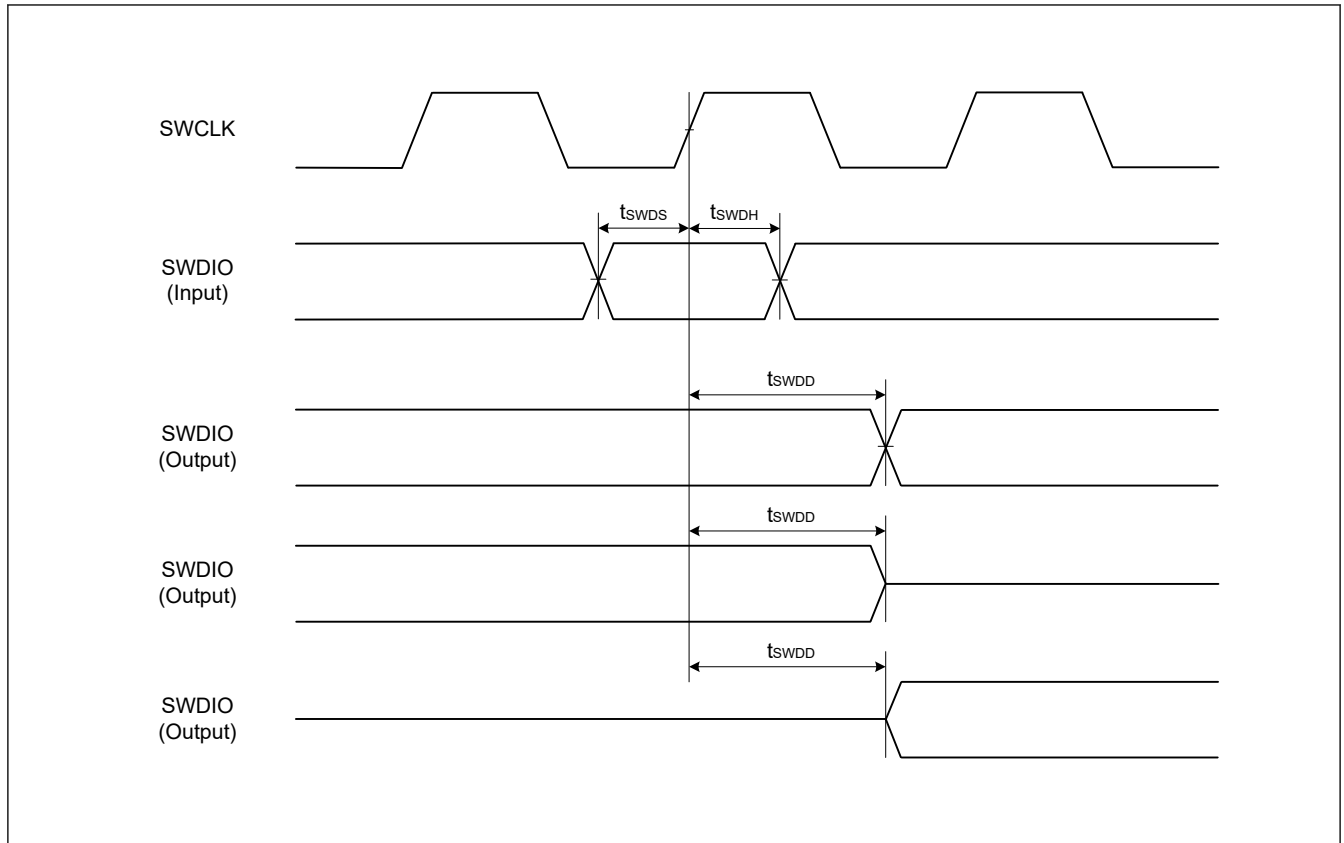


Figure 2.53 SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 2)

| Port name | Reset | Software Standby Mode |
|---|---------|--|
| P010/AN005 | Hi-Z | Keep-O |
| P011/AN006 | Hi-Z | Keep-O |
| P014/AN009 | Hi-Z | Keep-O |
| P015/AN010/IRQ7_A | Hi-Z | Keep-O ^{*1} |
| P100/AN022/AGTIO0_A/GTETRGA_A/ GTIOC8B_A/RXD9_E/MISO9_E/SCL9_E/ SCK9_E/MISOA_A/KRM00/IRQ2_A | Hi-Z | [AGTIO0_A output selected] AGTIO0_A output ^{*2} [Other than the above] Keep-O ^{*1} |
| P101/AN021/AGTEE0/GTETRGA_A/ GTIOC8A_A/TXD9_E/MOSI9_E/SDA9_E/ CTS9_RTS9_G/SS9_G/MOSIA_A/KRM01/ IRQ1_A | Hi-Z | Keep-O ^{*1} |
| P102/AN020/ADTRG0_A/AGTO0/ GTOWLO_A/GTIOC5B_A/SCK9_C/ TXD9_G/MOSI9_G/SDA9_G/RSPCKA_A/ KRM02/IRQ4_C | Hi-Z | [AGTO0 selected] AGTO0 output ^{*2} [Other than the above] Keep-O ^{*1} |
| P103/AN019/AGTOB0_B/GTOWUP_A/ GTIOC5A_A/CTS9_RTS9_E/SS9_E/ RXD9_I/MISO9_I/SCL9_I/SSLA0_A/KRM03/ IRQ6_C | Hi-Z | Keep-O ^{*1} |
| P108/SWDIO/AGTOA1_B/GTOULO_C/ GTIOC7B_C/TXD9_H/MOSI9_H/SDA9_H/ CTS9_RTS9_B/SS9_B/MOSIA_C/IRA5_C | Pull-up | Keep-O |
| P109/AGTO1_A/GTOVUP_C/GTIOC4A_A/ SCK9_F/TXD9_B/MOSI9_B/SDA9_B/ MISOA_C/KRM01_B/IRQ7_C/CLKOUT_B | Hi-Z | [CLKOUT selected] CLKOUT output [Other than the above] Keep-O |
| P110/AGTOA0_A/GTOVLO_A/GTIOC4B_A/ CTS9_RTS9_H/SS9_H/RXD9_B/MISO9_B/ SCL9_B/SSLA0_C/KRM00_B/IRQ3_A | Hi-Z | Keep-O ^{*1} |
| P111/AGTOA0/GTIOC6A_A/RXD9_G/ MISO9_G/SCL9_G/SCK9_B/KRM03_B/ IRQ4_A | Hi-Z | [AGTOA0 selected] AGTOA0 output ^{*2} [Other than the above] Keep-O ^{*1} |
| P112/AGTOB0/GTIOC6B_A/TXD9_J/ MOSI9_J/SDA9_J/CTS9_RTS9_I/SS9_I/ KRM02_B/IRQ1_C | Hi-Z | [AGTOB0 selected] AGTOB0 output ^{*2} [Other than the above] Keep-O |
| P200/NMI | Hi-Z | Hi-Z |
| P201/MD | Pull-up | Keep-O |
| P205/AGTO1/TXD9_I/MOSI9_I/SDA9_I/ CTS9_RTS9_A/SS9_A/KRM01_A/IRQ1/ CLKOUT_A | Hi-Z | [AGTO1 selected] AGTO1 output ^{*2} [CLKOUT selected] CLKOUT output [Other than the above] Keep-O ^{*1} |
| P300/SWCLK/AGTOB1_A/GTOUUP_C/ GTIOC7A_C/RXD9_H/MISO9_H/SCL9_H/ SCK9_G/RSPCKA_C/IRQ0_C | Pull-up | Keep-O |

Table 1.1 Port states in each processing mode (2 of 2)

| Port name | Reset | Software Standby Mode |
|---|-------|---|
| P400/CACREF_C/AGTIO1_C/GTIOC9A_A/ SCK9_D/TXD9_F/MOSI9_F/SDA9_F/ SCL0_A/KRM02_A/IRQ0_A | Hi-Z | [AGTIO1_C output selected] AGTIO1_C output* ² [Other than the above] Keep-O* ¹ |
| P401/AGTEE1_A/GTETRGA_B/ GTIOC9B_A/CTS9_RTS9_F/SS9_F/ RXD9_F/MISO9_F/SCL9_F/SDA0_A/IRQ5/ KRM03_A | Hi-Z | Keep-O* ¹ |
| P914/AGTOA1_A/GTETRGA_B/RXD9_J/ MISO9_J/SCL9_J/SCK9_H/KRM00_A/ IRQ2_C | Hi-Z | [AGTOA1 selected] AGTOA1 output* ² [Other than the above] Keep-O* ¹ |

Note: Hi-Z: High-impedance

Keep-O: Output pins retain their previous values. Input pins become high-impedance.

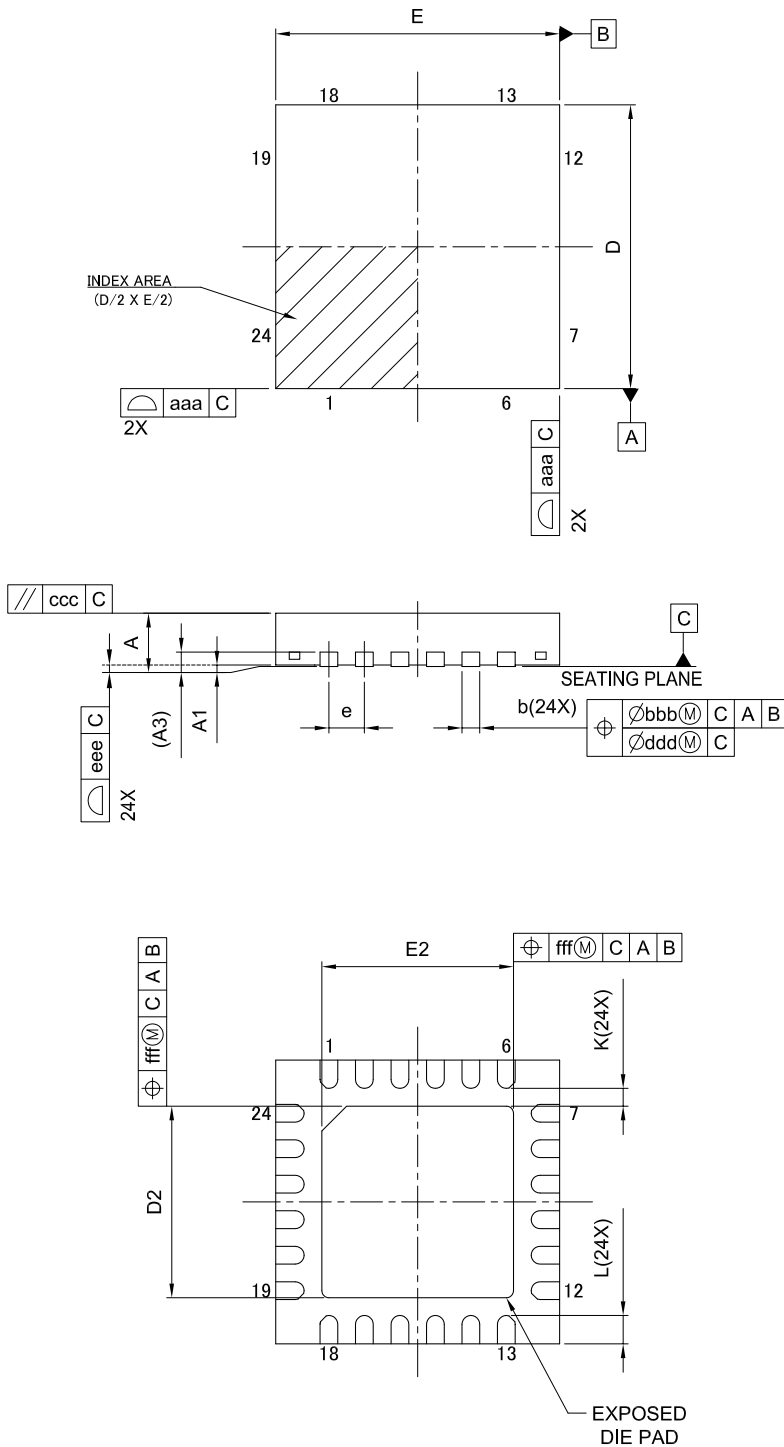
Note 1. Input is enabled if the pin is specified as the software standby canceling source while it is used as an external interrupt pin.

Note 2. AGTIO output is enabled while LOCO is selected as a count source.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in packages on the Renesas Electronics Corporation website.

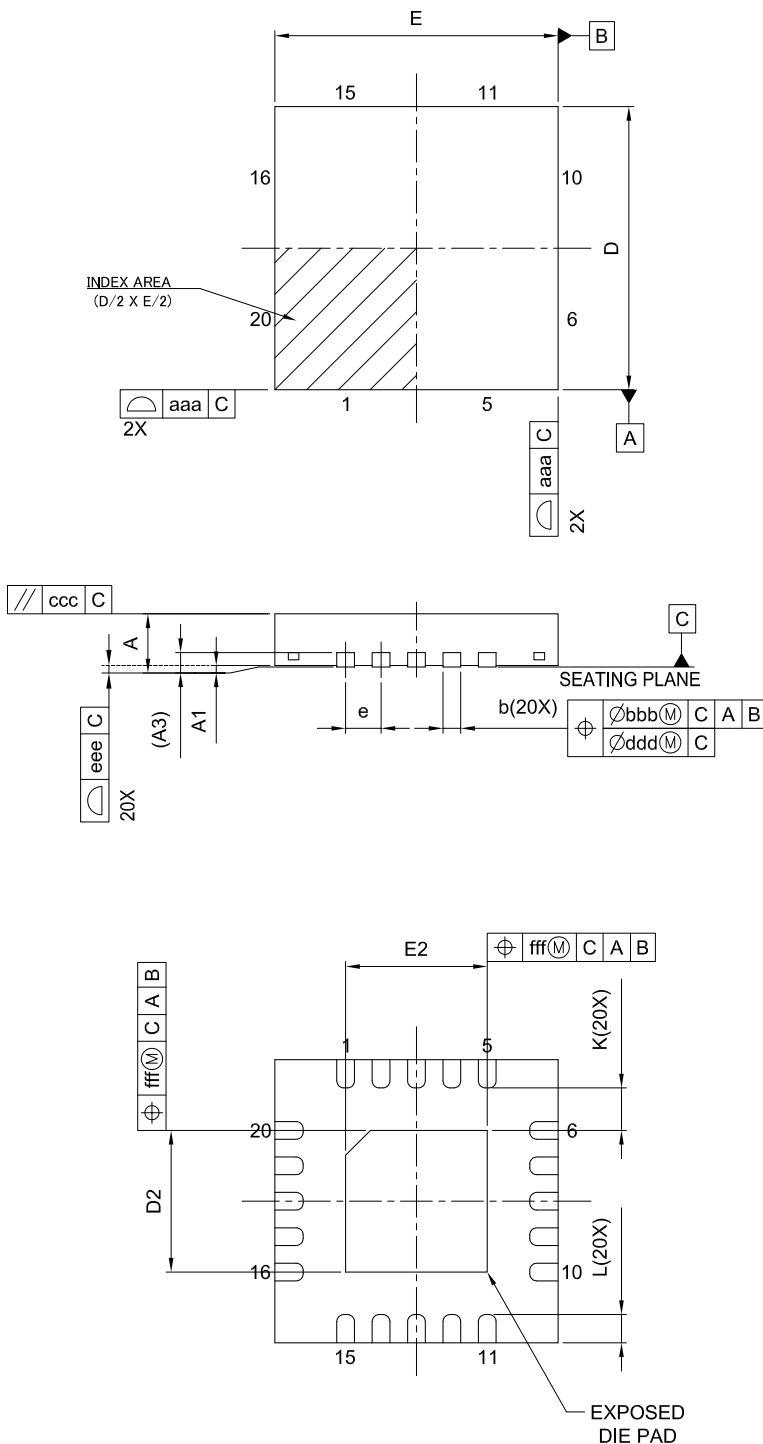
| | | |
|-----------------------|--------------|------------------|
| JEITA Package Code | RENESAS Code | MASS (Typ.) [g] |
| P-HWFQFN24-4 × 4-0.50 | PWQN0024KG-A | 0.04 |



| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| A ₁ | 0.00 | 0.02 | 0.05 |
| A ₃ | 0.203 REF. | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| D ₂ | 2.65 | 2.70 | 2.75 |
| E ₂ | 2.65 | 2.70 | 2.75 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Figure 2.1 HWQFN 24-pin

| | | |
|-----------------------|--------------|-----------------|
| JEITA Package Code | RENESAS Code | MASS (Typ.) [g] |
| P-HWFQFN20-4 × 4-0.50 | PWQN0020KC-A | 0.04 |



| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| A ₁ | 0.00 | 0.02 | 0.05 |
| A ₃ | 0.203 REF. | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| D ₂ | 1.95 | 2.00 | 2.05 |
| E ₂ | 1.95 | 2.00 | 2.05 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Figure 2.2 HWQFN 20-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

| Name | Description | Base address |
|---------|---|--------------|
| MPU | Memory Protection Unit | 0x4000_0000 |
| SRAM | SRAM Control | 0x4000_2000 |
| BUS | BUS Control | 0x4000_3000 |
| DTC | Data Transfer Controller | 0x4000_5400 |
| ICU | Interrupt Controller | 0x4000_6000 |
| CPU_DBG | Debug Function | 0x4001_B000 |
| SYSC | System Control | 0x4001_E000 |
| PORT0 | Port 0 Control Registers | 0x4004_0000 |
| PORT1 | Port 1 Control Registers | 0x4004_0020 |
| PORT2 | Port 2 Control Registers | 0x4004_0040 |
| PORT3 | Port 3 Control Registers | 0x4004_0060 |
| PORT4 | Port 4 Control Registers | 0x4004_0080 |
| PORT9 | Port 9 Control Registers | 0x4004_0120 |
| PFS | Pmn Pin Function Control Register | 0x4004_0800 |
| ELC | Event Link Controller | 0x4004_1000 |
| POEG | Port Output Enable Module for GPT | 0x4004_2000 |
| WDT | Watchdog Timer | 0x4004_4200 |
| IWDT | Independent Watchdog Timer | 0x4004_4400 |
| CAC | Clock Frequency Accuracy Measurement Circuit | 0x4004_4600 |
| MSTP | Module Stop Control B, C, D | 0x4004_7000 |
| I3C | I3C Bus Interface | 0x4008_3000 |
| DOC | Data Operation Circuit | 0x4005_4100 |
| ADC12 | 12-bit A/D Converter | 0x4005_C000 |
| SCI9 | Serial Communication Interface 9 | 0x4007_0120 |
| SPI0 | Serial Peripheral Interface 0 | 0x4007_2000 |
| CRC | CRC Calculator | 0x4007_4000 |
| GPT164 | General PWM Timer 4 (16-bit) | 0x4007_8400 |
| GPT165 | General PWM Timer 5 (16-bit) | 0x4007_8500 |
| GPT166 | General PWM Timer 6 (16-bit) | 0x4007_8600 |
| GPT167 | General PWM Timer 7 (16-bit) | 0x4007_8700 |
| GPT168 | General PWM Timer 8 (16-bit) | 0x4007_8800 |
| GPT169 | General PWM Timer 9 (16-bit) | 0x4007_8900 |
| GPT_OPS | Output Phase Switching Controller | 0x4007_8FF0 |
| KINT | Key Interrupt Function | 0x4008_0000 |
| AGTW0 | Low Power Asynchronous General Purpose Timer W0 | 0x4008_4000 |

Table 3.1 Peripheral base address (2 of 2)

| Name | Description | Base address |
|-------|---|--------------|
| AGTW1 | Low Power Asynchronous General Purpose Timer W1 | 0x4008_4100 |
| FLCN | Flash I/O Registers | 0x407E_C000 |

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to [Table 3.2](#):

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

[Table 3.2](#) shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules (1 of 2)

| Peripherals | Address | | Number of access cycles | | | | Cycle unit | Related function |
|---|-------------|-------------|-------------------------|-------|---------------|-------|------------|---|
| | | | ICLK = PCLK | | ICLK > PCLK*1 | | | |
| | | | Read | Write | Read | Write | | |
| MPU, SRAM, BUS, DTC, ICU, CPU_DBG | 0x4000_2000 | 0x4001_BFFF | 3 | | | | ICLK | Memory Protection Unit, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory |
| SYSC | 0x4001_E000 | 0x4001_E6FF | 4 | | | | ICLK | Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection |
| PORTn, PFS, ELC, POEG, WDT, IWDT, CAC, MSTP | 0x4004_0000 | 0x4004_7FFF | 3 | | 2 to 3 | | PCLKB | I/O Ports, Event Link Controller, Port Output Enable for GPT, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control |
| I3C, DOC, ADC12 | 0x4005_0000 | 0x4005_EFFF | 3 | | 2 to 3 | | PCLKB | I3C Bus Interface, Data Operation Circuit, 12-bit A/D Converter |
| SCIn (n = 9) | 0x4007_0000 | 0x4007_0EFF | 5 | | 2 to 3 | | PCLKB | Serial Communications Interface |
| SPIn (n = 0)*2 | 0x4007_2000 | 0x4007_2FFF | 5 | | 2 to 3 | | PCLKB | Serial Peripheral Interface |

Table 3.2 Access cycles for non-GPT modules (2 of 2)

| Peripherals | Address | | Number of access cycles | | | | Cycle unit | Related function |
|---------------------------------|-------------|-------------|-------------------------|-------|---------------|-------|------------|--|
| | | | ICLK = PCLK | | ICLK > PCLK*1 | | | |
| | From | To | Read | Write | Read | Write | | |
| CRC | 0x4007_4000 | 0x4007_4FFF | 3 | | 2 to 3 | | PCLKB | CRC Calculator |
| GPT16n (n = 4 to 9), GPT_OPS | 0x4007_8000 | 0x4007_BFFF | See Table 3.3. | | | | PCLKB | General PWM Timer |
| KINT | 0x4008_0000 | 0x4008_2FFF | 3 | | 2 to 3 | | PCLKB | Key interrupt Function, Capacitive Sensing Unit 2 |
| AGTWn | 0x4008_4000 | 0x4008_4FFF | 3 | | 2 to 3 | | PCLKB | Low Power Asynchronous General Purpose Timer |
| FLCN | 0x407E_C000 | 0x407E_FFFF | 7 | | 7 | | ICLK | Data Flash, Temperature Sensor, Capacitive Sensing Unit 2, Flash Control |

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.

Note 2. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

| Frequency ratio between ICLK and PCLK | Number of access cycles | | Cycle unit |
|---------------------------------------|-------------------------|--------|------------|
| | Read | Write | |
| ICLK > PCLKD = PCLKB | 5 to 6 | 3 to 4 | PCLKB |
| ICLK > PCLKD > PCLKB | 3 to 4 | 2 to 3 | PCLKB |
| PCLKD = ICLK = PCLKB | 6 | 4 | PCLKB |
| PCLKD = ICLK > PCLKB | 2 to 3 | 1 to 2 | PCLKB |
| PCLKD > ICLK = PCLKB | 4 | 3 | PCLKB |
| PCLKD > ICLK > PCLKB | 2 to 3 | 1 to 2 | PCLKB |

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.4 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.4 Register description (1 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|---|----------------|------|-----|-------------|------------|
| MPU | - | - | - | MMPUCTLA | Bus Master MPU Control Register | 0x000 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | MMPUPTA | Group A Protection of Register | 0x102 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | 4 | 0x010 | 0-3 | MMPUACA%s | Group A Region %s access control register | 0x200 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | 4 | 0x010 | 0-3 | MMPUSA%s | Group A Region %s Start Address Register | 0x204 | 32 | R/W | 0x00000000 | 0x00000003 |
| MPU | 4 | 0x010 | 0-3 | MMPUEA%s | Group A Region %s End Address Register | 0x208 | 32 | R/W | 0x00000003 | 0x00000003 |
| MPU | - | - | - | SMPUCTL | Slave MPU Control Register | 0xC00 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | SMPUMBIU | Access Control Register for Memory Bus 1 | 0xC10 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | SMPUFBIU | Access Control Register for Internal Peripheral Bus 9 | 0xC14 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | SMPUSRAM0 | Access Control Register for Memory Bus 4 | 0xC18 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | SMPUP0BIU | Access Control Register for Internal Peripheral Bus 1 | 0xC20 | 16 | R/W | 0x0000 | 0xFFFF |

Table 3.4 Register description (2 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|--|----------------|------|-----|--------------|------------|
| MPU | - | - | - | SMPUP2BIU | Access Control Register for Internal Peripheral Bus 3 | 0xC24 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | SMPUP6BIU | Access Control Register for Internal Peripheral Bus 7 | 0xC28 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | MSPMPUOAD | Stack Pointer Monitor Operation After Detection Register | 0xD00 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | MSPMPUCTL | Stack Pointer Monitor Access Control Register | 0xD04 | 16 | R/W | 0x0000 | 0xFEFF |
| MPU | - | - | - | MSPMPUPT | Stack Pointer Monitor Protection Register | 0xD06 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | MSPMPUSA | Main Stack Pointer (MSP) Monitor Start Address Register | 0xD08 | 32 | R/W | 0x00000000 | 0x00000000 |
| MPU | - | - | - | MSPMPUEA | Main Stack Pointer (MSP) Monitor End Address Register | 0xD0C | 32 | R/W | 0x00000000 | 0x00000000 |
| MPU | - | - | - | PSPMPUOAD | Stack Pointer Monitor Operation After Detection Register | 0xD10 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | PSPMPUCTL | Stack Pointer Monitor Access Control Register | 0xD14 | 16 | R/W | 0x0000 | 0xFEFF |
| MPU | - | - | - | PSPMPUPT | Stack Pointer Monitor Protection Register | 0xD16 | 16 | R/W | 0x0000 | 0xFFFF |
| MPU | - | - | - | PSPMPUSA | Process Stack Pointer (PSP) Monitor Start Address Register | 0xD18 | 32 | R/W | 0x00000000 | 0x00000000 |
| MPU | - | - | - | PSPMPUEA | Process Stack Pointer (PSP) Monitor End Address Register | 0xD1C | 32 | R/W | 0x00000000 | 0x00000000 |
| SRAM | - | - | - | PARIOAD | SRAM Parity Error Operation After Detection Register | 0x00 | 8 | R/W | 0x00 | 0xFF |
| SRAM | - | - | - | SRAMPCR | SRAM Protection Register | 0x04 | 8 | R/W | 0x00 | 0xFF |
| BUS | - | - | - | BUSMCNTSYS | Master Bus Control Register SYS | 0x1008 | 16 | R/W | 0x0000 | 0xFFFF |
| BUS | - | - | - | BUSMCNTDMA | Master Bus Control Register DMA | 0x100C | 16 | R/W | 0x0000 | 0xFFFF |
| BUS | - | - | - | BUS3ERRADD | Bus Error Address Register 3 | 0x1820 | 32 | R | 0x00000000 | 0x00000000 |
| BUS | - | - | - | BUS3ERRSTAT | BUS Error Status Register 3 | 0x1824 | 8 | R | 0x00 | 0xFE |
| BUS | - | - | - | BUS4ERRADD | Bus Error Address Register 4 | 0x1830 | 32 | R | 0x00000000 | 0x00000000 |
| BUS | - | - | - | BUS4ERRSTAT | BUS Error Status Register 4 | 0x1834 | 8 | R | 0x00 | 0xFE |
| DTC | - | - | - | DTCCR | DTC Control Register | 0x00 | 8 | R/W | 0x08 | 0xFF |
| DTC | - | - | - | DTCVBR | DTC Vector Base Register | 0x04 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| DTC | - | - | - | DTCST | DTC Module Start Register | 0x0C | 8 | R/W | 0x00 | 0xFF |
| DTC | - | - | - | DTCSTS | DTC Status Register | 0x0E | 16 | R | 0x0000 | 0xFFFF |
| ICU | 8 | 0x1 | 0-7 | IRQCR%s | IRQ Control Register | 0x000 | 8 | R/W | 0x00 | 0xFF |
| ICU | - | - | - | NMICR | NMI Pin Interrupt Control Register | 0x100 | 8 | R/W | 0x00 | 0xFF |
| ICU | - | - | - | NMIER | Non-Maskable Interrupt Enable Register | 0x120 | 16 | R/W | 0x0000 | 0xFFFF |
| ICU | - | - | - | NMICLR | Non-Maskable Interrupt Status Clear Register | 0x130 | 16 | R/W | 0x0000 | 0xFFFF |
| ICU | - | - | - | NMISR | Non-Maskable Interrupt Status Register | 0x140 | 16 | R | 0x0000 | 0xFFFF |
| ICU | - | - | - | WUPEN | Wake Up Interrupt Enable Register | 0x1A0 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| ICU | - | - | - | IELEN | ICU event Enable Register | 0x1C0 | 8 | R/W | 0x00 | 0xFF |
| ICU | - | - | - | SELSR0 | SYS Event Link Setting Register | 0x200 | 16 | R/W | 0x0000 | 0xFFFF |
| ICU | 32 | 0x4 | 0-31 | IELSR%s | ICU Event Link Setting Register %s | 0x300 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| CPU_DBG | - | - | - | DBGSTR | Debug Status Register | 0x00 | 32 | R | 0x00000000 | 0xFFFFFFFF |
| CPU_DBG | - | - | - | DBGSTOPCR | Debug Stop Control Register | 0x10 | 32 | R/W | 0x00000003 | 0xFFFFFFFF |
| SYSC | - | - | - | SBYCR | Standby Control Register | 0x00C | 16 | R/W | 0x0000 | 0xFFFF |
| SYSC | - | - | - | MSTPCRA | Module Stop Control Register A | 0x01C | 32 | R/W | 0xFFBFFFFFFF | 0xFFFFFFFF |
| SYSC | - | - | - | SCKDIVCR | System Clock Division Control Register | 0x020 | 32 | R/W | 0x04000404 | 0xFFFFFFFF |

Table 3.4 Register description (3 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|---|----------------|------|-----|-------------|------------|
| SYSC | - | - | - | SCKSCR | System Clock Source Control Register | 0x026 | 8 | R/W | 0x01 | 0xFF |
| SYSC | - | - | - | MEMWAIT | Memory Wait Cycle Control Register for Code Flash | 0x031 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | HOCOOCR | High-Speed On-Chip Oscillator Control Register | 0x036 | 8 | R/W | 0x00 | 0xFE |
| SYSC | - | - | - | MOCOOCR | Middle-Speed On-Chip Oscillator Control Register | 0x038 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | OSCSF | Oscillation Stabilization Flag Register | 0x03C | 8 | R | 0x00 | 0xFE |
| SYSC | - | - | - | CKOCR | Clock Out Control Register | 0x03E | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | LPOPT | Lower Power Operation Control Register | 0x04C | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | MOCOUTCR | MOCO User Trimming Control Register | 0x061 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | HOCOUTCR | HOCO User Trimming Control Register | 0x062 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | SNZCR | Snooze Control Register | 0x092 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | SNZEDCR0 | Snooze End Control Register | 0x094 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | SNZREQCR | Snooze Request Control Register | 0x098 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| SYSC | - | - | - | PSMCR | Power Save Memory Control Register | 0x09F | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | OPCCR | Operating Power Control Register | 0x0A0 | 8 | R/W | 0x01 | 0xFF |
| SYSC | - | - | - | HOCOWTCR | High-Speed On-Chip Oscillator Wait Control Register | 0x0A5 | 8 | R/W | 0x05 | 0xFF |
| SYSC | - | - | - | SOPCCR | Sub Operating Power Control Register | 0x0AA | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | RSTSR1 | Reset Status Register 1 | 0x0C0 | 16 | R/W | 0x0000 | 0xE2F8 |
| SYSC | - | - | - | LVD1CR1 | Voltage Monitor 1 Circuit Control Register | 0x0E0 | 8 | R/W | 0x01 | 0xFF |
| SYSC | - | - | - | LVD1SR | Voltage Monitor 1 Circuit Status Register | 0x0E1 | 8 | R/W | 0x02 | 0xFF |
| SYSC | - | - | - | LVD2CR1 | Voltage Monitor 2 Circuit Control Register 1 | 0x0E2 | 8 | R/W | 0x01 | 0xFF |
| SYSC | - | - | - | LVD2SR | Voltage Monitor 2 Circuit Status Register | 0x0E3 | 8 | R/W | 0x02 | 0xFF |
| SYSC | - | - | - | PRCR | Protect Register | 0x3FE | 16 | R/W | 0x0000 | 0xFFFF |
| SYSC | - | - | - | SYOCDCCR | System Control OCD Control Register | 0x040E | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | RSTSR0 | Reset Status Register 0 | 0x410 | 8 | R/W | 0x00 | 0xF0 |
| SYSC | - | - | - | RSTSR2 | Reset Status Register 2 | 0x411 | 8 | R/W | 0x00 | 0xFE |
| SYSC | - | - | - | LVMPCR | Voltage Monitor Circuit Control Register | 0x417 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | LVDLVLRL | Voltage Detection Level Select Register | 0x418 | 8 | R/W | 0x07 | 0xFF |
| SYSC | - | - | - | LVD1CR0 | Voltage Monitor 1 Circuit Control Register 0 | 0x41A | 8 | R/W | 0x80 | 0xF7 |
| SYSC | - | - | - | LVD2CR0 | Voltage Monitor 2 Circuit Control Register 0 | 0x41B | 8 | R/W | 0x80 | 0xF7 |
| SYSC | - | - | - | LOCOOCR | Low-Speed On-Chip Oscillator Control Register | 0x490 | 8 | R/W | 0x00 | 0xFF |
| SYSC | - | - | - | LOCOUTCR | LOCO User Trimming Control Register | 0x492 | 8 | R/W | 0x00 | 0xFF |
| PORT0,3-4,9 | - | - | - | PCNTR1 | Port Control Register 1 | 0x000 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| PORT0,3-4,9 | - | - | - | PODR | Port Control Register 1 | 0x000 | 16 | R/W | 0x0000 | 0xFFFF |
| PORT0,3-4,9 | - | - | - | PDR | Port Control Register 1 | 0x002 | 16 | R/W | 0x0000 | 0xFFFF |
| PORT0,3-4,9 | - | - | - | PCNTR2 | Port Control Register 2 | 0x004 | 32 | R | 0x00000000 | 0xFFFF0000 |
| PORT0,3-4,9 | - | - | - | PIDR | Port Control Register 2 | 0x006 | 16 | R | 0x0000 | 0x0000 |
| PORT0,3-4,9 | - | - | - | PCNTR3 | Port Control Register 3 | 0x008 | 32 | W | 0x00000000 | 0xFFFFFFFF |

Table 3.4 Register description (4 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|----------------|---------------|---------------------------------------|----------------|------|-----|-------------|-------------|
| PORT0,3-4,9 | - | - | - | PORR | Port Control Register 3 | 0x008 | 16 | W | 0x0000 | 0xFFFF |
| PORT0,3-4,9 | - | - | - | POSR | Port Control Register 3 | 0x00A | 16 | W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | PCNTR1 | Port Control Register 1 | 0x000 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| PORT1-2 | - | - | - | PODR | Port Control Register 1 | 0x000 | 16 | R/W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | PDR | Port Control Register 1 | 0x002 | 16 | R/W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | PCNTR2 | Port Control Register 2 | 0x004 | 32 | R | 0x00000000 | 0xFFFF0000 |
| PORT1-2 | - | - | - | EIDR | Port Control Register 2 | 0x004 | 16 | R | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | PIDR | Port Control Register 2 | 0x006 | 16 | R | 0x0000 | 0x0000 |
| PORT1-2 | - | - | - | PCNTR3 | Port Control Register 3 | 0x008 | 32 | W | 0x00000000 | 0xFFFFFFFF |
| PORT1-2 | - | - | - | PORR | Port Control Register 3 | 0x008 | 16 | W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | POSR | Port Control Register 3 | 0x00A | 16 | W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | PCNTR4 | Port Control Register 4 | 0x00C | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| PORT1-2 | - | - | - | EORR | Port Control Register 4 | 0x00C | 16 | R/W | 0x0000 | 0xFFFF |
| PORT1-2 | - | - | - | EOSR | Port Control Register 4 | 0x00E | 16 | R/W | 0x0000 | 0xFFFF |
| PFS | 4 | 0x4 | 10, 11, 14, 15 | P0%PFS | Port 0% Pin Function Select Register | 0x028 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | 4 | 0x4 | 10, 11, 14, 15 | P0%PFS_HA | Port 0% Pin Function Select Register | 0x02A | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | 4 | 0x4 | 10, 11, 14, 15 | P0%PFS_BY | Port 0% Pin Function Select Register | 0x02B | 8 | R/W | 0x00 | 0xFD |
| PFS | 4 | 0x4 | 0-3 | P10%PFS | Port 10% Pin Function Select Register | 0x040 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | 4 | 0x4 | 0-3 | P10%PFS_HA | Port 10% Pin Function Select Register | 0x042 | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | 4 | 0x4 | 0-3 | P10%PFS_BY | Port 10% Pin Function Select Register | 0x043 | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | P108PFS | Port 108 Pin Function Select Register | 0x060 | 32 | R/W | 0x00010010 | 0xFFFFFFFFD |
| PFS | - | - | - | P108PFS_HA | Port 108 Pin Function Select Register | 0x062 | 16 | R/W | 0x0010 | 0xFFFD |
| PFS | - | - | - | P108PFS_BY | Port 108 Pin Function Select Register | 0x063 | 8 | R/W | 0x10 | 0xFD |
| PFS | - | - | - | P109PFS | Port 109 Pin Function Select Register | 0x064 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | - | - | - | P109PFS_HA | Port 109 Pin Function Select Register | 0x066 | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | - | - | - | P109PFS_BY | Port 109 Pin Function Select Register | 0x067 | 8 | R/W | 0x00 | 0xFD |
| PFS | 3 | 0x4 | 10-12 | P1%PFS | Port 1% Pin Function Select Register | 0x068 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | 3 | 0x4 | 10-12 | P1%PFS_HA | Port 1% Pin Function Select Register | 0x06A | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | 3 | 0x4 | 10-12 | P1%PFS_BY | Port 1% Pin Function Select Register | 0x06B | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | P200PFS | Port 200 Pin Function Select Register | 0x080 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | - | - | - | P200PFS_HA | Port 200 Pin Function Select Register | 0x082 | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | - | - | - | P200PFS_BY | Port 200 Pin Function Select Register | 0x083 | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | P201PFS | Port 201 Pin Function Select Register | 0x084 | 32 | R/W | 0x00000010 | 0xFFFFFFFFD |
| PFS | - | - | - | P201PFS_HA | Port 201 Pin Function Select Register | 0x086 | 16 | R/W | 0x0010 | 0xFFFD |
| PFS | - | - | - | P201PFS_BY | Port 201 Pin Function Select Register | 0x087 | 8 | R/W | 0x10 | 0xFD |
| PFS | 1 | 0x4 | 5 | P20%PFS | Port 20% Pin Function Select Register | 0x094 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | 1 | 0x4 | 5 | P20%PFS_HA | Port 20% Pin Function Select Register | 0x096 | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | 1 | 0x4 | 5 | P20%PFS_BY | Port 20% Pin Function Select Register | 0x097 | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | P300PFS | Port 300 Pin Function Select Register | 0x0C0 | 32 | R/W | 0x00010000 | 0xFFFFFFFFD |
| PFS | - | - | - | P300PFS_HA | Port 300 Pin Function Select Register | 0x0C2 | 16 | R/W | 0x0000 | 0xFFFD |
| PFS | - | - | - | P300PFS_BY | Port 300 Pin Function Select Register | 0x0C3 | 8 | R/W | 0x00 | 0xFD |
| PFS | 2 | 0x4 | 0-1 | P40%PFS | Port 40% Pin Function Select Register | 0x100 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |

Table 3.4 Register description (5 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|--|----------------|------|-----|-------------|-------------|
| PFS | 2 | 0x4 | 0-1 | P40%PFS_HA | Port 40% Pin Function Select Register | 0x102 | 16 | R/W | 0x0000 | 0xFFFFD |
| PFS | 2 | 0x4 | 0-1 | P40%PFS_BY | Port 40% Pin Function Select Register | 0x103 | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | P914PFS | Port 914 Pin Function Select Register | 0xA78 | 32 | R/W | 0x00000000 | 0xFFFFFFFFD |
| PFS | - | - | - | P914PFS_HA | Port 914 Pin Function Select Register | 0xA7A | 16 | R/W | 0x0000 | 0xFFFFD |
| PFS | - | - | - | P914PFS_BY | Port 914 Pin Function Select Register | 0xA7B | 8 | R/W | 0x00 | 0xFD |
| PFS | - | - | - | PWPR | Write-Protect Register | 0x503 | 8 | R/W | 0x80 | 0xFF |
| PFS | - | - | - | PRWCNTR | Port Read Wait Control Register | 0x50F | 8 | R/W | 0x01 | 0xFF |
| ELC | - | - | - | ELCR | Event Link Controller Register | 0x00 | 8 | R/W | 0x00 | 0xFF |
| ELC | 2 | 0x02 | 0-1 | ELSEGR% | Event Link Software Event Generation Register %s | 0x02 | 8 | R/W | 0x80 | 0xFF |
| ELC | 4 | 0x04 | 0-3 | ELSR% | Event Link Setting Register %s | 0x10 | 16 | R/W | 0x0000 | 0xFFFF |
| ELC | 2 | 0x04 | 8-9 | ELSR% | Event Link Setting Register %s | 0x30 | 16 | R/W | 0x0000 | 0xFFFF |
| ELC | 2 | 0x04 | 14-15 | ELSR% | Event Link Setting Register %s | 0x48 | 16 | R/W | 0x0000 | 0xFFFF |
| ELC | - | - | - | ELSR18 | Event Link Setting Register 18 | 0x58 | 16 | R/W | 0x0000 | 0xFFFF |
| POEG | - | - | - | POEGGA | POEG Group A Setting Register | 0x000 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| POEG | - | - | - | POEGGB | POEG Group B Setting Register | 0x100 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| WDT | - | - | - | WDTRR | WDT Refresh Register | 0x00 | 8 | R/W | 0xFF | 0xFF |
| WDT | - | - | - | WDTCR | WDT Control Register | 0x02 | 16 | R/W | 0x0000 | 0xFFFF |
| WDT | - | - | - | WDTSR | WDT Status Register | 0x04 | 16 | R/W | 0x0000 | 0xFFFF |
| WDT | - | - | - | WDTRCR | WDT Reset Control Register | 0x06 | 8 | R/W | 0x80 | 0xFF |
| WDT | - | - | - | WDTCTPR | WDT Count Stop Control Register | 0x08 | 8 | R/W | 0x80 | 0xFF |
| IWDT | - | - | - | IWDTRR | IWDT Refresh Register | 0x00 | 8 | R/W | 0xFF | 0xFF |
| IWDT | - | - | - | IWDTSR | IWDT Status Register | 0x04 | 16 | R/W | 0x0000 | 0xFFFF |
| CAC | - | - | - | CACR0 | CAC Control Register 0 | 0x00 | 8 | R/W | 0x00 | 0xFF |
| CAC | - | - | - | CACR1 | CAC Control Register 1 | 0x01 | 8 | R/W | 0x00 | 0xFF |
| CAC | - | - | - | CACR2 | CAC Control Register 2 | 0x02 | 8 | R/W | 0x00 | 0xFF |
| CAC | - | - | - | CAICR | CAC Interrupt Control Register | 0x03 | 8 | R/W | 0x00 | 0xFF |
| CAC | - | - | - | CASTR | CAC Status Register | 0x04 | 8 | R | 0x00 | 0xFF |
| CAC | - | - | - | CAULVR | CAC Upper-Limit Value Setting Register | 0x06 | 16 | R/W | 0x0000 | 0xFFFF |
| CAC | - | - | - | CALLVR | CAC Lower-Limit Value Setting Register | 0x08 | 16 | R/W | 0x0000 | 0xFFFF |
| CAC | - | - | - | CACNTBR | CAC Counter Buffer Register | 0x0A | 16 | R | 0x0000 | 0xFFFF |
| MSTP | - | - | - | MSTPCRB | Module Stop Control Register B | 0x000 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| MSTP | - | - | - | MSTPCRC | Module Stop Control Register C | 0x004 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| MSTP | - | - | - | MSTPCRD | Module Stop Control Register D | 0x008 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| I3C | - | - | - | PRTS | Protocol Selection Register | 0x000 | 32 | R/W | 0x00000001 | 0xFFFFFFFF |
| I3C | - | - | - | BCTL | Bus Control Register | 0x014 | 32 | R/W | 0xA0000181 | 0xFFFFFFFF |
| I3C | - | - | - | MSDVAD | Master Device Address Register | 0x018 | 32 | R/W | 0x807F0000 | 0xFFFFFFFF |
| I3C | - | - | - | RSTCTL | Reset Control Register | 0x020 | 32 | R/W | 0x0001007F | 0xFFFFFFFF |
| I3C | - | - | - | PRSST | Present State Register | 0x024 | 32 | R/W | 0x00000004 | 0xFFFFFFFF |
| I3C | - | - | - | INST | Internal Status Register | 0x030 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | INSTE | Internal Status Enable Register | 0x034 | 32 | R/W | 0x00000400 | 0xFFFFFFFF |
| I3C | - | - | - | INIE | Internal Interrupt Enable Register | 0x038 | 32 | R/W | 0x00000400 | 0xFFFFFFFF |
| I3C | - | - | - | INSTFC | Internal Status Force Register | 0x03C | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | DVCT | Device Characteristic Table Register | 0x044 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | IBINCTL | IBI Notify Control Register | 0x058 | 32 | R/W | 0x0000000B | 0xFFFFFFFF |

Table 3.4 Register description (6 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|--|----------------|------|-----|-------------|------------|
| I3C | - | - | - | BFCTL | Bus Function Control Register | 0x060 | 32 | R/W | 0x0000107 | 0xFFFFFFFF |
| I3C | - | - | - | SVCTL | Slave Control Register | 0x064 | 32 | R/W | 0x00018061 | 0xFFFFFFFF |
| I3C | - | - | - | REFCKCTL | Reference Clock Control Register | 0x070 | 32 | R/W | 0x00000007 | 0xFFFFFFFF |
| I3C | - | - | - | STDBR | Standard Bit Rate Register | 0x074 | 32 | R/W | 0xBF3FFFFFF | 0xFFFFFFFF |
| I3C | - | - | - | EXTBR | Extended Bit Rate Register | 0x078 | 32 | R/W | 0x3F3FFFFFF | 0xFFFFFFFF |
| I3C | - | - | - | BFRECDT | Bus Free Condition Detection Time Register | 0x07C | 32 | R/W | 0x000001FF | 0xFFFFFFFF |
| I3C | - | - | - | BAVLCDT | Bus Available Condition Detection Time Register | 0x080 | 32 | R/W | 0x000001FF | 0xFFFFFFFF |
| I3C | - | - | - | BIDLCDT | Bus Idle Condition Detection Time Register | 0x084 | 32 | R/W | 0x0003FFFF | 0xFFFFFFFF |
| I3C | - | - | - | OUTCTL | Output Control Register | 0x088 | 32 | R/W | 0x00008713 | 0xFFFFFFFF |
| I3C | - | - | - | INCTL | Input Control Register | 0x08C | 32 | R/W | 0x000000DF | 0xFFFFFFFF |
| I3C | - | - | - | TMOCTL | Timeout Control Register | 0x090 | 32 | R/W | 0x000000F3 | 0xFFFFFFFF |
| I3C | - | - | - | ACKCTL | Acknowledge Control Register | 0x0A0 | 32 | R/W | 0x00000002 | 0xFFFFFFFF |
| I3C | - | - | - | SCSTRCTL | SCL Stretch Control Register | 0x0A4 | 32 | R/W | 0x00000003 | 0xFFFFFFFF |
| I3C | - | - | - | SCSTLCTL | SCL Stalling Control Register | 0x0B0 | 32 | R/W | 0xF000FFFF | 0xFFFFFFFF |
| I3C | - | - | - | SVTDLG0 | Slave Transfer Data Length Register 0 | 0x0C0 | 32 | R/W | 0xFFFF0000 | 0xFFFFFFFF |
| I3C | - | - | - | CNDCTL | Condition Control Register | 0x140 | 32 | R/W | 0x00000007 | 0xFFFFFFFF |
| I3C | - | - | - | NCMDQP | Normal Command Queue Port Register | 0x150 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NRSPQP | Normal Response Queue Port Register | 0x154 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NTDTBP0 | Normal Transfer Data Buffer Port Register 0 | 0x158 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| I3C | - | - | - | NIBIQP | Normal IBI Queue Port Register | 0x17C | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NRSQP | Normal Receive Status Queue Port Register | 0x180 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NQTHCTL | Normal Queue Threshold Control Register | 0x190 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| I3C | - | - | - | NTBTHCTL0 | Normal Transfer Data Buffer Threshold Control Register 0 | 0x194 | 32 | R/W | 0x07070707 | 0xFFFFFFFF |
| I3C | - | - | - | NRQTHCTL | Normal Receive Status Queue Threshold Control Register | 0x1C0 | 32 | R/W | 0x000000FF | 0xFFFFFFFF |
| I3C | - | - | - | BST | Bus Status Register | 0x1D0 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | BSTE | Bus Status Enable Register | 0x1D4 | 32 | R/W | 0x00110117 | 0xFFFFFFFF |
| I3C | - | - | - | BIE | Bus Interrupt Enable Register | 0x1D8 | 32 | R/W | 0x00110117 | 0xFFFFFFFF |
| I3C | - | - | - | BSTFC | Bus Status Force Register | 0x1DC | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NTST | Normal Transfer Status Register | 0x1E0 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | NTSTE | Normal Transfer Status Enable Register | 0x1E4 | 32 | R/W | 0x0010023F | 0xFFFFFFFF |
| I3C | - | - | - | NTIE | Normal Transfer Interrupt Enable Register | 0x1E8 | 32 | R/W | 0x0010023F | 0xFFFFFFFF |
| I3C | - | - | - | NTSTFC | Normal Transfer Status Force Register | 0x1EC | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | BCST | Bus Condition Status Register | 0x210 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | SVST | Slave Status Register | 0x214 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| I3C | - | - | - | DATBAS0 | Device Address Table Basic Register 0 | 0x224 | 32 | R/W | 0xE0FFF07F | 0xFFFFFFFF |
| I3C | - | - | - | DATBAS1 | Device Address Table Basic Register 1 | 0x22C | 32 | R/W | 0xE0FFF07F | 0xFFFFFFFF |
| I3C | - | - | - | DATBAS2 | Device Address Table Basic Register 2 | 0x234 | 32 | R/W | 0xE0FFF07F | 0xFFFFFFFF |
| I3C | - | - | - | DATBAS3 | Device Address Table Basic Register 3 | 0x23C | 32 | R/W | 0xE0FFF07F | 0xFFFFFFFF |
| I3C | - | - | - | EXDATBAS | Extended Device Address Table Basic Register | 0x2A0 | 32 | R/W | 0xE0FF007F | 0xFFFFFFFF |
| I3C | - | - | - | SDATBAS0 | Slave Device Address Table Basic Register 0 | 0x2B0 | 32 | R/W | 0x007F07FF | 0xFFFFFFFF |

Table 3.4 Register description (8 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-------------|---------------|--|----------------|------|-----|-------------|------------|
| ADC12 | - | - | - | ADCER | A/D Control Extended Register | 0x00E | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADSTRGR | A/D Conversion Start Trigger Select Register | 0x010 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADEXICR | A/D Conversion Extended Input Control Registers | 0x012 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADANSB0 | A/D Channel Select Register B0 | 0x014 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADANSB1 | A/D Channel Select Register B1 | 0x016 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADDBLDR | A/D Data Duplexing Register | 0x018 | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADTSDR | A/D Temperature Sensor Data Register | 0x01A | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADOCDR | A/D Internal Reference Voltage Data Register | 0x01C | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADRD | A/D Self-Diagnosis Data Register | 0x01E | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | 4 | 0x2 | 5, 6, 9, 10 | ADDR%s | A/D Data Registers %s | 0x020 | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | 4 | 0x2 | 19-22 | ADDR%s | A/D Data Registers %s | 0x042 | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADDISCR | A/D Disconnection Detection Control Register | 0x07A | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADACSR | A/D Conversion Operation Mode Select Register | 0x07E | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADGSPCR | A/D Group Scan Priority Control Register | 0x080 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADDBLDRA | A/D Data Duplexing Register A | 0x084 | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADDBLDRB | A/D Data Duplexing Register B | 0x086 | 16 | R | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADHVREFCNT | A/D High-Potential/Low-Potential Reference Voltage Control Register | 0x08A | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADWINMON | A/D Compare Function Window A/B Status Monitor Register | 0x08C | 8 | R | 0x00 | 0xFF |
| ADC12 | - | - | - | ADCMPCR | A/D Compare Function Control Register | 0x090 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPANSER | A/D Compare Function Window A Extended Input Select Register | 0x092 | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADCMPLER | A/D Compare Function Window A Extended Input Comparison Condition Setting Register | 0x093 | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADCMPANSR0 | A/D Compare Function Window A Channel Select Register 0 | 0x094 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPANSR1 | A/D Compare Function Window A Channel Select Register 1 | 0x096 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPLR0 | A/D Compare Function Window A Comparison Condition Setting Register 0 | 0x098 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPLR1 | A/D Compare Function Window A Comparison Condition Setting Register 1 | 0x09A | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | 2 | 0x2 | 0-1 | ADCMPDR%s | A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register | 0x09C | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPSR0 | A/D Compare Function Window A Channel Status Register 0 | 0x0A0 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPSR1 | A/D Compare Function Window A Channel Status Register1 | 0x0A2 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADCMPSER | A/D Compare Function Window A Extended Input Channel Status Register | 0x0A4 | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADCMPBNSR | A/D Compare Function Window B Channel Select Register | 0x0A6 | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADWINLLB | A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register | 0x0A8 | 16 | R/W | 0x0000 | 0xFFFF |
| ADC12 | - | - | - | ADWINULB | A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register | 0x0AA | 16 | R/W | 0x0000 | 0xFFFF |

Table 3.4 Register description (9 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-------------|---------------|--|----------------|------|-----|-------------|------------|
| ADC12 | - | - | - | ADCMPBSR | A/D Compare Function Window B Status Register | 0x0AC | 8 | R/W | 0x00 | 0xFF |
| ADC12 | - | - | - | ADSSTRL | A/D Sampling State Register | 0x0DD | 8 | R/W | 0x0D | 0xFF |
| ADC12 | - | - | - | ADSSTRT | A/D Sampling State Register | 0x0DE | 8 | R/W | 0x0D | 0xFF |
| ADC12 | - | - | - | ADSSTRO | A/D Sampling State Register | 0x0DF | 8 | R/W | 0x0D | 0xFF |
| ADC12 | 4 | 0x1 | 5, 6, 9, 10 | ADSSTR%s | A/D Sampling State Register | 0x0E0 | 8 | R/W | 0x0D | 0xFF |
| SCI9 | - | - | - | SMR | Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0) | 0x00 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SMR_SMC1 | Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1) | 0x00 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | BRR | Bit Rate Register | 0x01 | 8 | R/W | 0xFF | 0xFF |
| SCI9 | - | - | - | SCR | Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0) | 0x02 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SCR_SMC1 | Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1) | 0x02 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | TDR | Transmit Data Register | 0x03 | 8 | R/W | 0xFF | 0xFF |
| SCI9 | - | - | - | SSR | Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0) | 0x04 | 8 | R/W | 0x84 | 0xFF |
| SCI9 | - | - | - | SSR_SMC1 | Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1) | 0x04 | 8 | R/W | 0x84 | 0xFF |
| SCI9 | - | - | - | RDR | Receive Data Register | 0x05 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SCMR | Smart Card Mode Register | 0x06 | 8 | R/W | 0xF2 | 0xFF |
| SCI9 | - | - | - | SEMR | Serial Extended Mode Register | 0x07 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SNFR | Noise Filter Setting Register | 0x08 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SIMR1 | IIC Mode Register 1 | 0x09 | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SIMR2 | IIC Mode Register 2 | 0x0A | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SIMR3 | IIC Mode Register 3 | 0x0B | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | SISR | IIC Status Register | 0x0C | 8 | R | 0x00 | 0xCB |
| SCI9 | - | - | - | SPMR | SPI Mode Register | 0x0D | 8 | R/W | 0x00 | 0xFF |
| SCI9 | - | - | - | TDRHL | Transmit Data Register | 0x0E | 16 | R/W | 0xFFFF | 0xFFFF |
| SCI9 | - | - | - | RDRHL | Receive Data Register | 0x10 | 16 | R | 0x0000 | 0xFFFF |
| SCI9 | - | - | - | MDDR | Modulation Duty Register | 0x12 | 8 | R/W | 0xFF | 0xFF |
| SCI9 | - | - | - | DCCR | Data Compare Match Control Register | 0x13 | 8 | R/W | 0x40 | 0xFF |
| SCI9 | - | - | - | CDR | Compare Match Data Register | 0x1A | 16 | R/W | 0x0000 | 0xFFFF |
| SCI9 | - | - | - | SPTR | Serial Port Register | 0x1C | 8 | R/W | 0x03 | 0xFF |
| SPI0 | - | - | - | SPCR | SPI Control Register | 0x00 | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SSLP | SPI Slave Select Polarity Register | 0x01 | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SPPCR | SPI Pin Control Register | 0x02 | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SPSR | SPI Status Register | 0x03 | 8 | R/W | 0x20 | 0xFF |
| SPI0 | - | - | - | SPDR | SPI Data Register | 0x04 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| SPI0 | - | - | - | SPDR_HA | SPI Data Register | 0x04 | 16 | R/W | 0x0000 | 0xFFFF |
| SPI0 | - | - | - | SPBR | SPI Bit Rate Register | 0x0A | 8 | R/W | 0xFF | 0xFF |
| SPI0 | - | - | - | SPDCR | SPI Data Control Register | 0x0B | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SPCKD | SPI Clock Delay Register | 0x0C | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SSLND | SPI Slave Select Negation Delay Register | 0x0D | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SPND | SPI Next-Access Delay Register | 0x0E | 8 | R/W | 0x00 | 0xFF |
| SPI0 | - | - | - | SPCR2 | SPI Control Register 2 | 0x0F | 8 | R/W | 0x00 | 0xFF |

Table 3.4 Register description (10 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|---|----------------|------|-----|-------------|------------|
| SPI0 | - | - | - | SPCMD0 | SPI Command Register 0 | 0x10 | 16 | R/W | 0x070D | 0xFFFF |
| CRC | - | - | - | CRCCR0 | CRC Control Register 0 | 0x00 | 8 | R/W | 0x00 | 0xFF |
| CRC | - | - | - | CRCCR1 | CRC Control Register 1 | 0x01 | 8 | R/W | 0x00 | 0xFF |
| CRC | - | - | - | CRCDIR | CRC Data Input Register | 0x04 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| CRC | - | - | - | CRCDIR_BY | CRC Data Input Register | 0x04 | 8 | R/W | 0x00 | 0xFF |
| CRC | - | - | - | CRCDOR | CRC Data Output Register | 0x08 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| CRC | - | - | - | CRCDOR_HA | CRC Data Output Register | 0x08 | 16 | R/W | 0x0000 | 0xFFFF |
| CRC | - | - | - | CRCDOR_BY | CRC Data Output Register | 0x08 | 8 | R/W | 0x00 | 0xFF |
| CRC | - | - | - | CRCSAR | Snoop Address Register | 0x0C | 16 | R/W | 0x0000 | 0xFFFF |
| GPT164-9 | - | - | - | GTWP | General PWM Timer Write-Protection Register | 0x00 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTSTR | General PWM Timer Software Start Register | 0x04 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTSTP | General PWM Timer Software Stop Register | 0x08 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCLR | General PWM Timer Software Clear Register | 0x0C | 32 | W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTSSR | General PWM Timer Start Source Select Register | 0x10 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTSPSR | General PWM Timer Stop Source Select Register | 0x14 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCSR | General PWM Timer Clear Source Select Register | 0x18 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTUPSR | General PWM Timer Up Count Source Select Register | 0x1C | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTDNSR | General PWM Timer Down Count Source Select Register | 0x20 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTICASR | General PWM Timer Input Capture Source Select Register A | 0x24 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTICBSR | General PWM Timer Input Capture Source Select Register B | 0x28 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCR | General PWM Timer Control Register | 0x2C | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTUDDTYC | General PWM Timer Count Direction and Duty Setting Register | 0x30 | 32 | R/W | 0x00000001 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTIOR | General PWM Timer I/O Control Register | 0x34 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTINTAD | General PWM Timer Interrupt Output Setting Register | 0x38 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTST | General PWM Timer Status Register | 0x3C | 32 | R/W | 0x00008000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTBER | General PWM Timer Buffer Enable Register | 0x40 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCNT | General PWM Timer Counter | 0x48 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRA | General PWM Timer Compare Capture Register A | 0x4C | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRB | General PWM Timer Compare Capture Register B | 0x50 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRC | General PWM Timer Compare Capture Register C | 0x54 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRE | General PWM Timer Compare Capture Register E | 0x58 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRD | General PWM Timer Compare Capture Register D | 0x5C | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTCCRF | General PWM Timer Compare Capture Register F | 0x60 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |

Table 3.4 Register description (11 of 11)

| Peripheral name | Dim | Dim inc. | Dim index | Register name | Description | Address offset | Size | R/W | Reset value | Reset mask |
|-----------------|-----|----------|-----------|---------------|---|----------------|------|-----|----------------------------|------------|
| GPT164-9 | - | - | - | GTPR | General PWM Timer Cycle Setting Register | 0x64 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTPBR | General PWM Timer Cycle Setting Buffer Register | 0x68 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTDTCR | General PWM Timer Dead Time Control Register | 0x88 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| GPT164-9 | - | - | - | GTDVU | General PWM Timer Dead Time Value Register U | 0x8C | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| GPT_OPS | - | - | - | OPSCR | Output Phase Switching Control Register | 0x00 | 32 | R/W | 0x00000000 | 0xFFFFFFFF |
| KINT | - | - | - | KRCTL | Key Return Control Register | 0x00 | 8 | R/W | 0x00 | 0xFF |
| KINT | - | - | - | KRF | Key Return Flag Register | 0x04 | 8 | R/W | 0x00 | 0xFF |
| KINT | - | - | - | KRM | Key Return Mode Register | 0x08 | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGT | AGT Counter Register | 0x00 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| AGTW0-1 | - | - | - | AGTCMB | AGT Compare Match B Register | 0x08 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| AGTW0-1 | - | - | - | AGTCMA | AGT Compare Match A Register | 0x04 | 32 | R/W | 0xFFFFFFFF | 0xFFFFFFFF |
| AGTW0-1 | - | - | - | AGTCR | AGT Control Register | 0x0C | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTMR1 | AGT Mode Register 1 | 0x0D | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTMR2 | AGT Mode Register 2 | 0x0E | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTIOC | AGT I/O Control Register | 0x10 | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTISR | AGT Event Pin Select Register | 0x11 | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTCMSR | AGT Compare Match Function Select Register | 0x12 | 8 | R/W | 0x00 | 0xFF |
| AGTW0-1 | - | - | - | AGTIOSEL | AGT Pin Select Register | 0x00F | 8 | R/W | 0x00 | 0xFF |
| FLCN | - | - | - | DFLCTL | Data Flash Enable Register | 0x0090 | 8 | R/W | 0x00 | 0xFF |
| FLCN | - | - | - | TSCDR | Temperature Sensor Calibration Data Register | 0x0228 | 16 | R | Unique value for each chip | 0x0000 |
| FLCN | - | - | - | FLDWAITR | Memory Wait Cycle Control Register for Data Flash | 0x3FC4 | 8 | R/W | 0x00 | 0xFF |
| FLCN | - | - | - | PFBER | Prefetch Buffer Enable Register | 0x3FC8 | 8 | R/W | 0x00 | 0xFF |

Note: Peripheral name = Name of peripheral
 Dim = Number of elements in an array of registers
 Dim inc. = Address increment between two simultaneous registers of a register array in the address map
 Dim index = Sub string that replaces the %s placeholder within the register name
 Register name = Name of register
 Description = Register description
 Address offset = Address of the register relative to the base address defined by the peripheral of the register
 Size = Bit width of the register
 Reset value = Default reset value of a register
 Reset mask = Identifies which register bits have a defined reset value

Revision History

Revision 1.00 — August 18, 2021

First edition, issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
 5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
- Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
 8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.