

# Renesas RA4W1 Group

Datasheet

## 32-Bit MCU

Renesas Advanced (RA) Family  
Renesas RA4 Series

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (<http://www.renesas.com>).

High efficiency 48-MHz Arm® Cortex®-M4 core, 512-KB code flash memory, 96-KB SRAM, Segment LCD Controller, Capacitive Touch Sensing Unit, Bluetooth Low Energy, USB 2.0 Full-Speed, 14-Bit A/D Converter, 12-Bit D/A Converter, security and safety features.

## Features

### ■ Arm Cortex-M4 Core with Floating Point Unit (FPU)

- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 48 MHz
- Support for 4-GB address space
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: ITM, DWT, FPB, TPIU, and ETB
- CoreSight™ debug port: JTAG-DP and SW-DP

### ■ Memory

- 512-KB code flash memory
- 8-KB data flash memory (100,000 erase/write cycles)
- 96-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity

- Bluetooth Low Energy
  - Bluetooth 5.0 core specification compliant BLE transceiver and link layer
  - Supporting LE 1M, 2M and Coded PHY, and LE Advertising extension
  - Dedicated AES-CCM (128-bit blocks) encryption circuit
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 4
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I<sup>2</sup>C bus interface (IIC) × 2
- Controller Area Network (CAN) module

### ■ Analog

- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) × 2 (for ACMPPLP)
- Low Power Analog Comparator (ACMPPLP) × 2
- Operational Amplifier (OPAMP) × 1
- Temperature Sensor (TSN)

### ■ Timers

- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 3
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety

- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management

- Low power modes
- Realtime Clock (RTC) with calendar and Battery Backup support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 4
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption

- AES128/256
- GHASH
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)

- Segment LCD Controller (SLCDC)
  - Up to 9 segments × 4 commons
  - Capacitive Touch Sensing Unit (CTSU)

### ■ Multiple Clock Sources

- Main clock oscillator (MOSC)
  - (1 to 20 MHz when VCC = 2.4 to 3.6 V)
  - (1 to 8 MHz when VCC = 1.8 to 2.4 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  - (24, 32, 48, 64 MHz when VCC = 2.4 to 3.6 V)
  - (24, 32, 48 MHz when VCC = 1.8 to 3.6 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General Purpose I/O Ports

- Up to 35 input/output pins
  - Up to 3 CMOS input
  - Up to 32 CMOS input/output
  - Up to 4 input/output 5 V tolerant
  - Up to 1 high current (20 mA)

### ■ Operating Voltage

- VCC: 1.8 to 3.6 V

### ■ Operating Temperature and Packages

- Ta = -40°C to +85°C
  - 56-pin QFN (7 mm × 7 mm, 0.4 mm pitch)

## 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a low-power and high-performance Arm Cortex®-M4 32-bit core running up to 48 MHz, with the following features:

- 512-KB code flash memory
- 96-KB SRAM
- Bluetooth Low Energy (BLE)
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

### 1.1 Function Outline

**Table 1.1 Arm core**

| Feature            | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Arm Cortex-M4 core | <ul style="list-style-type: none"> <li>• Maximum operating frequency: up to 48 MHz</li> <li>• Arm Cortex-M4 core:               <ul style="list-style-type: none"> <li>- Revision: r0p1-01rel0</li> <li>- Armv7E-M architecture profile</li> <li>- Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008.</li> </ul> </li> <li>• Arm Memory Protection Unit (Arm MPU):               <ul style="list-style-type: none"> <li>- Armv7 Protected Memory System Architecture</li> <li>- 8 protect regions</li> </ul> </li> <li>• SysTick timer:               <ul style="list-style-type: none"> <li>- Driven by SYSTICCLK (LOCO) or ICLK.</li> </ul> </li> </ul> |

**Table 1.2 Memory**

| Feature                      | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Code flash memory            | Maximum 512 KB of code flash memory. See section 43, Flash Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                               |
| Data flash memory            | 8 KB of data flash memory. See section 43, Flash Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Option-setting memory        | The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                   |
| Memory Mirror Function (MMF) | The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual. |
| SRAM                         | On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). An area in SRAM0 provides error correction capability using ECC. See section 42, SRAM in User's Manual.                                                                                                                                                                                                                                                                                                            |

**Table 1.3 System (1 of 2)**

| Feature                                            | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operating modes                                    | Two operating modes: <ul style="list-style-type: none"> <li>• Single-chip mode</li> <li>• SCI/USB boot mode.</li> </ul> See section 3, Operating Modes in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Resets                                             | 14 resets: <ul style="list-style-type: none"> <li>• RES pin reset</li> <li>• Power-on reset</li> <li>• VBATT-selected voltage power-on reset</li> <li>• Independent watchdog timer reset</li> <li>• Watchdog timer reset</li> <li>• Voltage monitor 0 reset</li> <li>• Voltage monitor 1 reset</li> <li>• SRAM parity error reset</li> <li>• SRAM ECC error reset</li> <li>• Bus master MPU error reset</li> <li>• Bus slave MPU error reset</li> <li>• Stack pointer error reset</li> <li>• Software reset.</li> </ul> See section 6, Resets in User's Manual.                                                                    |
| Low Voltage Detection (LVD)                        | The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Clocks                                             | <ul style="list-style-type: none"> <li>• Main clock oscillator (MOSC)</li> <li>• Sub-clock oscillator (SOSC)</li> <li>• High-speed on-chip oscillator (HOCO)</li> <li>• Middle-speed on-chip oscillator (MOCO)</li> <li>• Low-speed on-chip oscillator (LOCO)</li> <li>• PLL frequency synthesizer</li> <li>• IWDG-dedicated on-chip oscillator</li> <li>• Bluetooth-dedicated clock oscillator</li> <li>• Bluetooth-dedicated low-speed on-chip oscillator</li> <li>• Clock out support.</li> </ul> See section 9, Clock Generation Circuit in User's Manual.                                                                     |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.<br>When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.       |
| Interrupt Controller Unit (ICU)                    | The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                        |
| Key Interrupt Function (KINT)                      | A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                             |
| Low Power Mode                                     | Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                  |
| Battery backup function                            | A battery backup function is provided for partial powering by a battery. The battery powered area includes RTC, SOSC, LOCO, wakeup control, backup memory, VBATT_R low voltage detection, and switch between VCC and VBATT.<br>During normal operation, the battery powered area is powered by the main power supply, which is the VCC pin. When a VCC voltage fall is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin.<br>When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 12, Battery Backup Function in User's Manual. |
| Register write protection                          | The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 1.3 System (2 of 2)**

| Feature                           | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Memory Protection Unit (MPU)      | Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Watchdog Timer (WDT)              | The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 26, Watchdog Timer (WDT) in User's Manual.                                                                                                                                                                            |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 27, Independent Watchdog Timer (IWDT) in User's Manual. |

**Table 1.4 Event link**

| Feature                     | Functional description                                                                                                                                                                                                                                                                             |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual. |

**Table 1.5 Direct memory access**

| Feature                        | Functional description                                                                                                                                                                                                                                                                           |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.                                                                                                               |
| DMA Controller (DMAC)          | A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual. |

**Table 1.6 Timers**

| Feature                                  | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| General PWM Timer (GPT)                  | The General PWM Timer (GPT) is a 32-bit timer with 4 channels and a 16-bit timer with 3 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.                                                                                                              |
| Port Output Enable for GPT (POEG)        | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.                                                                                                                                                                                                                                                                                                                    |
| Asynchronous General Purpose Timer (AGT) | The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 24, Asynchronous General Purpose Timer (AGT) in User's Manual.                                                               |
| Realtime Clock (RTC)                     | The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings.<br>For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years.<br>For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 25, Realtime Clock (RTC) in User's Manual. |

**Table 1.7 Communication interfaces (1 of 2)**

| Feature                               | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Serial Communications Interface (SCI) | The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> <li>• Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA))</li> <li>• 8-bit clock synchronous interface</li> <li>• Simple IIC (master-only)</li> <li>• Simple SPI</li> <li>• Smart card interface.</li> </ul> The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.<br>SCI0 and SCI1 have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 29, Serial Communications Interface (SCI) in User's Manual. |
| I <sup>2</sup> C bus interface (IIC)  | The 2-channel I <sup>2</sup> C bus interface (IIC) conforms with and provides a subset of the NXP I <sup>2</sup> C (Inter-Integrated Circuit) bus interface functions. See section 30, I <sup>2</sup> C Bus Interface (IIC) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Serial Peripheral Interface (SPI)     | Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 32, Serial Peripheral Interface (SPI) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Controller Area Network (CAN) module  | The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications.<br>The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 31, Controller Area Network (CAN) Module in User's Manual.                                                                                                                                                                                                                      |
| USB 2.0 Full-Speed (USBFS) module     | The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system.<br>The MCU supports revision 1.2 of the Battery Charging Specification. See section 28, USB 2.0 Full-Speed Module (USBFS) in User's Manual.                                        |

**Table 1.7 Communication interfaces (2 of 2)**

| Feature                   | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bluetooth low energy(BLE) | <ul style="list-style-type: none"> <li>On-chip RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification</li> <li>Bit rates: 1 Mbps, 2 Mbps, 500 kbps, and 125 kbps</li> <li>LE Advertising extension support</li> <li>Includes an RF transceiver power supply (selectable as a DC-to-DC converter or linear regulator)</li> <li>On-chip matching circuit to help reduce the number of external parts</li> <li>Transmission power: +4 dBm support</li> </ul> |

**Table 1.8 Analog**

| Feature                               | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14-bit A/D Converter (ADC14)          | A 14-bit successive approximation A/D converter is provided. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 34, 14-Bit A/D Converter (ADC14) in User's Manual.                                                                                                                                                                                                                                                                                            |
| 12-bit D/A Converter (DAC12)          | The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 35, 12-Bit D/A Converter (DAC12) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8-bit D/A Converter (DAC8) for ACMPLP | The 8-bit D/A Converter (DAC8) converts data and does not include an output amplifier. The DAC8 is used only as the reference voltage for ACMPLP. See section 39, 8-Bit D/A Converter (DAC8) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Temperature Sensor (TSN)              | The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 36, Temperature Sensor (TSN) in User's Manual.                                                                                                                                                                                                                                                                                             |
| Low-Power Analog Comparator (ACMPLP)  | <p>The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0,1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU.</p> <p>The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 38, Low Power Analog Comparator (ACMPLP) in User's Manual.</p> |
| Operational Amplifier (OPAMP)         | The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A differential operational amplifier unit with two input pins and one output pin are provided. See section 37, Operational Amplifier (OPAMP) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 1.9 Human machine interfaces**

| Feature                              | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Segment LCD Controller (SLCDC)       | <p>The SLCDC provides the following functions:</p> <ul style="list-style-type: none"> <li>Waveform A or B selectable</li> <li>The LCD driver voltage generator uses an external resistance division method</li> <li>Automatic output of segment and common signals based on automatic display data register read</li> <li>The LCD can be made to blink.</li> </ul> <p>See section 44, Segment LCD Controller (SLCDC) in User's Manual.</p>                                                                |
| Capacitive Touch Sensing Unit (CTSU) | The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode. See section 40, Capacitive Touch Sensing Unit (CTSU) in User's Manual. |

**Table 1.10 Data processing**

| Feature                                  | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 33, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |
| Data Operation Circuit (DOC)             | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 41, Data Operation Circuit (DOC) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 1.11 Security**

| Feature                       | Functional description                                                                                                                                                                                                                                                                                         |
|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Secure Crypto Engine 5 (SCE5) | <ul style="list-style-type: none"><li>• Security algorithm:<ul style="list-style-type: none"><li>- Symmetric algorithm: AES</li></ul></li><li>• Other support features:<ul style="list-style-type: none"><li>- TRNG (True Random Number Generator)</li><li>- Hash-value generation: GHASH.</li></ul></li></ul> |

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group may have a subset of the features.

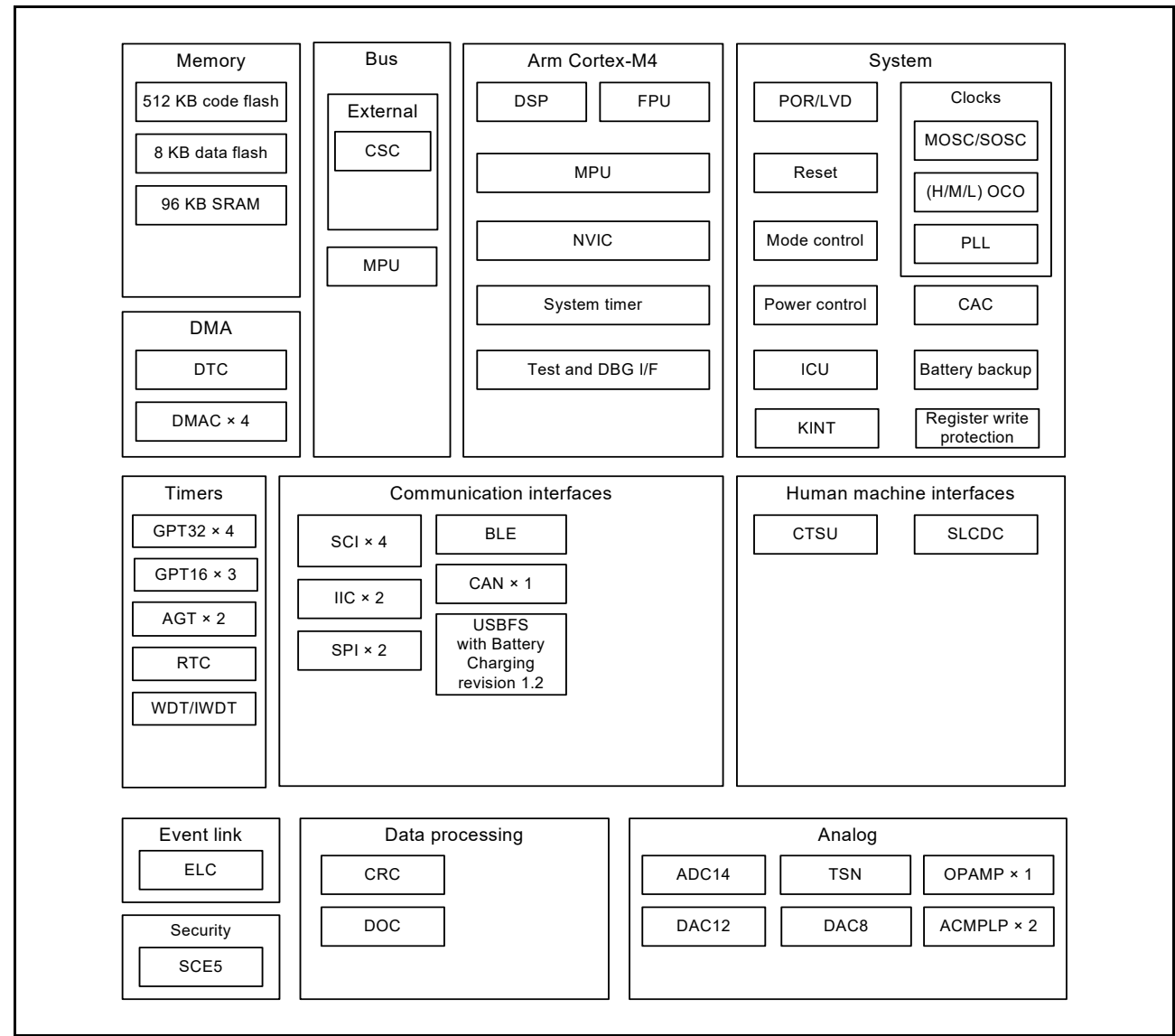


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows how to read the product part number information, including memory capacity, and package type. Table 1.13 shows a product list.

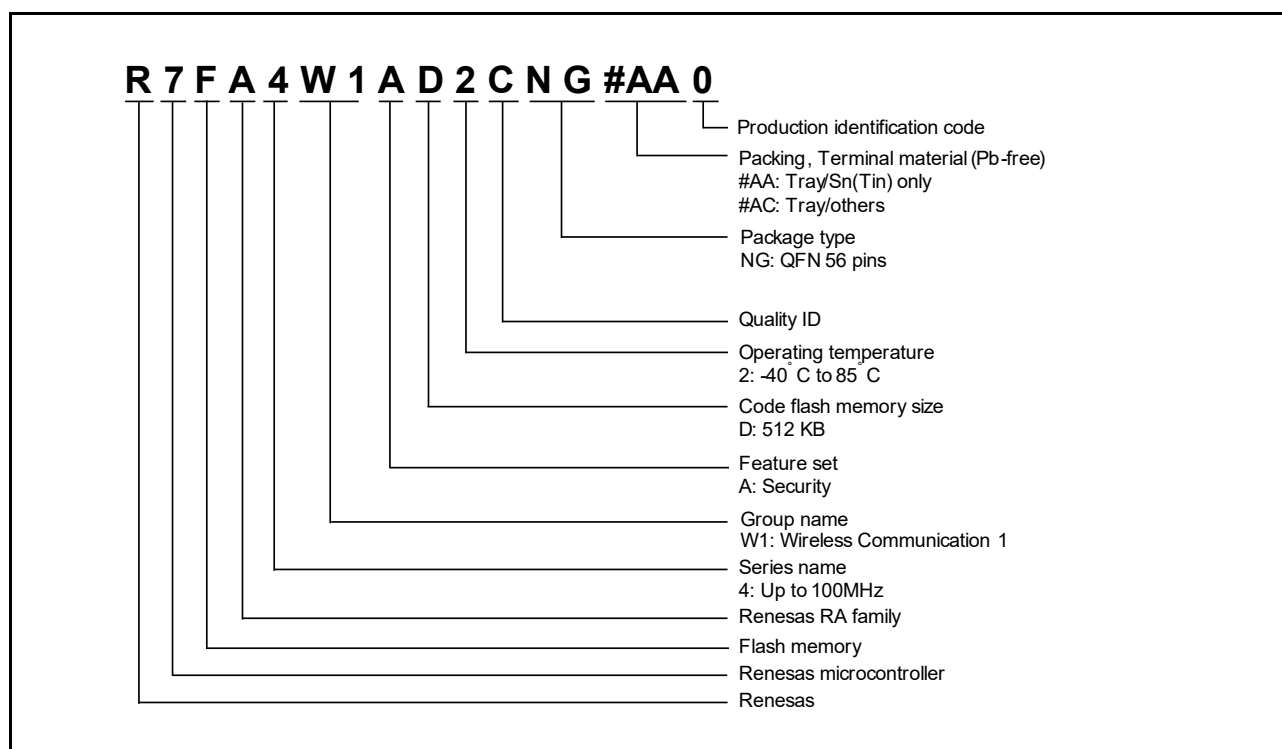


Figure 1.2 Part numbering scheme

Table 1.12 Product list

| Product part number | Orderable part number | Code flash | Data flash | SRAM  | Operating temperature |
|---------------------|-----------------------|------------|------------|-------|-----------------------|
| R7FA4W1AD2CNG       | R7FA4W1AD2CNG#AA0     | 512 KB     | 8 KB       | 96 KB | -40 to +85°C          |

## 1.4 Function Comparison

**Table 1.13 Function comparison**

| Part numbers      |                  | R7FA4W1AD2CNG                                                                          |
|-------------------|------------------|----------------------------------------------------------------------------------------|
| Pin count         |                  | 56                                                                                     |
| Package           |                  | QFN                                                                                    |
| Code flash memory |                  | 512 KB                                                                                 |
| Data flash memory |                  | 8 KB                                                                                   |
| SRAM              |                  | 96 KB                                                                                  |
|                   | Parity           | 80 KB                                                                                  |
|                   | ECC              | 16 KB                                                                                  |
|                   |                  |                                                                                        |
| System            | CPU clock        | 48 MHz                                                                                 |
|                   | Backup registers | 512 bytes                                                                              |
|                   | ICU              | Yes                                                                                    |
|                   | KINT             | 8                                                                                      |
| Event control     | ELC              | Yes                                                                                    |
| DMA               | DTC              | Yes                                                                                    |
|                   | DMAC             | 4                                                                                      |
| Timers            | GPT32            | 4                                                                                      |
|                   | GPT16            | 3                                                                                      |
|                   | AGT              | 2                                                                                      |
|                   | RTC              | Yes                                                                                    |
|                   | WDT/IWDT         | Yes                                                                                    |
| Communication     | SCI              | 6                                                                                      |
|                   | IIC              | 2                                                                                      |
|                   | SPI              | 2                                                                                      |
|                   | CAN              | 1                                                                                      |
|                   | USBFS            | Yes                                                                                    |
|                   | BLE              | An RF transceiver and link layer compliant with Bluetooth 5.0 low energy specification |
| Analog            | ADC14            | 8                                                                                      |
|                   | DAC12            | 1                                                                                      |
|                   | DAC8             | 2                                                                                      |
|                   | ACMPLP           | 2                                                                                      |
|                   | OPAMP            | 1                                                                                      |
|                   | TSN              | Yes                                                                                    |
| HMI               | SLCDC            | 4 com × 9 seg                                                                          |
|                   | CTSU             | 11                                                                                     |
| Data processing   | CRC              | Yes                                                                                    |
|                   | DOC              | Yes                                                                                    |
| Security          |                  | SCE5                                                                                   |

## 1.5 Pin Functions

| Function               | Signal                                               | I/O    | Description                                                                                                                                                            |
|------------------------|------------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power supply           | VCC                                                  | Input  | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.               |
|                        | VCL                                                  | Input  | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.                          |
|                        | VSS                                                  | Input  | Ground pin. Connect it to the system power supply (0 V).                                                                                                               |
|                        | VBATT                                                | Input  | Backup power pin                                                                                                                                                       |
| Clock                  | XTAL                                                 | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.                                                                             |
|                        | EXTAL                                                | Input  |                                                                                                                                                                        |
|                        | XCIN                                                 | Input  | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.                                                                    |
|                        | XCOUT                                                | Output |                                                                                                                                                                        |
|                        | CLKOUT_RF                                            | Output | Bluetooth-dedicated clock output pin for output of a 1-, 2-, or 4-MHz signal                                                                                           |
|                        | XTAL1_RF                                             | Input  | Pins for connecting the Bluetooth-dedicated clock oscillator. Connect a 32-MHz oscillator to these pins.                                                               |
|                        | XTAL2_RF                                             | Output |                                                                                                                                                                        |
|                        | CLKOUT                                               | Output | Clock output pin                                                                                                                                                       |
| Operating mode control | MD                                                   | Input  | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state. |
| System control         | RES                                                  | Input  | Reset signal input pin. The MCU enters the reset state when this signal goes low.                                                                                      |
| CAC                    | CACREF                                               | Input  | Measurement reference clock input pin                                                                                                                                  |
| Interrupt              | NMI                                                  | Input  | Non-maskable interrupt request pin                                                                                                                                     |
|                        | IRQ0 to IRQ4, IRQ6, IRQ7, IRQ9, IRQ11, IRQ14, IRQ15  | Input  | Maskable interrupt request pins                                                                                                                                        |
| KINT                   | KR00 to KR07                                         | Input  | A key interrupt can be generated by inputting a falling edge to the key interrupt input pins                                                                           |
| On-chip debug          | TMS                                                  | I/O    | On-chip emulator pins                                                                                                                                                  |
|                        | TDI                                                  | Input  |                                                                                                                                                                        |
|                        | TCK                                                  | Input  |                                                                                                                                                                        |
|                        | TDO                                                  | Output |                                                                                                                                                                        |
|                        | SWDIO                                                | I/O    | Serial Wire debug Data Input/Output pin                                                                                                                                |
|                        | SWCLK                                                | Input  | Serial Wire Clock pin                                                                                                                                                  |
|                        | SWO                                                  | Output | Serial Wire trace Output pin                                                                                                                                           |
| Battery backup         | VBATWIO0                                             | I/O    | Output wakeup signal for the VBATT wakeup control function.<br>External event input for the VBATT wakeup control function.                                             |
| GPT                    | GTETRGA, GTETRGB                                     | Input  | External trigger input pin                                                                                                                                             |
|                        | GTIO0A to GTIOA5A, GTIO8A, GTIO0B to GTIOA5B, GTIO8B | I/O    | Input capture, Output capture, or PWM output pin                                                                                                                       |
|                        | GTIU                                                 | Input  | Hall sensor input pin U                                                                                                                                                |
|                        | GTIV                                                 | Input  | Hall sensor input pin V                                                                                                                                                |
|                        | GTIW                                                 | Input  | Hall sensor input pin W                                                                                                                                                |
|                        | GTOUUP                                               | Output | 3-phase PWM output for BLDC motor control (positive U phase)                                                                                                           |
|                        | GTOULO                                               | Output | 3-phase PWM output for BLDC motor control (negative U phase)                                                                                                           |
|                        | GTOVUP                                               | Output | 3-phase PWM output for BLDC motor control (positive V phase)                                                                                                           |
|                        | GTOVLO                                               | Output | 3-phase PWM output for BLDC motor control (negative V phase)                                                                                                           |
|                        | GTOUWP                                               | Output | 3-phase PWM output for BLDC motor control (positive W phase)                                                                                                           |
|                        | GTOWLO                                               | Output | 3-phase PWM output for BLDC motor control (negative W phase)                                                                                                           |
| AGT                    | AGTEE0, AGTEE1                                       | Input  | External event input enable                                                                                                                                            |
|                        | AGTIO0, AGTIO1                                       | I/O    | External event input and pulse output                                                                                                                                  |
|                        | AGTO0, AGTO1                                         | Output | Pulse output                                                                                                                                                           |
|                        | AGTOB0                                               | Output | Output compare match B output                                                                                                                                          |

| Function            | Signal                                            | I/O    | Description                                                                                                                                                                                                     |
|---------------------|---------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RTC                 | RTCCOUT                                           | Output | Output pin for 1-Hz/64-Hz clock                                                                                                                                                                                 |
|                     | RTCCIC0, RTCCIC2                                  | Input  | Time capture event input pins                                                                                                                                                                                   |
| SCI                 | SCK0, SCK1, SCK4, SCK9                            | I/O    | Input/output pins for the clock (clock synchronous mode)                                                                                                                                                        |
|                     | RXD0, RXD1, RXD4, RXD9                            | Input  | Input pins for received data (asynchronous mode/clock synchronous mode)                                                                                                                                         |
|                     | TXD0, TXD1, TXD4, TXD9                            | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode)                                                                                                                                     |
|                     | CTS0_RTS0, CTS1_RTS1, CTS4_RTS4, CTS9_RTS9        | I/O    | Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low                                                                                |
|                     | SCL0, SCL1, SCL4, SCL9                            | I/O    | Input/output pins for the IIC clock (simple IIC)                                                                                                                                                                |
|                     | SDA0, SDA1, SDA4, SDA9                            | I/O    | Input/output pins for the IIC data (simple IIC)                                                                                                                                                                 |
|                     | SCK0, SCK1, SCK4, SCK9                            | I/O    | Input/output pins for the clock (simple SPI)                                                                                                                                                                    |
|                     | MISO0, MISO1, MISO4, MISO9                        | I/O    | Input/output pins for slave transmission of data (simple SPI)                                                                                                                                                   |
|                     | MOSI0, MOSI1, MOSI4, MOSI9                        | I/O    | Input/output pins for master transmission of data (simple SPI)                                                                                                                                                  |
|                     | SS0, SS1, SS4, SS9                                | Input  | Slave-select input pins (simple SPI), active-low                                                                                                                                                                |
| IIC                 | SCL0 to SCL1                                      | I/O    | Input/output pins for clock                                                                                                                                                                                     |
|                     | SDA0 to SDA1                                      | I/O    | Input/output pins for data                                                                                                                                                                                      |
| SPI                 | RSPCKA, RSPCKB                                    | I/O    | Clock input/output pin                                                                                                                                                                                          |
|                     | MOSIA, MOSIB                                      | I/O    | Inputs or outputs data output from the master                                                                                                                                                                   |
|                     | MISOA, MISOB                                      | I/O    | Inputs or outputs data output from the slave                                                                                                                                                                    |
|                     | SSLA0, SSLB0                                      | I/O    | Input or output pin for slave selection                                                                                                                                                                         |
|                     | SSLA1, SSLA2, SSLA3, SSLB1, SSLB3                 | Output | Output pin for slave selection                                                                                                                                                                                  |
| CAN                 | CRX0                                              | Input  | Receive data                                                                                                                                                                                                    |
|                     | CTX0                                              | Output | Transmit data                                                                                                                                                                                                   |
| USBFS               | VSS_USB                                           | Input  | Ground pins                                                                                                                                                                                                     |
|                     | VCC_USB_LDO                                       | Input  | Power supply pin for USB transceiver. Apply the same voltage as VCC_USB.                                                                                                                                        |
|                     | VCC_USB                                           | I/O    | Input: Power supply pin for USB transceiver.                                                                                                                                                                    |
|                     | USB_DP                                            | I/O    | D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.                                                                                                           |
|                     | USB_DM                                            | I/O    | D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.                                                                                                           |
|                     | USB_VBUS                                          | Input  | USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller. |
|                     | USB_VBUSEN                                        | Output | VBUS (5 V) supply enable signal for external power supply chip                                                                                                                                                  |
| Analog power supply | USB_OVRCURA, USB_OVRCURB                          | Input  | External overcurrent detection signals should be connected to these pins.                                                                                                                                       |
|                     | AVCC0                                             | Input  | Analog block power supply pin                                                                                                                                                                                   |
|                     | AVSS0                                             | Input  | Analog block power supply ground pin                                                                                                                                                                            |
|                     | VREFH0                                            | Input  | Reference power supply pin                                                                                                                                                                                      |
| ADC14               | VREFL0                                            | Input  | Reference power supply ground pin                                                                                                                                                                               |
|                     | AN004 to AN006, AN009, AN010, AN017, AN019, AN020 | Input  | Input pins for the analog signals to be processed by the A/D converter                                                                                                                                          |
|                     | ADTRG0                                            | Input  | Input pins for the external trigger signals that start the A/D conversion, active-low                                                                                                                           |
| DAC12               | DA0                                               | Output | Output pins for the analog signals to be processed by the D/A converter                                                                                                                                         |

| Function                   | Signal                                                           | I/O    | Description                                                                               |
|----------------------------|------------------------------------------------------------------|--------|-------------------------------------------------------------------------------------------|
| Comparator output          | VCOUT                                                            | Output | Comparator output pin                                                                     |
| ACMPLP                     | CMPREF0, CMPREF1                                                 | Input  | Reference voltage input pins                                                              |
|                            | CMPIN0, CMPIN1                                                   | Input  | Analog voltage input pins                                                                 |
| OPAMP                      | AMP2+                                                            | Input  | Analog voltage input pins                                                                 |
|                            | AMP2-                                                            | Input  | Analog voltage input pins                                                                 |
|                            | AMP2O                                                            | Output | Analog voltage output pins                                                                |
| CTSU                       | TS00, TS01, TS03, TS10, TS12, TS13, TS18, TS28, TS30, TS31, TS34 | Input  | Capacitive touch detection pins (touch pins)                                              |
|                            | TSCAP                                                            | —      | Secondary power supply pin for the touch driver                                           |
| I/O ports                  | P004, P010, P011, P014, P015                                     | I/O    | General-purpose input/output pins                                                         |
|                            | P100 to P111                                                     | I/O    | General-purpose input/output pins                                                         |
|                            | P200                                                             | Input  | General-purpose input pin                                                                 |
|                            | P201, P204 to P206, P212, P213                                   | I/O    | General-purpose input/output pins                                                         |
|                            | P214, P215                                                       | Input  | General-purpose input pins                                                                |
|                            | P300                                                             | I/O    | General-purpose input/output pins                                                         |
|                            | P402, P404, P407, P409, P414                                     | I/O    | General-purpose input/output pins                                                         |
|                            | P501                                                             | I/O    | General-purpose input/output pins                                                         |
| SLCDC                      | P914, P915                                                       | I/O    | General-purpose input/output pins                                                         |
|                            | VL1, VL2, VL4                                                    | I/O    | Voltage pin for driving the LCD                                                           |
|                            | COM0 to COM3                                                     | Output | Common signal output pins for the LCD controller/driver                                   |
| BLE (Bluetooth Low Energy) | SEG6, SEG9, SEG11, SEG12, SEG20, SEG23, SEG49, SEG52, SEG53      | Output | Segment signal output pins for the LCD controller/driver                                  |
|                            | ANT                                                              | I/O    | RF single I/O pin for the RF transceiver<br>Set the impedance of the signal line to 50 Ω. |
|                            | DCLOUT                                                           | Output | RF transceiver power-supply output pin                                                    |
|                            | DCLIN_A                                                          | Input  | RF transceiver power-supply output connection pin                                         |
|                            | DCLIN_D                                                          | Input  | RF transceiver power-supply output connection pin                                         |
|                            | VCC_RF                                                           | Input  | RF transceiver power supply pin                                                           |
|                            | AVCC_RF                                                          | Input  | RF transceiver power supply pin                                                           |
|                            | VSS_RF                                                           | Input  | RF transceiver ground pin                                                                 |

## 1.6 Pin Assignments

Figure 1.3 shows the pin assignments.

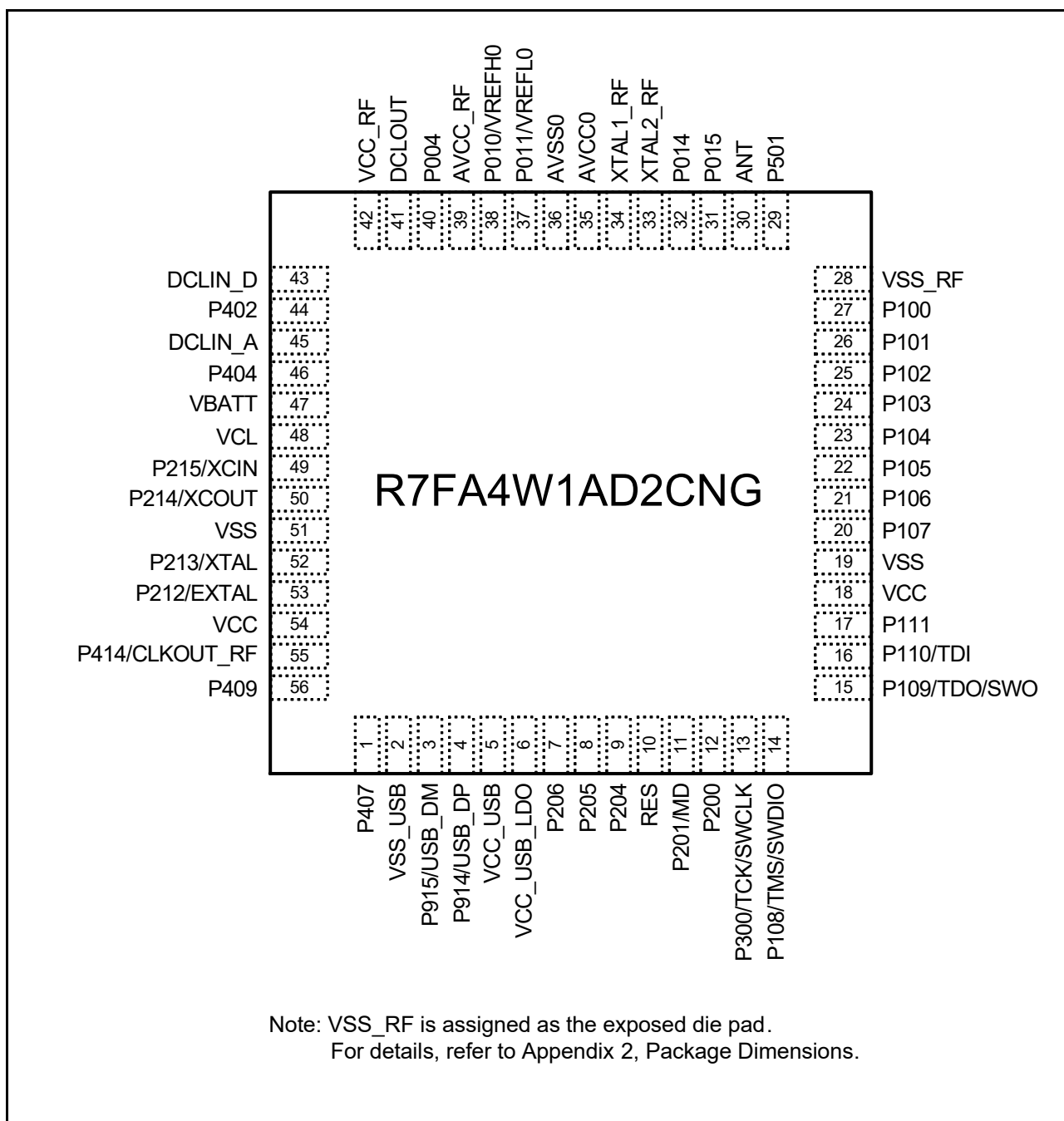


Figure 1.3 Pin assignment for QFN 56-pin (top view)

## 1.7 Pin Lists

| Pin number |                                         |            |           | Timers |               |         |        | Communication interfaces |                                   |      |        |    |               | Analog       |         |       | HMI   |  |
|------------|-----------------------------------------|------------|-----------|--------|---------------|---------|--------|--------------------------|-----------------------------------|------|--------|----|---------------|--------------|---------|-------|-------|--|
| QFN56      | Power, System, Clock, Debug, CAC, VBATT | Interrupt  | I/O Ports | AGT    | GPT_OPS, POEG | GPT     | RTC    | USBFS, CAN               | SCI                               | IIC  | SPI    | RF | ADC14         | DAC12, OPAMP | ACMPLP  | SLCDC | CTSU  |  |
| 1          |                                         |            | P407      | AGTIO0 |               |         | RTCOUT | USB_VBUS                 | CTS4_RTS4 /SS4                    | SDA0 | SSLB3  |    | ADTRG0        |              |         | SEG11 | TS3   |  |
| 2          | VSS_USB                                 |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 3          |                                         |            | P915      |        |               |         |        | USB_DM                   |                                   |      |        |    |               |              |         |       |       |  |
| 4          |                                         |            | P914      |        |               |         |        | USB_DP                   |                                   |      |        |    |               |              |         |       |       |  |
| 5          | VCC_USB                                 |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 6          | VCC_USB_LDO                             |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 7          |                                         | IRQ0       | P206      |        | GTIU          |         |        | USB_VBUS_EN              | RXD4/ MISO4/SCL4                  | SDA1 | SSLB1  |    |               |              |         | SEG12 | TS1   |  |
| 8          | CLKOUT                                  | IRQ1       | P205      | AGTO1  | GTIV          | GTIOC4A |        | USB_OVRC_UR A            | TXD4/ MOSI4/ SDA4/ CTS9_RTS9 /SS9 | SCL1 | SSLB0  |    |               |              |         | SEG20 | TSCAP |  |
| 9          | CACREF                                  |            | P204      | AGTO1  | GTIW          | GTIOC4B |        | USB_OVRC_UR B            | SCK4/SCK9                         | SCL0 | RSPCKB |    |               |              |         | SEG23 | TS0   |  |
| 10         | RES                                     |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 11         | MD                                      |            | P201      |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 12         |                                         | NMI        | P200      |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 13         | TCK/ SWCLK                              |            | P300      |        | GTOUUP        | GTIOC0A |        |                          |                                   |      | SSLB1  |    |               |              |         |       |       |  |
| 14         | TMS/ SWDIO                              |            | P108      |        | GTOULO        | GTIOC0B |        |                          | CTS9_RTS9 /SS9                    |      | SSLB0  |    |               |              |         |       |       |  |
| 15         | TDO/ SWO/ CLKOUT                        |            | P109      |        | GTOVUP        | GTIOC1A |        | CTX0                     | SCK1/ TXD9/ MOSI9/ SDA9           |      | MOSIB  |    |               |              |         | SEG52 | TS10  |  |
| 16         | TDI                                     | IRQ3       | P110      |        | GTOVLO        | GTIOC1B |        | CRX0                     | RXD9/ MISO9/SCL9                  |      | MISOB  |    |               |              | VCOUT   | SEG53 |       |  |
| 17         |                                         | IRQ4       | P111      |        |               | GTIOC3A |        |                          | SCK9                              |      | RSPCKB |    |               |              |         |       | TS12  |  |
| 18         | VCC                                     |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 19         | VSS                                     |            |           |        |               |         |        |                          |                                   |      |        |    |               |              |         |       |       |  |
| 20         |                                         | KR07       | P107      |        |               | GTIOC8A |        |                          |                                   |      |        |    |               |              |         | COM3  |       |  |
| 21         |                                         | KR06       | P106      |        |               | GTIOC8B |        |                          |                                   |      | SSLA3  |    |               |              |         | COM2  |       |  |
| 22         |                                         | KR05/ IRQ0 | P105      |        | GTETRGA       | GTIOC1A |        |                          |                                   |      | SSLA2  |    |               |              |         | COM1  | TS34  |  |
| 23         |                                         | KR04/ IRQ1 | P104      |        | GTETRGB       | GTIOC1B |        |                          | RXD0/ MISO0/SCL0                  |      | SSLA1  |    |               |              |         | COM0  | TS13  |  |
| 24         |                                         | KR03       | P103      |        | GTOWUP        | GTIOC2A |        | CTX0                     | CTS0_RTS0 /SS0                    |      | SSLA0  |    | AN019         |              | CMPREF1 | VL4   |       |  |
| 25         |                                         | KR02       | P102      | AGTO0  | GTOWLO        | GTIOC2B |        | CRX0                     | SCK0                              |      | RSPCKA |    | AN020/ ADTRG0 |              | CMPIN1  |       |       |  |
| 26         |                                         | KR01/ IRQ1 | P101      | AGTEE0 | GTETRGB       | GTIOC5A |        |                          | TXD0/ MOSI0/ SDA0/ CTS1_RTS1 /SS1 | SDA1 | MOSIA  |    |               |              | CMPREF0 | VL2   |       |  |

| Pin number |                                         |               |           | Timers            |               |         |        | Communication interfaces |                                  |      |       |          | Analog |              |        | HMI   |      |
|------------|-----------------------------------------|---------------|-----------|-------------------|---------------|---------|--------|--------------------------|----------------------------------|------|-------|----------|--------|--------------|--------|-------|------|
| QFN56      | Power, System, Clock, Debug, CAC, VBATT | Interrupt     | I/O Ports | AGT               | GPT_OPS, POEG | GPT     | RTC    | USBFS, CAN               | SCI                              | IIC  | SPI   | RF       | ADC14  | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 27         |                                         | KR00/<br>IRQ2 | P100      | AGTIO0            | GTETRGA       | GTIOC5B |        |                          | RXD0/<br>MISO0/<br>SCL0/<br>SCK1 | SCL1 | MISOA |          |        |              | CMPIN0 | VL1   |      |
| 28         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | VSS_RF   |        |              |        |       |      |
| 29         |                                         | IRQ11         | P501      | AGTOB0            | GTIV          | GTIOC2B |        | USB_OVRC<br>URA          |                                  |      |       |          | AN017  |              | CMPIN1 | SEG49 |      |
| 30         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | ANT      |        |              |        |       |      |
| 31         |                                         | IRQ7          | P015      |                   |               |         |        |                          |                                  |      |       |          | AN010  |              |        |       | TS28 |
| 32         |                                         |               | P014      |                   |               |         |        |                          |                                  |      |       |          | AN009  | DA0          |        |       |      |
| 33         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | XTAL2_RF |        |              |        |       |      |
| 34         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | XTAL1_RF |        |              |        |       |      |
| 35         | AVCC0                                   |               |           |                   |               |         |        |                          |                                  |      |       |          |        |              |        |       |      |
| 36         | AVSS0                                   |               |           |                   |               |         |        |                          |                                  |      |       |          |        |              |        |       |      |
| 37         | VREFL0                                  | IRQ15         | P011      |                   |               |         |        |                          |                                  |      |       |          | AN006  | AMP2+        |        |       | TS31 |
| 38         | VREFH0                                  | IRQ14         | P010      |                   |               |         |        |                          |                                  |      |       |          | AN005  | AMP2-        |        |       | TS30 |
| 39         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | AVCC_RF  |        |              |        |       |      |
| 40         |                                         | IRQ3          | P004      |                   |               |         |        |                          |                                  |      |       |          | AN004  | AMP20        |        |       |      |
| 41         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | DCLOUT   |        |              |        |       |      |
| 42         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | VCC_RF   |        |              |        |       |      |
| 43         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | DCLIN_D  |        |              |        |       |      |
| 44         | VBATWIO<br>0                            | IRQ4          | P402      | AGTIO0/<br>AGTIO1 |               |         | RTCIC0 | CRX0                     | RXD1/<br>MISO1/SCL1              |      |       |          |        |              |        | SEG6  | TS18 |
| 45         |                                         |               |           |                   |               |         |        |                          |                                  |      |       | DCLIN_A  |        |              |        |       |      |
| 46         |                                         |               | P404      |                   |               | GTIOC3B | RTCIC2 |                          |                                  |      |       |          |        |              |        |       |      |
| 47         | VBATT                                   |               |           |                   |               |         |        |                          |                                  |      |       |          |        |              |        |       |      |
| 48         | VCL                                     |               |           |                   |               |         |        |                          |                                  |      |       |          |        |              |        |       |      |

| Pin number |                                         |           |           | Timers |               |         |     | Communication interfaces |     |     |       |               | Analog |              |        | HMI   |      |
|------------|-----------------------------------------|-----------|-----------|--------|---------------|---------|-----|--------------------------|-----|-----|-------|---------------|--------|--------------|--------|-------|------|
| QFN56      | Power, System, Clock, Debug, CAC, VBATT | Interrupt | I/O Ports | AGT    | GPT_OPS, POEG | GPT     | RTC | USBFS, CAN               | SCI | IIC | SPI   | RF            | ADC14  | DAC12, OPAMP | ACMPLP | SLCDC | CTSU |
| 49         | XCIN                                    |           | P215      |        |               |         |     |                          |     |     |       |               |        |              |        |       |      |
| 50         | XCOUT                                   |           | P214      |        |               |         |     |                          |     |     |       |               |        |              |        |       |      |
| 51         | VSS                                     |           |           |        |               |         |     |                          |     |     |       |               |        |              |        |       |      |
| 52         | XTAL                                    | IRQ2      | P213      |        | GTETRGA       | GTIOC0A |     | TXD1/<br>MOSI1/<br>SDA1  |     |     |       |               |        |              |        |       |      |
| 53         | EXTAL                                   | IRQ3      | P212      | AGTEE1 | GTETRGB       | GTIOC0B |     | RXD1/<br>MISO1/SCL1      |     |     |       |               |        |              |        |       |      |
| 54         | VCC                                     |           |           |        |               |         |     |                          |     |     |       |               |        |              |        |       |      |
| 55         |                                         | IRQ9      | P414      |        |               | GTIOC0B |     |                          |     |     | SSLA1 | CLKOUT_<br>RF |        |              |        |       |      |
| 56         |                                         | IRQ6      | P409      |        | GTOWUP        | GTIOC5A |     | USB_EXICE<br>N           |     |     |       |               |        |              |        | SEG9  |      |

## 2. Electrical Characteristics

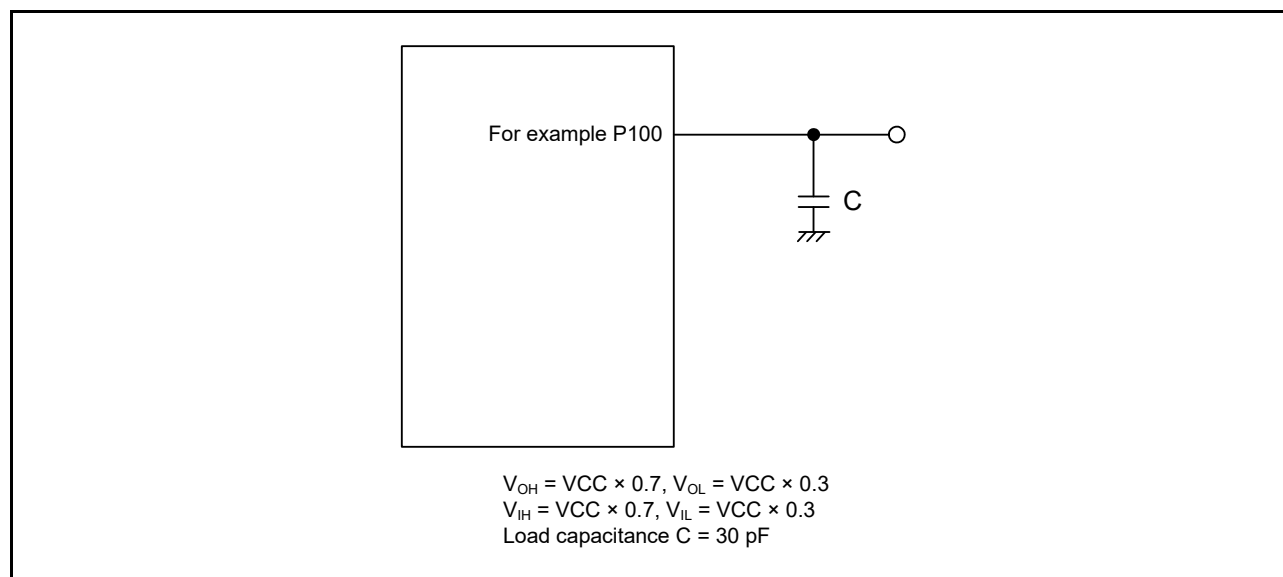
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$VCC^{*1} = AVCC0 = VCC\_USB^{*2} = VCC\_USB\_LDO^{*2} = VCC\_RF = AVCC\_RF = 1.8$  to  $3.6V$ ,  $VREFH0 = 1.8$  to  $AVCC0$ ,  $VBATT = 1.8$  to  $3.6V$ ,  $VSS = AVSS0 = VREFL0 = VSS\_RF = VSS\_USB = 0V$ ,  $T_a = T_{opr}$

Note 1. The typical condition is set to  $VCC = 3.3V$ .

Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.



**Figure 2.1 Input or output timing measurement conditions**

The measurement conditions of timing specifications in each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pin to meet your conditions.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC specification of each function is not guaranteed.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Parameter                      |                                            | Symbol           | Value               | Unit |
|--------------------------------|--------------------------------------------|------------------|---------------------|------|
| Power supply voltage           |                                            | VCC              | −0.5 to +4.0        | V    |
| Input voltage                  | 5V-tolerant ports*1                        | V <sub>in</sub>  | −0.3 to +6.5        | V    |
|                                | P004, P010, P011, P014, P015               | V <sub>in</sub>  | −0.3 to AVCC0 + 0.3 | V    |
|                                | ANT                                        | V <sub>in</sub>  | −1.0 to +1.4        | V    |
|                                | XTAL1_RF, XTAL2_RF                         | V <sub>in</sub>  | −0.3 to +1.4        | V    |
|                                | DCLIN_A, DCLIN_D                           | V <sub>in</sub>  | −0.3 to +2.2        | V    |
|                                | Others                                     | V <sub>in</sub>  | −0.3 to VCC + 0.3   | V    |
| Reference power supply voltage |                                            | VREFH0           | −0.3 to +4.0        | V    |
| VBATT power supply voltage     |                                            | VBATT            | −0.5 to +4.0        | V    |
| Analog power supply voltage    |                                            | AVCC0            | −0.5 to +4.0        | V    |
|                                |                                            | VCC_RF           | −0.3 to +4.0        | V    |
|                                |                                            | AVCC_RF          | −0.3 to +4.0        | V    |
| USB power supply voltage       |                                            | VCC_USB          | −0.5 to +4.0        | V    |
|                                |                                            | VCC_USB_LDO      | −0.5 to +4.0        | V    |
| Analog input voltage           | When AN004 to AN006, AN009, AN010 are used | V <sub>AN</sub>  | −0.3 to AVCC0 + 0.3 | V    |
|                                | When AN017, AN019, AN020 are used          |                  | −0.3 to VCC + 0.3   | V    |
| LCD voltage                    | VL1 voltage                                | V <sub>L1</sub>  | −0.3 to +2.8        | V    |
|                                | VL2 voltage                                | V <sub>L2</sub>  | −0.3 to +4.0        | V    |
|                                | VL4 voltage                                | V <sub>L4</sub>  | −0.3 to +4.0        | V    |
| Operating temperature*2        |                                            | T <sub>opr</sub> | −40 to +85          | °C   |
| Storage temperature            |                                            | T <sub>stg</sub> | −55 to +125         | °C   |

Note 1. Ports P205, P206, P402, P407 are 5V-tolerant.

Note 2. See [section 2.2.1, Tj/Ta Definition](#).

**Caution:** Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between VCC\_RF and VSS\_RF pins, between the AVDD\_RF and VSS\_RF pins, between the VCC\_USB and VSS\_USB pins, between the VREFH0 and VREFL0 pins. Place capacitors with values of about 2.2 μF in the case of the VCC\_RF pin and about 0.1 μF otherwise as close as possible to every power supply pin, and use the shortest and thickest possible traces for the connections. Also, connect capacitors as stabilization capacitance. Connect the VCL pin to a VSS pin by a 4.7 μF capacitor. The capacitor must be placed close to the pin. Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

**Table 2.2 Recommended operating conditions**

| Parameter                    | Symbol      | Value                                               | Min     | Typ | Max   | Unit |
|------------------------------|-------------|-----------------------------------------------------|---------|-----|-------|------|
| Power supply voltages        | VCC*1, *2   | When USBFS is not used                              | 1.8     | -   | 3.6   | V    |
|                              |             | When USBFS is used<br>USB Regulator Disable         | VCC_USB | -   | 3.6   | V    |
|                              | VSS         |                                                     | -       | 0   | -     | V    |
| USB power supply voltages    | VCC_USB     | When USBFS is not used                              | -       | VCC | -     | V    |
|                              |             | When USBFS is used<br>USB Regulator Disable (Input) | 3.0     | 3.3 | 3.6   | V    |
|                              | VCC_USB_LDO | When USBFS is not used                              | -       | VCC | -     | V    |
|                              |             | When USBFS is used                                  | -       | VCC | -     | V    |
|                              | VSS_USB     |                                                     | -       | 0   | -     | V    |
| VBATT power supply voltage   | VBATT       | When the battery backup function is not used        | -       | VCC | -     | V    |
|                              |             | When the battery backup function is used            | 1.8     | -   | 3.6   | V    |
| Analog power supply voltages | AVCC0*1, *2 |                                                     | 1.8     | -   | 3.6   | V    |
|                              | AVSS0       |                                                     | -       | 0   | -     | V    |
|                              | VREFH0      | When used as ADC14 Reference                        | 1.8     | -   | AVCC0 | V    |
|                              | VREFL0      |                                                     | -       | 0   | -     | V    |
| BLE power supply voltages    | VCC_RF*3    |                                                     | 1.8     | -   | 3.6   | V    |
|                              | AVCC_RF*3   |                                                     | 1.8     | -   | 3.6   |      |
|                              | VSS_RF      |                                                     | -       | 0   | -     |      |

Note: Bluetooth power supply voltage

VCC\_RF \*3 1.8 - 3.6 V

Note: AVCC\_RF \*3 1.8 - 3.6 V

Note: VCC\_RF - 0 - V

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when  $VCC \geq 2.2\text{ V}$  and  $AVCC0 \geq 2.2\text{ V}$

$AVCC0 = VCC$  when  $VCC < 2.2\text{ V}$  or  $AVCC0 < 2.2\text{ V}$

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Note 3. Use  $VCC = VCC\_RF = AVCC\_RF$

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

**Table 2.3 DC characteristics**

 Conditions: Products with operating temperature ( $T_a$ )  $-40$  to  $+85^{\circ}\text{C}$ 

| Parameter                        | Symbol | Typ | Max   | Unit               | Test conditions                                                                                 |
|----------------------------------|--------|-----|-------|--------------------|-------------------------------------------------------------------------------------------------|
| Permissible junction temperature | $T_j$  | -   | 105*1 | $^{\circ}\text{C}$ | High-speed mode<br>Middle-speed mode<br>Low-voltage mode<br>Low-speed mode<br>Subosc-speed mode |

Note: Make sure that  $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$ , where total power consumption =  $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$ .

Note 1. The upper limit of operating temperature is  $85^{\circ}\text{C}$ . For details, see [section 1.3, Part Numbering](#). If the part number shows the operation temperature at  $85^{\circ}\text{C}$ , then the maximum value of  $T_j$  is  $105^{\circ}\text{C}$ .

### 2.2.2 I/O $V_{IH}$ , $V_{IL}$

**Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$  (1)**

 Conditions:  $V_{CC} = AVCC0 = V_{CC\_USB} = V_{CC\_USB\_LDO} = 2.7$  to  $3.6\text{V}$ ,  $V_{BATT} = 1.8$  to  $3.6\text{V}$ ,  $V_{SS} = AVSS0 = 0\text{V}$ 

| Parameter                                                     |                                                                | Symbol       | Min                      | Typ | Max                      | Unit | Test conditions |
|---------------------------------------------------------------|----------------------------------------------------------------|--------------|--------------------------|-----|--------------------------|------|-----------------|
| Schmitt trigger input voltage                                 | IIC*1                                                          | $V_{IH}$     | $V_{CC} \times 0.7$      | -   | 5.8                      | V    | -               |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.3$      |      |                 |
|                                                               |                                                                | $\Delta V_T$ | $V_{CC} \times 0.05$     | -   | -                        |      |                 |
|                                                               | RES, NMI<br>Other peripheral input pins<br>excluding IIC       | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | -                        |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
|                                                               |                                                                | $\Delta V_T$ | $V_{CC} \times 0.1$      | -   | -                        |      |                 |
| Input voltage<br>(except for<br>Schmitt trigger<br>input pin) | 5V-tolerant ports*2                                            | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | 5.8                      |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
|                                                               | P914, P915                                                     | $V_{IH}$     | $V_{CC\_USB} \times 0.8$ | -   | $V_{CC\_USB} + 0.3$      |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{CC\_USB} \times 0.2$ |      |                 |
|                                                               | P004, P010                                                     | $V_{IH}$     | $AVCC0 \times 0.8$       | -   | -                        |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $AVCC0 \times 0.2$       |      |                 |
|                                                               | EXTAL<br>Input ports pins except for<br>P004, P010, P914, P915 | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | -                        |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
| When $V_{BATT}$<br>power supply is<br>selected                | P402                                                           | $V_{IH}$     | $V_{BATT} \times 0.8$    | -   | $V_{BATT} + 0.3$         |      |                 |
|                                                               |                                                                | $V_{IL}$     | -                        | -   | $V_{BATT} \times 0.2$    |      |                 |
|                                                               |                                                                | $\Delta V_T$ | $V_{BATT} \times 0.05$   | -   | -                        |      |                 |

Note 1. P205, P206, P407 (total 3 pins).

Note 2. P205, P206, P402, P407 (total 4 pins).

**Table 2.5 I/O  $V_{IH}$ ,  $V_{IL}$  (2)**Conditions:  $V_{CC} = AV_{CC0} = V_{CC\_USB} = V_{CC\_USB\_LDO} = 1.8$  to  $2.7$  V,  $V_{BATT} = 1.8$  to  $3.6$  V,  $V_{SS} = AV_{SS0} = 0$  V

| Parameter                                            |                                                 | Symbol       | Min                      | Typ | Max                      | Unit | Test conditions |
|------------------------------------------------------|-------------------------------------------------|--------------|--------------------------|-----|--------------------------|------|-----------------|
| Schmitt trigger input voltage                        | RES, NMI<br>Peripheral input pins               | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | -                        | V    | -               |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
|                                                      |                                                 | $\Delta V_T$ | $V_{CC} \times 0.01$     | -   | -                        |      |                 |
| Input voltage (except for Schmitt trigger input pin) | 5V-tolerant ports*1                             | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | 5.8                      |      |                 |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
|                                                      | P914, P915                                      | $V_{IH}$     | $V_{CC\_USB} \times 0.8$ | -   | $V_{CC\_USB} + 0.3$      |      |                 |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $V_{CC\_USB} \times 0.2$ |      |                 |
|                                                      | P004, P010                                      | $V_{IH}$     | $AV_{CC0} \times 0.8$    | -   | -                        |      |                 |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $AV_{CC0} \times 0.2$    |      |                 |
|                                                      | EXTAL<br>Input ports pins except for P004, P010 | $V_{IH}$     | $V_{CC} \times 0.8$      | -   | -                        |      |                 |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $V_{CC} \times 0.2$      |      |                 |
| When $V_{BATT}$ power supply is selected             | P402, P404                                      | $V_{IH}$     | $V_{BATT} \times 0.8$    | -   | $V_{BATT} + 0.3$         |      |                 |
|                                                      |                                                 | $V_{IL}$     | -                        | -   | $V_{BATT} \times 0.2$    |      |                 |
|                                                      |                                                 | $\Delta V_T$ | $V_{BATT} \times 0.01$   | -   | -                        |      |                 |

Note 1. P205, P206, P402, P407 (total 4 pins).

2.2.3 I/O  $I_{OH}$ ,  $I_{OL}$ **Table 2.6** I/O  $I_{OH}$ ,  $I_{OL}$ 

Conditions: VCC = AVCC0 = VCC\_USB = VCC\_USB\_LDO = 1.8 to 3.6 V

| Parameter                                             |                                                                  |                                      | Symbol                      | Min | Typ | Max   | Unit |
|-------------------------------------------------------|------------------------------------------------------------------|--------------------------------------|-----------------------------|-----|-----|-------|------|
| Permissible output current<br>(average value per pin) | Ports P212, P213                                                 | -                                    | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       | Port P409                                                        | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2<br>VCC = 2.7 to 3.0 V | $I_{OH}$                    | -   | -   | -8.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
|                                                       |                                                                  | Middle drive*2<br>VCC = 3.0 to 3.6 V | $I_{OH}$                    | -   | -   | -20.0 | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 20.0  | mA   |
|                                                       | Ports P100 to P111,<br>P201, P204, P300, P501<br>(total 16 pins) | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2                       | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
|                                                       | Ports P914, P915                                                 | -                                    | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       | Other output pin*3                                               | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2                       | $I_{OH}$                    | -   | -   | -8.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
| Permissible output current<br>(Max value per pin)     | Ports P212, P213                                                 | -                                    | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       | Port P409                                                        | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2<br>VCC = 2.7 to 3.0 V | $I_{OH}$                    | -   | -   | -8.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
|                                                       |                                                                  | Middle drive*2<br>VCC = 3.0 to 3.6 V | $I_{OH}$                    | -   | -   | -20.0 | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 20.0  | mA   |
|                                                       | Ports P100 to P111,<br>P201, P204, P300, P501<br>(total 16 pins) | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2                       | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
|                                                       | Ports P914, P915                                                 | -                                    | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       | Other output pin*3                                               | Low drive*1                          | $I_{OH}$                    | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 4.0   | mA   |
|                                                       |                                                                  | Middle drive*2                       | $I_{OH}$                    | -   | -   | -8.0  | mA   |
|                                                       |                                                                  |                                      | $I_{OL}$                    | -   | -   | 8.0   | mA   |
| Permissible output current<br>(max value total pins)  | Total of ports P004, P010                                        |                                      | $\Sigma I_{OH}(\text{max})$ | -   | -   | -30   | mA   |
|                                                       |                                                                  |                                      | $\Sigma I_{OL}(\text{max})$ | -   | -   | 30    | mA   |
|                                                       | Ports P914, P915                                                 |                                      | $\Sigma I_{OH}(\text{max})$ | -   | -   | -4.0  | mA   |
|                                                       |                                                                  |                                      | $\Sigma I_{OL}(\text{min})$ | -   | -   | 4.0   | mA   |
|                                                       | Total of all output pin*5                                        |                                      | $\Sigma I_{OH}(\text{max})$ | -   | -   | -60   | mA   |
|                                                       |                                                                  |                                      | $\Sigma I_{OL}(\text{max})$ | -   | -   | 60    | mA   |

**Caution:** To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100  $\mu\text{s}$ .

- Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in PmnPFS register.  
 Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.  
 Note 3. Except for ports P200, P214, P215, which are input ports.  
 Note 4. This is the value when middle driving ability for IIC Fast-mode is selected with the Port Drive Capability bit in PmnPFS register.  
 Note 5. For details on the permissible output current used with CTSU, see [section 2.11, CTSU Characteristics](#).

## 2.2.4 I/O $V_{OH}$ , $V_{OL}$ , and Other Characteristics

**Table 2.7 I/O  $V_{OH}$ ,  $V_{OL}$  (1)**

Conditions:  $V_{CC} = AVCC0 = VCC\_USB = VCC\_USB\_LDO = 2.7$  to  $3.6$  V

| Parameter      |                             |                | Symbol           | Min              | Typ | Max | Unit | Test conditions                       |
|----------------|-----------------------------|----------------|------------------|------------------|-----|-----|------|---------------------------------------|
| Output voltage | IIC*1                       |                | $V_{OL}$         | -                | -   | 0.4 | V    | $I_{OL} = 3.0$ mA                     |
|                |                             |                | $V_{OL}^{*2,*5}$ | -                | -   | 0.6 |      | $I_{OL} = 6.0$ mA                     |
|                | Ports P409*2, *3            |                | $V_{OH}$         | $V_{CC} - 1.0$   | -   | -   |      | $I_{OH} = -20$ mA<br>$V_{CC} = 3.3$ V |
|                |                             |                | $V_{OL}$         | -                | -   | 1.0 |      | $I_{OL} = 20$ mA<br>$V_{CC} = 3.3$ V  |
|                | Ports P004, P010            | Low drive      | $V_{OH}$         | $AVCC0 - 0.5$    | -   | -   |      | $I_{OH} = -1.0$ mA                    |
|                |                             |                | $V_{OL}$         | -                | -   | 0.5 |      | $I_{OL} = 1.0$ mA                     |
|                |                             | Middle drive   | $V_{OH}$         | $AVCC0 - 0.5$    | -   | -   |      | $I_{OH} = -2.0$ mA                    |
|                |                             |                | $V_{OL}$         | -                | -   | 0.5 |      | $I_{OL} = 2.0$ mA                     |
|                | Ports P914, P915            |                | $V_{OH}$         | $VCC\_USB - 0.5$ | -   | -   |      | $I_{OH} = -1.0$ mA                    |
|                |                             |                | $V_{OL}$         | -                | -   | 0.5 |      | $I_{OL} = 1.0$ mA                     |
|                | Other output pins<br>*4, *6 | Low drive      | $V_{OH}$         | $VCC - 0.5$      | -   | -   |      | $I_{OH} = -1.0$ mA                    |
|                |                             |                | $V_{OL}$         | -                | -   | 0.5 |      | $I_{OL} = 1.0$ mA                     |
|                |                             | Middle drive*5 | $V_{OH}$         | $VCC - 0.5$      | -   | -   |      | $I_{OH} = -2.0$ mA                    |
|                |                             |                | $V_{OL}$         | -                | -   | 0.5 |      | $I_{OL} = 2.0$ mA                     |

- Note 1. P100, P101, P204, P205, P206, P407 (total 6 pins).  
 Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.  
 Note 3. Based on characterization data, not tested in production.  
 Note 4. Except for ports P200, P214, P215, which are input ports.  
 Note 5. Except for P212, P213.  
 Note 6. This excludes the CLKOUT\_RF pin.

**Table 2.8 I/O  $V_{OH}$ ,  $V_{OL}$  (2)**

Conditions:  $V_{CC} = AVCC0 = VCC\_USB = VCC\_USB\_LDO = 1.8$  to  $2.7$  V

| Parameter      |                             |                | Symbol   | Min              | Typ | Max | Unit | Test conditions    |
|----------------|-----------------------------|----------------|----------|------------------|-----|-----|------|--------------------|
| Output voltage | Ports P004, P010            | Low drive      | $V_{OH}$ | $AVCC0 - 0.3$    | -   | -   | V    | $I_{OH} = -0.5$ mA |
|                |                             |                | $V_{OL}$ | -                | -   | 0.3 |      | $I_{OL} = 0.5$ mA  |
|                |                             | Middle drive   | $V_{OH}$ | $AVCC0 - 0.3$    | -   | -   |      | $I_{OH} = -1.0$ mA |
|                |                             |                | $V_{OL}$ | -                | -   | 0.3 |      | $I_{OL} = 1.0$ mA  |
|                | Ports P914, P915            |                | $V_{OH}$ | $VCC\_USB - 0.3$ | -   | -   |      | $I_{OH} = -0.5$ mA |
|                |                             |                | $V_{OL}$ | -                | -   | 0.3 |      | $I_{OL} = 0.5$ mA  |
|                | Other output pins<br>*1, *3 | Low drive      | $V_{OH}$ | $VCC - 0.3$      | -   | -   |      | $I_{OH} = -0.5$ mA |
|                |                             |                | $V_{OL}$ | -                | -   | 0.3 |      | $I_{OL} = 0.5$ mA  |
|                |                             | Middle drive*2 | $V_{OH}$ | $VCC - 0.3$      | -   | -   |      | $I_{OH} = -1.0$ mA |
|                |                             |                | $V_{OL}$ | -                | -   | 0.3 |      | $I_{OL} = 1.0$ mA  |

- Note 1. Except for ports P200, P214, P215, which are input ports.  
 Note 2. Except for P212, P213.  
 Note 3. This excludes the CLKOUT\_RF pin.

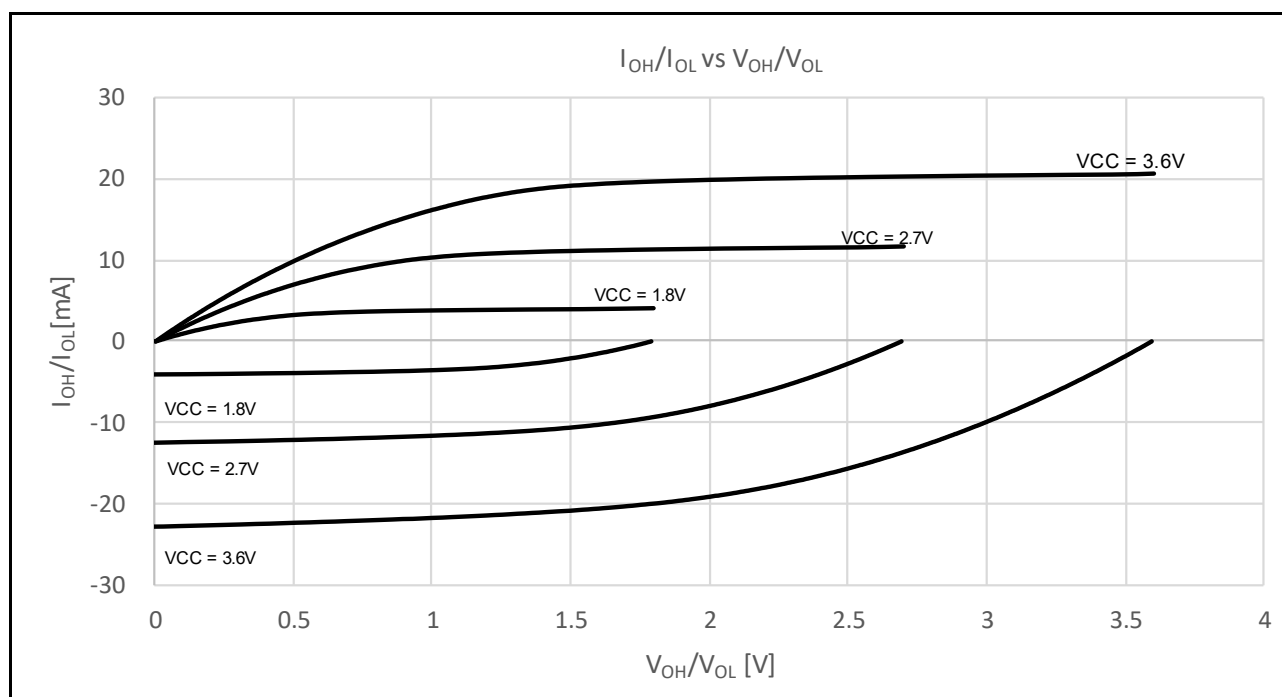
**Table 2.9 I/O  $V_{OH}$ ,  $V_{OL}$  (3)**Conditions:  $3.0V \leq VCC = AVCC0 = VCC\_USB = VCC\_USB\_LDO = VCC\_RF = AVCC\_RF \leq 3.6V$ 

| Parameter   |           | Symbol   | Min             | Max | Unit | Test conditions           |
|-------------|-----------|----------|-----------------|-----|------|---------------------------|
| Output low  | CLKOUT_RF | $V_{OL}$ | -               | 0.3 | V    | $I_{OL} = 0.5\text{ mA}$  |
| Output high | CLKOUT_RF | $V_{OH}$ | $VCC\_RF - 0.3$ | -   | V    | $I_{OH} = -0.5\text{ mA}$ |

**Table 2.10 I/O other characteristics**Conditions:  $VCC = AVCC0 = 1.8\text{ to }3.6\text{ V}$ 

| Parameter                               |                                                                  | Symbol      | Min | Typ | Max | Unit          | Test conditions                                                         |
|-----------------------------------------|------------------------------------------------------------------|-------------|-----|-----|-----|---------------|-------------------------------------------------------------------------|
| Input leakage current                   | RES, P200, P214, P215                                            | $ I_{in} $  | -   | -   | 1.0 | $\mu\text{A}$ | $V_{in} = 0\text{ V}$<br>$V_{in} = VCC$                                 |
| Three-state leakage current (off state) | 5V-tolerant ports                                                | $ I_{TSI} $ | -   | -   | 1.0 | $\mu\text{A}$ | $V_{in} = 0\text{ V}$<br>$V_{in} = 5.8\text{ V}$                        |
|                                         | Other ports (except for ports P200, P214, P215 and 5 V tolerant) |             | -   | -   | 1.0 |               | $V_{in} = 0\text{ V}$<br>$V_{in} = VCC$                                 |
| Input pull-up resistor                  | All ports (except for ports P200, P214, P215, P914, P915)        | $R_U$       | 10  | 20  | 50  | $k\Omega$     | $V_{in} = 0\text{ V}$                                                   |
| Input capacitance                       | P914, P915, P100 to P103, P111, P200                             | $C_{in}$    | -   | -   | 30  | $\text{pF}$   | $V_{in} = 0\text{ V}$<br>$f = 1\text{ MHz}$<br>$T_a = 25^\circ\text{C}$ |
|                                         | Other input pins                                                 |             | -   | -   | 15  |               |                                                                         |

### 2.2.5 I/O Pin Output Characteristics of Low Drive Capacity



**Figure 2.2  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when low drive output is selected (reference data)**

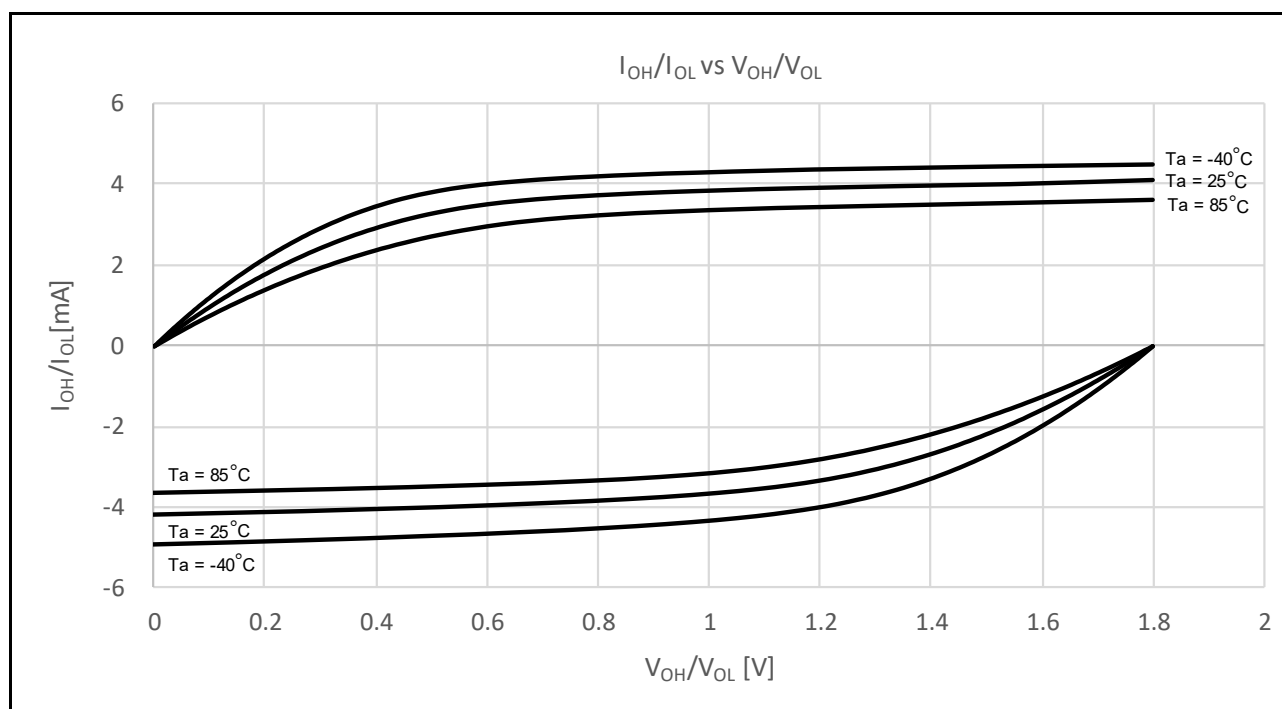


Figure 2.3  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 1.8$  V when low drive output is selected (reference data)

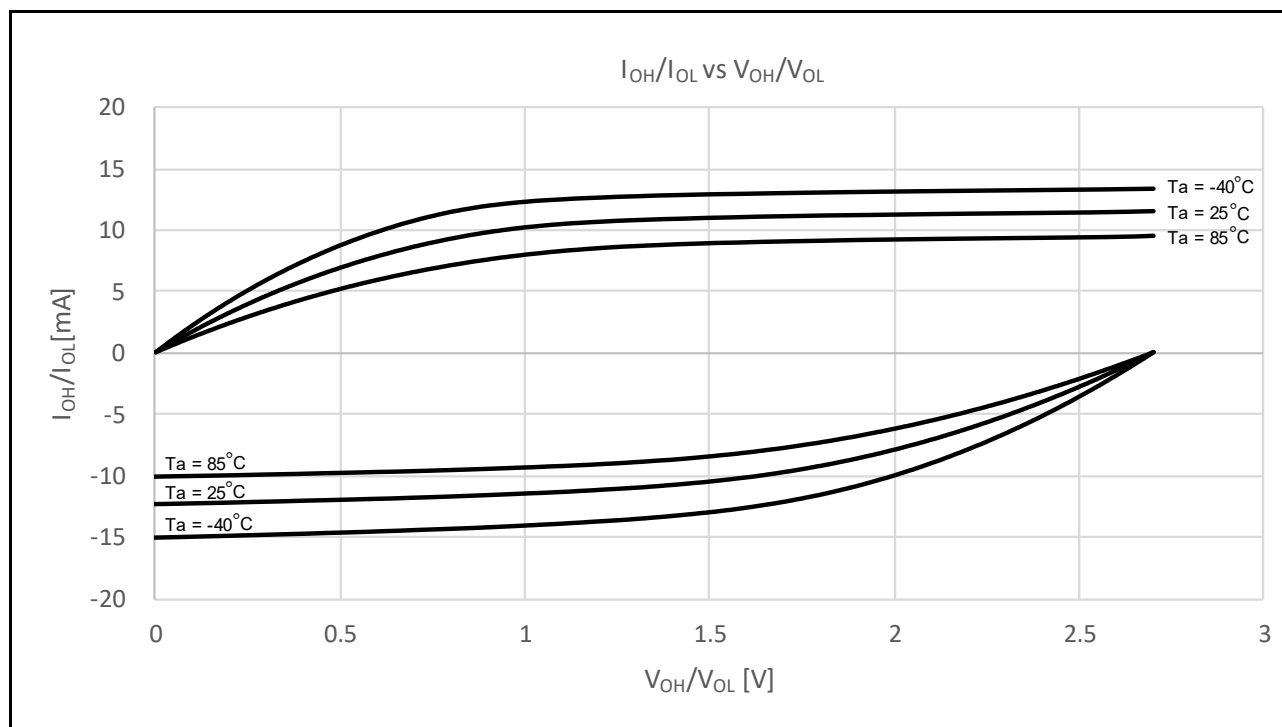
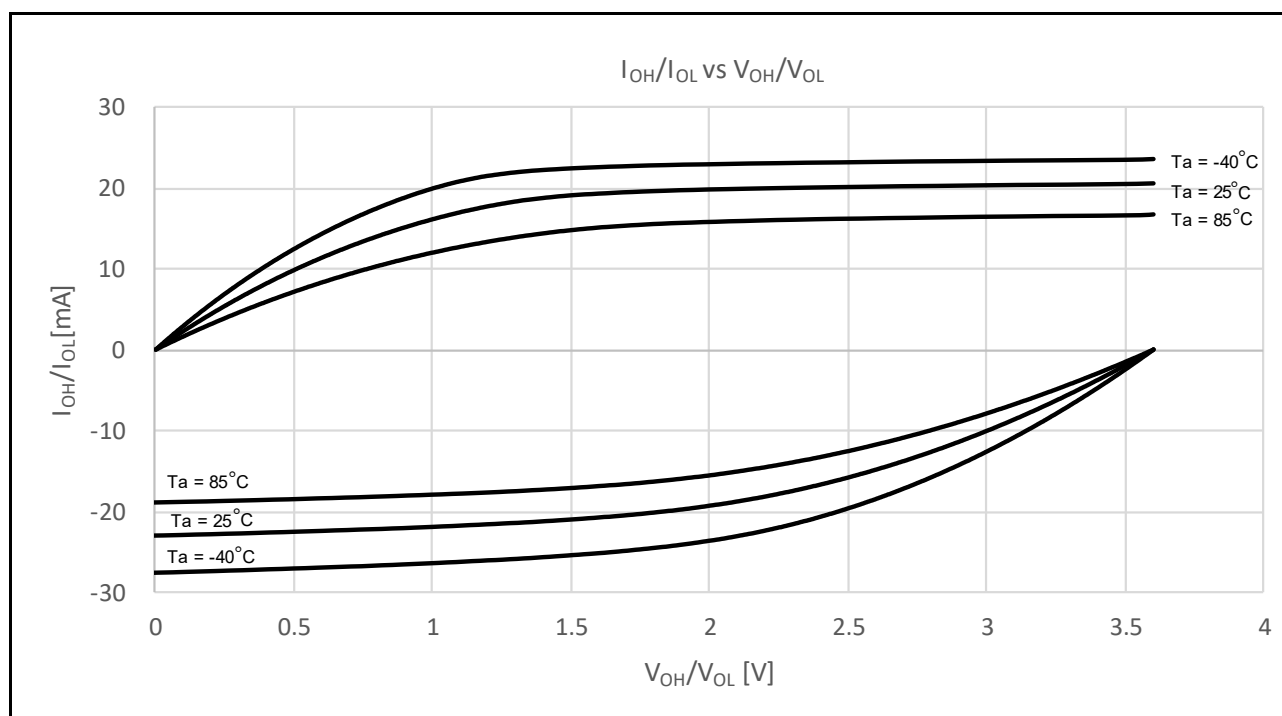
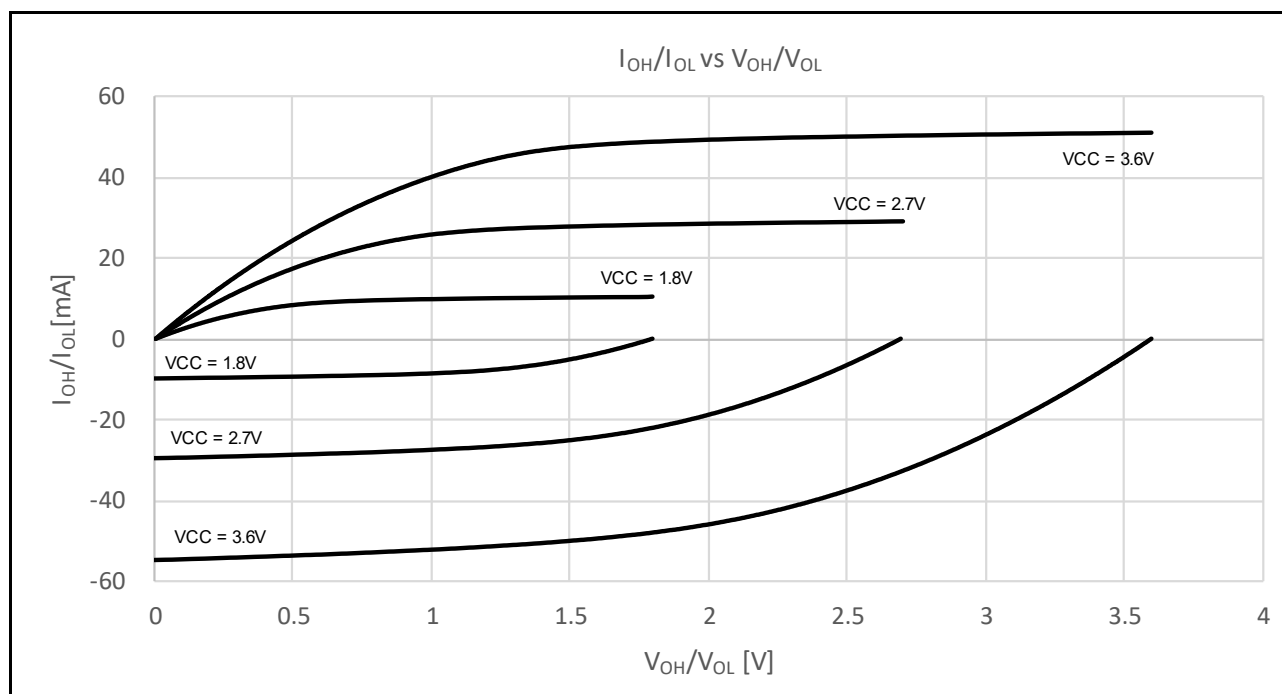


Figure 2.4  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7$  V when low drive output is selected (reference data)



**Figure 2.5**  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.6$  V when low drive output is selected (reference data)

## 2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity



**Figure 2.6**  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when middle drive output is selected (reference data)

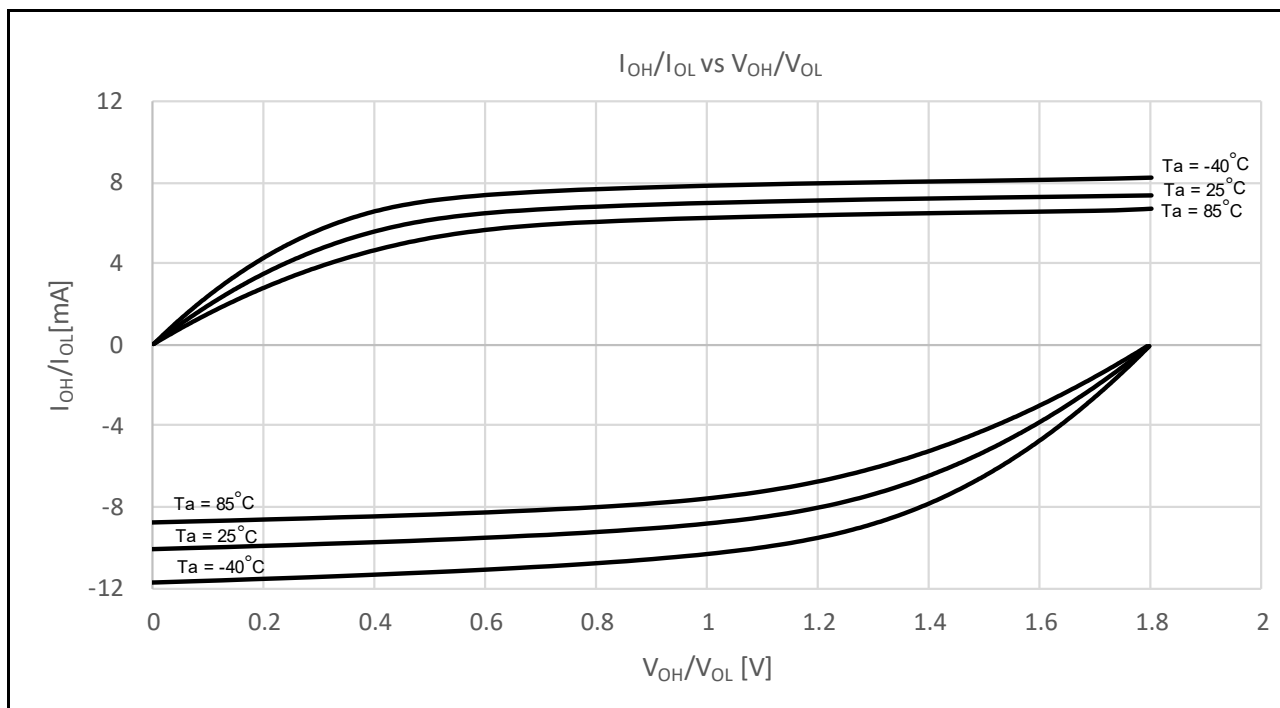


Figure 2.7  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 1.8$  V when middle drive output is selected (reference data)

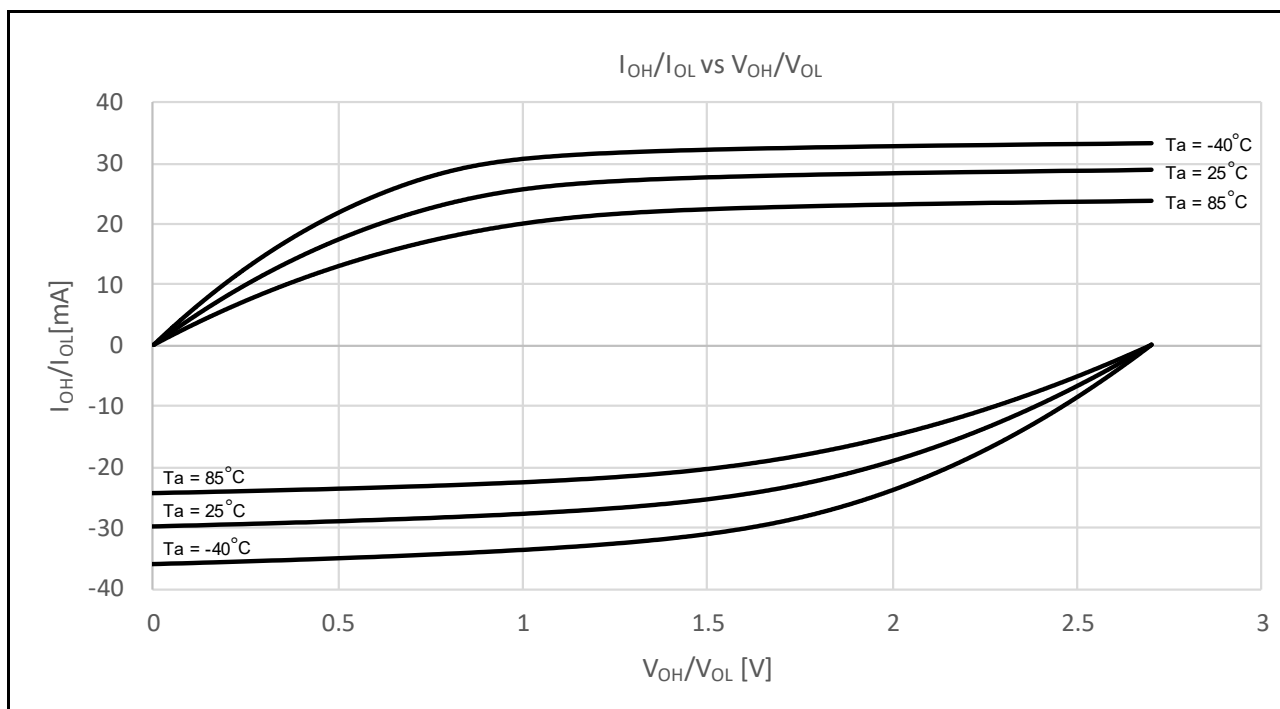
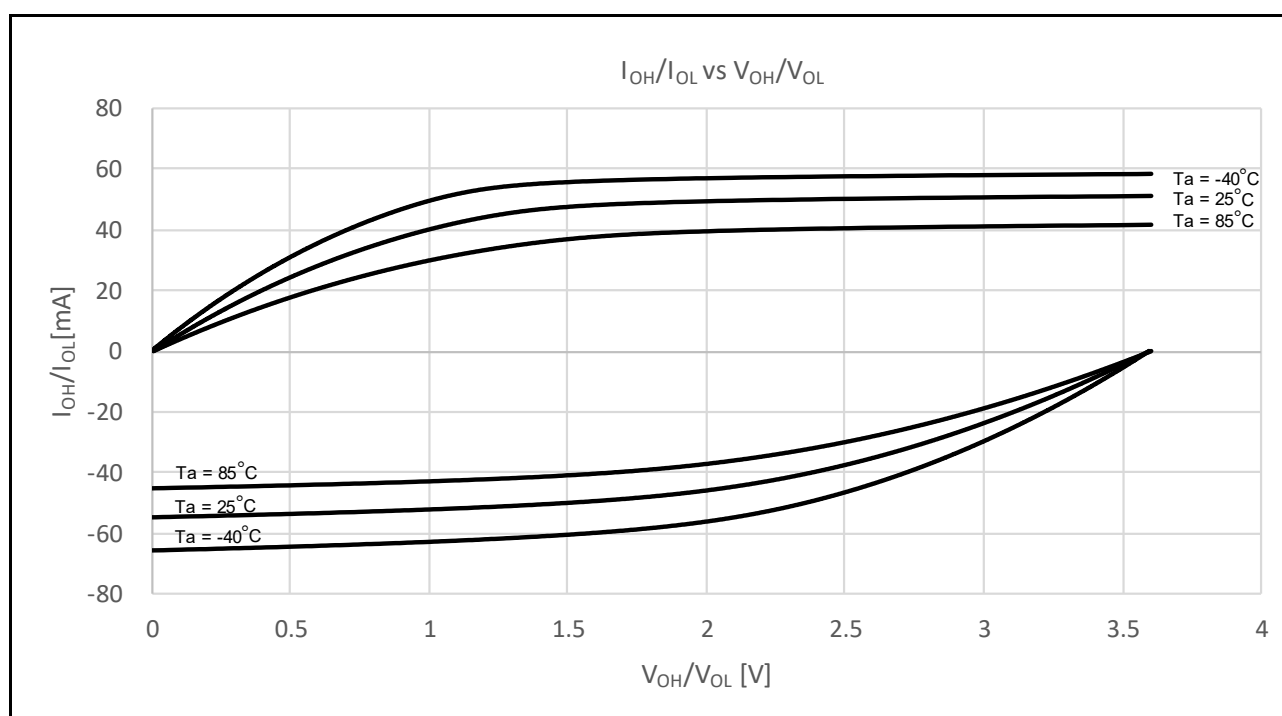
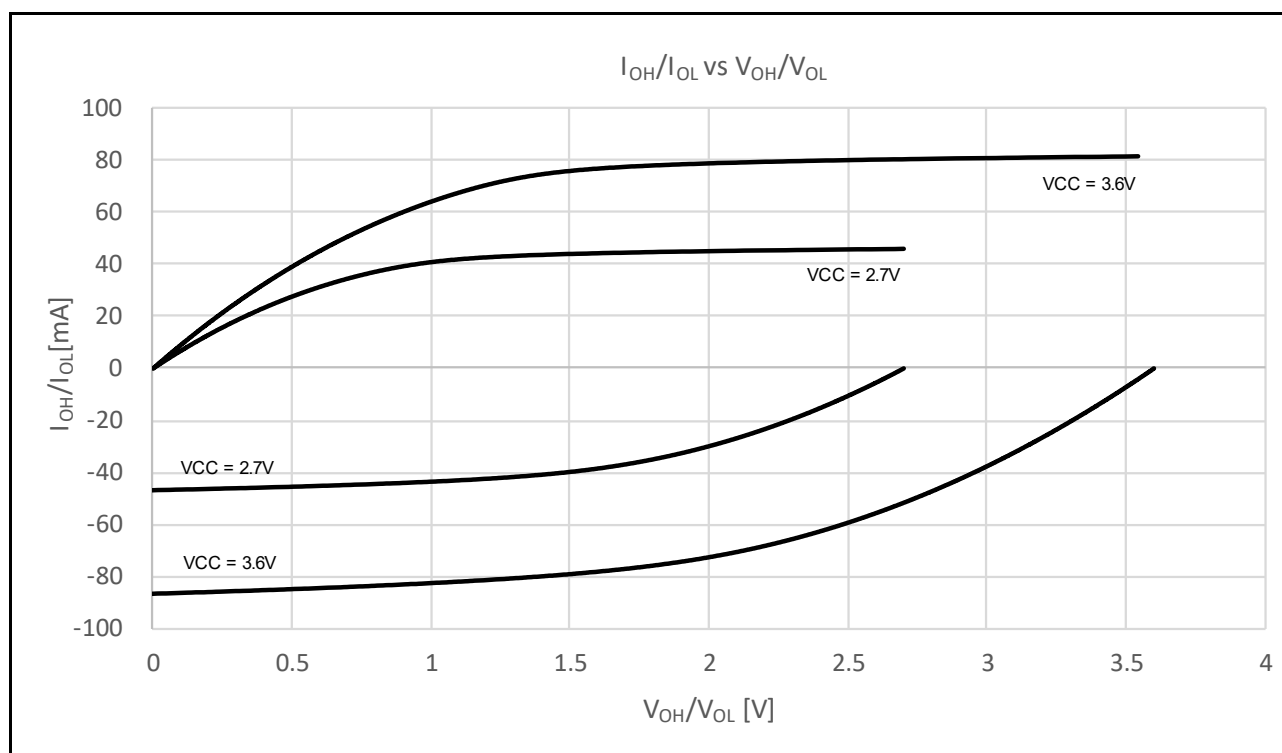


Figure 2.8  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7$  V when middle drive output is selected (reference data)



**Figure 2.9**  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.6\text{ V}$  when middle drive output is selected (reference data)

## 2.2.7 P409 I/O Pin Output Characteristics of Middle Drive Capacity



**Figure 2.10**  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$  when middle drive output is selected (reference data)

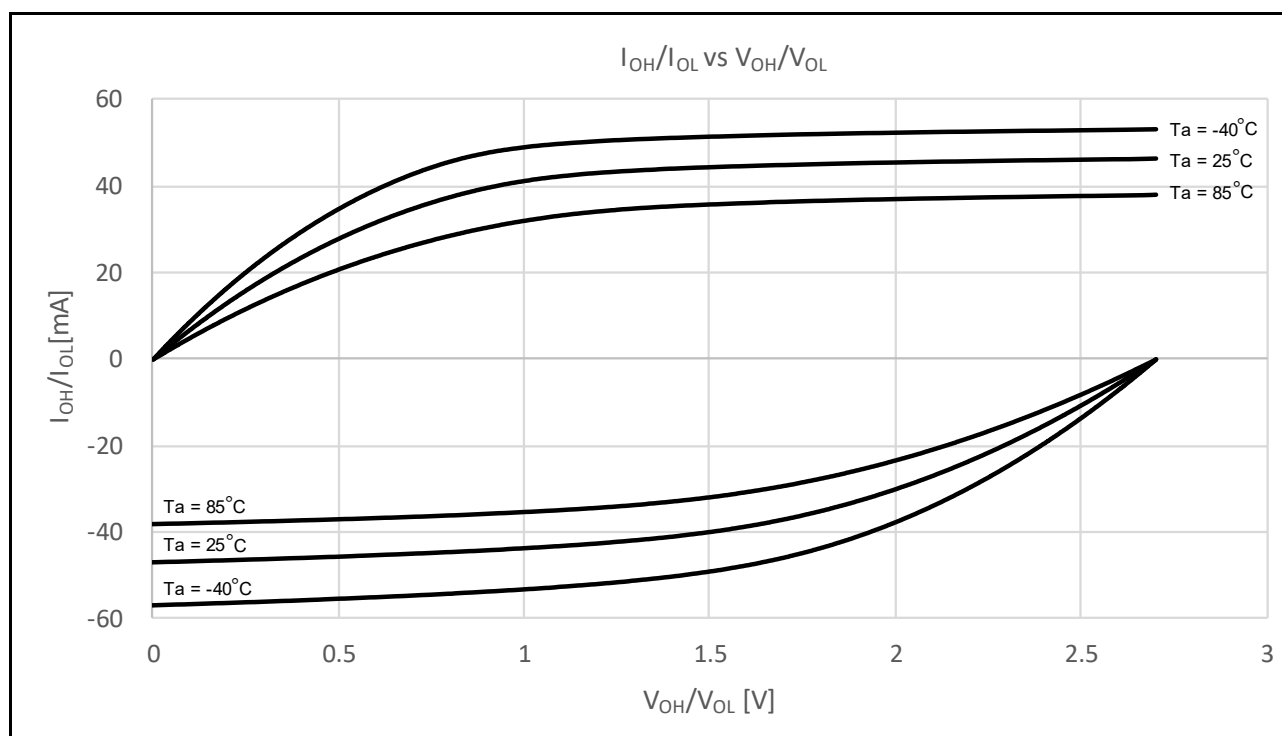


Figure 2.11  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 2.7$  V when middle drive output is selected (reference data)

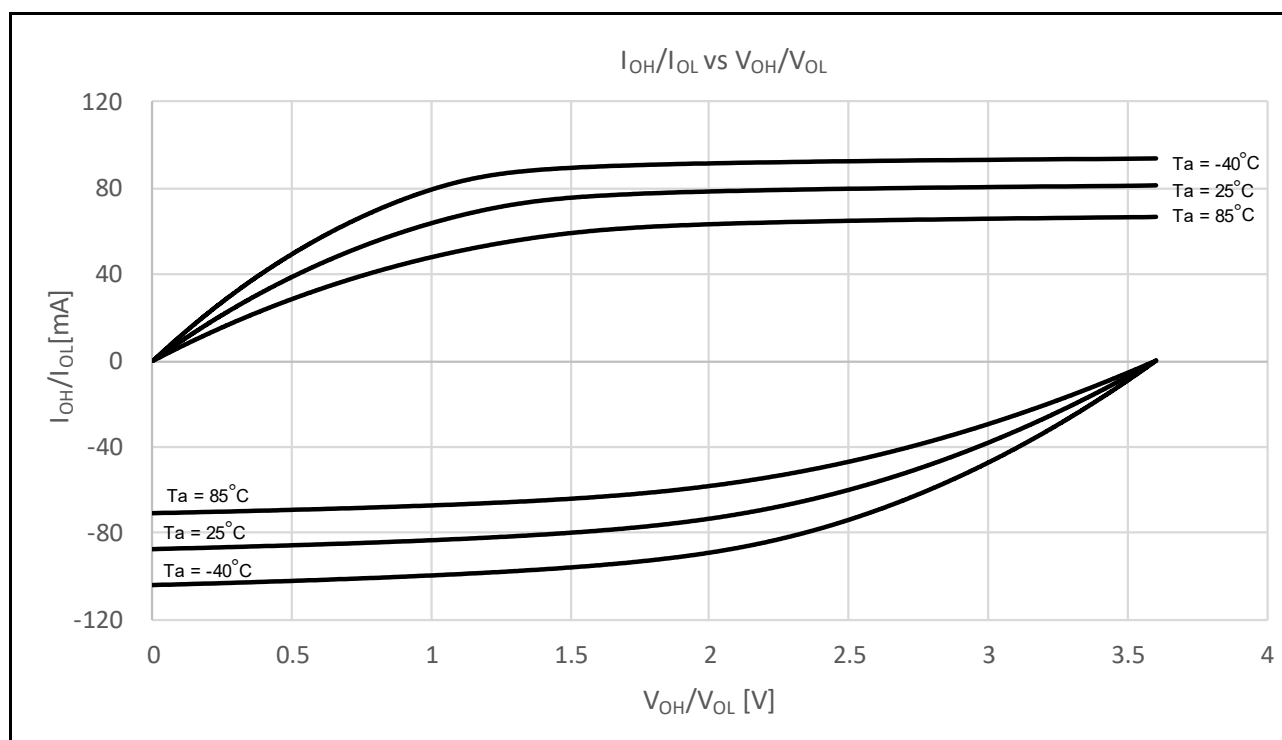


Figure 2.12  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  temperature characteristics at  $V_{CC} = 3.6$  V when middle drive output is selected (reference data)

## 2.2.8 IIC I/O Pin Output Characteristics

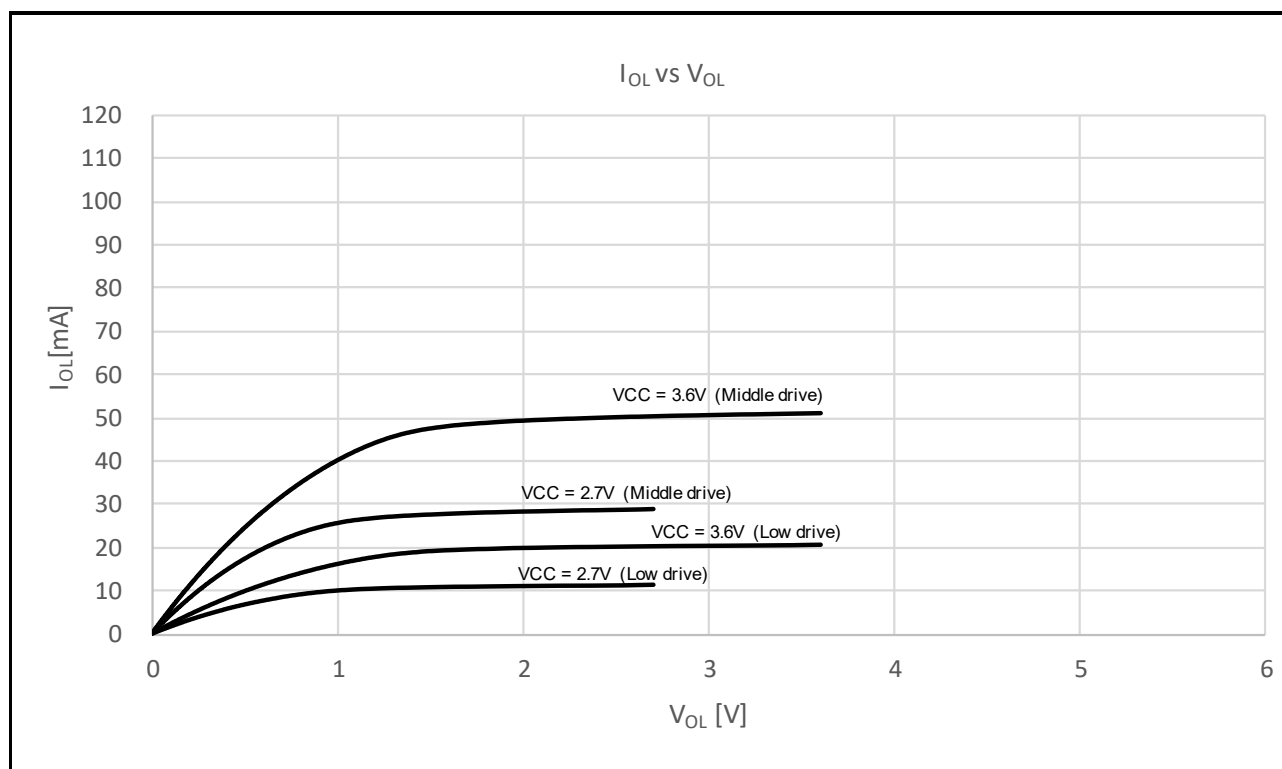


Figure 2.13  $V_{OH}/V_{OL}$  and  $I_{OH}/I_{OL}$  voltage characteristics at  $T_a = 25^\circ\text{C}$

## 2.2.9 Operating and Standby Current

**Table 2.11 Operating and standby current (1) (1 of 2)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter                                                |                     |                                 |                                                                      |               | Symbol          | Typ*10 | Max  | Unit | Test conditions |
|----------------------------------------------------------|---------------------|---------------------------------|----------------------------------------------------------------------|---------------|-----------------|--------|------|------|-----------------|
| Supply current*1                                         | High-speed mode*2   | Normal mode                     | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 48 MHz | I <sub>CC</sub> | 8.4    | -    | mA   | *7              |
|                                                          |                     |                                 |                                                                      | ICLK = 32 MHz |                 | 5.9    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 16 MHz |                 | 3.5    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 2.3    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock disabled, CoreMark code executing from flash*5  | ICLK = 48 MHz |                 | 17.9   | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 32 MHz |                 | 12.4   | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 16 MHz |                 | 7.0    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 4.3    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock enabled, while (1) code executing from flash*5  | ICLK = 48 MHz |                 | 21.2   | -    |      | *9              |
|                                                          |                     |                                 |                                                                      | ICLK = 32 MHz |                 | 16.0   | -    |      | *8              |
|                                                          |                     |                                 |                                                                      | ICLK = 16 MHz |                 | 8.8    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 5.1    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock enabled, code executing from SRAM*5             | ICLK = 48 MHz |                 | -      | 56.0 |      | *9              |
|                                                          |                     | Sleep mode                      | All peripheral clock disabled*5                                      | ICLK = 48 MHz |                 | 3.7    | -    |      | *7              |
|                                                          |                     |                                 |                                                                      | ICLK = 32 MHz |                 | 2.7    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 16 MHz |                 | 2.0    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 1.5    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock enabled*5                                       | ICLK = 48 MHz |                 | 16.4   | -    |      | *9              |
|                                                          |                     |                                 |                                                                      | ICLK = 32 MHz |                 | 12.7   | -    |      | *8              |
|                                                          |                     |                                 |                                                                      | ICLK = 16 MHz |                 | 7.2    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 4.3    | -    |      |                 |
|                                                          |                     |                                 | Increase during BGO operation*6                                      |               |                 |        | 2.5  |      | -               |
|                                                          | Middle-speed mode*2 | Normal mode                     | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 12 MHz | I <sub>CC</sub> | 2.5    | -    | mA   | *7              |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 2.1    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 1 MHz  |                 | 1.0    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock disabled, CoreMark code executing from flash*5  | ICLK = 12 MHz |                 | 5.2    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 8 MHz  |                 | 4.0    | -    |      |                 |
|                                                          |                     |                                 |                                                                      | ICLK = 1 MHz  |                 | 1.3    | -    |      |                 |
|                                                          |                     |                                 | All peripheral clock enabled, while (1) code executing from flash*5  | ICLK = 12 MHz |                 | 6.5    | -    |      | *8              |
| ICLK = 8 MHz                                             |                     |                                 |                                                                      | 4.8           |                 | -      |      |      |                 |
| ICLK = 1 MHz                                             |                     |                                 |                                                                      | 1.6           |                 | -      |      |      |                 |
| All peripheral clock enabled, code executing from SRAM*5 |                     |                                 | ICLK = 12 MHz                                                        | -             |                 | 23.0   |      |      |                 |
| Sleep mode                                               |                     | All peripheral clock disabled*5 | ICLK = 12 MHz                                                        | 1.4           |                 | -      | *7   |      |                 |
|                                                          |                     |                                 | ICLK = 8 MHz                                                         | 1.3           |                 | -      |      |      |                 |
|                                                          |                     |                                 | ICLK = 1 MHz                                                         | 0.9           |                 | -      |      |      |                 |
|                                                          |                     | All peripheral clock enabled*5  | ICLK = 12 MHz                                                        | 5.3           |                 | -      | *8   |      |                 |
|                                                          |                     |                                 | ICLK = 8 MHz                                                         | 4.0           |                 | -      |      |      |                 |
|                                                          |                     |                                 | ICLK = 1 MHz                                                         | 1.5           |                 | -      |      |      |                 |
| Increase during BGO operation*6                          |                     |                                 |                                                                      | 2.5           |                 | -      | -    |      |                 |

**Table 2.11 Operating and standby current (1) (2 of 2)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter        |                     |             |                                                                      |                   | Symbol          | Typ*10 | Max   | Unit | Test conditions |
|------------------|---------------------|-------------|----------------------------------------------------------------------|-------------------|-----------------|--------|-------|------|-----------------|
| Supply current*1 | Low-speed mode*3    | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 1 MHz      | I <sub>CC</sub> | 0.4    | -     | mA   | *7              |
|                  |                     |             | All peripheral clock disabled, CoreMark code executing from flash*5  | ICLK = 1 MHz      |                 | 0.6    | -     |      |                 |
|                  |                     |             | All peripheral clock enabled, while (1) code executing from flash*5  | ICLK = 1 MHz      |                 | 1.1    | -     |      |                 |
|                  |                     |             | All peripheral clock enabled, code executing from SRAM*5             | ICLK = 1 MHz      |                 | -      | 2.5   |      |                 |
|                  |                     | Sleep mode  | All peripheral clock disabled*5                                      | ICLK = 1 MHz      | I <sub>CC</sub> | 0.3    | -     | mA   | *7              |
|                  |                     |             | All peripheral clock enabled*5                                       | ICLK = 1 MHz      |                 | 1.0    | -     |      | *8              |
|                  | Low-voltage mode*3  | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 4 MHz      | I <sub>CC</sub> | 1.8    | -     | mA   | *7              |
|                  |                     |             | All peripheral clock disabled, CoreMark code executing from flash*5  | ICLK = 4 MHz      |                 | 3.0    | -     |      |                 |
|                  |                     |             | All peripheral clock enabled, while (1) code executing from flash*5  | ICLK = 4 MHz      |                 | 3.3    | -     |      |                 |
|                  |                     |             | All peripheral clock enabled, code executing from SRAM*5             | ICLK = 4 MHz      |                 | -      | 9.0   |      |                 |
|                  |                     | Sleep mode  | All peripheral clock disabled*5                                      | ICLK = 4 MHz      | I <sub>CC</sub> | 1.4    | -     | mA   | *7              |
|                  |                     |             | All peripheral clock enabled*5                                       | ICLK = 4 MHz      |                 | 2.9    | -     |      | *8              |
|                  | Subosc-speed mode*4 | Normal mode | All peripheral clock disabled, while (1) code executing from flash*5 | ICLK = 32.768 kHz | I <sub>CC</sub> | 9.3    | -     | μA   | *8              |
|                  |                     |             | All peripheral clock enabled, while (1) code executing from flash*5  | ICLK = 32.768 kHz |                 | 17.2   | -     |      |                 |
|                  |                     |             | All peripheral clock enabled, code executing from SRAM*5             | ICLK = 32.768 kHz |                 | -      | 106.0 |      |                 |
|                  |                     | Sleep mode  | All peripheral clock disabled*5                                      | ICLK = 32.768 kHz |                 | 6.0    | -     |      |                 |
|                  |                     |             | All peripheral clock enabled*5                                       | ICLK = 32.768 kHz |                 | 14.0   | -     |      |                 |
|                  |                     |             |                                                                      |                   |                 |        |       |      |                 |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The clock source is HOCO.

Note 3. The clock source is MOCO.

Note 4. The clock source is the sub-clock oscillator.

Note 5. This does not include BGO operation.

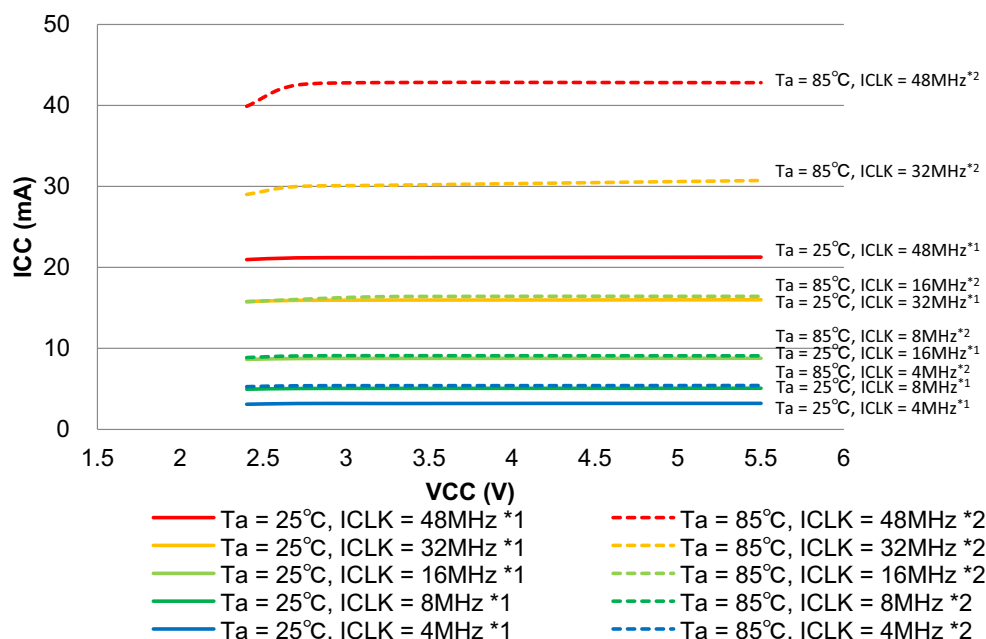
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Note 7. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.

Note 8. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.

Note 9. FCLK and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.

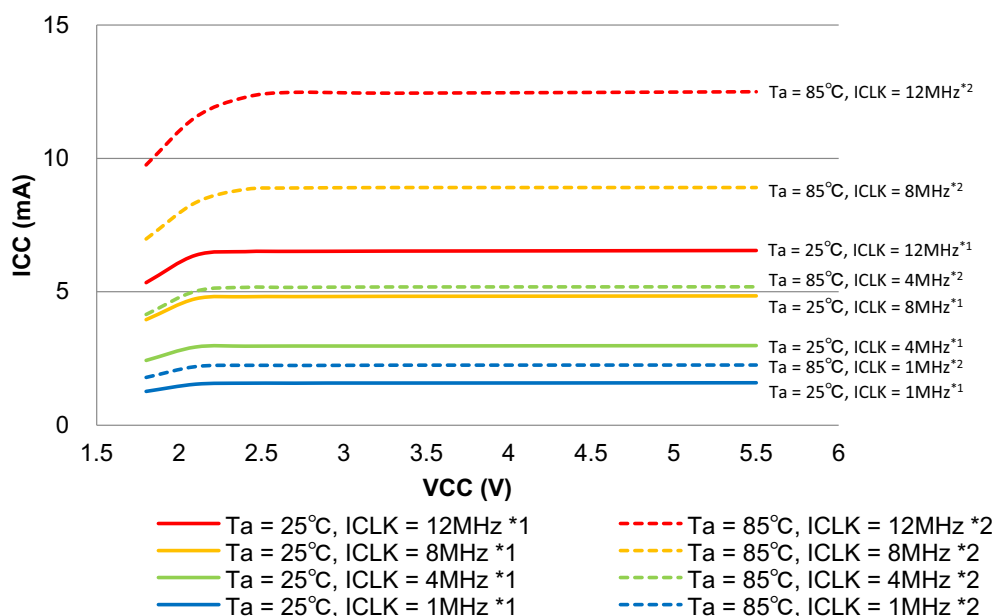
Note 10. VCC = 3.3 V.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

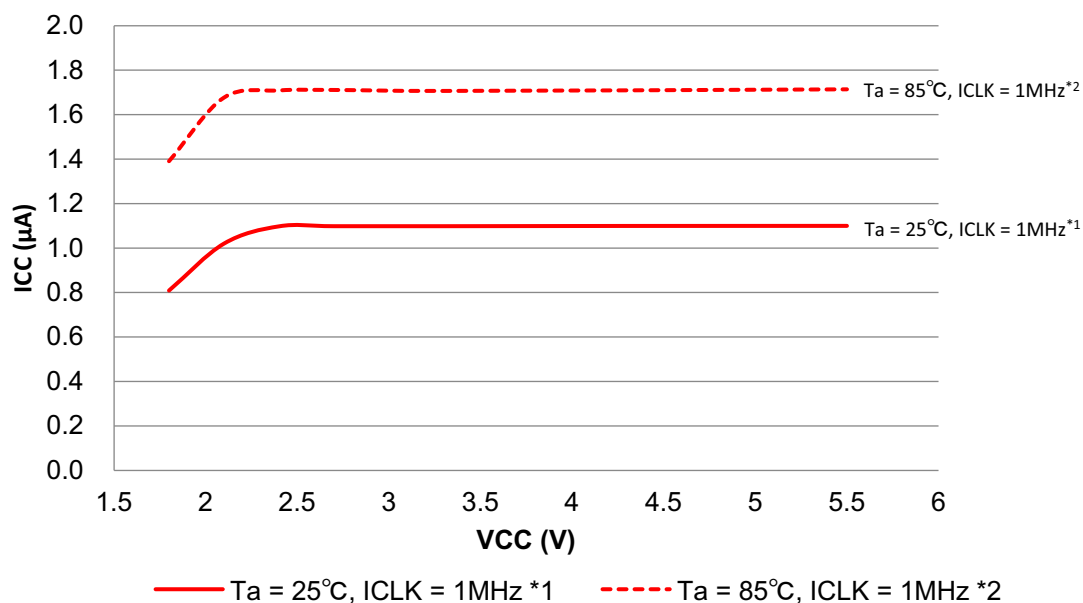
Figure 2.14 Voltage dependency in high-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

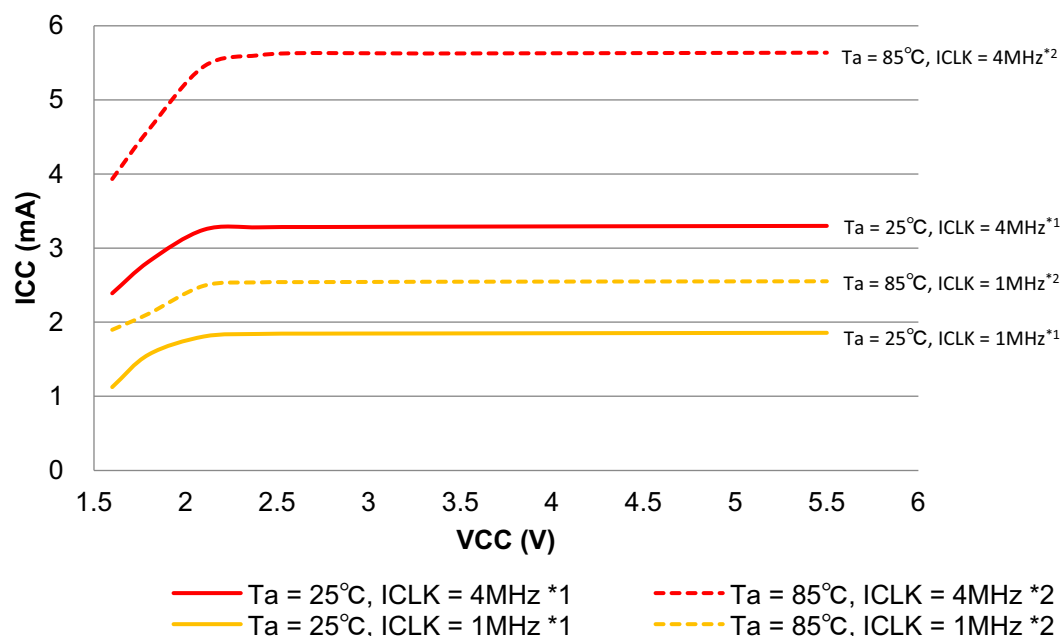
Figure 2.15 Voltage dependency in middle-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.16 Voltage dependency in low-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.17 Voltage dependency in low-voltage mode (reference data)

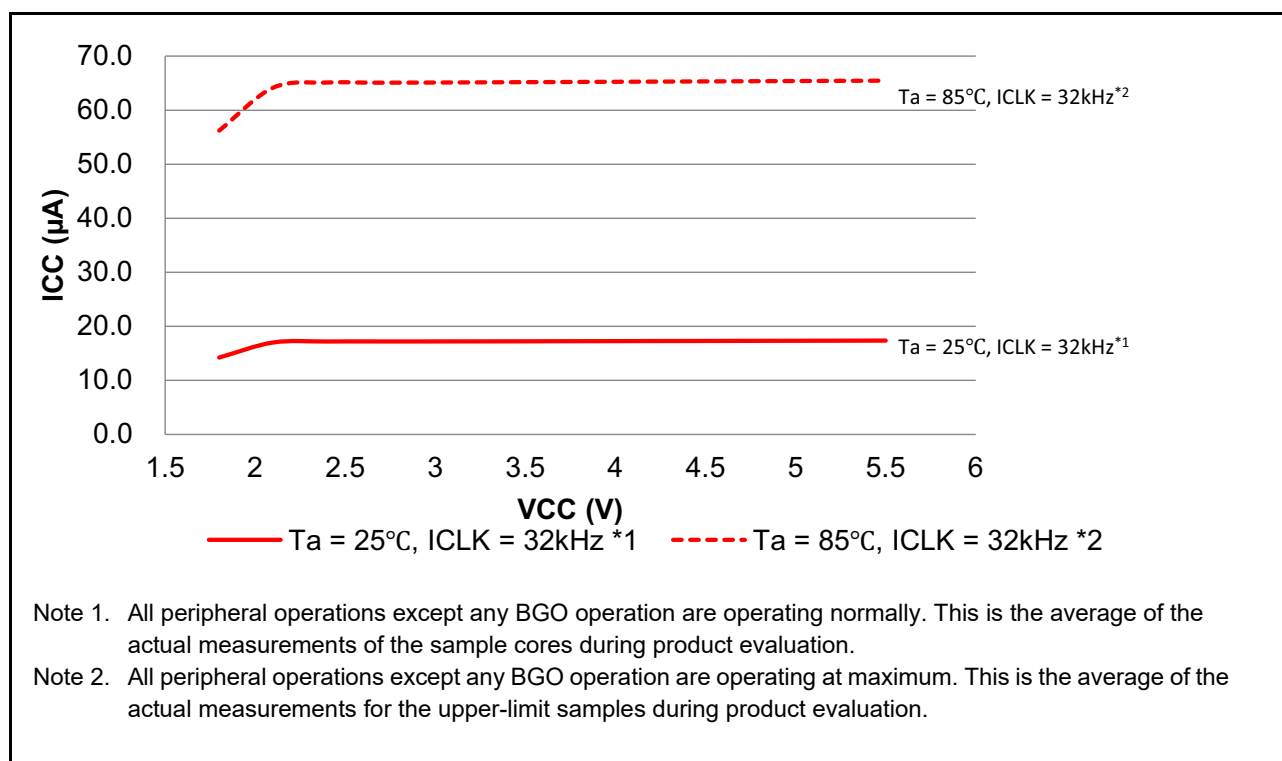


Figure 2.18 Voltage dependency in subosc-speed mode (reference data)

Table 2.12 Operating and standby current (2)

Conditions:  $V_{CC} = AVCC0 = 1.8$  to  $3.6$  V

| Parameter        |                                                                 |                       | Symbol          | Typ*4 | Max  | Unit                                        | Test conditions                       |
|------------------|-----------------------------------------------------------------|-----------------------|-----------------|-------|------|---------------------------------------------|---------------------------------------|
| Supply current*1 | Software Standby mode*2                                         | T <sub>a</sub> = 25°C | I <sub>CC</sub> | 0.9   | 5.0  | µA                                          | PSMCR.PSMC[1:0] = 01b (48-KB SRAM on) |
|                  |                                                                 | T <sub>a</sub> = 55°C |                 | 1.5   | 8.1  |                                             |                                       |
|                  |                                                                 | T <sub>a</sub> = 85°C |                 | 3.6   | 22.1 |                                             |                                       |
|                  |                                                                 | T <sub>a</sub> = 25°C |                 | 1.0   | 5.6  |                                             | PSMCR.PSMC[1:0] = 00b (All SRAM on)   |
|                  |                                                                 | T <sub>a</sub> = 55°C |                 | 1.6   | 8.4  |                                             |                                       |
|                  |                                                                 | T <sub>a</sub> = 85°C |                 | 4.3   | 26.7 |                                             |                                       |
|                  | Increment for RTC operation with low-speed on-chip oscillator*3 |                       |                 | 0.5   | -    | -                                           |                                       |
|                  | Increment for RTC operation with sub-clock oscillator*3         |                       |                 | 0.4   | -    | SOMCR.SODRV[1:0] are 11b (Low power mode 3) |                                       |
|                  |                                                                 |                       |                 | 1.2   | -    | SOMCR.SODRV[1:0] are 00b (Normal mode)      |                                       |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDG and LVD are not operating.

Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.

Note 4.  $V_{CC} = 3.3$  V.

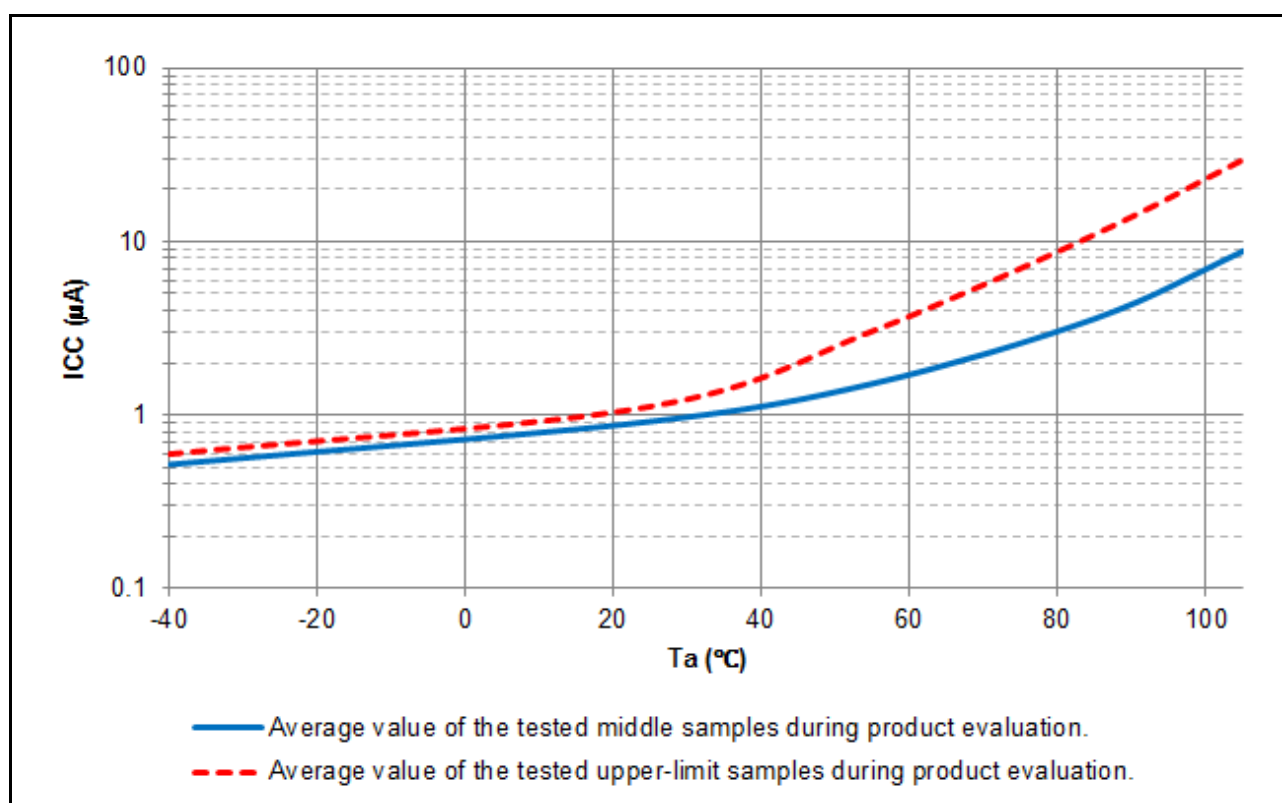


Figure 2.19 Temperature dependency in Software Standby mode 48-KB SRAM on (reference data)

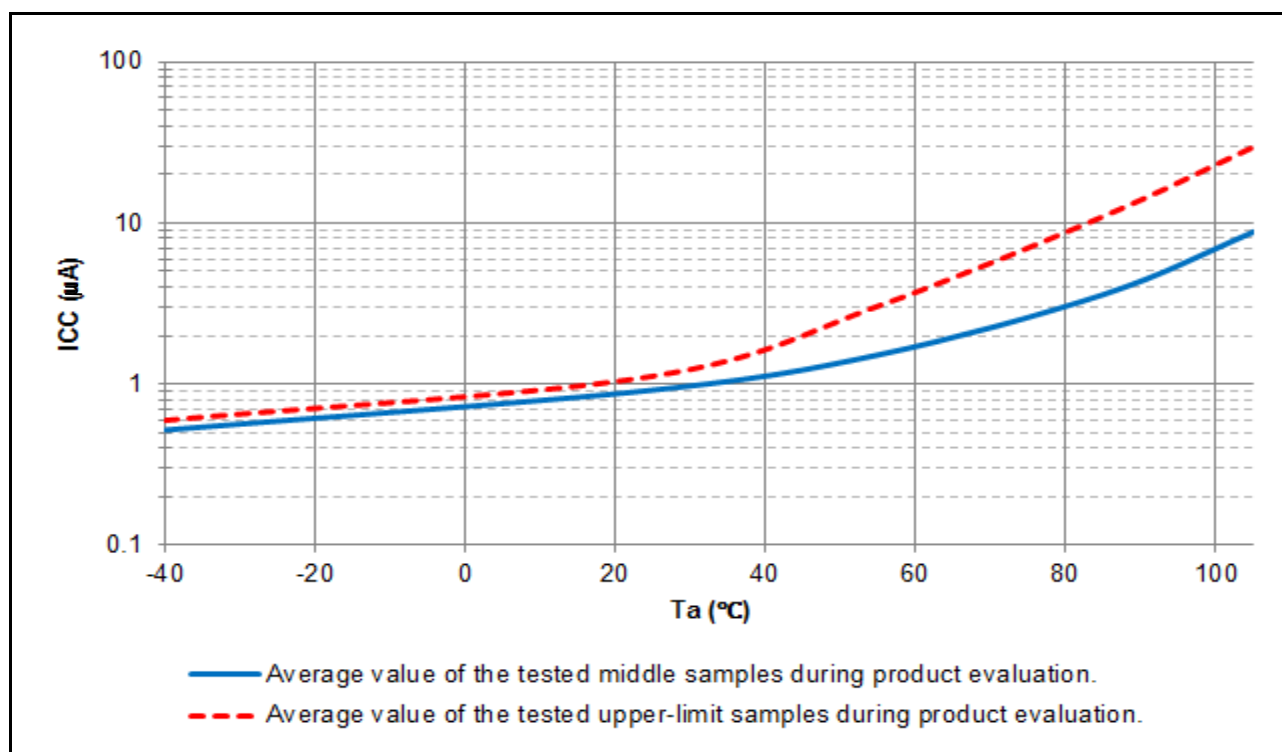


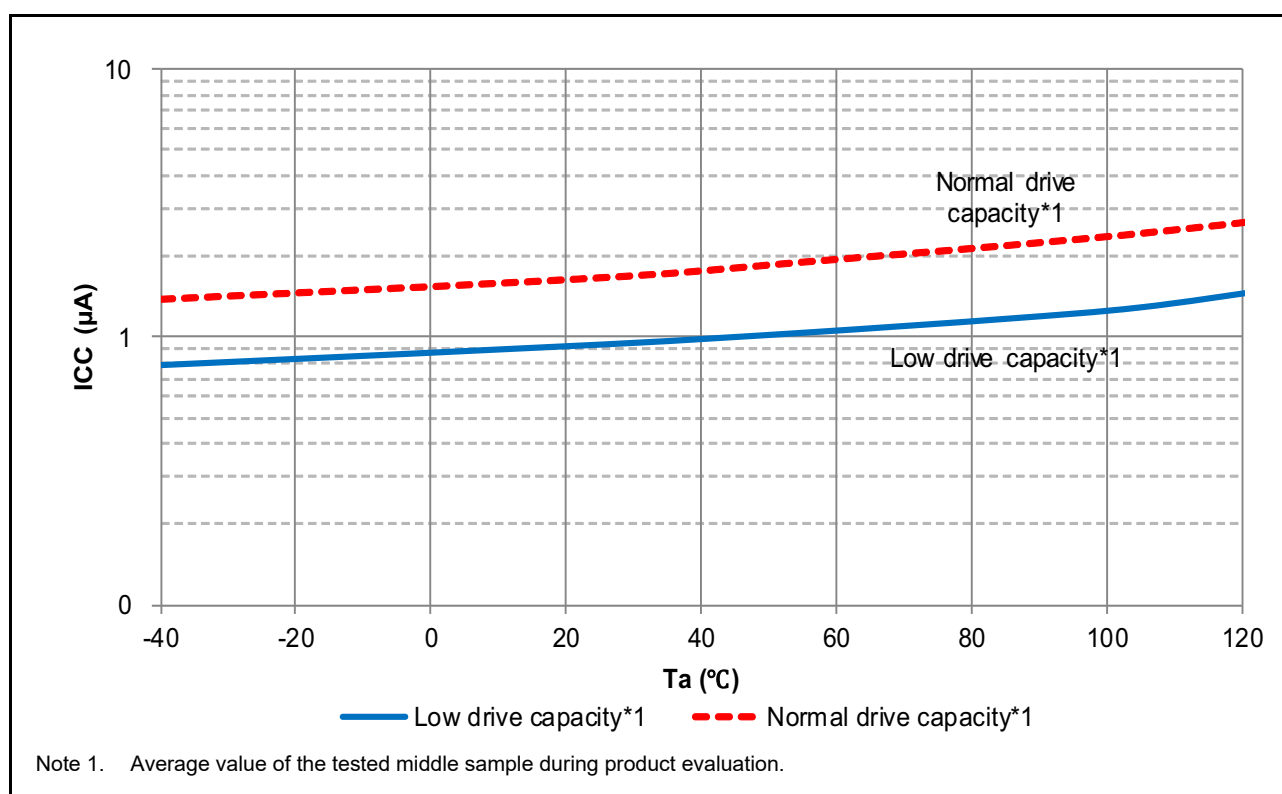
Figure 2.20 Temperature dependency in Software Standby mode all SRAM on (reference data)

**Table 2.13 Operating and standby current (3)**

Conditions: VCC = AVCC0 = 0V, VBATT = 1.8 to 3.6 V, VSS = AVSS0 = 0V

| Parameter        |                               |                       | Symbol          | Typ | Max | Unit | Test conditions                                                |
|------------------|-------------------------------|-----------------------|-----------------|-----|-----|------|----------------------------------------------------------------|
| Supply current*1 | RTC operation when VCC is off | T <sub>a</sub> = 25°C | I <sub>CC</sub> | 0.8 | -   | μA   | VBATT = 2.0 V<br>SOMCR.SORDRV[1:0] = 11b<br>(Low power mode 3) |
|                  |                               | T <sub>a</sub> = 55°C |                 | 0.9 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 85°C |                 | 1.1 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 25°C |                 | 0.9 | -   |      | VBATT = 3.3 V<br>SOMCR.SORDRV[1:0] = 11b<br>(Low power mode 3) |
|                  |                               | T <sub>a</sub> = 55°C |                 | 1.0 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 85°C |                 | 1.2 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 25°C |                 | 1.6 | -   |      | VBATT = 2.0 V<br>SOMCR.SORDRV[1:0] = 00b<br>(Normal mode)      |
|                  |                               | T <sub>a</sub> = 55°C |                 | 1.8 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 85°C |                 | 2.1 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 25°C |                 | 1.7 | -   |      | VBATT = 3.3 V<br>SOMCR.SORDRV[1:0] = 00b<br>(Normal mode)      |
|                  |                               | T <sub>a</sub> = 55°C |                 | 1.9 | -   |      |                                                                |
|                  |                               | T <sub>a</sub> = 85°C |                 | 2.2 | -   |      |                                                                |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

**Figure 2.21 Temperature dependency of RTC operation with VCC off (reference data)**

**Table 2.14 Operating and standby current (4)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V, VREFH0 = 2.7 V to AVCC0

| Parameter                                     |                                                                                                                                                                                                                                                                                             |                  | Symbol               | Min | Typ                           | Max | Unit | Test conditions |
|-----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|----------------------|-----|-------------------------------|-----|------|-----------------|
| Analog power supply current                   | During A/D conversion (at high-speed conversion)                                                                                                                                                                                                                                            |                  | I <sub>AVCC</sub>    | -   | -                             | 3.0 | mA   | -               |
|                                               | During A/D conversion (at low power conversion)                                                                                                                                                                                                                                             |                  |                      | -   | -                             | 1.0 | mA   | -               |
|                                               | During D/A conversion (per channel)*1                                                                                                                                                                                                                                                       |                  |                      | -   | 0.4                           | 0.8 | mA   | -               |
|                                               | Waiting for A/D and D/A conversion (all units)*6                                                                                                                                                                                                                                            |                  |                      | -   | -                             | 1.0 | μA   | -               |
| Reference power supply current                | During A/D conversion                                                                                                                                                                                                                                                                       |                  | I <sub>REFH0</sub>   | -   | -                             | 150 | μA   | -               |
|                                               | Waiting for A/D conversion (all units)                                                                                                                                                                                                                                                      |                  |                      | -   | -                             | 60  | nA   | -               |
|                                               | During D/A conversion                                                                                                                                                                                                                                                                       |                  | I <sub>REFH</sub>    | -   | 50                            | 100 | μA   | -               |
|                                               | Waiting for D/A conversion (all units)                                                                                                                                                                                                                                                      |                  |                      | -   | -                             | 100 | μA   | -               |
| Temperature sensor                            |                                                                                                                                                                                                                                                                                             |                  | I <sub>TNS</sub>     | -   | 75                            | -   | μA   | -               |
| Low-Power Analog Comparator operating current | Window mode                                                                                                                                                                                                                                                                                 |                  | I <sub>CMLP</sub>    | -   | 15                            | -   | μA   | -               |
|                                               | Comparator High-speed mode                                                                                                                                                                                                                                                                  |                  |                      | -   | 10                            | -   | μA   | -               |
|                                               | Comparator Low-speed mode                                                                                                                                                                                                                                                                   |                  |                      | -   | 2                             | -   | μA   | -               |
|                                               | Comparator Low-speed mode using DAC8                                                                                                                                                                                                                                                        |                  |                      | -   | 820                           | -   | μA   | -               |
| Operational Amplifier operating current       | Low power mode                                                                                                                                                                                                                                                                              | 1 unit operating | I <sub>AMP</sub>     | -   | 2.5                           | 4.0 | μA   | -               |
|                                               | High speed mode                                                                                                                                                                                                                                                                             | 1 unit operating |                      | -   | 140                           | 220 | μA   | -               |
| LCD operating current                         | External resistance division method<br>f <sub>LCD</sub> = f <sub>SUB</sub> = 128 Hz, 1/3 bias, and 4-time slice                                                                                                                                                                             |                  | I <sub>LCD1</sub> *5 | -   | 0.34                          | -   | μA   | -               |
| USB operating current                         | During USB communication operation under the following settings and conditions:<br>• Host controller operation is set to full-speed mode<br>Bulk OUT transfer (64 bytes) × 1,<br>bulk IN transfer (64 bytes) × 1<br>• Connect peripheral devices via a 1-meter USB cable from the USB port. |                  | I <sub>USBH</sub> *2 | -   | 4.3 (VCC)<br>0.9 (VCC_USB)*4  | -   | mA   | -               |
|                                               | During USB communication operation under the following settings and conditions:<br>• Device controller operation is set to full-speed mode<br>Bulk OUT transfer (64 bytes) × 1,<br>bulk IN transfer (64 bytes) × 1<br>• Connect the host device via a 1-meter USB cable from the USB port.  |                  | I <sub>USBF</sub> *2 | -   | 3.6 (VCC)<br>1.1 (VCC_USB)*4  | -   | mA   | -               |
|                                               | During suspended state under the following setting and conditions:<br>• Device controller operation is set to full-speed mode (pull up the USB_DP pin)<br>• Software standby mode<br>• Connect the host device via a 1-meter USB cable from the USB port.                                   |                  | I <sub>SUSP</sub> *3 | -   | 0.35 (VCC)<br>170 (VCC_USB)*4 | -   | μA   | -               |

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. Current consumed only by the USBFS.

Note 3. Includes the current supplied from the pull-up resistor of the USB\_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.

Note 4. When VCC = VCC\_USB = 3.3 V.

Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.

Note 6. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 Module Stop bit) is in the module-stop state.

**Table 2.15 Operating and standby current (5)**

Conditions: VCC = VCC\_RF = AVCC\_RF = 3.3 V, VSS = VSS\_RF = 0 V, Ta = +25°C

| Parameter                                                    |                                         | Symbol   | Min | Typ                   |       | Max | Unit | Test conditions |
|--------------------------------------------------------------|-----------------------------------------|----------|-----|-----------------------|-------|-----|------|-----------------|
|                                                              |                                         |          |     | Transmit output power |       |     |      |                 |
|                                                              |                                         |          |     | 0 dBm                 | 4 dBm |     |      |                 |
| BLE operating current<br>(When DC-DC converter is selected)  | Transmit mode, 2 Mbps                   | Idd_tx   | -   | 4.5                   | 8.7   | -   | mA   | -               |
|                                                              | Transmit mode, 1 Mbps                   |          | -   |                       |       | -   | mA   | -               |
|                                                              | Transmit mode, 500 kbps                 |          | -   |                       |       | -   | mA   | -               |
|                                                              | Transmit mode, 125 kbps                 |          | -   |                       |       | -   | mA   | -               |
|                                                              | Receive mode, 2 Mbps<br>Prf = -67 dBm   | Idd_rx   | -   | 3.3                   | 3.5   | -   | mA   | -               |
|                                                              | Receive mode, 1 Mbps<br>Prf = -67 dBm   |          | -   |                       |       | -   | mA   | -               |
|                                                              | Receive mode, 500 kbps<br>Prf = -72 dBm |          | -   |                       |       | -   | mA   | -               |
|                                                              | Receive mode, 125 kbps<br>Prf = -79 dBm |          | -   |                       |       | -   | mA   | -               |
|                                                              | Idle mode                               | Idd_idle | -   | 0.5                   |       | -   | mA   | -               |
|                                                              | Deep sleep mode                         | Idd_slp  | -   | 1.5                   |       | -   | μA   | -               |
|                                                              | Power down mode                         | Idd_down | -   | 0.1                   |       | -   | μA   | -               |
| BLE operating current<br>(When linear regulator is selected) | Transmit mode, 2 Mbps                   | Idd_tx   | -   | 10.2                  | 18.1  | -   | mA   | -               |
|                                                              | Transmit mode, 1 Mbps                   |          | -   |                       |       | -   | mA   | -               |
|                                                              | Transmit mode, 500 kbps                 |          | -   |                       |       | -   | mA   | -               |
|                                                              | Transmit mode, 125 kbps                 |          | -   |                       |       | -   | mA   | -               |
|                                                              | Receive mode, 2M bps<br>Prf = -67 dBm   | Idd_rx   | -   | 6.9                   |       | -   | mA   | -               |
|                                                              | Receive mode, 1 Mbps<br>Prf = -67 dBm   |          | -   | 6.9                   |       | -   | mA   | -               |
|                                                              | Receive mode, 500 kbps<br>Prf = -72 dBm |          | -   | 6.9                   |       | -   | mA   | -               |
|                                                              | Receive mode, 125 kbps<br>Prf = -79 dBm |          | -   | 7.1                   |       | -   | mA   | -               |
|                                                              | Idd_idle                                | Idd_idle | -   | 0.7                   |       | -   | mA   | -               |
|                                                              | Idd_slp                                 | Idd_slp  | -   | 1.5                   |       | -   | μA   | -               |
|                                                              | Idd_down                                | Idd_down | -   | 0.1                   |       | -   | μA   | -               |

## 2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.16 Rise and fall gradient characteristics**

Conditions: VCC = AVCC0 = 0 to 3.6 V

| Parameter                    |                                                              | Symbol | Min  | Typ | Max | Unit | Test conditions |
|------------------------------|--------------------------------------------------------------|--------|------|-----|-----|------|-----------------|
| Power-on VCC rising gradient | Voltage monitor 0 reset disabled at startup (normal startup) | SrVCC  | 0.02 | -   | 2   | ms/V | -               |
|                              | Voltage monitor 0 reset enabled at startup*1                 |        | 0.02 | -   | -   |      |                 |
|                              | SCI/USB Boot mode*2                                          |        | 0.02 | -   | 2   |      |                 |

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

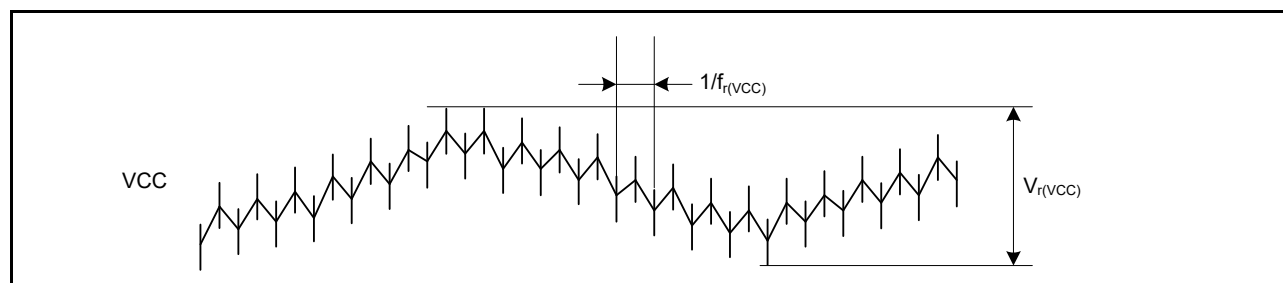
**Table 2.17 Rising and falling gradient and ripple frequency characteristics**

Conditions: VCC = AVCC0 = VCC\_USB = 1.8 to 3.6 V

The ripple voltage must meet the allowable ripple frequency  $f_r(VCC)$  within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).

When VCC change exceeds VCC  $\pm 10\%$ , the allowable voltage change rising/falling gradient  $dt/dVCC$  must be met.

| Parameter                                            | Symbol     | Min | Typ | Max | Unit | Test conditions                                |
|------------------------------------------------------|------------|-----|-----|-----|------|------------------------------------------------|
| Allowable ripple frequency                           | $f_r(VCC)$ | -   | -   | 10  | kHz  | Figure 2.22<br>$V_r(VCC) \leq VCC \times 0.2$  |
|                                                      |            | -   | -   | 1   | MHz  | Figure 2.22<br>$V_r(VCC) \leq VCC \times 0.08$ |
|                                                      |            | -   | -   | 10  | MHz  | Figure 2.22<br>$V_r(VCC) \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$  | 1.0 | -   | -   | ms/V | When VCC change exceeds VCC $\pm 10\%$         |



**Figure 2.22 Ripple waveform**

## 2.3 AC Characteristics

### 2.3.1 Frequency

**Table 2.18 Operation frequency value in high-speed operating mode**

Conditions: VCC = AVCC0 = 2.4 to 3.6 V

| Parameter           |                                       |              | Symbol | Min      | Typ | Max*5 | Unit |
|---------------------|---------------------------------------|--------------|--------|----------|-----|-------|------|
| Operation frequency | System clock (ICLK)*4                 | 2.7 to 3.6 V | f      | 0.032768 | -   | 48    | MHz  |
|                     |                                       | 2.4 to 2.7 V |        | 0.032768 | -   | 16    |      |
|                     | FlashIF clock (FCLK)*1, *2, *4        | 2.7 to 3.6 V |        | 0.032768 | -   | 32    |      |
|                     |                                       | 2.4 to 2.7 V |        | 0.032768 | -   | 16    |      |
|                     | Peripheral module clock (PCLKA)*4     | 2.7 to 3.6 V |        | -        | -   | 48    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 16    |      |
|                     | Peripheral module clock (PCLKB)*4     | 2.7 to 3.6 V |        | -        | -   | 32    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 16    |      |
|                     | Peripheral module clock (PCLKC)*3, *4 | 2.7 to 3.6 V |        | -        | -   | 64    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 16    |      |
|                     | Peripheral module clock (PCLKD)*4     | 2.7 to 3.6 V |        | -        | -   | 64    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 16    |      |

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
- Note 5. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.23, Clock timing](#).

**Table 2.19 Operation frequency value in Middle-speed mode**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter           |                                       |              | Symbol | Min      | Typ | Max*5 | Unit |
|---------------------|---------------------------------------|--------------|--------|----------|-----|-------|------|
| Operation frequency | System clock (ICLK)*4                 | 2.7 to 3.6 V | f      | 0.032768 | -   | 12    | MHz  |
|                     |                                       | 2.4 to 2.7 V |        | 0.032768 | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | 0.032768 | -   | 8     |      |
|                     | FlashIF clock (FCLK)*1, *2, *4        | 2.7 to 3.6 V |        | 0.032768 | -   | 12    |      |
|                     |                                       | 2.4 to 2.7 V |        | 0.032768 | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | 0.032768 | -   | 8     |      |
|                     | Peripheral module clock (PCLKA)*4     | 2.7 to 3.6 V |        | -        | -   | 12    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | -        | -   | 8     |      |
|                     | Peripheral module clock (PCLKB)*4     | 2.7 to 3.6 V |        | -        | -   | 12    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | -        | -   | 8     |      |
|                     | Peripheral module clock (PCLKC)*3, *4 | 2.7 to 3.6 V |        | -        | -   | 12    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | -        | -   | 8     |      |
|                     | Peripheral module clock (PCLKD)*4     | 2.7 to 3.6 V |        | -        | -   | 12    |      |
|                     |                                       | 2.4 to 2.7 V |        | -        | -   | 12    |      |
|                     |                                       | 1.8 to 2.4 V |        | -        | -   | 8     |      |

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
- Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.23, Clock timing](#).

**Table 2.20 Operation frequency value in Low-speed mode**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter           |                                       |              | Symbol | Min      | Typ | Max*4 | Unit |
|---------------------|---------------------------------------|--------------|--------|----------|-----|-------|------|
| Operation frequency | System clock (ICLK)*3                 | 1.8 to 3.6 V | f      | 0.032768 | -   | 1     | MHz  |
|                     | FlashIF clock (FCLK)*1, *3            | 1.8 to 3.6 V |        | 0.032768 | -   | 1     |      |
|                     | Peripheral module clock (PCLKA)*3     | 1.8 to 3.6 V |        | -        | -   | 1     |      |
|                     | Peripheral module clock (PCLKB)*3     | 1.8 to 3.6 V |        | -        | -   | 1     |      |
|                     | Peripheral module clock (PCLKC)*2, *3 | 1.8 to 3.6 V |        | -        | -   | 1     |      |
|                     | Peripheral module clock (PCLKD)*3     | 1.8 to 3.6 V |        | -        | -   | 1     |      |

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.
- Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.
- Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
- Note 4. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.23, Clock timing](#).

**Table 2.21 Operation frequency value in low-voltage mode**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter           |                                       |              | Symbol | Min      | Typ | Max*5 | Unit |
|---------------------|---------------------------------------|--------------|--------|----------|-----|-------|------|
| Operation frequency | System clock (ICLK)*4                 | 1.8 to 3.6 V | f      | 0.032768 | -   | 4     | MHz  |
|                     | FlashIF clock (FCLK)*1, *2, *4        | 1.8 to 3.6 V |        | 0.032768 | -   | 4     |      |
|                     | Peripheral module clock (PCLKA)*4     | 1.8 to 3.6 V |        | -        | -   | 4     |      |
|                     | Peripheral module clock (PCLKB)*4     | 1.8 to 3.6 V |        | -        | -   | 4     |      |
|                     | Peripheral module clock (PCLKC)*3, *4 | 1.8 to 3.6 V |        | -        | -   | 4     |      |
|                     | Peripheral module clock (PCLKD)*4     | 1.8 to 3.6 V |        | -        | -   | 4     |      |

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of FCLK must be  $\pm 3.5\%$  while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK.
- Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.23, Clock timing](#).

**Table 2.22 Operation frequency value in Subosc-speed mode**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

| Parameter           |                                       |              | Symbol | Min     | Typ    | Max     | Unit |
|---------------------|---------------------------------------|--------------|--------|---------|--------|---------|------|
| Operation frequency | System clock (ICLK)*3                 | 1.8 to 3.6 V | f      | 27.8528 | 32.768 | 37.6832 | kHz  |
|                     | FlashIF clock (FCLK)*1, *3            | 1.8 to 3.6 V |        | 27.8528 | 32.768 | 37.6832 |      |
|                     | Peripheral module clock (PCLKA)*3     | 1.8 to 3.6 V |        | -       | -      | 37.6832 |      |
|                     | Peripheral module clock (PCLKB)*3     | 1.8 to 3.6 V |        | -       | -      | 37.6832 |      |
|                     | Peripheral module clock (PCLKC)*2, *3 | 1.8 to 3.6 V |        | -       | -      | 37.6832 |      |
|                     | Peripheral module clock (PCLKD)*3     | 1.8 to 3.6 V |        | -       | -      | 37.6832 |      |

Note 1. Programming and erasing the flash memory is not possible.

Note 2. The 14-bit A/D converter cannot be used.

Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

### 2.3.2 Clock Timing

**Table 2.23 Clock timing (1 of 2)**

| Parameter                                                              | Symbol                 | Min     | Typ    | Max     | Unit | Test conditions                      |
|------------------------------------------------------------------------|------------------------|---------|--------|---------|------|--------------------------------------|
| EXTAL external clock input cycle time                                  | t <sub>Xcyc</sub>      | 50      | -      | -       | ns   | Figure 2.23                          |
| EXTAL external clock input high pulse width                            | t <sub>XH</sub>        | 20      | -      | -       | ns   |                                      |
| EXTAL external clock input low pulse width                             | t <sub>XL</sub>        | 20      | -      | -       | ns   |                                      |
| EXTAL external clock rising time                                       | t <sub>Xr</sub>        | -       | -      | 5       | ns   |                                      |
| EXTAL external clock falling time                                      | t <sub>Xf</sub>        | -       | -      | 5       | ns   |                                      |
| EXTAL external clock input wait time*1                                 | t <sub>EXWT</sub>      | 0.3     | -      | -       | μs   | -                                    |
| EXTAL external clock input frequency                                   | f <sub>EXTAL</sub>     | -       | -      | 20      | MHz  | 2.4 ≤ VCC ≤ 3.6                      |
|                                                                        |                        | -       | -      | 8       |      | 1.8 ≤ VCC < 2.4                      |
| Main clock oscillator oscillation frequency                            | f <sub>MAIN</sub>      | 1       | -      | 20      | MHz  | 2.4 ≤ VCC ≤ 3.6                      |
|                                                                        |                        | 1       | -      | 8       |      | 1.8 ≤ VCC < 2.4                      |
| Main clock oscillator stabilization wait time (crystal)*9              | t <sub>MAINOSCWT</sub> | -       | -      | ~*9     | ms   |                                      |
| LOCO clock oscillation frequency                                       | f <sub>LOCO</sub>      | 27.8528 | 32.768 | 37.6832 | kHz  | -                                    |
| LOCO clock oscillation stabilization time                              | t <sub>LOCO</sub>      | -       | -      | 100     | μs   | Figure 2.24                          |
| IWDT-dedicated clock oscillation frequency                             | f <sub>ILOCO</sub>     | 12.75   | 15     | 17.25   | kHz  | -                                    |
| Bluetooth-dedicated clock oscillation frequency                        | f <sub>BLECK</sub>     | -       | 32     | -       | MHz  |                                      |
| Bluetooth-dedicated low-speed on-chip oscillator oscillation frequency | f <sub>BLELOCO</sub>   | -       | 32.768 | -       | kHz  |                                      |
| MOCO clock oscillation frequency                                       | f <sub>MOCO</sub>      | 6.8     | 8      | 9.2     | MHz  | -                                    |
| MOCO clock oscillation stabilization time                              | t <sub>MOCO</sub>      | -       | -      | 1       | μs   | -                                    |
| HOCO clock oscillation frequency                                       | f <sub>HOCO24</sub>    | 23.64   | 24     | 24.36   | MHz  | Ta = -40 to -20°C<br>1.8 ≤ VCC ≤ 3.6 |
|                                                                        |                        | 23.76   | 24     | 24.24   |      | Ta = -20 to 85°C<br>1.8 ≤ VCC ≤ 3.6  |
|                                                                        | f <sub>HOCO32</sub>    | 31.52   | 32     | 32.48   |      | Ta = -40 to -20°C<br>1.8 ≤ VCC ≤ 3.6 |
|                                                                        |                        | 31.68   | 32     | 32.32   |      | Ta = -20 to 85°C<br>1.8 ≤ VCC ≤ 3.6  |
|                                                                        | f <sub>HOCO48</sub> *4 | 47.28   | 48     | 48.72   |      | Ta = -40 to -20°C<br>1.8 ≤ VCC ≤ 3.6 |
|                                                                        |                        | 47.52   | 48     | 48.48   |      | Ta = -20 to 85°C<br>1.8 ≤ VCC ≤ 3.6  |
|                                                                        | f <sub>HOCO64</sub> *5 | 63.04   | 64     | 64.96   |      | Ta = -40 to -20°C<br>2.4 ≤ VCC ≤ 3.6 |
|                                                                        |                        | 63.36   | 64     | 64.64   |      | Ta = -20 to 85°C<br>2.4 ≤ VCC ≤ 3.6  |

**Table 2.23 Clock timing (2 of 2)**

| Parameter                                       |                         | Symbol       | Min | Typ    | Max   | Unit    | Test conditions |
|-------------------------------------------------|-------------------------|--------------|-----|--------|-------|---------|-----------------|
| HOCO clock oscillation stabilization time*6, *7 | Except low-voltage mode | $t_{HOCO24}$ | -   | -      | 37.1  | $\mu$ s | Figure 2.25     |
|                                                 |                         | $t_{HOCO32}$ | -   | -      |       |         |                 |
|                                                 |                         | $t_{HOCO48}$ | -   | -      | 43.3  |         |                 |
|                                                 | Low-Voltage mode        | $t_{HOCO64}$ | -   | -      | 80.6  |         |                 |
|                                                 |                         | $t_{HOCO24}$ | -   | -      | 100.9 |         |                 |
|                                                 |                         | $t_{HOCO32}$ | -   | -      |       |         |                 |
| PLL input frequency*2                           |                         | $f_{PLLIN}$  | 4   | -      | 12.5  | MHz     | -               |
| PLL circuit oscillation frequency*2             |                         | $f_{PLL}$    | 24  | -      | 64    | MHz     | -               |
| PLL clock oscillation stabilization time*8      |                         | $t_{PLL}$    | -   | -      | 55.5  | $\mu$ s | Figure 2.27     |
| PLL free-running oscillation frequency          |                         | $f_{PLLFR}$  | -   | 8      | -     | MHz     | -               |
| Sub-clock oscillator oscillation frequency      |                         | $f_{SUB}$    | -   | 32.768 | -     | kHz     | -               |
| Sub-clock oscillation stabilization time*3      |                         | $t_{SUBOSC}$ | -   | -      | -*3   | s       | Figure 2.28     |

Note 1. Time until the clock can be used after the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. The VCC range that the PLL can be used is 2.4 to 3.6 V.

Note 3. After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapses, that is greater than or equal to the value recommended by the oscillator manufacturer.

Note 4. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 3.6 V.

Note 5. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 3.6 V.

Note 6. This is a characteristic when HOCOCCR.HCSTP bit is set to 0 (oscillation) in MOCO stop state.

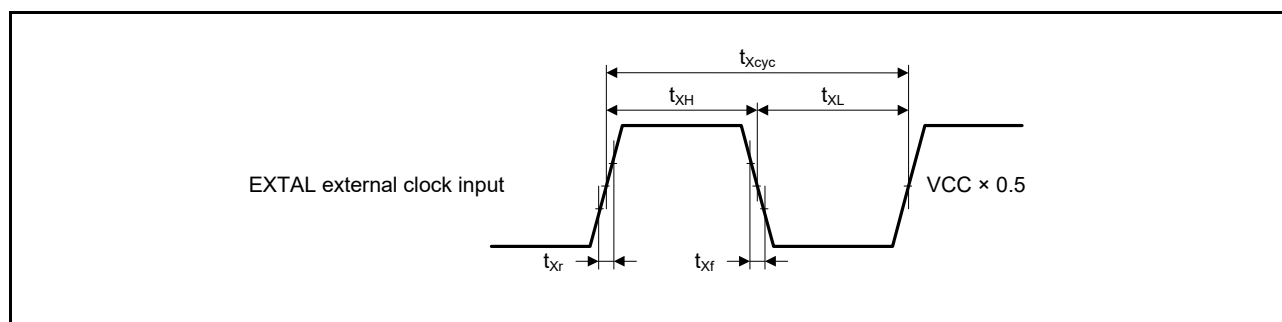
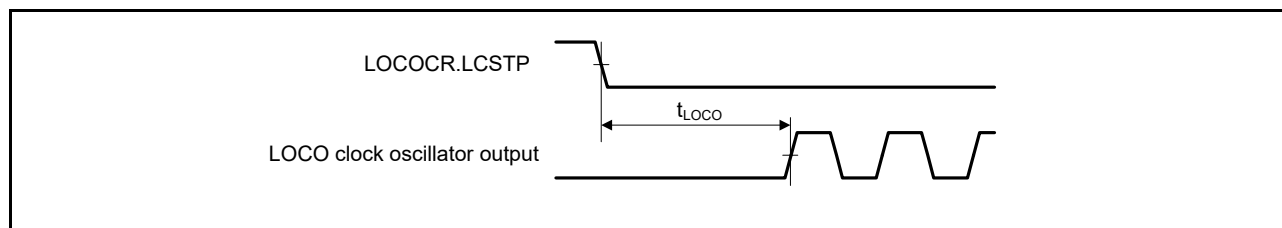
When HOCOCCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1  $\mu$ s.

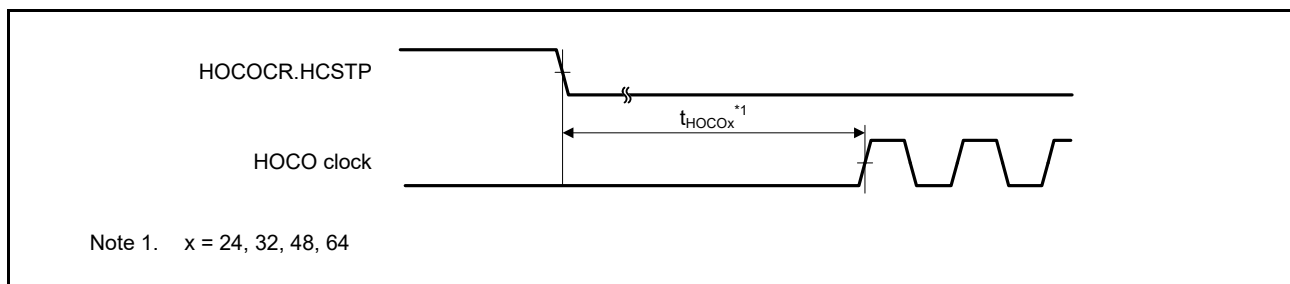
Note 7. Whether stabilization time has elapsed can be confirmed by OSCSF.HOCOSF.

Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in MOCO stop state.

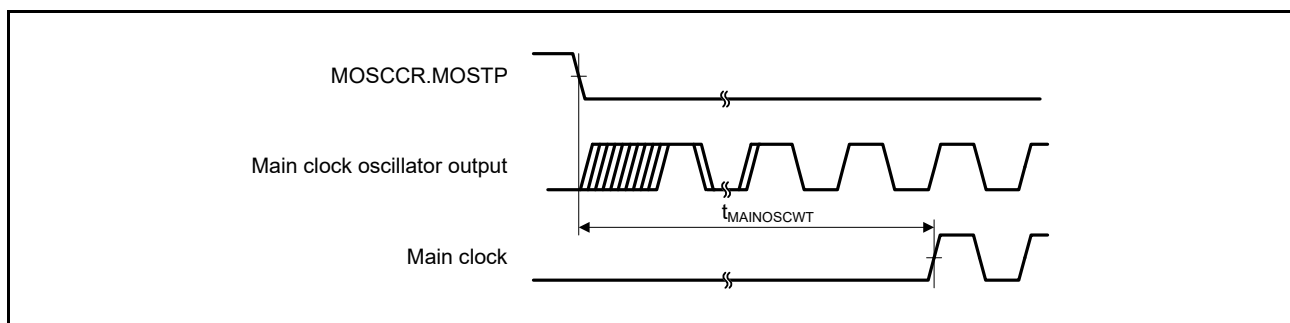
When PLLCR.PLLSTP bit is set to 0 (operation) during MOCO oscillation, this specification is shortened by 1  $\mu$ s.

Note 9. When setting up the main clock, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended stabilization time. After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCSF.MOSCSF flag to confirm that it is 1, then start using the main clock.

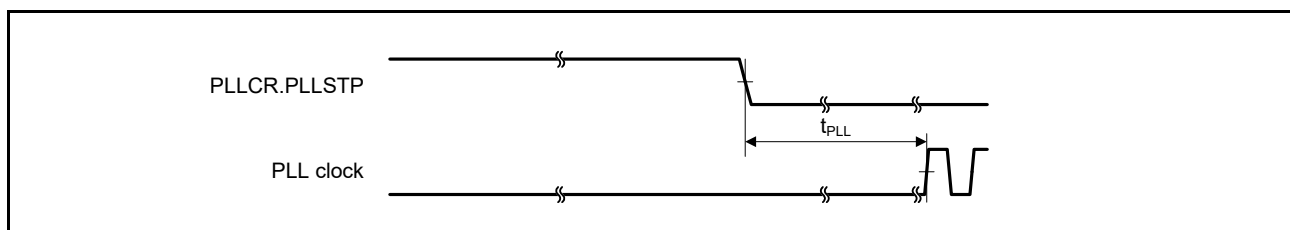
**Figure 2.23 EXTAL external clock input timing****Figure 2.24 LOCO clock oscillator start timing**



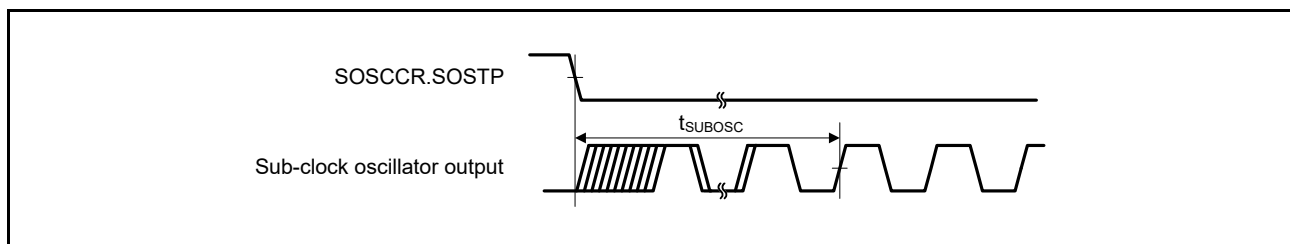
**Figure 2.25** HOCO clock oscillation start timing (started by setting HOCOCR.HCSTP bit)



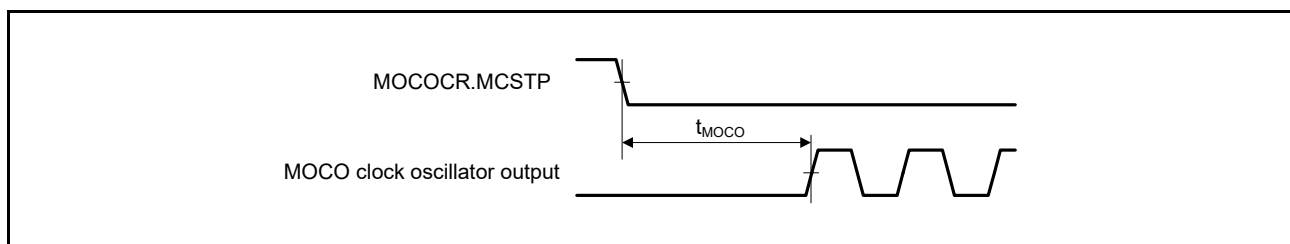
**Figure 2.26** Main clock oscillation start timing



**Figure 2.27** PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)



**Figure 2.28** Sub-clock oscillation start timing



**Figure 2.29** MOCO clock oscillation start timing

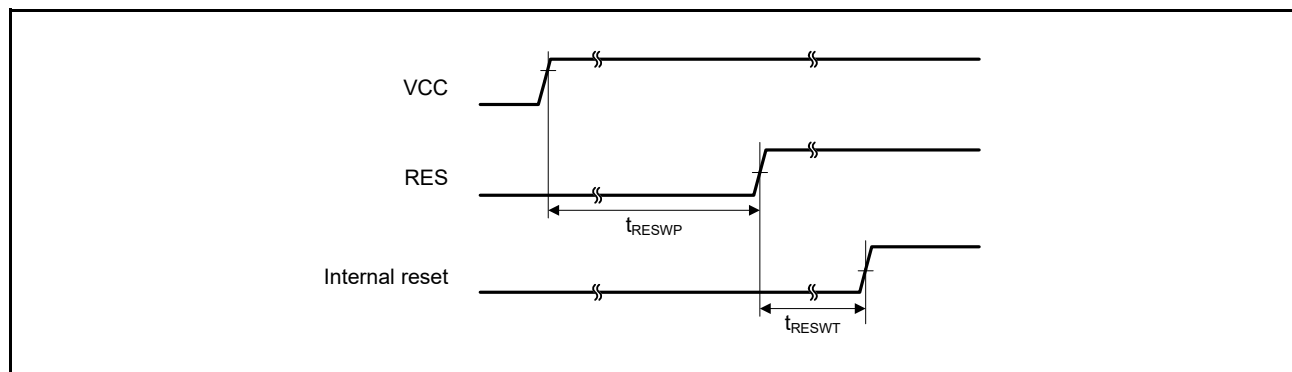
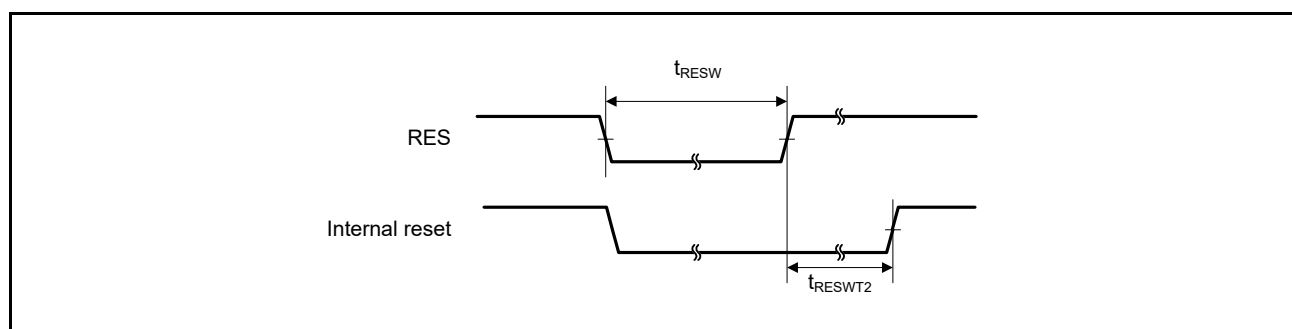
### 2.3.3 Reset Timing

**Table 2.24 Reset timing**

| Parameter                                                                                                                                                                                                |                  | Symbol       | Min | Typ  | Max | Unit    | Test conditions             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|-----|------|-----|---------|-----------------------------|
| RES pulse width                                                                                                                                                                                          | At power-on      | $t_{RESWP}$  | 3   | -    | -   | ms      | <a href="#">Figure 2.30</a> |
|                                                                                                                                                                                                          | Other than above | $t_{RESW}$   | 30  | -    | -   | $\mu$ s | <a href="#">Figure 2.31</a> |
| Wait time after RES cancellation (at power-on)                                                                                                                                                           | LVD0: enable*1   | $t_{RESWT}$  | -   | 0.7  | -   | ms      | <a href="#">Figure 2.30</a> |
|                                                                                                                                                                                                          | LVD0: disable*2  |              | -   | 0.3  | -   |         |                             |
| Wait time after RES cancellation (during powered-on state)                                                                                                                                               | LVD0: enable*1   | $t_{RESWT2}$ | -   | 0.5  | -   | ms      | <a href="#">Figure 2.31</a> |
|                                                                                                                                                                                                          | LVD0: disable*2  |              | -   | 0.05 | -   |         |                             |
| Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, Stack pointer error reset, Software reset) | LVD0: enable*1   | $t_{RESWT3}$ | -   | 0.6  | -   | ms      |                             |
|                                                                                                                                                                                                          | LVD0: disable*2  |              | -   | 0.15 | -   |         |                             |

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.


**Figure 2.30 Reset input timing at power-on**

**Figure 2.31 Reset input timing (1)**

### 2.3.4 Wakeup Time

**Table 2.25 Timing of recovery from low power modes (1)**

| Parameter                                  |                 |                                                      |                                                                  | Symbol             | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------------|-----------------|------------------------------------------------------|------------------------------------------------------------------|--------------------|-----|-----|-----|------|-----------------|
| Recovery time from Software Standby mode*1 | High-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (20 MHz)*2          | t <sub>SBYMC</sub> | -   | 2   | 3   | ms   | Figure 2.32     |
|                                            |                 |                                                      | System clock source is PLL (48 MHz) with Main clock oscillator*2 | t <sub>SBYPC</sub> | -   | 2   | 3   | ms   |                 |
|                                            |                 | External clock input to main clock oscillator        | System clock source is main clock oscillator (20 MHz)*3          | t <sub>SBYEX</sub> | -   | 14  | 25  | μs   |                 |
|                                            |                 |                                                      | System clock source is PLL (48 MHz) with Main clock oscillator*3 | t <sub>SBYPE</sub> | -   | 53  | 76  | μs   |                 |
|                                            |                 | System clock source is HOCO*4 (HOCO clock is 32 MHz) |                                                                  | t <sub>SBYHO</sub> | -   | 43  | 52  | μs   |                 |
|                                            |                 | System clock source is HOCO*4 (HOCO clock is 48 MHz) |                                                                  | t <sub>SBYHO</sub> | -   | 44  | 52  | μs   |                 |
|                                            |                 | System clock source is HOCO*5 (HOCO clock is 64 MHz) |                                                                  | t <sub>SBYHO</sub> | -   | 82  | 110 | μs   |                 |
|                                            |                 | System clock source is MOCO                          |                                                                  | t <sub>SBYMO</sub> | -   | 16  | 25  | μs   |                 |

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.

Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

**Table 2.26 Timing of recovery from low power modes (2)**

| Parameter                                  |                   |                                                      |                                                                  | Symbol             | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------------|-------------------|------------------------------------------------------|------------------------------------------------------------------|--------------------|-----|-----|-----|------|-----------------|
| Recovery time from Software Standby mode*1 | Middle-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (12 MHz)*2          | t <sub>SBYMC</sub> | -   | 2   | 3   | ms   | Figure 2.32     |
|                                            |                   |                                                      | System clock source is PLL (24 MHz) with main clock oscillator*2 | t <sub>SBYPC</sub> | -   | 2   | 3   | ms   |                 |
|                                            |                   | External clock input to main clock oscillator        | System clock source is main clock oscillator (12 MHz)*3          | t <sub>SBYEX</sub> | -   | 2.9 | 10  | μs   |                 |
|                                            |                   |                                                      | System clock source is PLL (24 MHz) with main clock oscillator*3 | t <sub>SBYPE</sub> | -   | 49  | 76  | μs   |                 |
|                                            |                   | System clock source is HOCO (24 MHz)                 |                                                                  | t <sub>SBYHO</sub> | -   | 38  | 50  | μs   |                 |
|                                            |                   | System clock source is MOCO                          |                                                                  | t <sub>SBYMO</sub> | -   | 3.5 | 5.5 | μs   |                 |

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.27 Timing of recovery from low power modes (3)**

| Parameter                                              |                |                                                      |                                                                    | Symbol      | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------------------------|----------------|------------------------------------------------------|--------------------------------------------------------------------|-------------|-----|-----|-----|------|-----------------|
| Recovery time from Software Standby mode* <sup>1</sup> | Low-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (1 MHz)* <sup>2</sup> | $t_{SBYMC}$ | -   | 2   | 3   | ms   | Figure 2.32     |
|                                                        |                | External clock input to main clock oscillator        | System clock source is main clock oscillator (1 MHz)* <sup>3</sup> | $t_{SBYEX}$ | -   | 28  | 50  | μs   |                 |
|                                                        |                | System clock source is MOCO                          |                                                                    | $t_{SBYMO}$ | -   | 25  | 35  | μs   |                 |

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.28 Timing of recovery from low power modes (4)**

| Parameter                                              |                  |                                                      |                                                                    | Symbol      | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------------------------|------------------|------------------------------------------------------|--------------------------------------------------------------------|-------------|-----|-----|-----|------|-----------------|
| Recovery time from Software Standby mode* <sup>1</sup> | Low-voltage mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (4 MHz)* <sup>2</sup> | $t_{SBYMC}$ | -   | 2   | 3   | ms   | Figure 2.32     |
|                                                        |                  | External clock input to main clock oscillator        | System clock source is main clock oscillator (4 MHz)* <sup>3</sup> | $t_{SBYEX}$ | -   | 108 | 130 | μs   |                 |
|                                                        |                  | System clock source is HOCO                          |                                                                    | $t_{SBYHO}$ | -   | 108 | 130 | μs   |                 |

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined by the following expression.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

**Table 2.29 Timing of recovery from low power modes (5)**

| Parameter                                  |                   |                                                          | Symbol             | Min | Typ  | Max | Unit | Test conditions |
|--------------------------------------------|-------------------|----------------------------------------------------------|--------------------|-----|------|-----|------|-----------------|
| Recovery time from Software Standby mode*1 | Subosc-speed mode | System clock source is sub-clock oscillator (32.768 kHz) | t <sub>SBYSC</sub> | -   | 0.85 | 1   | ms   | Figure 2.32     |
|                                            |                   | System clock source is LOCO (32.768 kHz)                 | t <sub>SBYLO</sub> | -   | 0.85 | 1.2 | ms   |                 |

Note 1. The sub-clock oscillator or LOCO itself continues to oscillate in Software Standby mode during Subosc-speed mode.

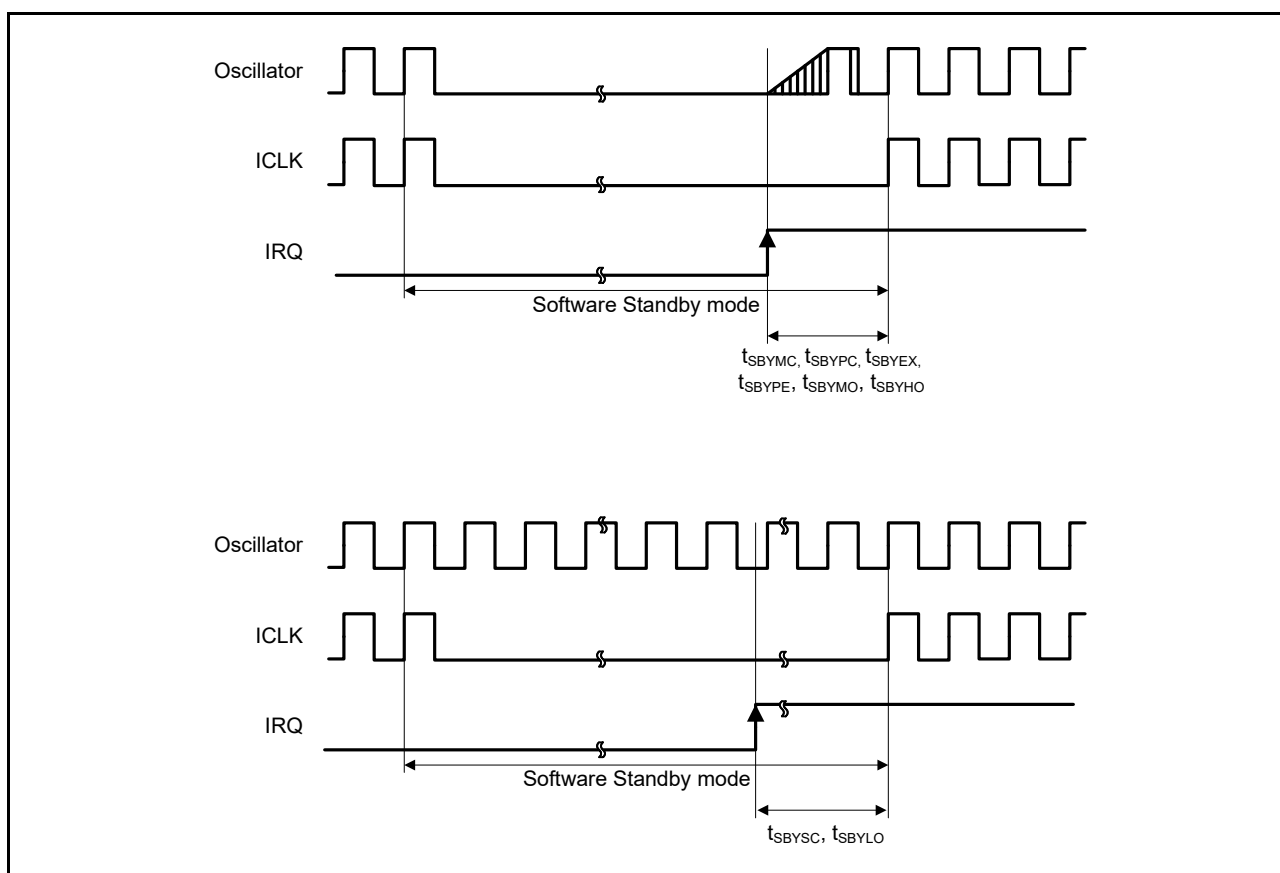
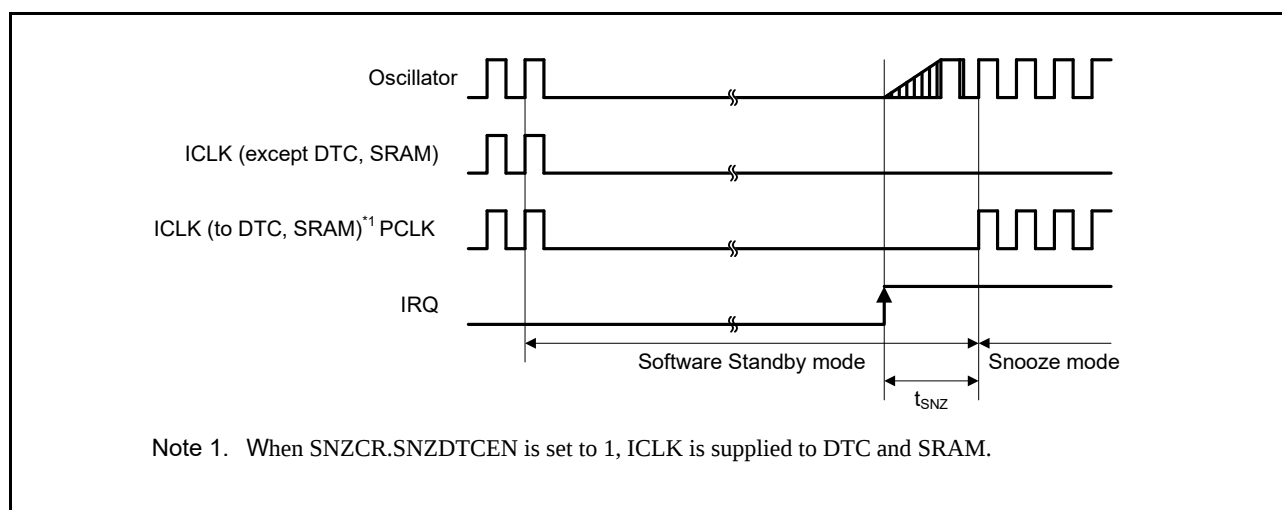


Figure 2.32 Software Standby mode cancellation timing

Table 2.30 Timing of recovery from low power modes (6)

| Parameter                                               |                                                  | Symbol    | Min | Typ | Max | Unit    | Test conditions |
|---------------------------------------------------------|--------------------------------------------------|-----------|-----|-----|-----|---------|-----------------|
| Recovery time from Software Standby mode to Snooze mode | High-speed mode<br>System clock source is HOCO   | $t_{SNZ}$ | -   | 36  | 45  | $\mu s$ | Figure 2.33     |
|                                                         | Middle-speed mode<br>System clock source is MOCO | $t_{SNZ}$ | -   | 1.3 | 3.6 | $\mu s$ |                 |
|                                                         | Low-speed mode<br>System clock source is MOCO    | $t_{SNZ}$ | -   | 10  | 13  | $\mu s$ |                 |
|                                                         | Low-voltage mode<br>System clock source is HOCO  | $t_{SNZ}$ | -   | 87  | 110 | $\mu s$ |                 |



**Figure 2.33** Recovery timing from Software Standby mode to Snooze mode

## 2.3.5 NMI and IRQ Noise Filter

**Table 2.31 NMI and IRQ noise filter**

| Parameter       | Symbol            | Min                                | Typ | Max | Unit | Test conditions             |                                                 |
|-----------------|-------------------|------------------------------------|-----|-----|------|-----------------------------|-------------------------------------------------|
| NMI pulse width | $t_{\text{NMIW}}$ | 200                                | -   | -   | ns   | NMI digital filter disabled | $t_{\text{Pcyc}} \times 2 \leq 200 \text{ ns}$  |
|                 |                   | $t_{\text{Pcyc}} \times 2^{*1}$    | -   | -   |      |                             | $t_{\text{Pcyc}} \times 2 > 200 \text{ ns}$     |
|                 |                   | 200                                | -   | -   |      | NMI digital filter enabled  | $t_{\text{NMICK}} \times 3 \leq 200 \text{ ns}$ |
|                 |                   | $t_{\text{NMICK}} \times 3.5^{*2}$ | -   | -   |      |                             | $t_{\text{NMICK}} \times 3 > 200 \text{ ns}$    |
| IRQ pulse width | $t_{\text{IRQW}}$ | 200                                | -   | -   | ns   | IRQ digital filter disabled | $t_{\text{Pcyc}} \times 2 \leq 200 \text{ ns}$  |
|                 |                   | $t_{\text{Pcyc}} \times 2^{*1}$    | -   | -   |      |                             | $t_{\text{Pcyc}} \times 2 > 200 \text{ ns}$     |
|                 |                   | 200                                | -   | -   |      | IRQ digital filter enabled  | $t_{\text{IRQCK}} \times 3 \leq 200 \text{ ns}$ |
|                 |                   | $t_{\text{IRQCK}} \times 3.5^{*3}$ | -   | -   |      |                             | $t_{\text{IRQCK}} \times 3 > 200 \text{ ns}$    |

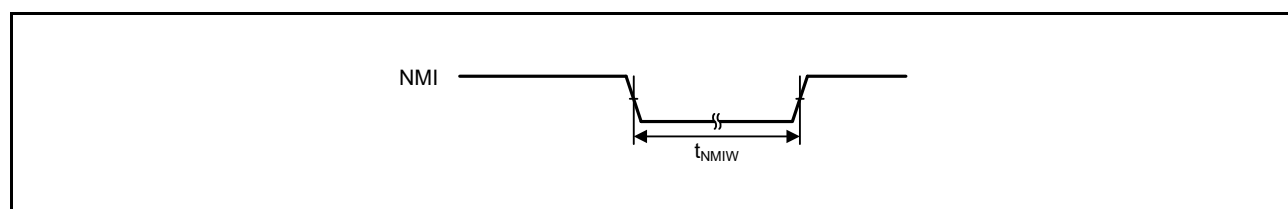
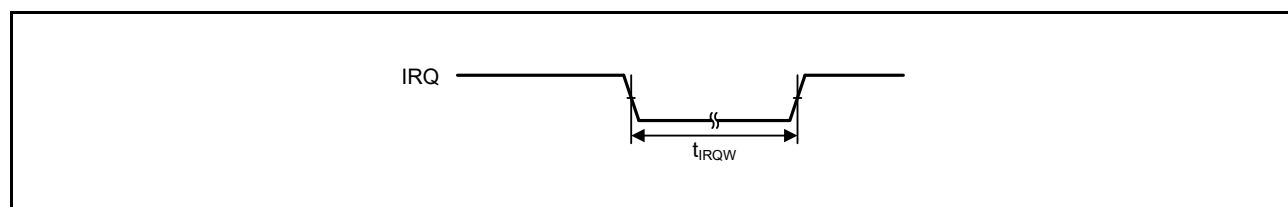
Note: 200 ns minimum in Software Standby mode.

Note: If the clock source is switched, add 4 clock cycles of the switched source.

Note 1.  $t_{\text{Pcyc}}$  indicates the cycle of PCLKB.

Note 2.  $t_{\text{NMICK}}$  indicates the cycle of the NMI digital filter sampling clock.

Note 3.  $t_{\text{IRQCK}}$  indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 15).

**Figure 2.34 NMI interrupt input timing****Figure 2.35 IRQ interrupt input timing**

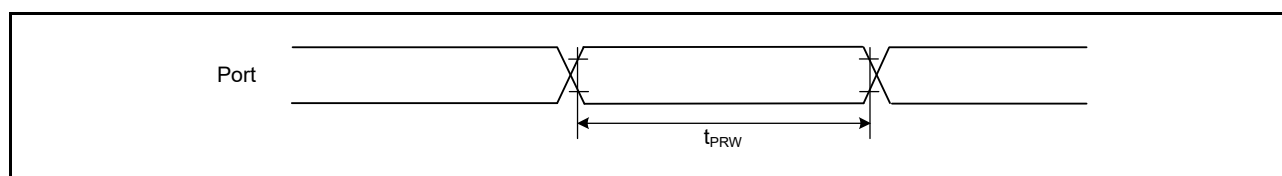
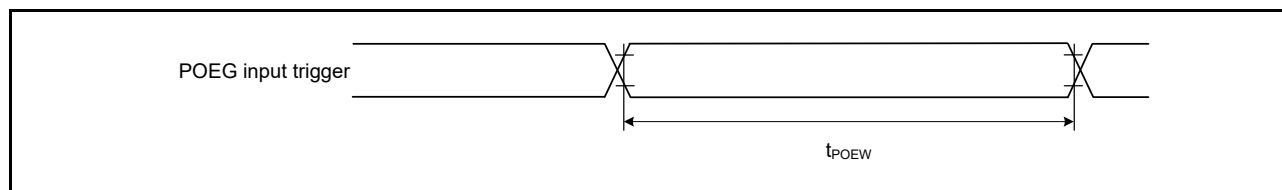
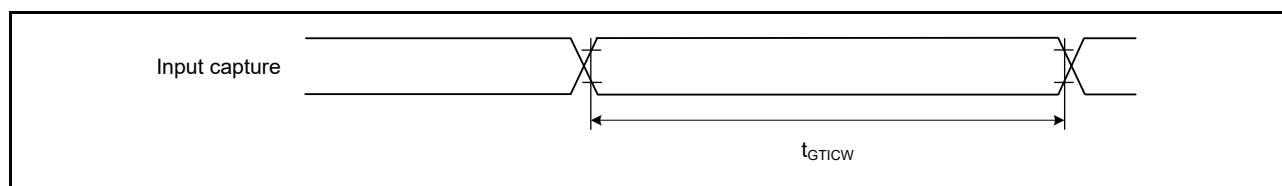
## 2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

**Table 2.32 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing**

| Parameter |                                                      |                                           | Symbol          | Min  | Max | Unit        | Test conditions |
|-----------|------------------------------------------------------|-------------------------------------------|-----------------|------|-----|-------------|-----------------|
| I/O ports | Input data pulse width                               |                                           | $t_{PRW}$       | 1.5  | -   | $t_{Pcyc}$  | Figure 2.36     |
|           | Input/output data cycle (P004)                       |                                           | $t_{POcyc}$     | 10   | -   | us          |                 |
| POEG      | POEG input trigger pulse width                       |                                           | $t_{POEW}$      | 3    | -   | $t_{Pcyc}$  | Figure 2.37     |
| GPT       | Input capture pulse width                            | Single edge                               | $t_{GTICW}$     | 1.5  | -   | $t_{PDcyc}$ | Figure 2.38     |
|           |                                                      | Dual edge                                 |                 | 2.5  | -   |             |                 |
| AGT       | AGTIO, AGTEE input cycle                             | $2.7\text{ V} \leq VCC \leq 3.6\text{ V}$ | $t_{ACYC}^{*1}$ | 250  | -   | ns          | Figure 2.39     |
|           |                                                      | $2.4\text{ V} \leq VCC < 2.7\text{ V}$    |                 | 500  | -   | ns          |                 |
|           |                                                      | $1.8\text{ V} \leq VCC < 2.4\text{ V}$    |                 | 1000 | -   | ns          |                 |
|           | AGTIO, AGTEE input high level width, low-level width | $2.7\text{ V} \leq VCC \leq 3.6\text{ V}$ | $t_{ACKWH}$     | 100  | -   | ns          |                 |
|           |                                                      | $2.4\text{ V} \leq VCC < 2.7\text{ V}$    | $t_{ACKWL}$     | 200  | -   | ns          |                 |
|           |                                                      | $1.8\text{ V} \leq VCC < 2.4\text{ V}$    |                 | 400  | -   | ns          |                 |
|           | AGTIO, AGTO, AGTOB output cycle                      | $2.7\text{ V} \leq VCC \leq 3.6\text{ V}$ | $t_{ACYC2}$     | 62.5 | -   | ns          | Figure 2.39     |
|           |                                                      | $2.4\text{ V} \leq VCC < 2.7\text{ V}$    |                 | 125  | -   | ns          |                 |
|           |                                                      | $1.8\text{ V} \leq VCC < 2.4\text{ V}$    |                 | 250  | -   | ns          |                 |
| ADC14     | 14-bit A/D converter trigger input pulse width       |                                           | $t_{TRGW}$      | 1.5  | -   | $t_{Pcyc}$  | Figure 2.40     |
| KINT      | KRn (n = 00 to 07) pulse width                       |                                           | $t_{KR}$        | 250  | -   | ns          | Figure 2.41     |

Note 1. Constraints on input cycle:  
 When not switching the source clock:  $t_{Pcyc} \times 2 < t_{ACYC}$  should be satisfied.  
 When switching the source clock:  $t_{Pcyc} \times 6 < t_{ACYC}$  should be satisfied.

Note:  $t_{Pcyc}$ : PCLKB cycle,  $t_{PDcyc}$ : PCLKD cycle

**Figure 2.36 I/O ports input timing****Figure 2.37 POEG input trigger timing****Figure 2.38 GPT input capture timing**

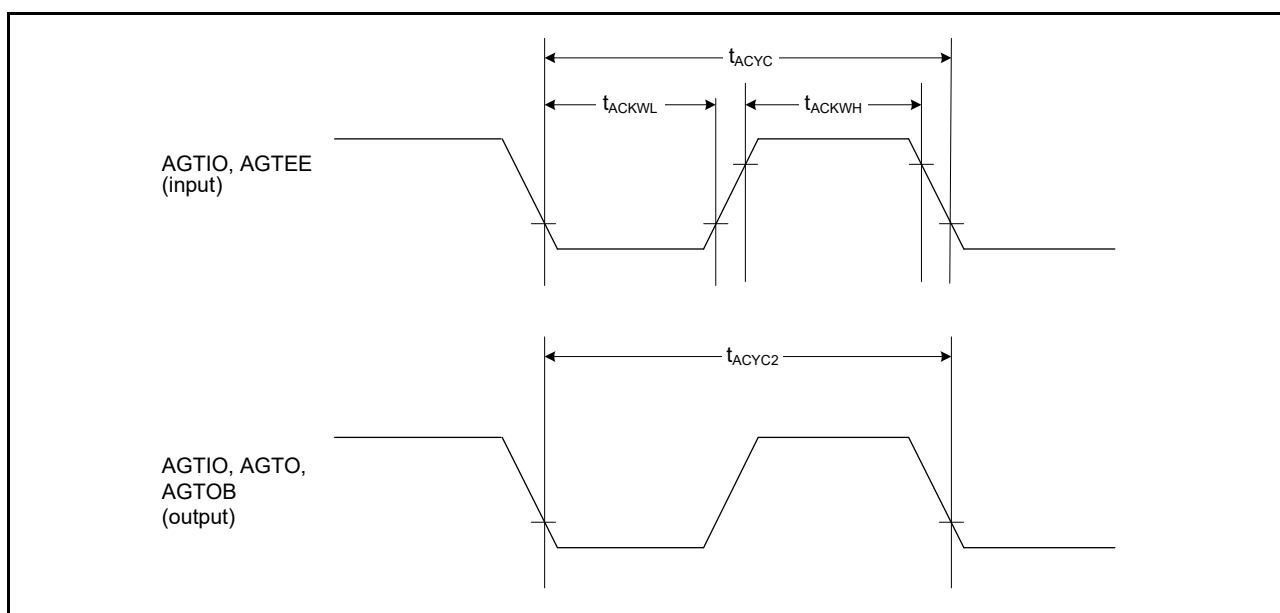


Figure 2.39 AGT I/O timing

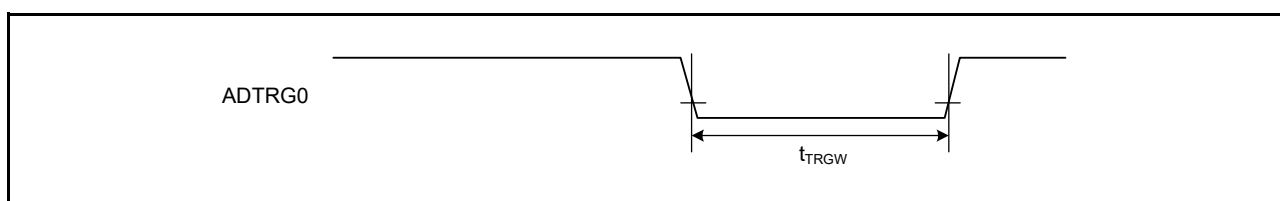


Figure 2.40 ADC14 trigger input timing

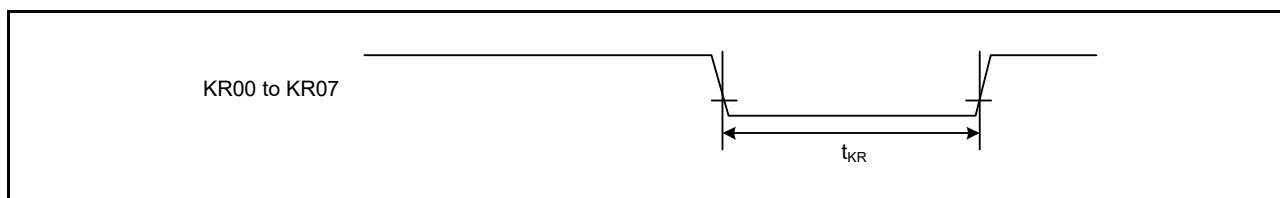


Figure 2.41 Key interrupt input timing

### 2.3.7 CAC Timing

Table 2.33 CAC timing

| Parameter |                          |                                    | Symbol       | Min                                            | Typ | Max | Unit | Test conditions |
|-----------|--------------------------|------------------------------------|--------------|------------------------------------------------|-----|-----|------|-----------------|
| CAC       | CACREF input pulse width | $t_{PBcyc}^{*1} \leq t_{cac}^{*2}$ | $t_{CACREF}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}^{*1}$ | -   | -   | ns   | -               |
|           |                          | $t_{PBcyc}^{*1} > t_{cac}^{*2}$    |              | $5 \times t_{cac} + 6.5 \times t_{PBcyc}^{*1}$ | -   | -   | ns   |                 |

Note 1.  $t_{PBcyc}$ : PCLKB cycle.

Note 2.  $t_{cac}$ : CAC count clock source cycle.

## 2.3.8 SCI Timing

Table 2.34 SCI timing (1)

| Parameter |                                  |                   | Symbol         | Min | Max | Unit*1     | Test conditions |
|-----------|----------------------------------|-------------------|----------------|-----|-----|------------|-----------------|
| SCI       | Input clock cycle                | Asynchronous      | $t_{Scyc}$     | 4   | -   | $t_{Pcyc}$ | Figure 2.42     |
|           |                                  | Clock synchronous |                | 6   | -   |            |                 |
|           | Input clock pulse width          |                   | $t_{SCKW}$     | 0.4 | 0.6 | $t_{Scyc}$ |                 |
|           | Input clock rise time            |                   | $t_{SCKr}$     | -   | 20  | ns         |                 |
|           | Input clock fall time            |                   | $t_{SCKf}$     | -   | 20  | ns         |                 |
|           | Output clock cycle               | Asynchronous      | $t_{Scyc}$     | 6   | -   | $t_{Pcyc}$ |                 |
|           |                                  | Clock synchronous |                | 4   | -   |            |                 |
|           | Output clock pulse width         |                   | $t_{SCKW}$     | 0.4 | 0.6 | $t_{Scyc}$ |                 |
|           | Output clock rise time           | 1.8 V or above    | $t_{SCKr}$     | -   | 20  | ns         |                 |
|           | Output clock fall time           | 1.8 V or above    | $t_{SCKf}$     | -   | 20  | ns         |                 |
|           | Transmit data delay (master)     | Clock synchronous | $t_{TXD}$      | -   | 40  | ns         | Figure 2.43     |
|           | Transmit data delay (slave)      | Clock synchronous | 2.7 V or above | -   | 55  | ns         |                 |
|           |                                  |                   | 2.4 V or above | -   | 60  |            |                 |
|           |                                  |                   | 1.8 V or above | -   | 100 |            |                 |
|           | Receive data setup time (master) | Clock synchronous | 2.7 V or above | 45  | -   | ns         |                 |
|           |                                  |                   | 2.4 V or above | 55  | -   |            |                 |
|           |                                  |                   | 1.8 V or above | 90  | -   |            |                 |
|           | Receive data setup time (slave)  | Clock synchronous | 2.7 V or above | 40  | -   | ns         |                 |
|           |                                  |                   | 1.8 V or above | 45  | -   |            |                 |
|           | Receive data hold time (master)  | Clock synchronous | $t_{RXH}$      | 5   | -   | ns         |                 |
|           | Receive data hold time (slave)   | Clock synchronous | $t_{RXH}$      | 40  | -   | ns         |                 |

Note 1.  $t_{Pcyc}$ : PCLKA cycle.

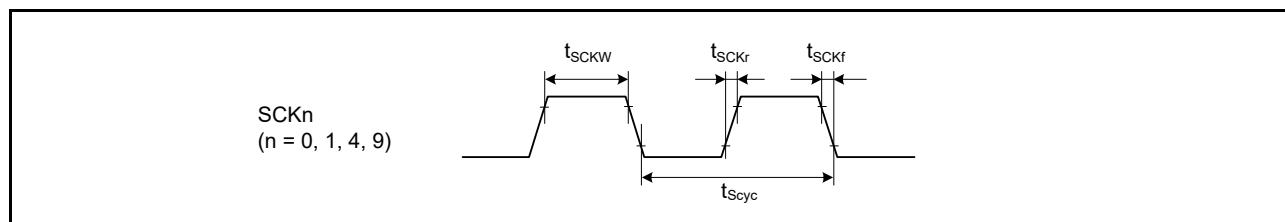


Figure 2.42 SCK clock input timing

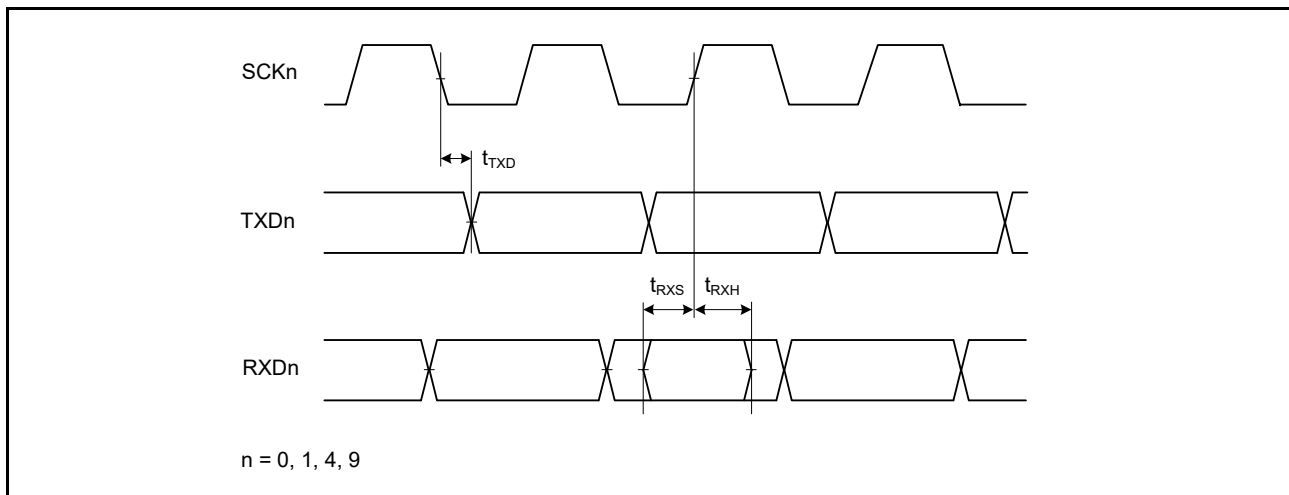


Figure 2.43 SCI input/output timing in clock synchronous mode

Table 2.35 SCI timing (2)

| Parameter                 |                                 |                |                | Symbol                       | Min                 | Max                                        | Unit        | Test conditions                |             |
|---------------------------|---------------------------------|----------------|----------------|------------------------------|---------------------|--------------------------------------------|-------------|--------------------------------|-------------|
| Simple SPI                | SCK clock cycle output (master) |                |                | $t_{SPcyc}$                  | 4                   | 65536                                      | $t_{Pcyc}$  | Figure 2.44                    |             |
|                           | SCK clock cycle input (slave)   |                |                |                              | 6                   | 65536                                      |             |                                |             |
|                           | SCK clock high pulse width      |                |                | $t_{SPCKWH}$                 | 0.4                 | 0.6                                        | $t_{SPcyc}$ |                                |             |
|                           | SCK clock low pulse width       |                |                | $t_{SPCKWL}$                 | 0.4                 | 0.6                                        | $t_{SPcyc}$ |                                |             |
|                           | SCK clock rise and fall time    |                | 1.8 V or above | $t_{SPCKr}$ ,<br>$t_{SPCKf}$ | -                   | 20                                         | ns          |                                |             |
|                           | Data input setup time           | Master         | 2.7 V or above | $t_{SU}$                     | 45                  | -                                          | ns          | Figure 2.45 to<br>Figure 2.48  |             |
|                           |                                 |                | 2.4 V or above |                              | 55                  | -                                          |             |                                |             |
|                           |                                 |                | 1.8 V or above |                              | 80                  | -                                          |             |                                |             |
|                           |                                 | Slave          | 2.7 V or above |                              | 40                  | -                                          |             |                                |             |
|                           |                                 |                | 1.8 V or above |                              | 45                  | -                                          |             |                                |             |
|                           | Data input hold time            | Master         |                | $t_H$                        | 33.3                | -                                          | ns          |                                |             |
|                           |                                 | Slave          |                |                              | 40                  | -                                          |             |                                |             |
|                           | SS input setup time             |                |                |                              | $t_{LEAD}$          | 1                                          | -           |                                | $t_{SPcyc}$ |
|                           | SS input hold time              |                |                |                              | $t_{LAG}$           | 1                                          | -           |                                | $t_{SPcyc}$ |
| Data output delay         | Master                          | 1.8 V or above | $t_{OD}$       | -                            | 40                  | ns                                         |             |                                |             |
|                           | Slave                           | 2.4 V or above |                | -                            | 65                  |                                            |             |                                |             |
|                           |                                 | 1.8 V or above |                | -                            | 100                 |                                            |             |                                |             |
| Data output hold time     | Master                          | 2.7 V or above | $t_{OH}$       | -10                          | -                   | ns                                         |             |                                |             |
|                           |                                 | 2.4 V or above |                | -20                          | -                   |                                            |             |                                |             |
|                           |                                 | 1.8 V or above |                | -30                          | -                   |                                            |             |                                |             |
|                           | Slave                           |                |                | -10                          | -                   |                                            |             |                                |             |
|                           | Data rise and fall time         | Master         |                | 1.8 V or above               | $t_{Dr}$ , $t_{Df}$ |                                            | -           | 20                             | ns          |
| Slave                     |                                 | 1.8 V or above | -              | 20                           |                     |                                            |             |                                |             |
| Slave access time         |                                 |                |                | $t_{SA}$                     | -                   | 10 (PCLKA > 32 MHz),<br>6 (PCLKA ≤ 32 MHz) | $t_{Pcyc}$  | Figure 2.47 and<br>Figure 2.48 |             |
| Slave output release time |                                 |                |                | $t_{REL}$                    | -                   | 10 (PCLKA > 32 MHz),<br>6 (PCLKA ≤ 32 MHz) | $t_{Pcyc}$  |                                |             |

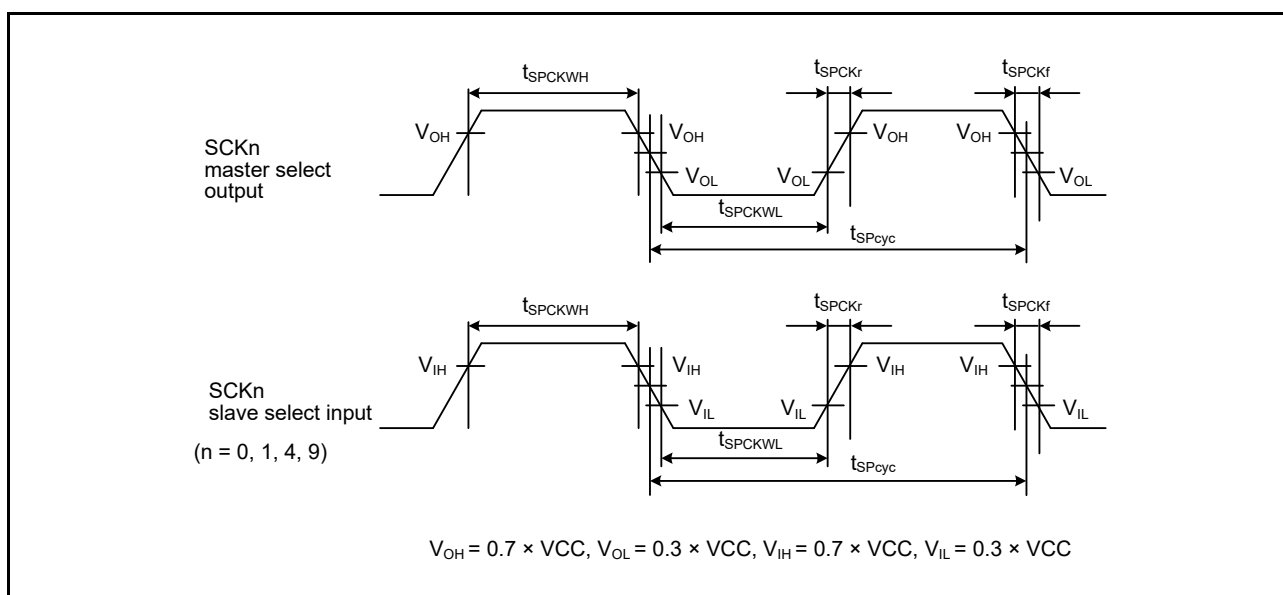


Figure 2.44 SCI simple SPI mode clock timing

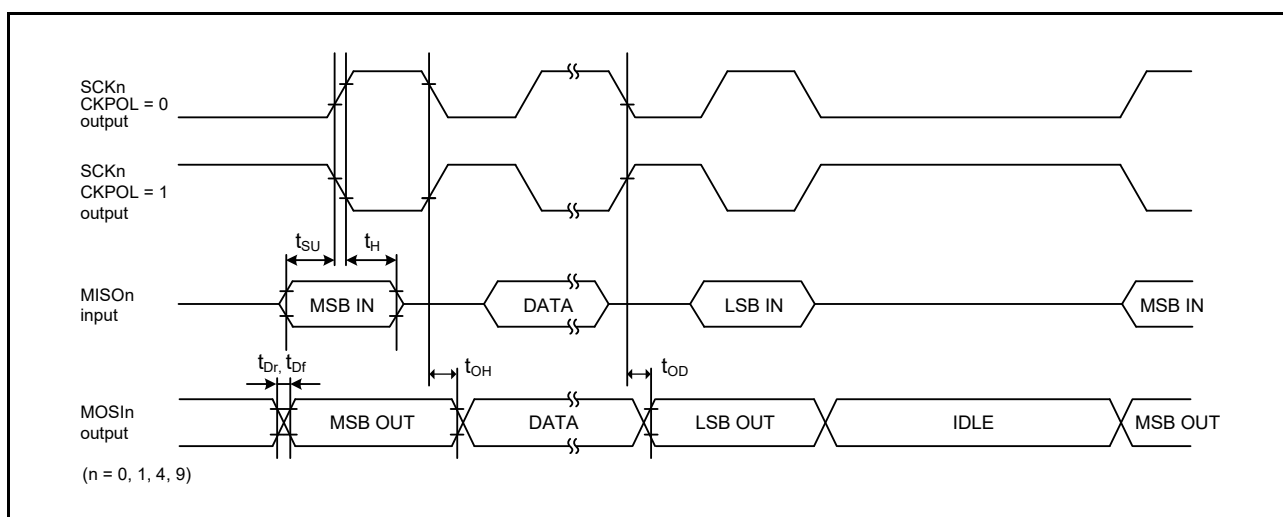


Figure 2.45 SCI simple SPI mode timing (master, CKPH = 1)

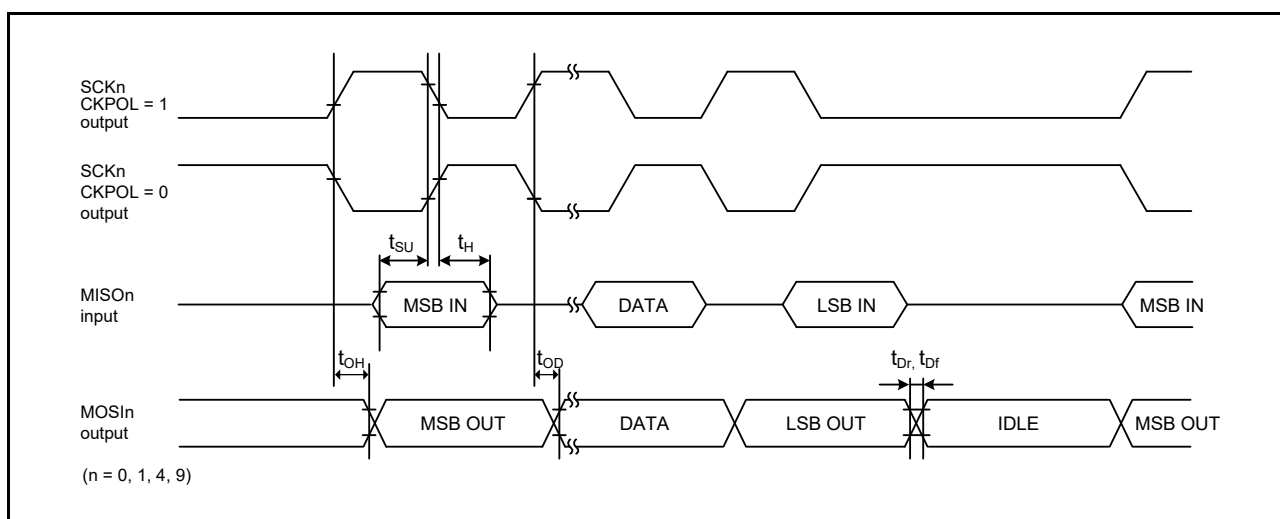


Figure 2.46 SCI simple SPI mode timing (master, CKPH = 0)

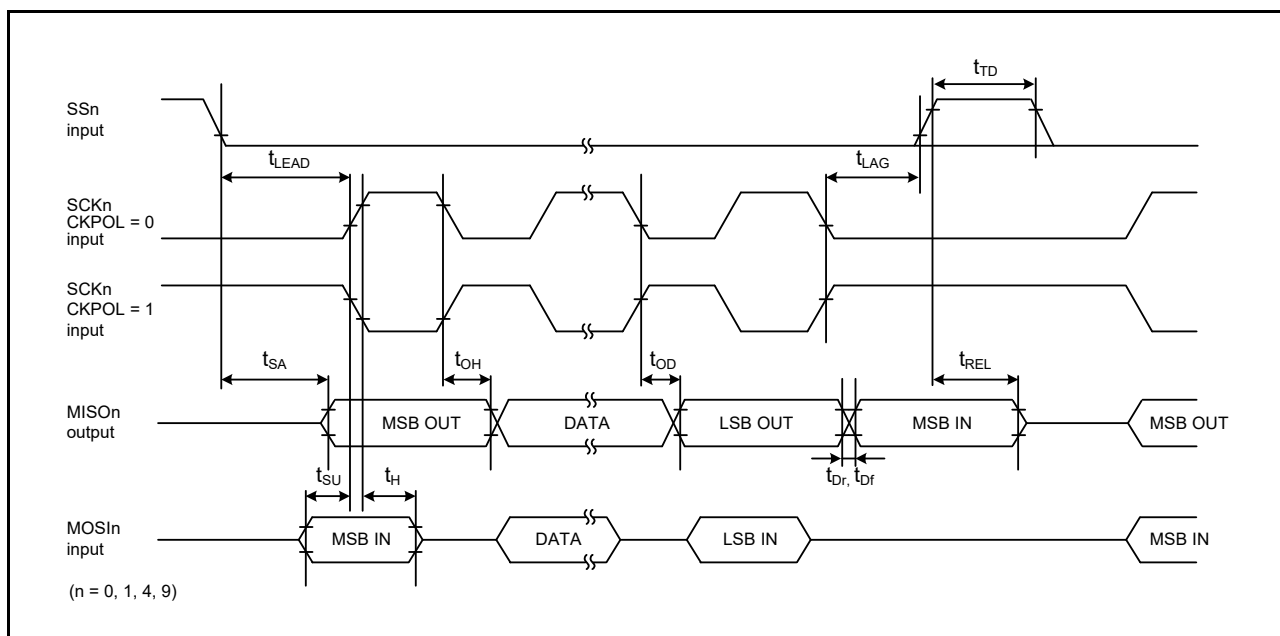
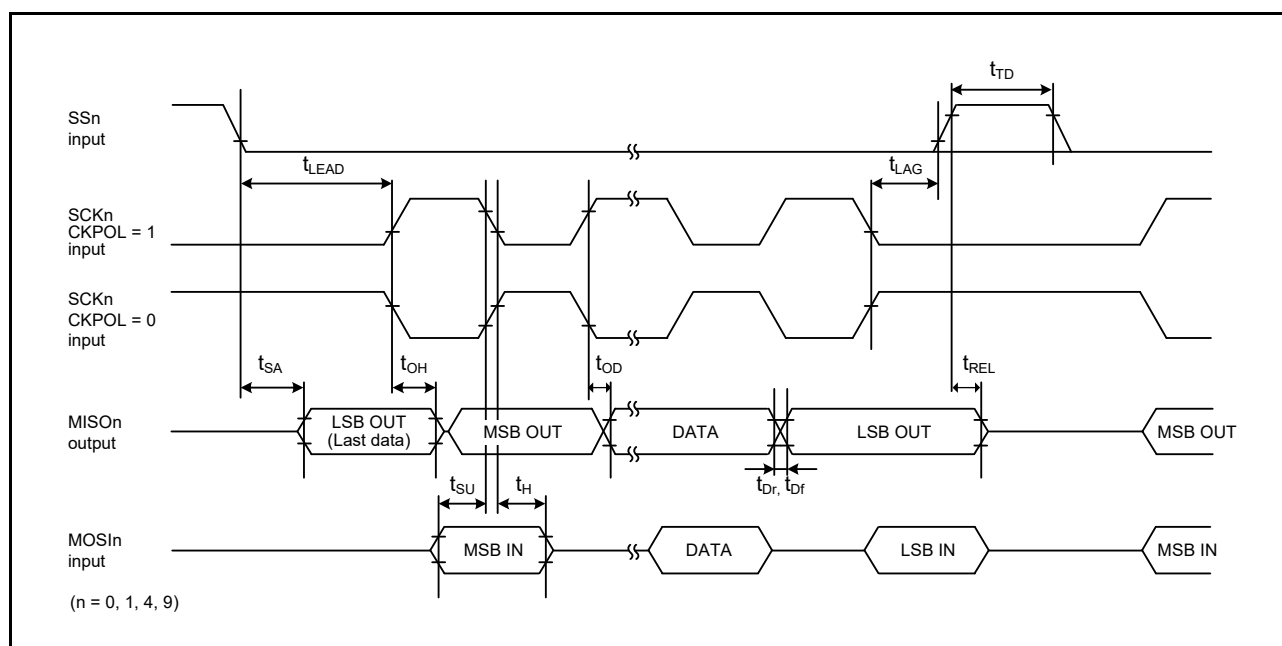


Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 1)



**Figure 2.48** SCI simple SPI mode timing (slave, CKPH = 0)

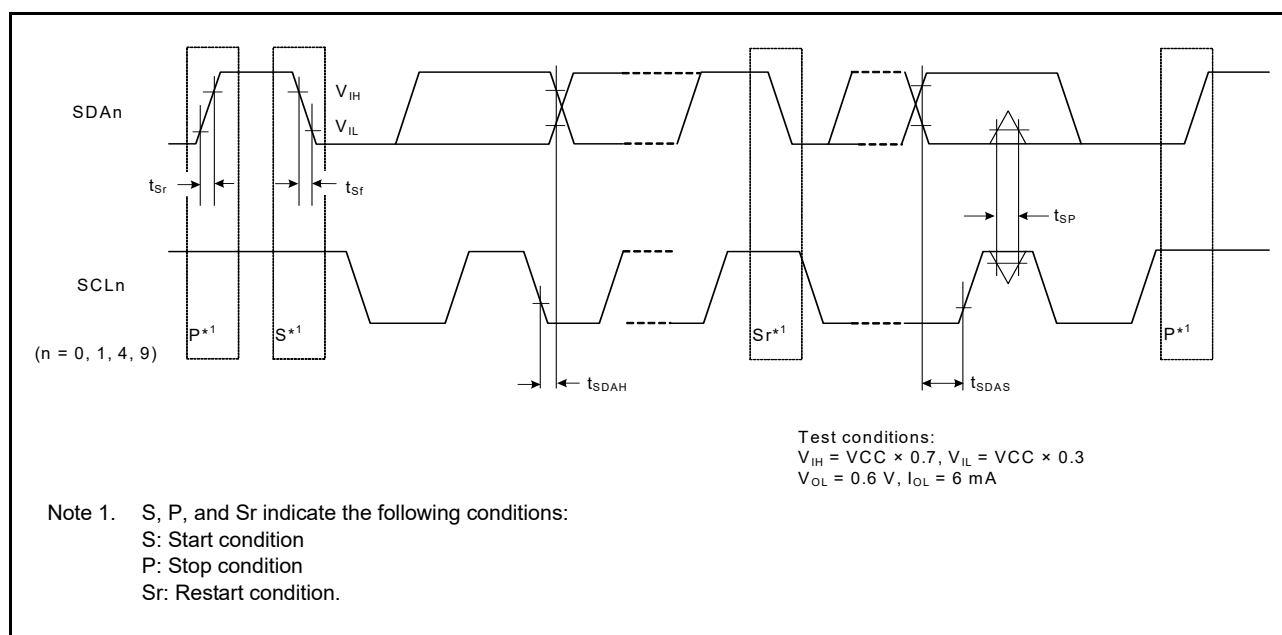
**Table 2.36** SCI timing (3)

Conditions: VCC = 2.7 to 3.6 V

| Parameter                     | Symbol                             | Min        | Max | Unit                       | Test conditions |
|-------------------------------|------------------------------------|------------|-----|----------------------------|-----------------|
| Simple IIC<br>(Standard mode) | SDA input rise time                | $t_{Sr}$   | -   | 1000                       | ns              |
|                               | SDA input fall time                | $t_{Sf}$   | -   | 300                        | ns              |
|                               | SDA input spike pulse removal time | $t_{SP}$   | 0   | $4 \times t_{IICcyc}^{*1}$ | ns              |
|                               | Data input setup time              | $t_{SDAS}$ | 250 | -                          | ns              |
|                               | Data input hold time               | $t_{SDAH}$ | 0   | -                          | ns              |
|                               | SCL, SDA capacitive load           | $C_b^{*2}$ | -   | 400                        | pF              |
| Simple IIC<br>(Fast mode)     | SDA input rise time                | $t_{Sr}$   | -   | 300                        | ns              |
|                               | SDA input fall time                | $t_{Sf}$   | -   | 300                        | ns              |
|                               | SDA input spike pulse removal time | $t_{SP}$   | 0   | $4 \times t_{IICcyc}^{*1}$ | ns              |
|                               | Data input setup time              | $t_{SDAS}$ | 100 | -                          | ns              |
|                               | Data input hold time               | $t_{SDAH}$ | 0   | -                          | ns              |
|                               | SCL, SDA capacitive load           | $C_b^{*2}$ | -   | 400                        | pF              |

Note 1.  $t_{IICcyc}$ : Clock cycle selected by the SMR.CKS[1:0] bits.

Note 2.  $C_b$  indicates the total capacity of the bus line.



**Figure 2.49** SCI simple IIC mode timing

## 2.3.9 SPI Timing

**Table 2.37 SPI timing (1 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

| Parameter                        |                                |                                     |                  | Symbol                          | Min                                           | Max     | Unit*1                     | Test conditions            |
|----------------------------------|--------------------------------|-------------------------------------|------------------|---------------------------------|-----------------------------------------------|---------|----------------------------|----------------------------|
| SPI                              | RSPCK clock cycle              | Master                              |                  | $t_{SPcyc}$                     | 2*4                                           | 4096    | $t_{Pcyc}$                 | Figure 2.50                |
|                                  |                                | Slave                               |                  |                                 | 6                                             | 4096    |                            |                            |
|                                  | RSPCK clock high pulse width   | Master                              |                  | $t_{SPCKWH}$                    | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | -       | ns                         |                            |
|                                  |                                | Slave                               |                  |                                 | $3 \times t_{Pcyc}$                           | -       |                            |                            |
|                                  | RSPCK clock low pulse width    | Master                              |                  | $t_{SPCKWL}$                    | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | -       | ns                         |                            |
|                                  |                                | Slave                               |                  |                                 | $3 \times t_{Pcyc}$                           | -       |                            |                            |
|                                  | RSPCK clock rise and fall time | Output                              | 2.7 V or above   | $t_{SPCKr}, t_{SPCKf}$          | -                                             | 10      | ns                         |                            |
|                                  |                                |                                     | 2.4 V or above   |                                 | -                                             | 15      |                            |                            |
|                                  |                                |                                     | 1.8 V or above   |                                 | -                                             | 20      |                            |                            |
|                                  |                                | Input                               |                  |                                 | -                                             | 1       | $\mu s$                    |                            |
|                                  | Data input setup time          | Master                              |                  | $t_{SU}$                        | 10                                            | -       | ns                         | Figure 2.51 to Figure 2.56 |
|                                  |                                | Slave                               | 2.4 V or above   |                                 | 10                                            | -       |                            |                            |
|                                  |                                |                                     | 1.8 V or above   |                                 | 15                                            | -       |                            |                            |
|                                  | Data input hold time           | Master (RSPCK is PCLKA/2)           |                  | $t_{HF}$                        | 0                                             | -       | ns                         |                            |
|                                  |                                | Master (RSPCK is other than above.) |                  | $t_H$                           | $t_{Pcyc}$                                    | -       |                            |                            |
|                                  |                                | Slave                               |                  | $t_H$                           | 20                                            | -       |                            |                            |
|                                  | SSL setup time                 | Master                              | 1.8 V or above   | $t_{LEAD}$                      | $-30 + N \times t_{SpCyc}^{*2}$               | -       | ns                         |                            |
| Slave                            |                                | $6 \times t_{Pcyc}$                 | -                |                                 |                                               |         |                            |                            |
| SSL hold time                    | Master                         |                                     | $t_{LAG}$        | $-30 + N \times t_{SpCyc}^{*3}$ | -                                             | ns      |                            |                            |
|                                  | Slave                          |                                     |                  | $6 \times t_{Pcyc}$             | -                                             |         |                            |                            |
| Data output delay                | Master                         | 2.7 V or above                      | $t_{OD}$         | -                               | 14                                            | ns      | Figure 2.51 to Figure 2.56 |                            |
|                                  |                                | 2.4 V or above                      |                  | -                               | 20                                            |         |                            |                            |
|                                  |                                | 1.8 V or above                      |                  | -                               | 25                                            |         |                            |                            |
|                                  | Slave                          | 2.7 V or above                      |                  | -                               | 50                                            |         |                            |                            |
|                                  |                                | 2.4 V or above                      |                  | -                               | 60                                            |         |                            |                            |
|                                  |                                | 1.8 V or above                      |                  | -                               | 85                                            |         |                            |                            |
| Data output hold time            | Master                         |                                     | $t_{OH}$         | 0                               | -                                             | ns      |                            |                            |
|                                  | Slave                          |                                     |                  | 0                               | -                                             |         |                            |                            |
| Successive transmission delay    | Master                         |                                     | $t_{TD}$         | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$      | ns      |                            |                            |
|                                  | Slave                          |                                     |                  | $6 \times t_{Pcyc}$             | -                                             |         |                            |                            |
| MOSI and MISO rise and fall time | Output                         | 2.7 V or above                      | $t_{Dr}, t_{Df}$ | -                               | 10                                            | ns      |                            |                            |
|                                  |                                | 2.4 V or above                      |                  | -                               | 15                                            |         |                            |                            |
|                                  |                                | 1.8 V or above                      |                  | -                               | 20                                            |         |                            |                            |
|                                  | Input                          |                                     |                  | -                               | 1                                             | $\mu s$ |                            |                            |

**Table 2.37 SPI timing (2 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

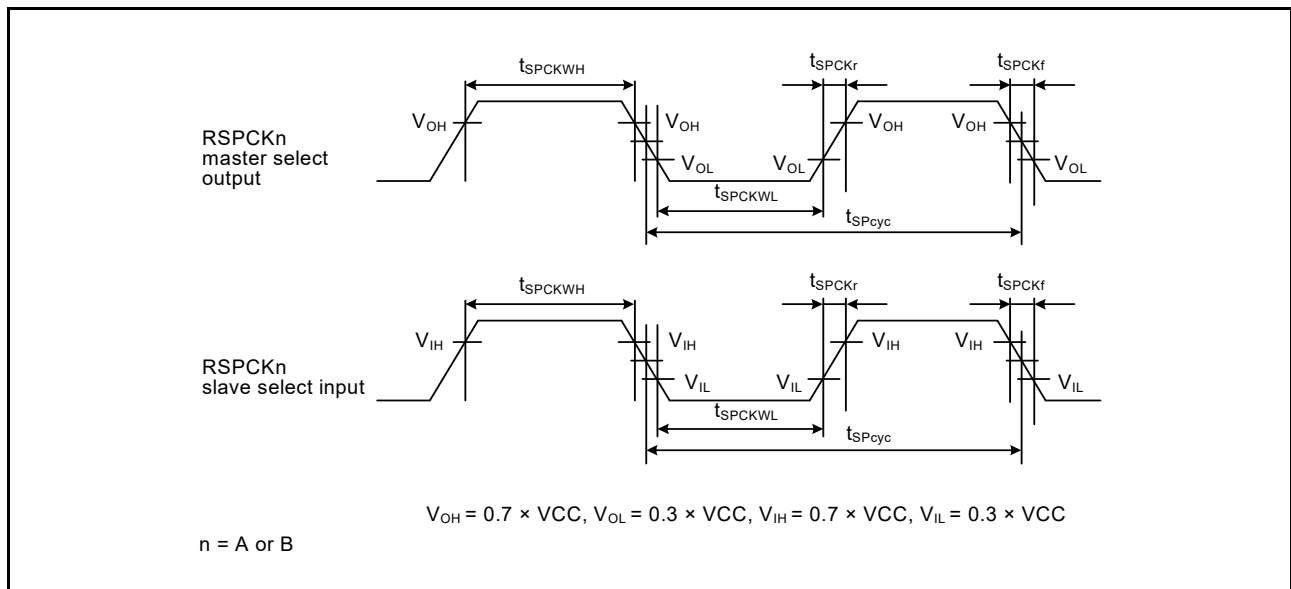
| Parameter |                           |                                  |                | Symbol                     | Min                       | Max | Unit*1                         | Test conditions               |
|-----------|---------------------------|----------------------------------|----------------|----------------------------|---------------------------|-----|--------------------------------|-------------------------------|
| SPI       | SSL rise and fall time    | Output                           | 2.7 V or above | $t_{SSLr}$ ,<br>$t_{SSLf}$ | -                         | 10  | ns                             | Figure 2.51 to<br>Figure 2.56 |
|           |                           |                                  | 2.4 V or above |                            | -                         | 15  |                                |                               |
|           |                           |                                  | 1.8 V or above |                            | -                         | 20  |                                |                               |
|           |                           | Input                            | -              |                            | 1                         | μs  |                                |                               |
|           | Slave access time         | 2.4 V or above<br>1.8 V or above | $t_{SA}$       | -                          | $2 \times t_{Pcyc} + 100$ | ns  | Figure 2.55 and<br>Figure 2.56 |                               |
|           |                           |                                  |                | -                          | $2 \times t_{Pcyc} + 140$ |     |                                |                               |
|           | Slave output release time | 2.4 V or above<br>1.8 V or above | $t_{REL}$      | -                          | $2 \times t_{Pcyc} + 100$ | ns  |                                |                               |
|           |                           |                                  |                | -                          | $2 \times t_{Pcyc} + 140$ |     |                                |                               |

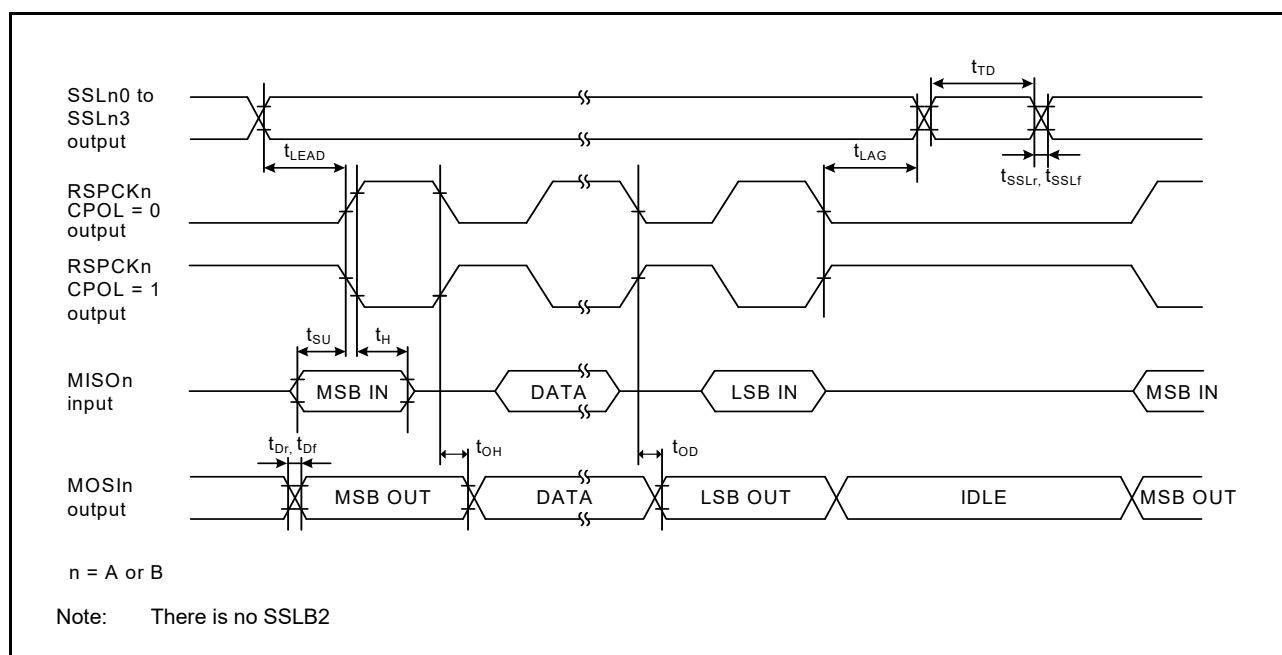
Note 1.  $t_{Pcyc}$ : PCLKA cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

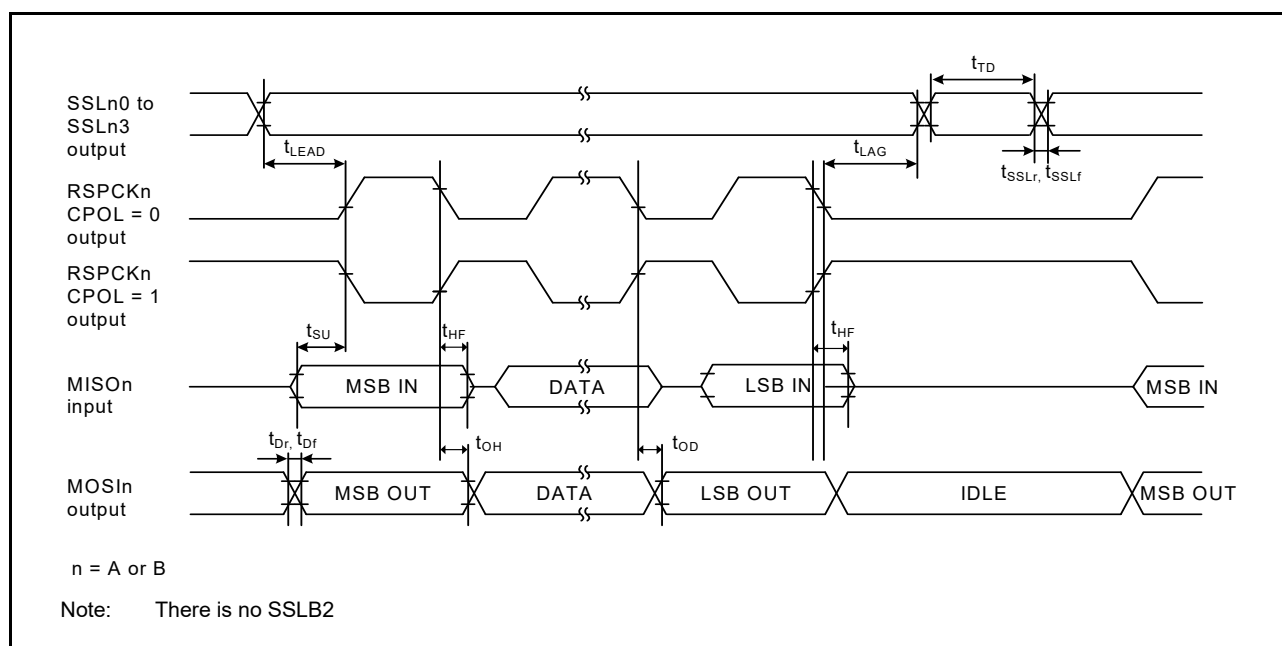
Note 3. N is set as an integer from 1 to 8 by the SSLND register.

Note 4. The upper limit of RSPCK is 16 MHz.

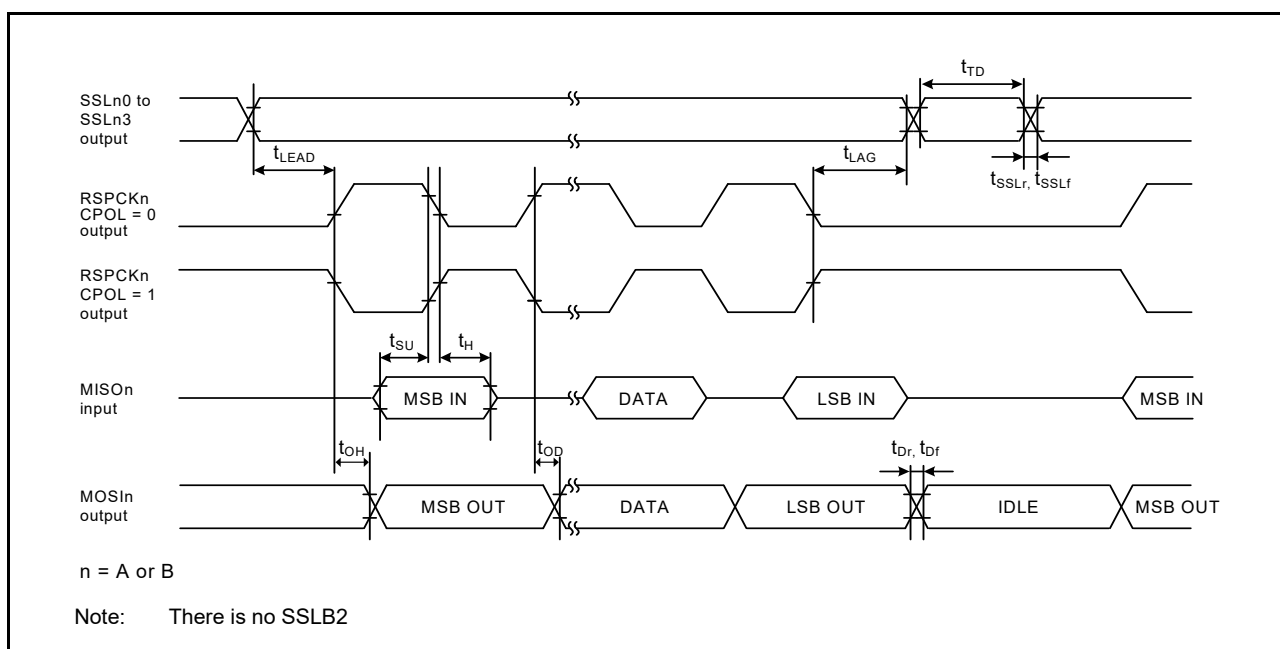
**Figure 2.50 SPI clock timing**



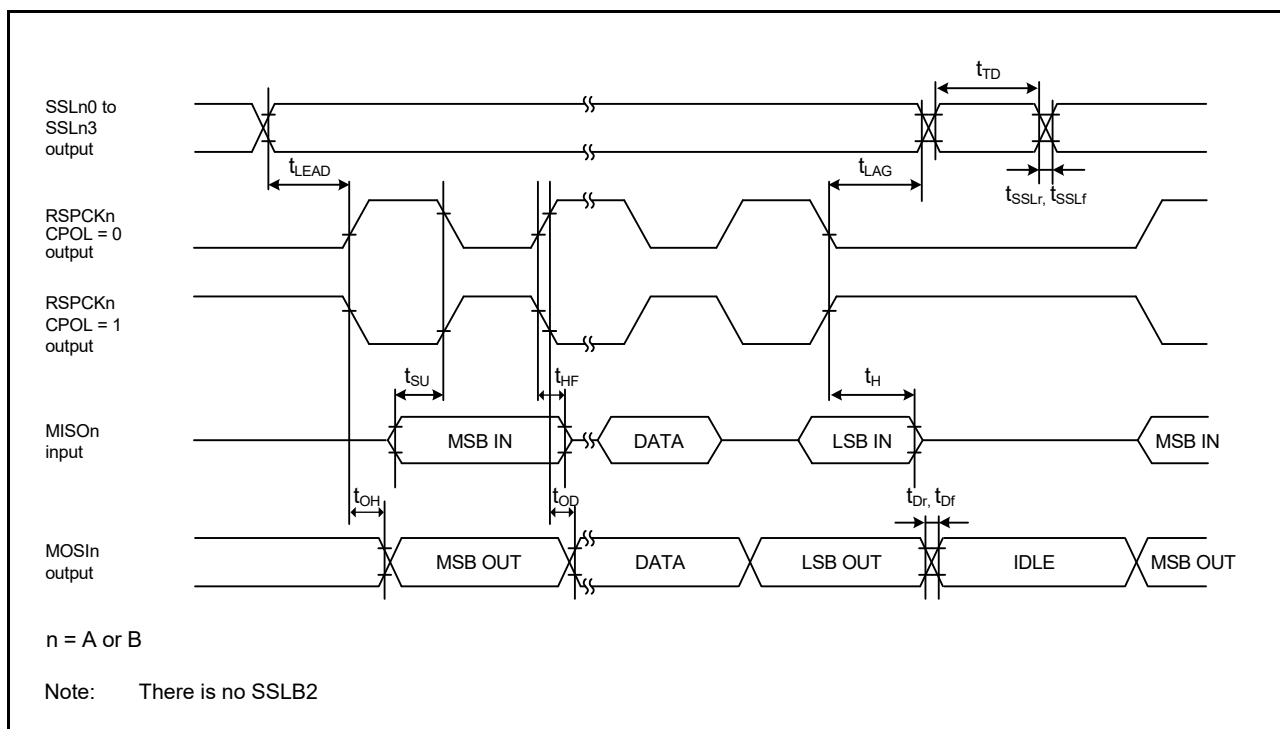
**Figure 2.51** SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to any value other than 1/2)



**Figure 2.52** SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)



**Figure 2.53** SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to any value other than 1/2)



**Figure 2.54** SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to 1/2)

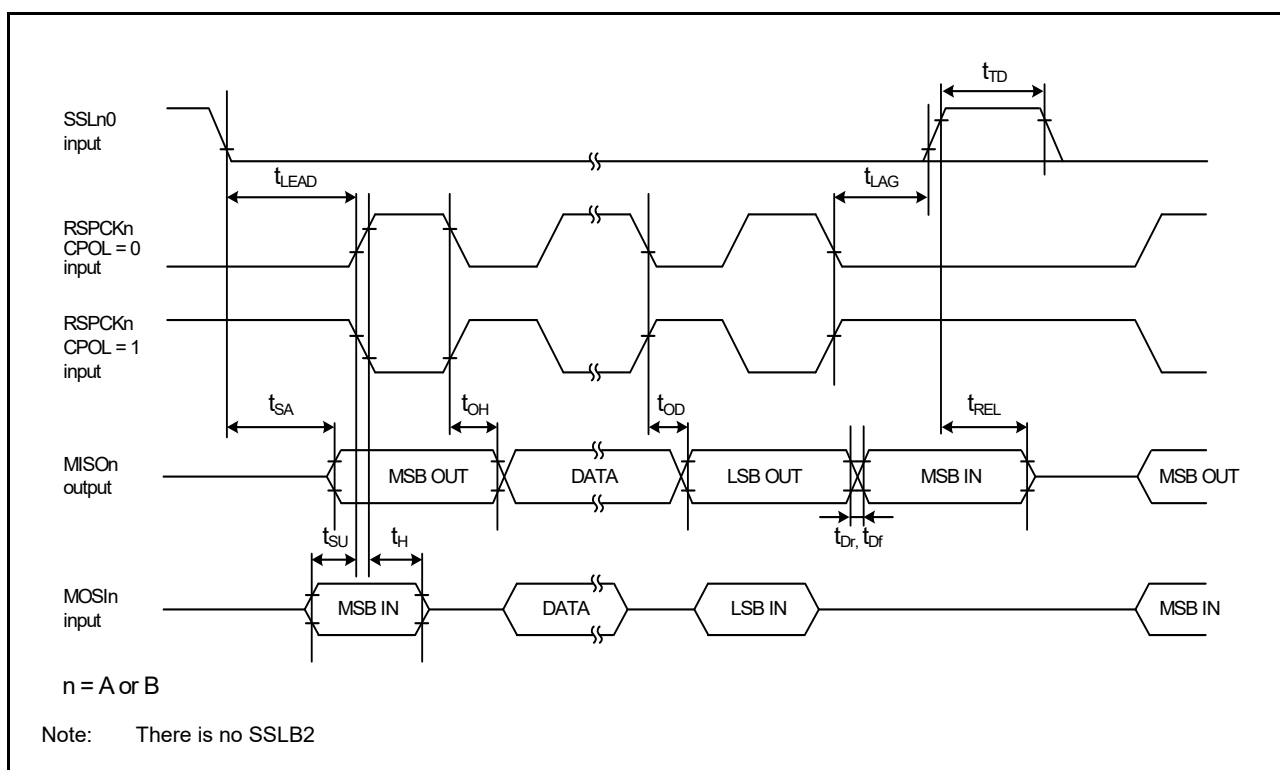


Figure 2.55 SPI timing (slave, CPHA = 0)

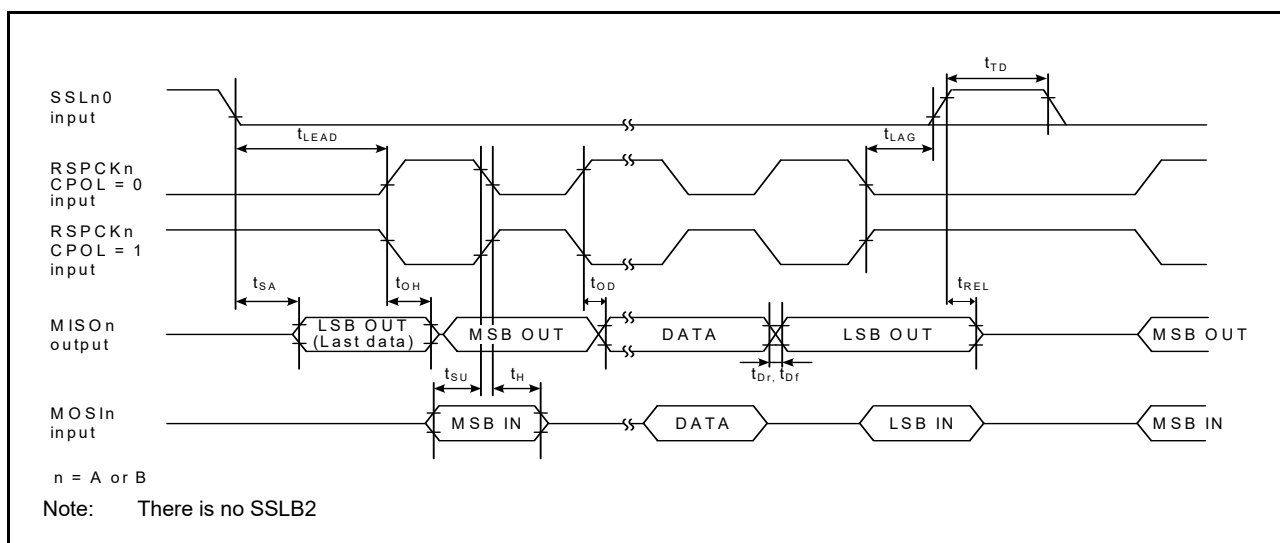


Figure 2.56 SPI timing (slave, CPHA = 1)

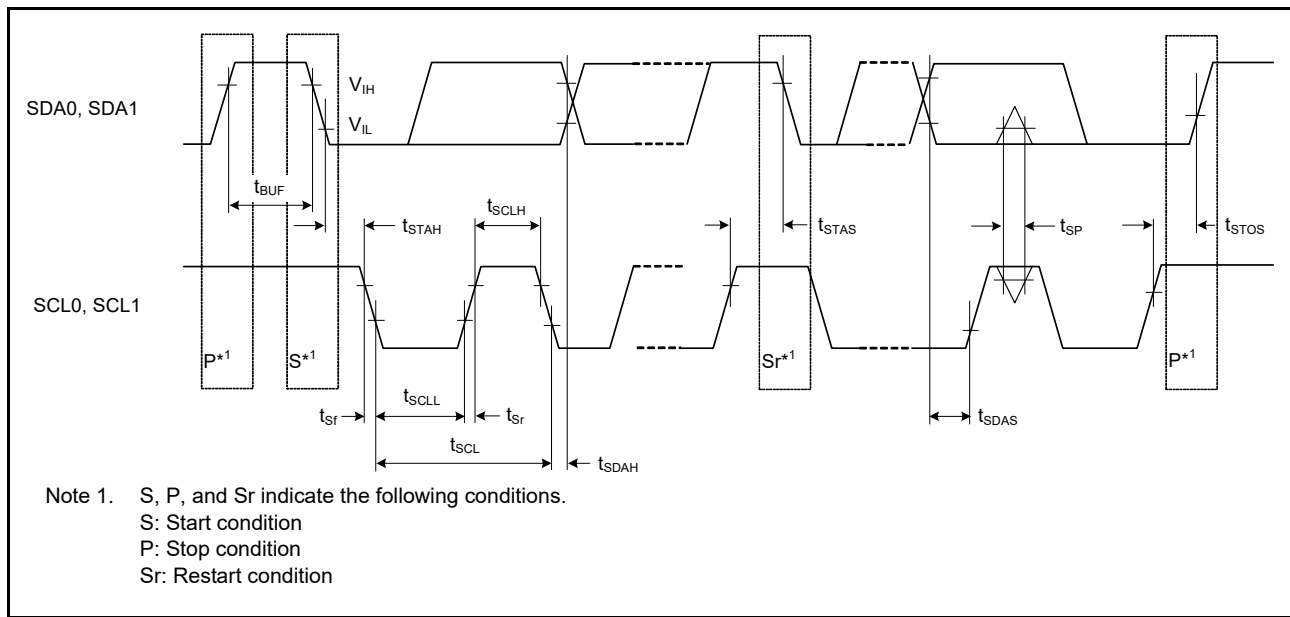
## 2.3.10 IIC Timing

**Table 2.38 IIC timing**  
Conditions: VCC = 2.7 to 3.6 V

| Parameter                        |                                                                       | Symbol     | Min*1                                               | Max                       | Unit | Test conditions                                                 |
|----------------------------------|-----------------------------------------------------------------------|------------|-----------------------------------------------------|---------------------------|------|-----------------------------------------------------------------|
| IIC<br>(standard mode,<br>SMBus) | SCL input cycle time                                                  | $t_{SCL}$  | $6 (12) \times t_{IICcyc} + 1300$                   | -                         | ns   | Figure 2.57                                                     |
|                                  | SCL input high pulse width                                            | $t_{SCLH}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SCL input low pulse width                                             | $t_{SCLL}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SCL, SDA input rise time                                              | $t_{Sr}$   | -                                                   | 1000                      | ns   |                                                                 |
|                                  | SCL, SDA input fall time                                              | $t_{Sf}$   | -                                                   | 300                       | ns   |                                                                 |
|                                  | SCL, SDA input spike pulse removal time                               | $t_{SP}$   | 0                                                   | $1 (4) \times t_{IICcyc}$ | ns   |                                                                 |
|                                  | SDA input bus free time<br>(When wakeup function is disabled)         | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SDA input bus free time<br>(When wakeup function is enabled)          | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | -                         | ns   |                                                                 |
|                                  | START condition input hold time<br>(When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc} + 300$                                  | -                         | ns   |                                                                 |
|                                  | START condition input hold time<br>(When wakeup function is enabled)  | $t_{STAH}$ | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$          | -                         | ns   |                                                                 |
|                                  | Repeated START condition input setup time                             | $t_{STAS}$ | 1000                                                | -                         | ns   |                                                                 |
|                                  | STOP condition input setup time                                       | $t_{STOS}$ | 1000                                                | -                         | ns   |                                                                 |
|                                  | Data input setup time                                                 | $t_{SDAS}$ | $t_{IICcyc} + 50$                                   | -                         | ns   |                                                                 |
|                                  | Data input hold time                                                  | $t_{SDAH}$ | 0                                                   | -                         | ns   |                                                                 |
|                                  | SCL, SDA capacitive load                                              | $C_b$      | -                                                   | 400                       | pF   |                                                                 |
| IIC<br>(Fast mode)               | SCL input cycle time                                                  | $t_{SCL}$  | $6 (12) \times t_{IICcyc} + 600$                    | -                         | ns   | Figure 2.57<br>For all ports, use PmnPFS.DS CR of middle drive. |
|                                  | SCL input high pulse width                                            | $t_{SCLH}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SCL input low pulse width                                             | $t_{SCLL}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SCL, SDA input rise time                                              | $t_{Sr}$   | -                                                   | 300                       | ns   |                                                                 |
|                                  | SCL, SDA input fall time                                              | $t_{Sf}$   | -                                                   | 300                       | ns   |                                                                 |
|                                  | SCL, SDA input spike pulse removal time                               | $t_{SP}$   | 0                                                   | $1 (4) \times t_{IICcyc}$ | ns   |                                                                 |
|                                  | SDA input bus free time<br>(When wakeup function is disabled)         | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                                                                 |
|                                  | SDA input bus free time<br>(When wakeup function is enabled)          | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | -                         | ns   |                                                                 |
|                                  | START condition input hold time<br>(When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc} + 300$                                  | -                         | ns   |                                                                 |
|                                  | START condition input hold time<br>(When wakeup function is enabled)  | $t_{STAH}$ | $1(5) \times t_{IICcyc} + t_{Pcyc} + 300$           | -                         | ns   |                                                                 |
|                                  | Repeated START condition input setup time                             | $t_{STAS}$ | 300                                                 | -                         | ns   |                                                                 |
|                                  | STOP condition input setup time                                       | $t_{STOS}$ | 300                                                 | -                         | ns   |                                                                 |
|                                  | Data input setup time                                                 | $t_{SDAS}$ | $t_{IICcyc} + 50$                                   | -                         | ns   |                                                                 |
|                                  | Data input hold time                                                  | $t_{SDAH}$ | 0                                                   | -                         | ns   |                                                                 |
|                                  | SCL, SDA capacitive load                                              | $C_b$      | -                                                   | 400                       | pF   |                                                                 |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IICφ) cycle,  $t_{Pcyc}$ : PCLKB cycle

Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Figure 2.57 I<sup>2</sup>C bus interface input/output timing

## 2.3.11 CLKOUT Timing

Table 2.39 CLKOUT timing

| Parameter   |                                |                      | Symbol              | Min  | Max | Unit*1 | Test conditions |
|-------------|--------------------------------|----------------------|---------------------|------|-----|--------|-----------------|
| CLKOUT      | CLKOUT pin output cycle*1      | VCC = 2.7 V or above | t <sub>Cyc</sub>    | 62.5 | -   | ns     | Figure 2.58     |
|             |                                | VCC = 1.8 V or above |                     | 125  | -   |        |                 |
|             | CLKOUT pin high pulse width*2  | VCC = 2.7 V or above | t <sub>CH</sub>     | 15   | -   | ns     |                 |
|             |                                | VCC = 1.8 V or above |                     | 30   | -   |        |                 |
|             | CLKOUT pin low pulse width*2   | VCC = 2.7 V or above | t <sub>CL</sub>     | 15   | -   | ns     |                 |
|             |                                | VCC = 1.8 V or above |                     | 30   | -   |        |                 |
|             | CLKOUT pin output rise time    | VCC = 2.7 V or above | t <sub>Cr</sub>     | -    | 12  | ns     |                 |
|             |                                | VCC = 1.8 V or above |                     | -    | 25  |        |                 |
|             | CLKOUT pin output fall time    | VCC = 2.7 V or above | t <sub>Cf</sub>     | -    | 12  | ns     |                 |
|             |                                | VCC = 1.8 V or above |                     | -    | 25  |        |                 |
| CLKOUT_RF*3 | CLKOUT_RF pin output cycle     |                      | t <sub>CRFcyc</sub> | 250  | -   | ns     | Figure 2.59     |
|             | CLKOUT_RF pin high pulse width |                      | t <sub>CRFH</sub>   | 100  | -   | ns     |                 |
|             | CLKOUT_RF pin low pulse width  |                      | t <sub>CRFL</sub>   | 100  | -   | ns     |                 |
|             | CLKOUT_RF pin output rise time |                      | t <sub>CRFr</sub>   | -    | 5   | ns     |                 |
|             | CLKOUT_RF pin output fall time |                      | t <sub>CRFf</sub>   | -    | 5   | ns     |                 |

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

Note 3. The voltage for VCC\_RF when CLKOUT\_RF pin is to be used is between 3.0 V and 3.6 V.

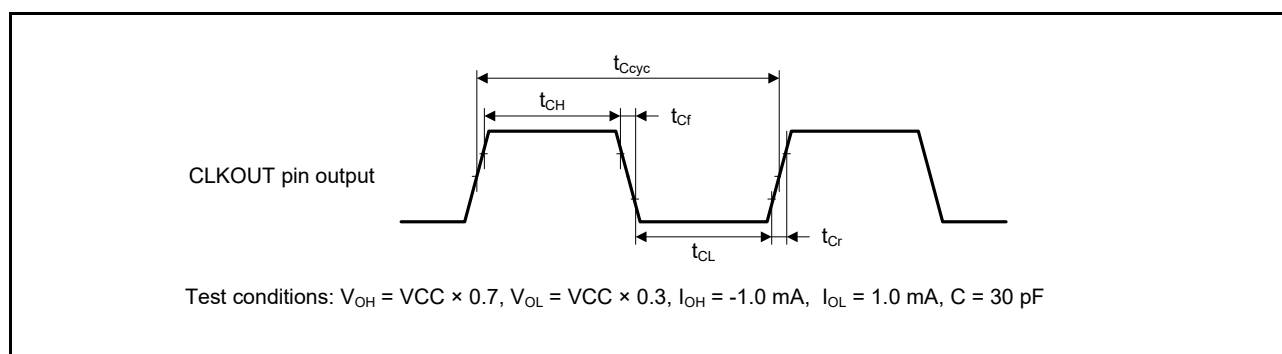


Figure 2.58 CLKOUT output timing

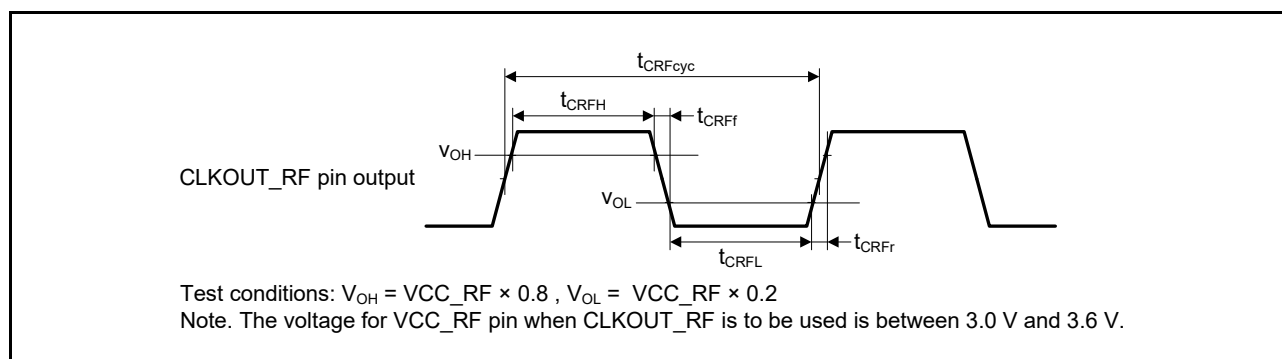


Figure 2.59 CLKOUT\_RF Output Timing

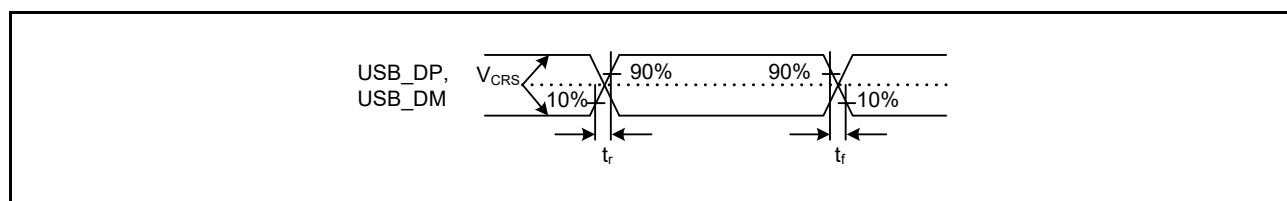
## 2.4 USB Characteristics

### 2.4.1 USBFS Timing

**Table 2.40 USB characteristics**

 Conditions:  $V_{CC} = V_{CC\_USB} = 3.0$  to  $3.6$  V,  $T_a = -20$  to  $+85^\circ\text{C}$  (USBCLKSEL = 1)

| Parameter                              |                                | Symbol         | Min                 | Max                 | Unit          | Test conditions                                                  |
|----------------------------------------|--------------------------------|----------------|---------------------|---------------------|---------------|------------------------------------------------------------------|
| Input characteristics                  | Input high level voltage       | $V_{IH}$       | 2.0                 | -                   | V             | -                                                                |
|                                        | Input low level voltage        | $V_{IL}$       | -                   | 0.8                 | V             | -                                                                |
|                                        | Differential input sensitivity | $V_{DI}$       | 0.2                 | -                   | V             | USB_DP - USB_DM                                                  |
|                                        | Differential common mode range | $V_{CM}$       | 0.8                 | 2.5                 | V             | -                                                                |
| Output characteristics                 | Output high level voltage      | $V_{OH}$       | 2.8                 | $V_{CC\_USB}$       | V             | $I_{OH} = -200\ \mu\text{A}$                                     |
|                                        | Output low level voltage       | $V_{OL}$       | 0.0                 | 0.3                 | V             | $I_{OL} = 2\ \text{mA}$                                          |
|                                        | Cross-over voltage             | $V_{CRS}$      | 1.3                 | 2.0                 | V             | Figure 2.60,<br>Figure 2.61,<br>Figure 2.62                      |
|                                        | Rise time                      | FS             | $t_r$               | 4                   | 20            |                                                                  |
|                                        |                                | LS             |                     | 75                  | 300           |                                                                  |
|                                        | Fall time                      | FS             | $t_f$               | 4                   | 20            |                                                                  |
|                                        |                                | LS             |                     | 75                  | 300           |                                                                  |
|                                        | Rise/fall time ratio           | FS             | $t_r/t_f$           | 90                  | 111.11        |                                                                  |
|                                        |                                | LS             |                     | 80                  | 125           |                                                                  |
|                                        | Output resistance              | $Z_{DRV}$      | 28                  | 44                  | $\Omega$      | (Adjusting the resistance of external elements is not required.) |
| VBUS characteristics                   | VBUS input voltage             | $V_{IH}$       | $V_{CC} \times 0.8$ | -                   | V             | -                                                                |
|                                        |                                | $V_{IL}$       | -                   | $V_{CC} \times 0.2$ | V             | -                                                                |
| Pull-up, pull-down                     | Pull-down resistor             | $R_{PD}$       | 14.25               | 24.80               | k $\Omega$    | -                                                                |
|                                        | Pull-up resistor               | $R_{PUI}$      | 0.9                 | 1.575               | k $\Omega$    | During idle state                                                |
|                                        |                                | $R_{PUA}$      | 1.425               | 3.09                | k $\Omega$    | During reception                                                 |
| Battery Charging Specification Ver 1.2 | D + sink current               | $I_{DP\_SINK}$ | 25                  | 175                 | $\mu\text{A}$ | -                                                                |
|                                        | D - sink current               | $I_{DM\_SINK}$ | 25                  | 175                 | $\mu\text{A}$ | -                                                                |
|                                        | DCD source current             | $I_{DP\_SRC}$  | 7                   | 13                  | $\mu\text{A}$ | -                                                                |
|                                        | Data detection voltage         | $V_{DAT\_REF}$ | 0.25                | 0.4                 | V             | -                                                                |
|                                        | D + source voltage             | $V_{DP\_SRC}$  | 0.5                 | 0.7                 | V             | Output current = 250 $\mu\text{A}$                               |
|                                        | D - source voltage             | $V_{DM\_SRC}$  | 0.5                 | 0.7                 | V             | Output current = 250 $\mu\text{A}$                               |


**Figure 2.60 USB\_DP and USB\_DM output timing**

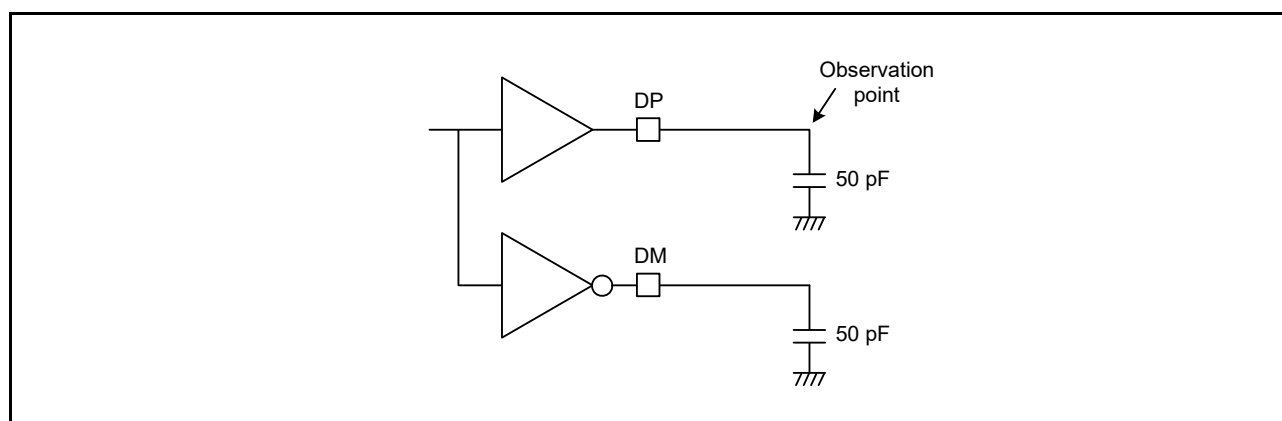


Figure 2.61 Test circuit for Full-Speed (FS) connection

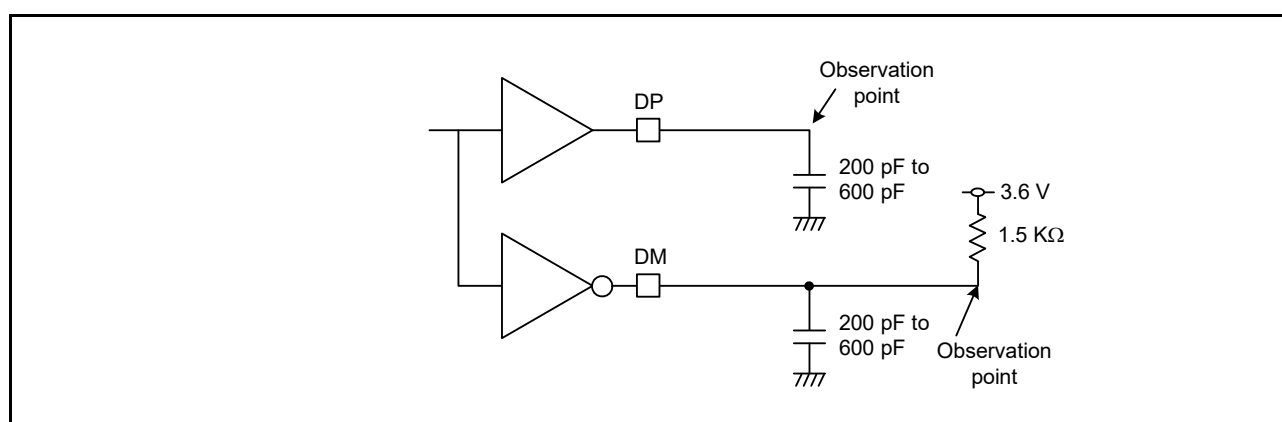


Figure 2.62 Test circuit for Low-Speed (LS) connection

## 2.5 ADC14 Characteristics

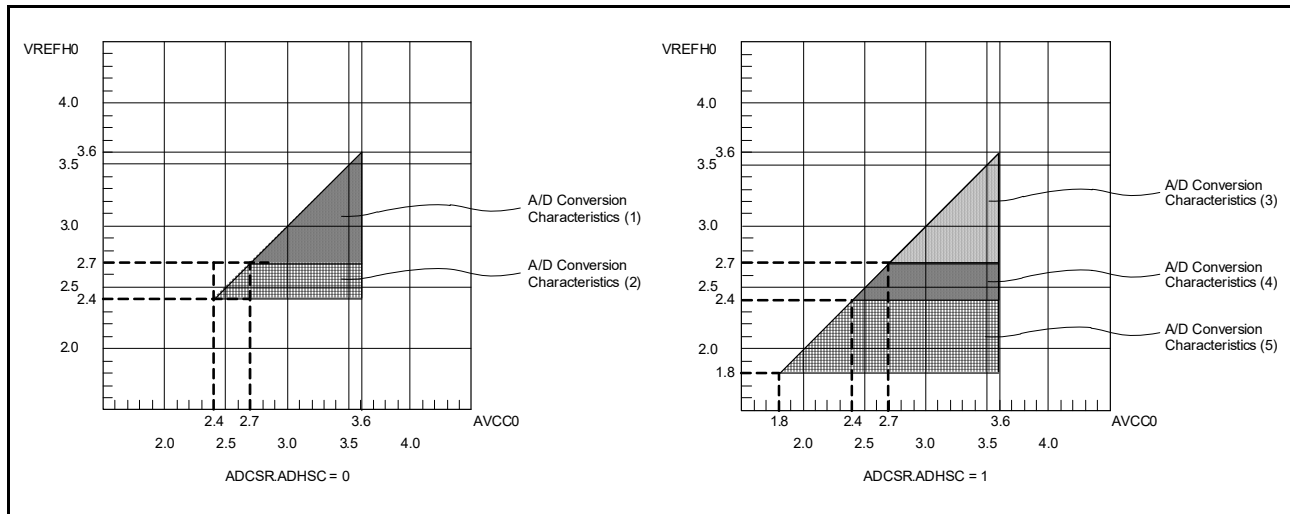


Figure 2.63 AVCC0 to VREFH0 voltage range

**Table 2.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min   | Typ  | Max                  | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|-------|------|----------------------|------|-----------------------------------------------------------------------|
| Frequency                                             |                                                         | 1     | -    | 48                   | MHz  | -                                                                     |
| Analog input capacitance*2                            | Cs                                                      | -     | -    | 8 (reference data)   | pF   | High-precision channel                                                |
|                                                       |                                                         | -     | -    | 9 (reference data)   | pF   | Normal-precision channel                                              |
| Analog input resistance                               | Rs                                                      | -     | -    | 2.5 (reference data) | kΩ   | High-precision channel                                                |
|                                                       |                                                         | -     | -    | 6.7 (reference data) | kΩ   | Normal-precision channel                                              |
| Analog input voltage range                            | Ain                                                     | 0     | -    | VREFH0               | V    | -                                                                     |
| 12-bit mode                                           |                                                         |       |      |                      |      |                                                                       |
| Resolution                                            |                                                         | -     | -    | 12                   | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 48 MHz) | Permissible signal<br>source impedance<br>Max. = 0.3 kΩ | 0.94  | -    | -                    | μs   | High-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 1.50  | -    | -                    | μs   | Normal-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | ±0.5  |      | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |       |      | ±6.0                 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | ±0.75 |      | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |       |      | ±6.0                 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | ±0.5  | -    | -                    | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | ±1.25 |      | ±5.0                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |       |      | ±8.0                 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | ±1.0  | -    | -                    | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | ±1.0  | ±3.0 | -                    | LSB  | -                                                                     |
| 14-bit mode                                           |                                                         |       |      |                      |      |                                                                       |
| Resolution                                            |                                                         | -     | -    | 14                   | Bit  | -                                                                     |

**Table 2.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ  | Max   | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|------|-------|------|-----------------------------------------------------------------------|
| Conversion time*1<br>(Operation at<br>PCLKC = 48 MHz) | Permissible signal<br>source impedance<br>Max. = 0.3 kΩ | 1.06 | -    | -     | μs   | High-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 1.63 | -    | -     | μs   | Normal-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±2.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±3.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5 | -     | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±5.0 | ±20   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±32.0 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±4.0 | -     | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±4.0 | ±12.0 | LSB  | -                                                                     |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V<sub>OH</sub>, V<sub>OL</sub>, and Other Characteristics](#).

**Table 2.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ   | Max                  | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|-------|----------------------|------|-----------------------------------------------------------------------|
| Frequency                                             |                                                         | 1    | -     | 32                   | MHz  | -                                                                     |
| Analog input capacitance*2                            | Cs                                                      | -    | -     | 8 (reference data)   | pF   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 9 (reference data)   | pF   | Normal-precision channel                                              |
| Analog input resistance                               | Rs                                                      | -    | -     | 2.5 (reference data) | kΩ   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 6.7 (reference data) | kΩ   | Normal-precision channel                                              |
| Analog input voltage range                            | Ain                                                     | 0    | -     | VREFH0               | V    | -                                                                     |
| 12-bit mode                                           |                                                         |      |       |                      |      |                                                                       |
| Resolution                                            |                                                         | -    | -     | 12                   | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 32 MHz) | Permissible signal<br>source impedance<br>Max. = 1.3 kΩ | 1.41 | -     | -                    | μs   | High-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 2.25 | -     | -                    | μs   | Normal-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±0.5  | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±0.75 | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5  | -                    | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±1.25 | ±5.0                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±8.0                 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±1.0  | -                    | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±1.0  | ±3.0                 | LSB  | -                                                                     |
| 14-bit mode                                           |                                                         |      |       |                      |      |                                                                       |

**Table 2.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ  | Max   | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|------|-------|------|-----------------------------------------------------------------------|
| Resolution                                            |                                                         | -    | -    | 14    | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 32 MHz) | Permissible signal<br>source impedance<br>Max. = 1.3 kΩ | 1.59 | -    | -     | μs   | High-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 2.44 | -    | -     | μs   | Normal-precision channel<br>ADCSR.ADHSC = 0<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±2.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±3.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5 | -     | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±5.0 | ±20   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±32.0 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±4.0 | -     | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±4.0 | ±12.0 | LSB  | -                                                                     |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V<sub>OH</sub>, V<sub>OL</sub>, and Other Characteristics](#).

**Table 2.43 A/D conversion characteristics (3) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ   | Max                  | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|-------|----------------------|------|-----------------------------------------------------------------------|
| Frequency                                             |                                                         | 1    | -     | 24                   | MHz  | -                                                                     |
| Analog input capacitance*2                            | Cs                                                      | -    | -     | 8 (reference data)   | pF   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 9 (reference data)   | pF   | Normal-precision channel                                              |
| Analog input resistance                               | Rs                                                      | -    | -     | 2.5 (reference data) | kΩ   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 6.7 (reference data) | kΩ   | Normal-precision channel                                              |
| Analog input voltage range                            | Ain                                                     | 0    | -     | VREFH0               | V    | -                                                                     |
| 12-bit mode                                           |                                                         |      |       |                      |      |                                                                       |
| Resolution                                            |                                                         | -    | -     | 12                   | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 24 MHz) | Permissible signal<br>source impedance<br>Max. = 1.1 kΩ | 2.25 | -     | -                    | μs   | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 3.38 | -     | -                    | μs   | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±0.5  | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±0.75 | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5  | -                    | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±1.25 | ±5.0                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±8.0                 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±1.0  | -                    | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±1.0  | ±3.0                 | LSB  | -                                                                     |

**Table 2.43 A/D conversion characteristics (3) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.7 to 3.6 V, VREFH0 = 2.7 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ  | Max   | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|------|-------|------|-----------------------------------------------------------------------|
| 14-bit mode                                           |                                                         |      |      |       |      |                                                                       |
| Resolution                                            |                                                         | -    | -    | 14    | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 24 MHz) | Permissible signal<br>source impedance<br>Max. = 1.1 kΩ | 2.50 | -    | -     | μs   | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 3.63 | -    | -     | μs   | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±2.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±3.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5 | -     | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±5.0 | ±20   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±32.0 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±4.0 | -     | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±4.0 | ±12.0 | LSB  | -                                                                     |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V<sub>OH</sub>, V<sub>OL</sub>, and Other Characteristics](#).

**Table 2.44 A/D conversion characteristics (4) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ   | Max                  | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|-------|----------------------|------|-----------------------------------------------------------------------|
| Frequency                                             |                                                         | 1    | -     | 16                   | MHz  | -                                                                     |
| Analog input capacitance*2                            | Cs                                                      | -    | -     | 8 (reference data)   | pF   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 9 (reference data)   | pF   | Normal-precision channel                                              |
| Analog input resistance                               | Rs                                                      | -    | -     | 2.5 (reference data) | kΩ   | High-precision channel                                                |
|                                                       |                                                         | -    | -     | 6.7 (reference data) | kΩ   | Normal-precision channel                                              |
| Analog input voltage range                            | Ain                                                     | 0    | -     | VREFH0               | V    | -                                                                     |
| 12-bit mode                                           |                                                         |      |       |                      |      |                                                                       |
| Resolution                                            |                                                         | -    | -     | 12                   | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 16 MHz) | Permissible signal<br>source impedance<br>Max. = 2.2 kΩ | 3.38 | -     | -                    | μs   | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 5.06 | -     | -                    | μs   | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±0.5  | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±0.75 | ±4.5                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±6.0                 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5  | -                    | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±1.25 | ±5.0                 | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |       | ±8.0                 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±1.0  | -                    | LSB  | -                                                                     |

**Table 2.44 A/D conversion characteristics (4) in low power A/D conversion mode (2 of 2)**

Conditions: VCC = AVCC0 = 2.4 to 3.6 V, VREFH0 = 2.4 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                             |                                                         | Min  | Typ  | Max   | Unit | Test conditions                                                       |
|-------------------------------------------------------|---------------------------------------------------------|------|------|-------|------|-----------------------------------------------------------------------|
| INL integral nonlinearity error                       |                                                         | -    | ±1.0 | ±3.0  | LSB  | -                                                                     |
| 14-bit mode                                           |                                                         |      |      |       |      |                                                                       |
| Resolution                                            |                                                         | -    | -    | 14    | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 16 MHz) | Permissible signal<br>source impedance<br>Max. = 2.2 kΩ | 3.75 | -    | -     | μs   | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                       |                                                         | 5.44 | -    | -     | μs   | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                          |                                                         | -    | ±2.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Full-scale error                                      |                                                         | -    | ±3.0 | ±18   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±24.0 | LSB  | Other than above                                                      |
| Quantization error                                    |                                                         | -    | ±0.5 | -     | LSB  | -                                                                     |
| Absolute accuracy                                     |                                                         | -    | ±5.0 | ±20   | LSB  | High-precision channel                                                |
|                                                       |                                                         |      |      | ±32.0 | LSB  | Other than above                                                      |
| DNL differential nonlinearity error                   |                                                         | -    | ±4.0 | -     | LSB  | -                                                                     |
| INL integral nonlinearity error                       |                                                         | -    | ±4.0 | ±12.0 | LSB  | -                                                                     |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V<sub>OH</sub>, V<sub>OL</sub>, and Other Characteristics](#).

**Table 2.45 A/D conversion characteristics (5) in low power A/D conversion mode (1 of 2)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V (AVCC0 = VCC when VCC &lt; 2.0 V), VREFH0 = 1.8 to 3.6 V

Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter                                            |                                                       | Min   | Typ  | Max                  | Unit | Test conditions                                                       |
|------------------------------------------------------|-------------------------------------------------------|-------|------|----------------------|------|-----------------------------------------------------------------------|
| Frequency                                            |                                                       | 1     | -    | 8                    | MHz  | -                                                                     |
| Analog input capacitance*2                           | Cs                                                    | -     | -    | 8 (reference data)   | pF   | High-precision channel                                                |
|                                                      |                                                       | -     | -    | 9 (reference data)   | pF   | Normal-precision channel                                              |
| Analog input resistance                              | Rs                                                    | -     | -    | 3.8 (reference data) | kΩ   | High-precision channel                                                |
|                                                      |                                                       | -     | -    | 8.2 (reference data) | kΩ   | Normal-precision channel                                              |
| Analog input voltage range                           | Ain                                                   | 0     | -    | VREFH0               | V    | -                                                                     |
| 12-bit mode                                          |                                                       |       |      |                      |      |                                                                       |
| Resolution                                           |                                                       | -     | -    | 12                   | Bit  | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 8 MHz) | Permissible signal<br>source impedance<br>Max. = 5 kΩ | 6.75  | -    | -                    | μs   | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                      |                                                       | 10.13 | -    | -                    | μs   | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                         |                                                       | -     | ±1.0 | ±7.5                 | LSB  | High-precision channel                                                |
|                                                      |                                                       |       |      | ±10.0                | LSB  | Other than above                                                      |
| Full-scale error                                     |                                                       | -     | ±1.5 | ±7.5                 | LSB  | High-precision channel                                                |
|                                                      |                                                       |       |      | ±10.0                | LSB  | Other than above                                                      |
| Quantization error                                   |                                                       | -     | ±0.5 | -                    | LSB  | -                                                                     |
| Absolute accuracy                                    |                                                       | -     | ±3.0 | ±8.0                 | LSB  | High-precision channel                                                |
|                                                      |                                                       |       |      | ±12.0                | LSB  | Other than above                                                      |

**Table 2.45 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)**

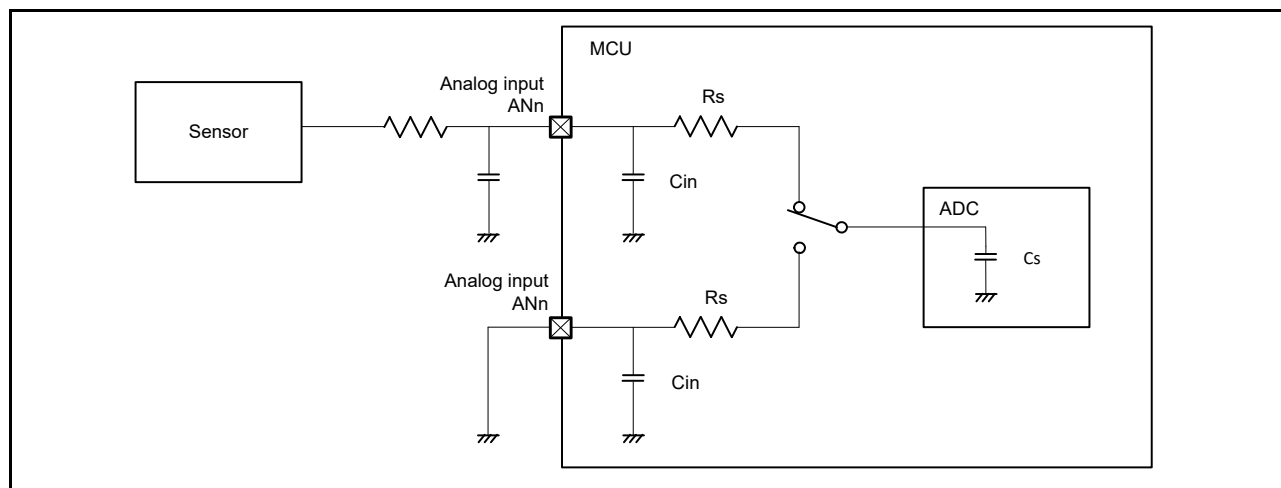
Conditions:  $V_{CC} = AV_{CC0} = 1.8$  to  $3.6$  V ( $AV_{CC0} = V_{CC}$  when  $V_{CC} < 2.0$  V),  $V_{REFH0} = 1.8$  to  $3.6$  V  
 Reference voltage range applied to the  $V_{REFH0}$  and  $V_{REFL0}$ .

| Parameter                                            | Min                                                           | Typ        | Max        | Unit    | Test conditions                                                       |
|------------------------------------------------------|---------------------------------------------------------------|------------|------------|---------|-----------------------------------------------------------------------|
| DNL differential nonlinearity error                  | -                                                             | $\pm 1.0$  | -          | LSB     | -                                                                     |
| INL integral nonlinearity error                      | -                                                             | $\pm 1.0$  | $\pm 3.0$  | LSB     | -                                                                     |
| 14-bit mode                                          |                                                               |            |            |         |                                                                       |
| Resolution                                           | -                                                             | -          | 14         | Bit     | -                                                                     |
| Conversion time*1<br>(Operation at<br>PCLKC = 8 MHz) | Permissible signal<br>source impedance<br>Max. = 5 k $\Omega$ | 7.50       | -          | $\mu$ s | High-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 0Dh   |
|                                                      |                                                               | 10.88      | -          | $\mu$ s | Normal-precision channel<br>ADCSR.ADHSC = 1<br>ADSSTRn.SST[7:0] = 28h |
| Offset error                                         |                                                               | $\pm 4.0$  | $\pm 30.0$ | LSB     | High-precision channel                                                |
|                                                      |                                                               |            | $\pm 40.0$ | LSB     | Other than above                                                      |
| Full-scale error                                     |                                                               | $\pm 6.0$  | $\pm 30.0$ | LSB     | High-precision channel                                                |
|                                                      |                                                               |            | $\pm 40.0$ | LSB     | Other than above                                                      |
| Quantization error                                   | -                                                             | $\pm 0.5$  | -          | LSB     | -                                                                     |
| Absolute accuracy                                    |                                                               | $\pm 12.0$ | $\pm 32.0$ | LSB     | High-precision channel                                                |
|                                                      |                                                               |            | $\pm 48.0$ | LSB     | Other than above                                                      |
| DNL differential nonlinearity error                  | -                                                             | $\pm 4.0$  | -          | LSB     | -                                                                     |
| INL integral nonlinearity error                      | -                                                             | $\pm 4.0$  | $\pm 12.0$ | LSB     | -                                                                     |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O  \$V\_{OH}\$ ,  \$V\_{OL}\$ , and Other Characteristics](#).

**Figure 2.64 Equivalent circuit for analog input****Table 2.46 14-bit A/D converter channel classification (1 of 2)**

| Classification                           | Channel                      | Conditions                  | Remarks                                                                                                                                |
|------------------------------------------|------------------------------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| High-precision channel                   | AN004 to AN006, AN009, AN010 | $AV_{CC0} = 1.8$ to $3.6$ V | Pins AN004 to AN006, AN009 and AN010 cannot be used as general I/O, IRQ3 inputs, and TS transmission, when the A/D converter is in use |
| Normal-precision channel                 | AN017, AN019, AN020          |                             |                                                                                                                                        |
| Internal reference voltage input channel | Internal reference voltage   | $AV_{CC0} = 2.0$ to $3.6$ V | -                                                                                                                                      |

**Table 2.46 14-bit A/D converter channel classification (2 of 2)**

| Classification                   | Channel                   | Conditions           | Remarks |
|----------------------------------|---------------------------|----------------------|---------|
| Temperature sensor input channel | Temperature sensor output | AVCC0 = 2.0 to 3.6 V | -       |

**Table 2.47 A/D internal reference voltage characteristics**

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 3.6 V\*1

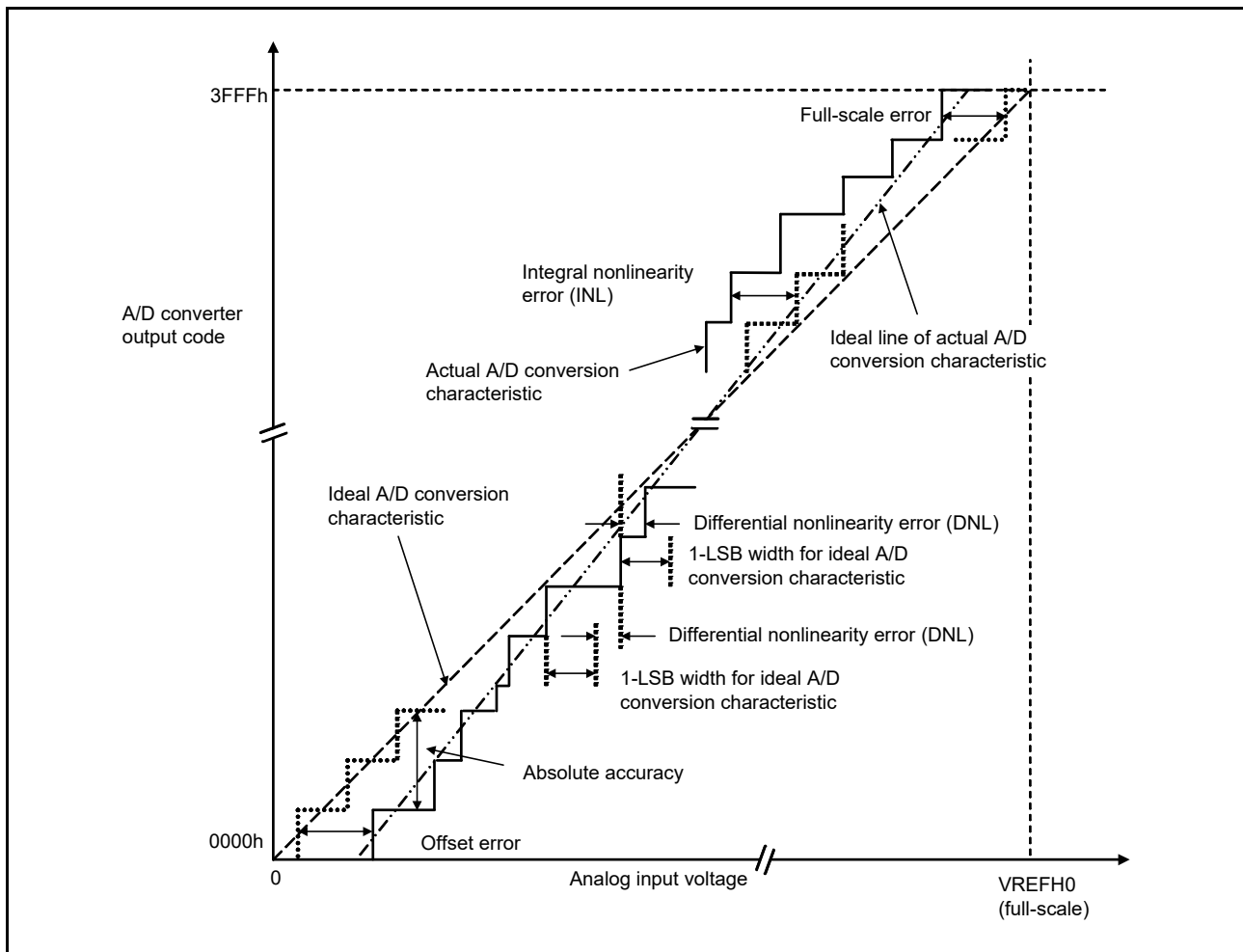
| Parameter                                  | Min  | Typ  | Max  | Unit | Test conditions |
|--------------------------------------------|------|------|------|------|-----------------|
| Internal reference voltage input channel*2 | 1.36 | 1.43 | 1.50 | V    | -               |
| Frequency*3                                | 1    | -    | 2    | MHz  | -               |
| Sampling time*4                            | 5.0  | -    | -    | μs   | -               |

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 &lt; 2.0 V.

Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.

Note 3. This is a parameter for ADC14 when the internal reference voltage is used as a high-potential reference voltage.

Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.



**Figure 2.65** Illustration of 14-bit A/D converter characteristic terms

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage  $V_{REFH0} = 3.072$  V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of  $\pm 5$  LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

## 2.6 DAC12 Characteristics

**Table 2.48 D/A conversion characteristics (1)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Reference voltage = AVCC0 or AVSS0 selected

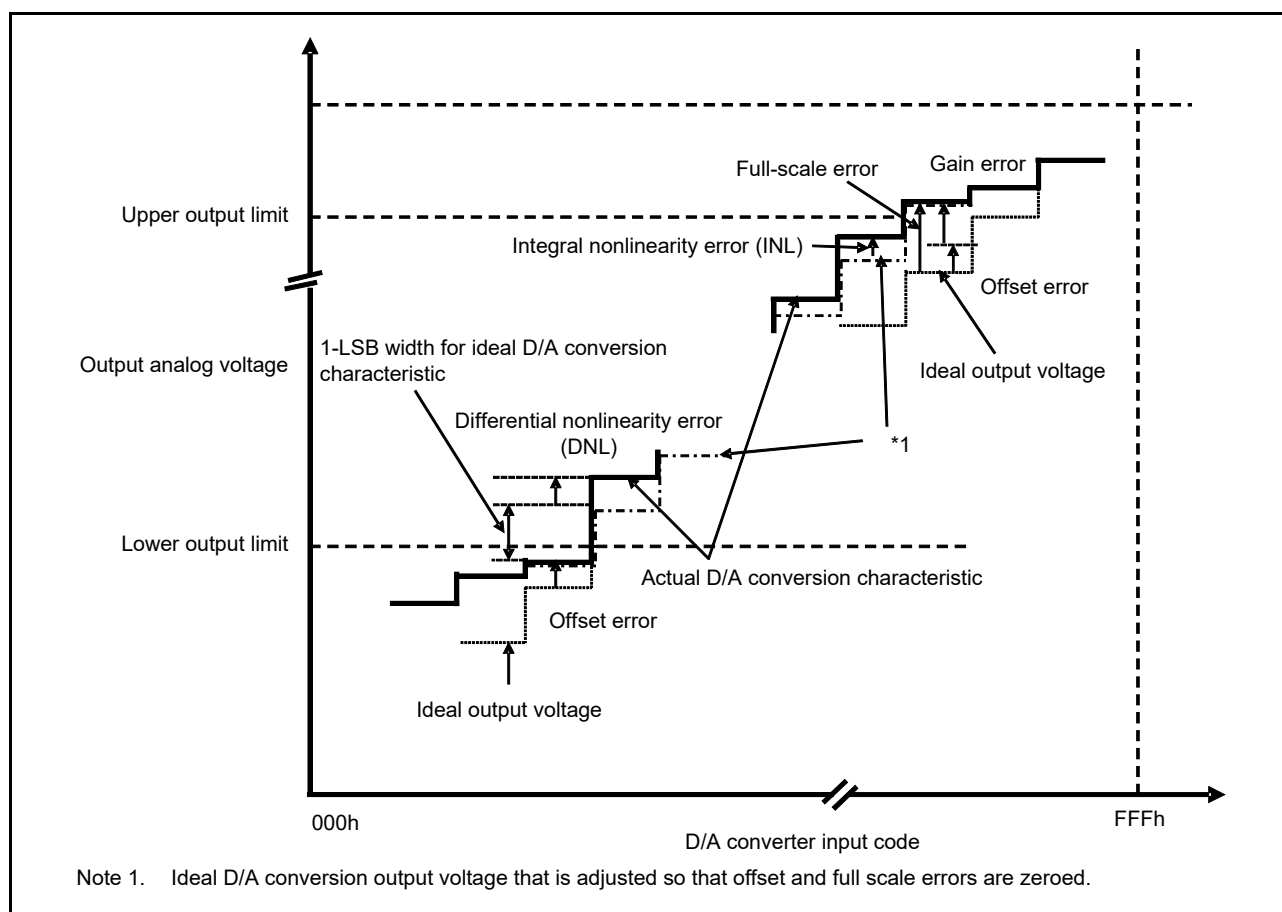
| Parameter                           | Min  | Typ  | Max          | Unit | Test conditions |
|-------------------------------------|------|------|--------------|------|-----------------|
| Resolution                          | -    | -    | 12           | bit  | -               |
| Resistive load                      | 30   | -    | -            | kΩ   | -               |
| Capacitive load                     | -    | -    | 50           | pF   | -               |
| Output voltage range                | 0.35 | -    | AVCC0 – 0.47 | V    | -               |
| DNL differential nonlinearity error | -    | ±0.5 | ±2.0         | LSB  | -               |
| INL integral nonlinearity error     | -    | ±2.0 | ±8.0         | LSB  | -               |
| Offset error                        | -    | -    | ±30          | mV   | -               |
| Full-scale error                    | -    | -    | ±30          | mV   | -               |
| Output impedance                    | -    | 5    | -            | Ω    | -               |
| Conversion time                     | -    | -    | 30           | μs   | -               |

**Table 2.49 D/A conversion characteristics (2)**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Reference voltage = internal reference voltage selected

| Parameter                           | Min  | Typ  | Max   | Unit | Test conditions |
|-------------------------------------|------|------|-------|------|-----------------|
| Resolution                          | -    | -    | 12    | bit  | -               |
| Internal reference voltage (Vbgr)   | 1.36 | 1.43 | 1.50  | V    | -               |
| Resistive load                      | 30   | -    | -     | kΩ   | -               |
| Capacitive load                     | -    | -    | 50    | pF   | -               |
| Output voltage range                | 0.35 | -    | Vbgr  | V    | -               |
| DNL differential nonlinearity error | -    | ±2.0 | ±16.0 | LSB  | -               |
| INL integral nonlinearity error     | -    | ±8.0 | ±16.0 | LSB  | -               |
| Offset error                        | -    | -    | ±30   | mV   | -               |
| Output impedance                    | -    | 5    | -     | Ω    | -               |
| Conversion time                     | -    | -    | 30    | μs   | -               |



**Figure 2.66 Illustration of D/A converter characteristic terms**

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

### Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

### Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

## 2.7 TSN Characteristics

**Table 2.50 TSN characteristics**

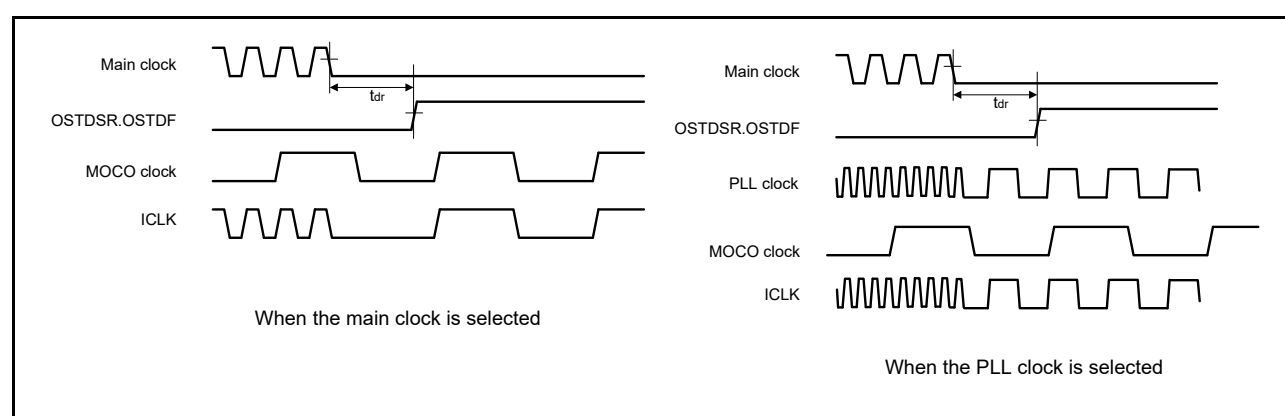
Conditions: VCC = AVCC0 = 2.0 to 3.6 V

| Parameter                     | Symbol             | Min | Typ   | Max | Unit  | Test conditions |
|-------------------------------|--------------------|-----|-------|-----|-------|-----------------|
| Relative accuracy             | -                  | -   | ±1.5  | -   | °C    | 2.4 V or above  |
|                               | -                  | -   | ±2.0  | -   | °C    | Below 2.4 V     |
| Temperature slope             | -                  | -   | -3.65 | -   | mV/°C | -               |
| Output voltage (at 25°C)      | -                  | -   | 1.05  | -   | V     | VCC = 3.3 V     |
| Temperature sensor start time | t <sub>START</sub> | -   | -     | 5   | μs    | -               |
| Sampling time                 | -                  | 5   | -     | -   | μs    | -               |

## 2.8 OSC Stop Detect Characteristics

**Table 2.51 Oscillation stop detection circuit characteristics**

| Parameter      | Symbol          | Min | Typ | Max | Unit | Test conditions             |
|----------------|-----------------|-----|-----|-----|------|-----------------------------|
| Detection time | t <sub>dr</sub> | -   | -   | 1   | ms   | <a href="#">Figure 2.67</a> |


**Figure 2.67 Oscillation stop detection timing**

## 2.9 POR and LVD Characteristics

**Table 2.52 Power-on reset circuit and voltage detection circuit characteristics (1)**

| Parameter                 |                                    | Symbol              | Min  | Typ  | Max  | Unit | Test conditions                                              |
|---------------------------|------------------------------------|---------------------|------|------|------|------|--------------------------------------------------------------|
| Voltage detection level*1 | Power-on reset (POR)               | V <sub>POR</sub>    | 1.27 | 1.42 | 1.57 | V    | <a href="#">Figure 2.68</a> ,<br><a href="#">Figure 2.69</a> |
|                           | Voltage detection circuit (LVD0)*2 | V <sub>det0_1</sub> | 2.68 | 2.85 | 2.96 | V    | <a href="#">Figure 2.70</a><br>At falling edge<br>VCC        |
|                           |                                    | V <sub>det0_2</sub> | 2.38 | 2.53 | 2.64 |      |                                                              |
|                           |                                    | V <sub>det0_3</sub> | 1.78 | 1.90 | 2.02 |      |                                                              |
|                           | Voltage detection circuit (LVD1)*3 | V <sub>det1_4</sub> | 2.98 | 3.10 | 3.22 | V    | <a href="#">Figure 2.71</a><br>At falling edge<br>VCC        |
|                           |                                    | V <sub>det1_5</sub> | 2.89 | 3.00 | 3.11 |      |                                                              |
|                           |                                    | V <sub>det1_6</sub> | 2.79 | 2.90 | 3.01 |      |                                                              |
|                           |                                    | V <sub>det1_7</sub> | 2.68 | 2.79 | 2.90 |      |                                                              |
|                           |                                    | V <sub>det1_8</sub> | 2.58 | 2.68 | 2.78 |      |                                                              |
|                           |                                    | V <sub>det1_9</sub> | 2.48 | 2.58 | 2.68 |      |                                                              |
|                           |                                    | V <sub>det1_A</sub> | 2.38 | 2.48 | 2.58 |      |                                                              |
|                           |                                    | V <sub>det1_B</sub> | 2.10 | 2.20 | 2.30 |      |                                                              |
|                           |                                    | V <sub>det1_C</sub> | 1.84 | 1.96 | 2.05 |      |                                                              |
|                           |                                    | V <sub>det1_D</sub> | 1.74 | 1.86 | 1.95 |      |                                                              |
|                           |                                    | V <sub>det1_E</sub> | 1.63 | 1.75 | 1.84 |      |                                                              |
|                           |                                    | V <sub>det1_F</sub> | 1.60 | 1.65 | 1.73 |      |                                                              |

Note 1. These characteristics apply when noise is not superimposed on the power supply.

Note 2. # in the symbol V<sub>det0\_#</sub> denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol V<sub>det1\_#</sub> denotes the value of the LVDLVL.LVD1LVL[4:0] bits.

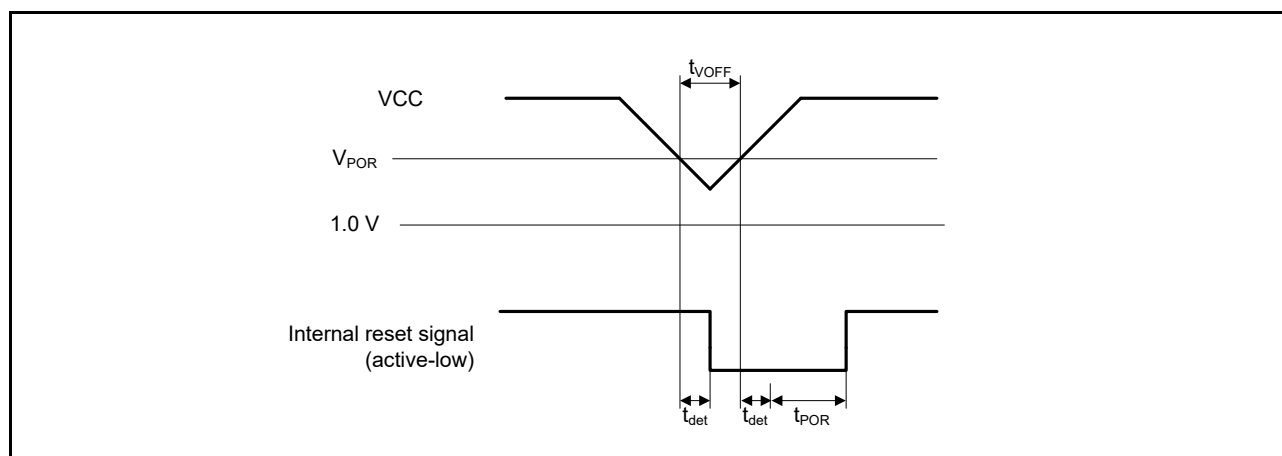
**Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (2)**

| Parameter                                               |                | Symbol       | Min | Typ | Max | Unit    | Test conditions                         |
|---------------------------------------------------------|----------------|--------------|-----|-----|-----|---------|-----------------------------------------|
| Wait time after power-on reset cancellation             | LVD0:enable    | $t_{POR}$    | -   | 1.7 | -   | ms      | -                                       |
|                                                         | LVD0:disable   | $t_{POR}$    | -   | 1.3 | -   | ms      | -                                       |
| Wait time after voltage monitor 0,1 reset cancellation  | LVD0:enable*1  | $t_{LVD0,1}$ | -   | 0.6 | -   | ms      | -                                       |
|                                                         | LVD0:disable*2 | $t_{LVD1}$   | -   | 0.2 | -   | ms      | -                                       |
| Response delay*3                                        |                | $t_{det}$    | -   | -   | 350 | $\mu$ s | Figure 2.68, Figure 2.69                |
| Minimum VCC down time                                   |                | $t_{VOFF}$   | 450 | -   | -   | $\mu$ s | Figure 2.68, VCC = 1.0 V or above       |
| Power-on reset enable time                              |                | $t_W$ (POR)  | 1   | -   | -   | ms      | Figure 2.69, VCC = below 1.0 V          |
| LVD operation stabilization time (after LVD is enabled) |                | $t_d$ (E-A)  | -   | -   | 300 | $\mu$ s | Figure 2.71                             |
| Hysteresis width (POR)                                  |                | $V_{PORH}$   | -   | 110 | -   | mV      | -                                       |
| Hysteresis width (LVD0 and LVD1)                        |                | $V_{LVH}$    | -   | 60  | -   | mV      | LVD0 selected                           |
|                                                         |                |              | -   | 60  | -   |         | $V_{det1\_4}$ to $V_{det1\_9}$ selected |
|                                                         |                |              | -   | 50  | -   |         | $V_{det1\_A}$ or $V_{det1\_B}$ selected |
|                                                         |                |              | -   | 40  | -   |         | $V_{det1\_C}$ or $V_{det1\_F}$ selected |

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels  $V_{POR}$ ,  $V_{det0}$  and  $V_{det1}$  for the POR/LVD.

**Figure 2.68 Voltage detection reset timing**

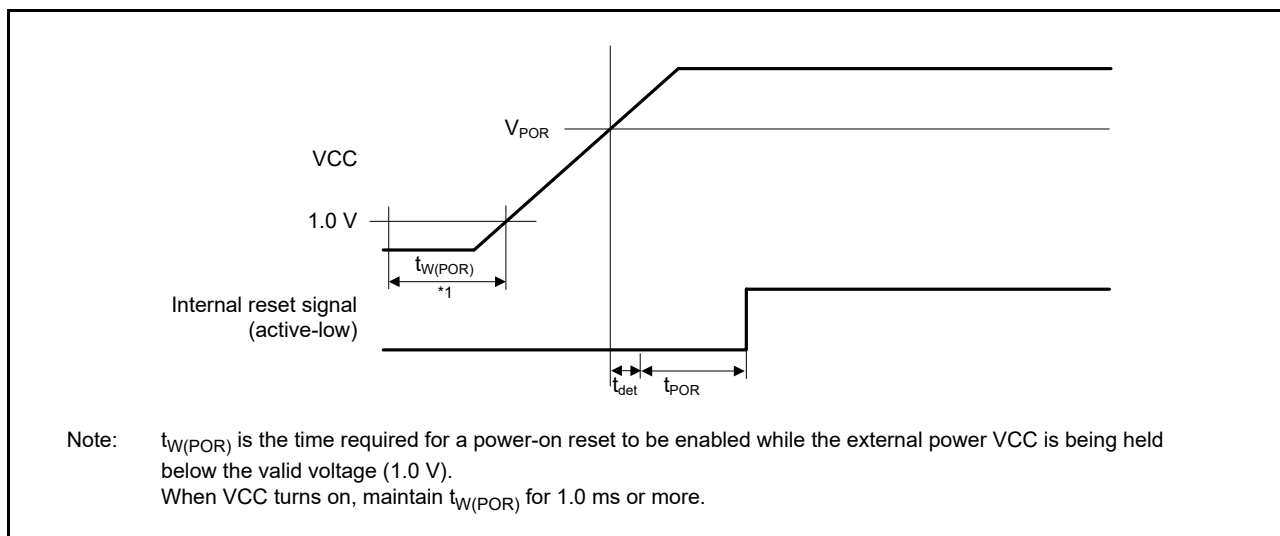
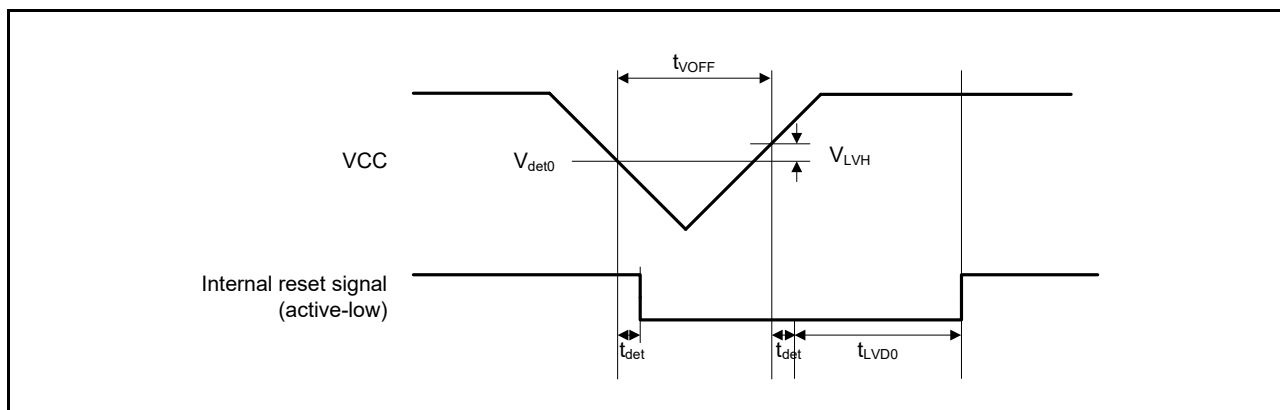
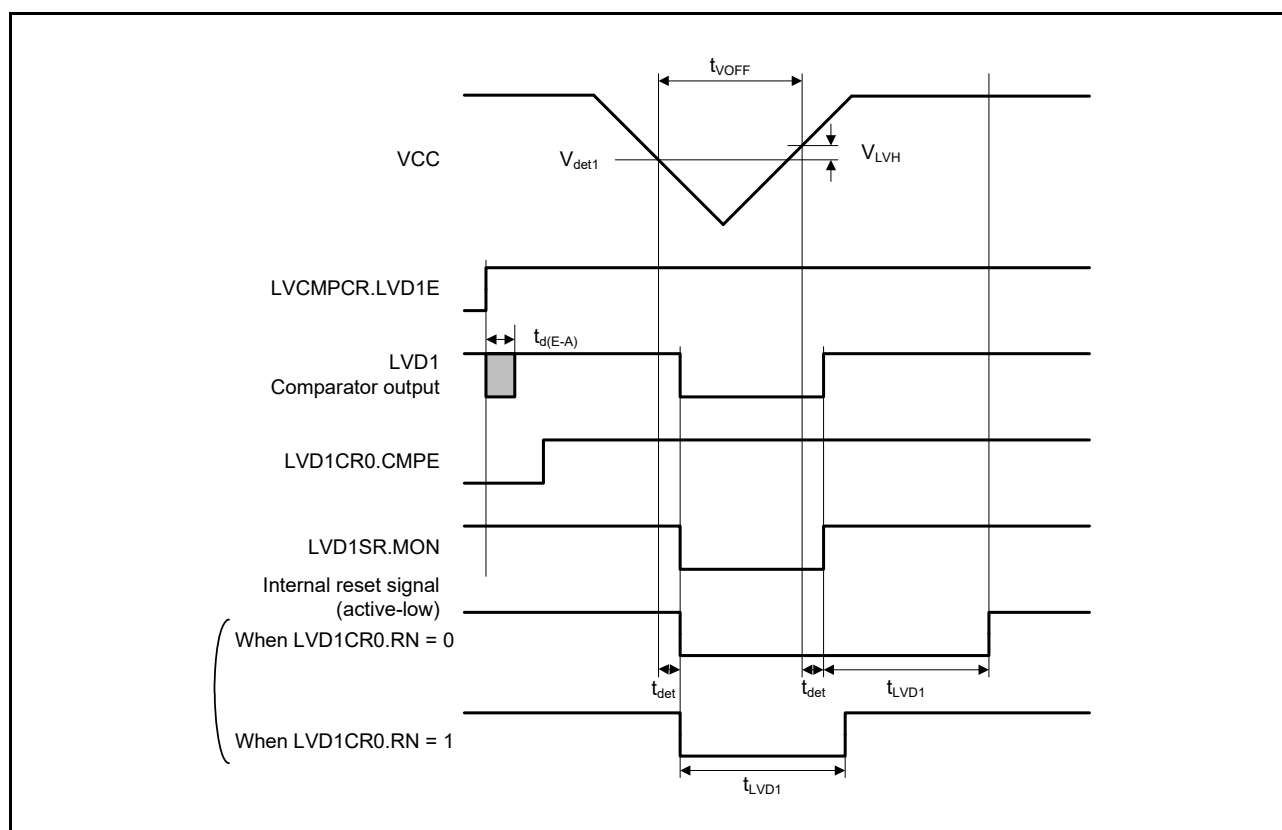


Figure 2.69 Power-on reset timing

Figure 2.70 Voltage detection circuit timing ( $V_{det0}$ )



**Figure 2.71** Voltage detection circuit timing ( $V_{det1}$ )

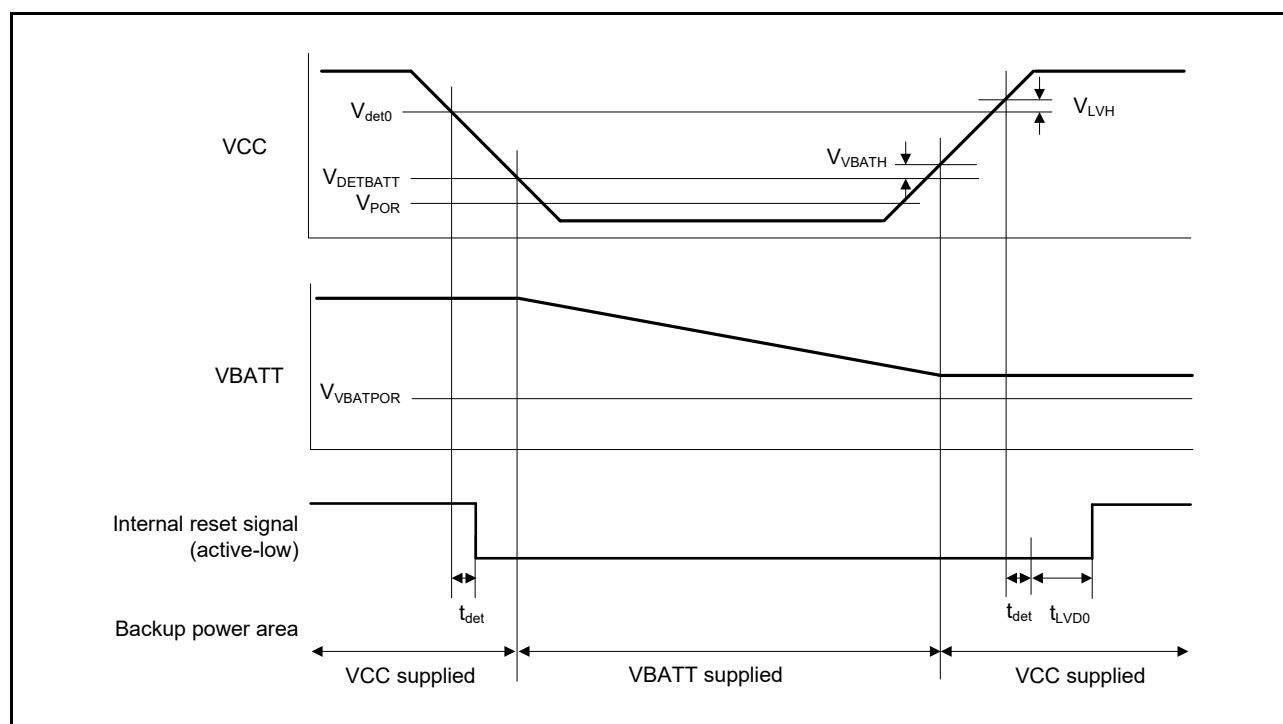
## 2.10 VBATT Characteristics

**Table 2.54 Battery backup function characteristics**

Conditions: VCC = AVCC0 = 1.8V to 3.6V, VBATT = 1.6 to 3.6 V

| Parameter                                                      |                      | Symbol                            | Min  | Typ  | Max  | Unit | Test conditions             |
|----------------------------------------------------------------|----------------------|-----------------------------------|------|------|------|------|-----------------------------|
| Voltage level for switching to battery backup (falling)        |                      | V <sub>DET<sub>BATT</sub></sub>   | 1.99 | 2.09 | 2.19 | V    | Figure 2.72,<br>Figure 2.73 |
| Hysteresis width for switching to battery back up              |                      | V <sub>VBATTH</sub>               | -    | 100  | -    | mV   |                             |
| VCC-off period for starting power supply switching             |                      | t <sub>VOFF<sub>BATT</sub></sub>  | 300  | -    | -    | µs   | -                           |
| Voltage detection level<br>VBATT_Power-on reset (VBATT_POR)    |                      | V <sub>VBATPOR</sub>              | 1.30 | 1.40 | 1.50 | V    | Figure 2.72,<br>Figure 2.73 |
| Wait time after VBATT_POR reset time cancellation              |                      | t <sub>VBATPOR</sub>              | -    | -    | 3    | mS   |                             |
| Level for detection of voltage drop on the VBATT pin (falling) | VBTLVDLVL[1:0] = 10b | V <sub>DET<sub>BATLVD</sub></sub> | 2.11 | 2.2  | 2.29 | V    | Figure 2.74                 |
|                                                                | VBTLVDLVL[1:0] = 11b |                                   | 1.92 | 2    | 2.08 | V    |                             |
| Hysteresis width for VBATT pin LVD                             |                      | V <sub>VBATLVDTH</sub>            | -    | 50   | -    | mV   |                             |
| VBATT pin LVD operation stabilization time                     |                      | t <sub>d_vbat</sub>               | -    | -    | 300  | µs   | Figure 2.74                 |
| VBATT pin LVD response delay time                              |                      | t <sub>det_vbat</sub>             | -    | -    | 350  | µs   |                             |
| Allowable voltage change rising/falling gradient               |                      | dt/dVCC                           | 1.0  | -    | -    | ms/V | -                           |
| VCC voltage level for access to the VBATT backup registers     |                      | V <sub>BKBATT</sub>               | 1.8  | -    | -    | V    | -                           |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ( $V_{DET\text{BATT}}$ ).

**Figure 2.72 Power supply switching and LVD0 reset timing**

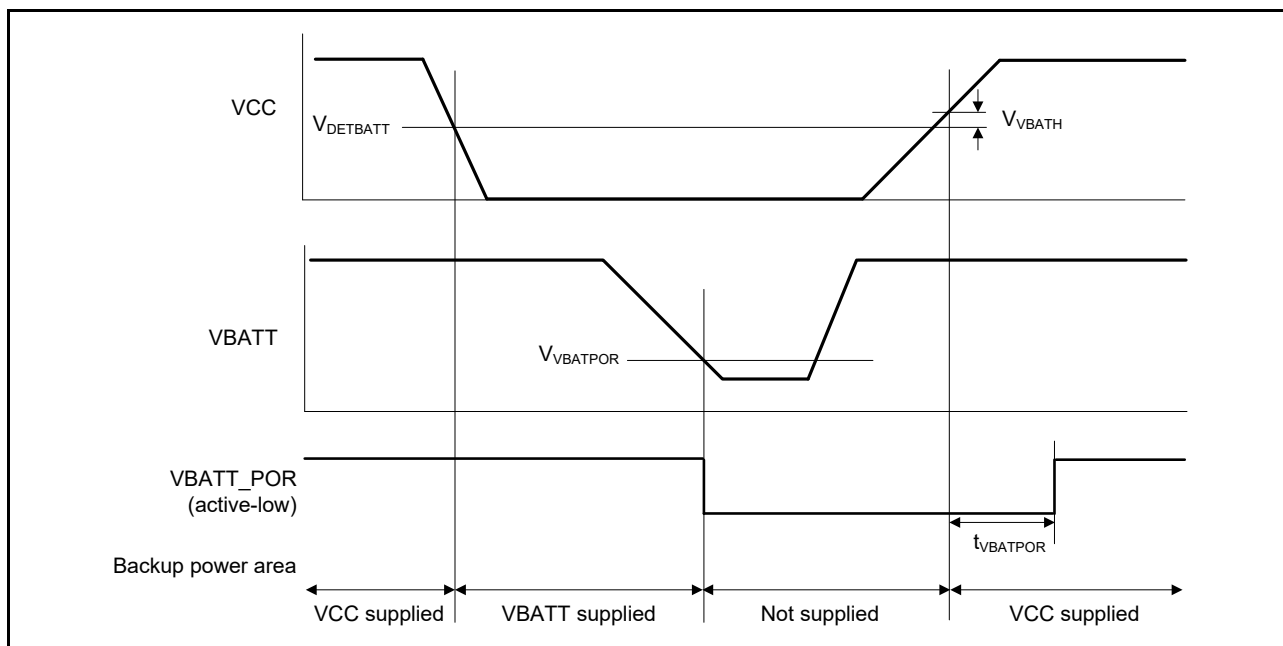


Figure 2.73 VBATT\_POR reset timing

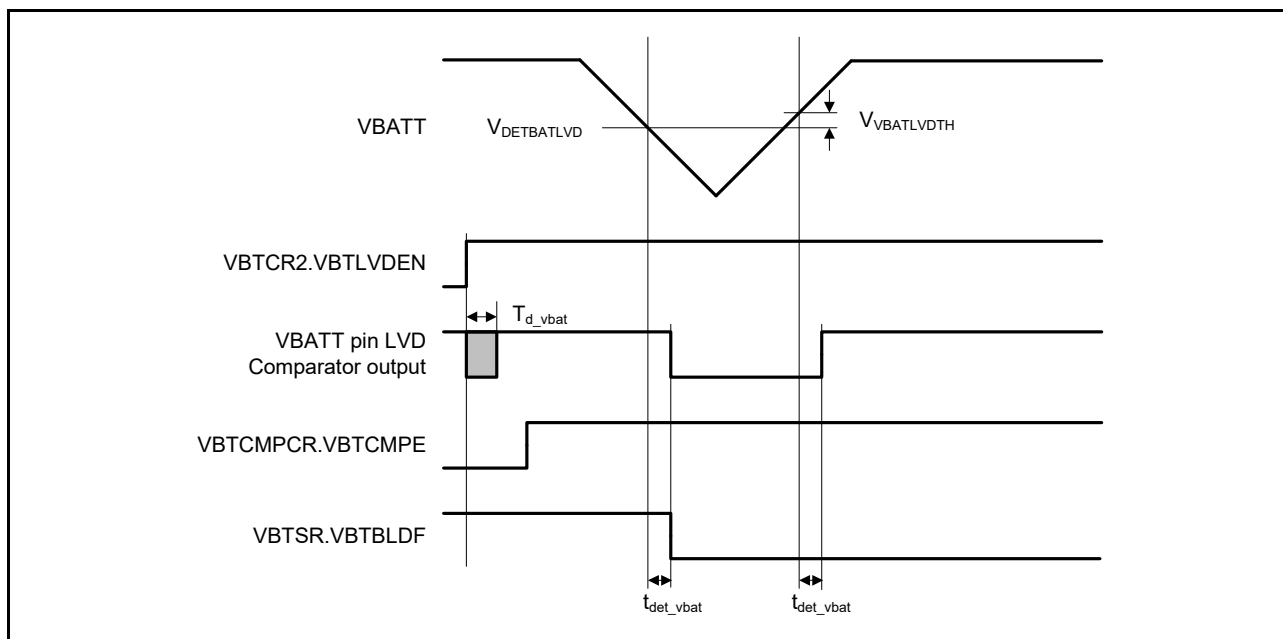


Figure 2.74 VBATT pin voltage detection circuit timing

**Table 2.55 VBATT-I/O characteristics**

| Parameter                                   |                      |                                                | Symbol   | Min           | Typ | Max | Unit | Test conditions       |
|---------------------------------------------|----------------------|------------------------------------------------|----------|---------------|-----|-----|------|-----------------------|
| VBATWIO nI/O output characteristics (n = 0) | $VCC > V_{DET BATT}$ | $VCC = 2.7 \text{ to } 3.6 \text{ V}$          | $V_{OH}$ | $VCC - 0.5$   | -   | -   |      | $I_{OH} = -100 \mu A$ |
|                                             |                      |                                                | $V_{OL}$ | -             | -   | 0.5 |      | $I_{OL} = 100 \mu A$  |
|                                             |                      | $VCC = V_{DET BATT} \text{ to } 2.7 \text{ V}$ | $V_{OH}$ | $VCC - 0.3$   | -   | -   |      | $I_{OH} = -50 \mu A$  |
|                                             |                      |                                                | $V_{OL}$ | -             | -   | 0.3 |      | $I_{OL} = 50 \mu A$   |
|                                             | $VCC < V_{DET BATT}$ | $VBATT = 2.7 \text{ to } 3.6 \text{ V}$        | $V_{OH}$ | $VBATT - 0.5$ | -   | -   |      | $I_{OH} = -100 \mu A$ |
|                                             |                      |                                                | $V_{OL}$ | -             | -   | 0.5 |      | $I_{OL} = 100 \mu A$  |
|                                             |                      | $VBATT = 1.8 \text{ to } 2.7 \text{ V}$        | $V_{OH}$ | $VBATT - 0.3$ | -   | -   |      | $I_{OH} = -50 \mu A$  |
|                                             |                      |                                                | $V_{OL}$ | -             | -   | 0.3 |      | $I_{OL} = 50 \mu A$   |

## 2.11 CTSU Characteristics

**Table 2.56 CTSU characteristics**Conditions:  $VCC = AVCC0 = 1.8 \text{ to } 3.6 \text{ V}$ 

| Parameter                                   | Symbol          | Min | Typ | Max | Unit | Test conditions                               |
|---------------------------------------------|-----------------|-----|-----|-----|------|-----------------------------------------------|
| External capacitance connected to TSCAP pin | $C_{tscap}$     | 9   | 10  | 11  | nF   | -                                             |
| TS pin capacitive load                      | $C_{base}$      | -   | -   | 50  | pF   | -                                             |
| Permissible output high current             | $\Sigma I_{OH}$ | -   | -   | -24 | mA   | When the mutual capacitance method is applied |

## 2.12 Segment LCD Controller Characteristics

### 2.12.1 Resistance Division Method

[Static Display Mode]

**Table 2.57 Resistance division method LCD characteristics (1)**

Conditions:  $V_{L4} \leq V_{CC} \leq 3.6$  V

| Parameter         | Symbol   | Min | Typ | Max | Unit | Test conditions |
|-------------------|----------|-----|-----|-----|------|-----------------|
| LCD drive voltage | $V_{L4}$ | 2.0 | -   | VCC | V    | -               |

[1/2 Bias Method, 1/4 Bias Method]

**Table 2.58 Resistance division method LCD characteristics (2)**

Conditions:  $V_{L4} \leq V_{CC} \leq 3.6$  V

| Parameter         | Symbol   | Min | Typ | Max | Unit | Test conditions |
|-------------------|----------|-----|-----|-----|------|-----------------|
| LCD drive voltage | $V_{L4}$ | 2.7 | -   | VCC | V    | -               |

[1/3 Bias Method]

**Table 2.59 Resistance division method LCD characteristics (3)**

Conditions:  $V_{L4} \leq V_{CC} \leq 3.6$  V

| Parameter         | Symbol   | Min | Typ | Max | Unit | Test conditions |
|-------------------|----------|-----|-----|-----|------|-----------------|
| LCD drive voltage | $V_{L4}$ | 2.5 | -   | VCC | V    | -               |

## 2.13 Comparator Characteristics

**Table 2.60 ACMPLP characteristics**

Conditions:  $V_{CC} = 1.8$  to  $3.6$  V

| Parameter                         |                 |                   | Symbol           | Min  | Typ  | Max     | Unit                                                 | Test conditions |
|-----------------------------------|-----------------|-------------------|------------------|------|------|---------|------------------------------------------------------|-----------------|
| Reference voltage range           | Standard mode   | IVREFn<br>(n=0,1) | VREF             | 0    | -    | VCC−1.4 | V                                                    | -               |
|                                   | Window mode*2   | IVREF1            | VREFH            | 1.4  | -    | VCC     | V                                                    | -               |
|                                   |                 | IVREF0            | VREFL            | 0    | -    | VCC−1.4 | V                                                    | -               |
| Input voltage range               |                 |                   | VI               | 0    | -    | VCC     | V                                                    | -               |
| Internal reference voltage        |                 |                   | -                | 1.36 | 1.44 | 1.50    | V                                                    | -               |
| Output delay                      | High-speed mode | Td                | -                | -    | 1.2  | μs      | VCC = 3.0<br>Slew rate of input<br>signal > 50 mV/μs |                 |
|                                   | Low-speed mode  |                   | -                | -    | 5    | μs      |                                                      |                 |
|                                   | Window mode     |                   | -                | -    | 2    | μs      |                                                      |                 |
| Offset voltage*1                  | High-speed mode | -                 | -                | -    | 50   | mV      | -                                                    |                 |
|                                   | Low-speed mode  | -                 | -                | -    | 40   | mV      | -                                                    |                 |
|                                   | Window mode     | -                 | -                | -    | 60   | mV      | -                                                    |                 |
| Operation stabilization wait time |                 |                   | T <sub>cmp</sub> | 100  | -    | -       | μs                                                   | -               |

Note 1. When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to  $2.5 \times V_{CC}/256$ .

Note 2. In window mode, be sure to satisfy the following condition:  $IVREF1 - IVREF0 \geq 0.2$  V.

## 2.14 OPAMP Characteristics

**Table 2.61 OPAMP characteristics**

Conditions: VCC = AVCC0 = 1.8 to 3.6 V (AVCC0 = VCC when VCC &lt; 2.0 V)

| Parameter                          | Symbol  | Conditions                                                                                     | Min             | Typ  | Max         | Unit                   |
|------------------------------------|---------|------------------------------------------------------------------------------------------------|-----------------|------|-------------|------------------------|
| Common mode input range            | Vicm1   | Low-power mode                                                                                 | 0.2             | -    | AVCC0 – 0.5 | V                      |
|                                    | Vicm2   | High-speed mode                                                                                | 0.3             | -    | AVCC0 – 0.6 | V                      |
| Output voltage range               | Vo1     | Low-power mode                                                                                 | 0.1             | -    | AVCC0 – 0.1 | V                      |
|                                    | Vo2     | High-speed mode                                                                                | 0.1             | -    | AVCC0 – 0.1 | V                      |
| Input offset voltage               | Vioff   | 3 $\sigma$                                                                                     | –10             | -    | 10          | mV                     |
| Open gain                          | Av      |                                                                                                | 60              | 120  | -           | dB                     |
| Gain-bandwidth (GB) product        | GBW1    | Low-power mode                                                                                 | -               | 0.04 | -           | MHz                    |
|                                    | GBW2    | High-speed mode                                                                                | -               | 1.7  | -           | MHz                    |
| Phase margin                       | PM      | CL = 20 pF                                                                                     | 50              | -    | -           | deg                    |
| Gain margin                        | GM      | CL = 20 pF                                                                                     | 10              | -    | -           | dB                     |
| Equivalent input noise             | Vnoise1 | f = 1 kHz                                                                                      | -               | 230  | -           | nV/ $\sqrt{\text{Hz}}$ |
|                                    | Vnoise2 | f = 10 kHz                                                                                     |                 | 200  |             | nV/ $\sqrt{\text{Hz}}$ |
|                                    | Vnoise3 | f = 1 kHz                                                                                      | -               | 90   | -           | nV/ $\sqrt{\text{Hz}}$ |
|                                    | Vnoise4 | f = 2 kHz                                                                                      |                 | 70   |             | nV/ $\sqrt{\text{Hz}}$ |
| Power supply reduction ratio       | PSRR    |                                                                                                | -               | 90   | -           | dB                     |
| Common mode signal reduction ratio | CMRR    |                                                                                                | -               | 90   | -           | dB                     |
| Stabilization wait time            | Tstd1   | CL = 20 pF<br>Only operational amplifier is activated *1                                       | Low-power mode  | 650  | -           | $\mu\text{s}$          |
|                                    | Tstd2   |                                                                                                | High-speed mode | 13   | -           | $\mu\text{s}$          |
|                                    | Tstd3   | CL = 20 pF<br>Operational amplifier and reference current circuit are activated simultaneously | Low-power mode  | 650  | -           | $\mu\text{s}$          |
|                                    | Tstd4   |                                                                                                | High-speed mode | 13   | -           | $\mu\text{s}$          |
| Settling time                      | Tset1   | CL = 20 pF                                                                                     | Low-power mode  | -    | 750         | $\mu\text{s}$          |
|                                    | Tset2   |                                                                                                | High-speed mode | -    | 13          | $\mu\text{s}$          |
| Slew rate                          | Tslew1  | CL = 20 pF                                                                                     | Low-power mode  | 0.02 | -           | V/ $\mu\text{s}$       |
|                                    | Tslew2  |                                                                                                | High-speed mode | 1.1  | -           | V/ $\mu\text{s}$       |
| Load current                       | Iload1  | Low power mode                                                                                 | –100            | -    | 100         | $\mu\text{A}$          |
|                                    | Iload2  | High-speed mode                                                                                | –100            | -    | 100         | $\mu\text{A}$          |
| Load capacitance                   | CL      |                                                                                                | -               | -    | 20          | pF                     |

Note 1. When the operational amplifier reference current circuit is activated in advance.

## 2.15 Flash Memory Characteristics

### 2.15.1 Code Flash Memory Characteristics

**Table 2.62 Code flash characteristics (1)**

| Parameter                     | Symbol                               | Min              | Typ      | Max | Unit  | Test conditions        |
|-------------------------------|--------------------------------------|------------------|----------|-----|-------|------------------------|
| Reprogramming/erasure cycle*1 | N <sub>PEC</sub>                     | 1000             | -        | -   | Times | -                      |
| Data hold time                | After 1000 times of N <sub>PEC</sub> | t <sub>DRP</sub> | 20*2, *3 | -   | Year  | T <sub>a</sub> = +85°C |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

**Table 2.63 Code flash characteristics (2)**

High-speed operating mode

Conditions: VCC = 2.7 to 3.6 V

| Parameter                                |        | Symbol            | FCLK = 1 MHz |      |      | FCLK = 32 MHz |      |      | Unit |
|------------------------------------------|--------|-------------------|--------------|------|------|---------------|------|------|------|
|                                          |        |                   | Min          | Typ  | Max  | Min           | Typ  | Max  |      |
| Programming time                         | 8-byte | t <sub>P8</sub>   | -            | 116  | 998  | -             | 54   | 506  | μs   |
| Erasure time                             | 2-KB   | t <sub>E2K</sub>  | -            | 9.03 | 287  | -             | 5.67 | 222  | ms   |
| Blank check time                         | 8-byte | t <sub>BC8</sub>  | -            | -    | 56.8 | -             | -    | 16.6 | μs   |
|                                          | 2-KB   | t <sub>BC2K</sub> | -            | -    | 1899 | -             | -    | 140  | μs   |
| Erase suspended time                     |        | t <sub>SED</sub>  | -            | -    | 22.5 | -             | -    | 10.7 | μs   |
| Startup area switching setting time      |        | t <sub>SAS</sub>  | -            | 21.7 | 585  | -             | 12.1 | 447  | ms   |
| Access window time                       |        | t <sub>AWS</sub>  | -            | 21.7 | 585  | -             | 12.1 | 447  | ms   |
| OCD/serial programmer ID setting time    |        | t <sub>OSIS</sub> | -            | 21.7 | 585  | -             | 12.1 | 447  | ms   |
| Flash memory mode transition wait time 1 |        | t <sub>DIS</sub>  | 2            | -    | -    | 2             | -    | -    | μs   |
| Flash memory mode transition wait time 2 |        | t <sub>MS</sub>   | 5            | -    | -    | 5             | -    | -    | μs   |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 2.64 Code flash characteristics (3)**

Middle-speed operating mode

Conditions: VCC = 1.8 to 3.6 V, Ta = -40 to +85°C

| Parameter                                |        | Symbol            | FCLK = 1 MHz |      |      | FCLK = 8 MHz |      |      | Unit |
|------------------------------------------|--------|-------------------|--------------|------|------|--------------|------|------|------|
|                                          |        |                   | Min          | Typ  | Max  | Min          | Typ  | Max  |      |
| Programming time                         | 8-byte | t <sub>PG</sub>   | -            | 157  | 1411 | -            | 101  | 966  | μs   |
| Erase time                               | 2-KB   | t <sub>E2K</sub>  | -            | 9.10 | 289  | -            | 6.10 | 228  | ms   |
| Blank check time                         | 8-byte | t <sub>BC8</sub>  | -            | -    | 87.7 | -            | -    | 52.5 | μs   |
|                                          | 2-KB   | t <sub>BC2K</sub> | -            | -    | 1930 | -            | -    | 414  | μs   |
| Erase suspended time                     |        | t <sub>SED</sub>  | -            | -    | 32.7 | -            | -    | 21.6 | μs   |
| Startup area switching setting time      |        | t <sub>SAS</sub>  | -            | 22.5 | 592  | -            | 14.0 | 464  | ms   |
| Access window time                       |        | t <sub>AWS</sub>  | -            | 22.5 | 592  | -            | 14.0 | 464  | ms   |
| OCD/serial programmer ID setting time    |        | t <sub>OSIS</sub> | -            | 22.5 | 592  | -            | 14.0 | 464  | ms   |
| Flash memory mode transition wait time 1 |        | t <sub>DIS</sub>  | 2            | -    | -    | 2            | -    | -    | μs   |
| Flash memory mode transition wait time 2 |        | t <sub>MS</sub>   | 720          | -    | -    | 720          | -    | -    | ns   |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

## 2.15.2 Data Flash Memory Characteristics

**Table 2.65 Data flash characteristics (1)**

| Parameter                   |                                          | Symbol            | Min      | Typ     | Max | Unit  | Test conditions |
|-----------------------------|------------------------------------------|-------------------|----------|---------|-----|-------|-----------------|
| Reprogramming/erase cycle*1 |                                          | N <sub>DPEC</sub> | 100000   | 1000000 | -   | Times | -               |
| Data hold time              | After 10000 times of N <sub>DPEC</sub>   | t <sub>DDRP</sub> | 20*2, *3 | -       | -   | Year  | Ta = +85°C      |
|                             | After 100000 times of N <sub>DPEC</sub>  |                   | 5*2, *3  | -       | -   | Year  |                 |
|                             | After 1000000 times of N <sub>DPEC</sub> |                   | -        | 1*2, *3 | -   | Year  | Ta = +25°C      |

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited).

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are obtained from reliability testing.

**Table 2.66 Data flash characteristics (2)**

High-speed operating mode

Conditions: VCC = 2.7 to 3.6 V

| Parameter                     |        | Symbol             | FCLK = 4 MHz |      |      | FCLK = 32 MHz |      |      | Unit |
|-------------------------------|--------|--------------------|--------------|------|------|---------------|------|------|------|
|                               |        |                    | Min          | Typ  | Max  | Min           | Typ  | Max  |      |
| Programming time              | 1-byte | t <sub>DP1</sub>   | -            | 52.4 | 463  | -             | 42.1 | 387  | μs   |
| Erase time                    | 1-KB   | t <sub>DE1K</sub>  | -            | 8.98 | 286  | -             | 6.42 | 237  | ms   |
| Blank check time              | 1-byte | t <sub>DBC1</sub>  | -            | -    | 24.3 | -             | -    | 16.6 | μs   |
|                               | 1-KB   | t <sub>DBC1K</sub> | -            | -    | 1872 | -             | -    | 512  | μs   |
| Suspended time during erasing |        | t <sub>DSER</sub>  | -            | -    | 13.0 | -             | -    | 10.7 | μs   |
| Data flash STOP recovery time |        | t <sub>DSTOP</sub> | 5            | -    | -    | 5             | -    | -    | μs   |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 2.67 Data flash characteristics (3)**

Middle-speed operating mode

Conditions: VCC = 1.8 to 3.6 V, Ta = -40 to +85°C

| Parameter                     |        | Symbol             | FCLK = 4 MHz |      |      | FCLK = 8 MHz |      |      | Unit |
|-------------------------------|--------|--------------------|--------------|------|------|--------------|------|------|------|
|                               |        |                    | Min          | Typ  | Max  | Min          | Typ  | Max  |      |
| Programming time              | 1-byte | t <sub>DP1</sub>   | -            | 94.7 | 886  | -            | 89.3 | 849  | μs   |
| Erase time                    | 1-KB   | t <sub>DE1K</sub>  | -            | 9.59 | 299  | -            | 8.29 | 273  | ms   |
| Blank check time              | 1-byte | t <sub>DBC1</sub>  | -            | -    | 56.2 | -            | -    | 52.5 | μs   |
|                               | 1-KB   | t <sub>DBC1K</sub> | -            | -    | 2.17 | -            | -    | 1.51 | ms   |
| Suspended time during erasing |        | t <sub>DSED</sub>  | -            | -    | 23.0 | -            | -    | 21.7 | μs   |
| Data flash STOP recovery time |        | t <sub>DSTOP</sub> | 720          | -    | -    | 720          | -    | -    | ns   |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

## 2.16 Joint Test Action Group (JTAG)

**Table 2.68 JTAG (debug) characteristics (1)**

Conditions: VCC = 2.4 to 3.6 V

| Parameter                  | Symbol              | Min | Typ | Max | Unit | Test conditions |
|----------------------------|---------------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time       | t <sub>TCKcyc</sub> | 80  | -   | -   | ns   | Figure 2.75     |
| TCK clock high pulse width | t <sub>TCKH</sub>   | 35  | -   | -   | ns   |                 |
| TCK clock low pulse width  | t <sub>TCKL</sub>   | 35  | -   | -   | ns   |                 |
| TCK clock rise time        | t <sub>TCKr</sub>   | -   | -   | 5   | ns   |                 |
| TCK clock fall time        | t <sub>TCKf</sub>   | -   | -   | 5   | ns   |                 |
| TMS setup time             | t <sub>TMSS</sub>   | 16  | -   | -   | ns   | Figure 2.76     |
| TMS hold time              | t <sub>TMSH</sub>   | 16  | -   | -   | ns   |                 |
| TDI setup time             | t <sub>TDIS</sub>   | 16  | -   | -   | ns   |                 |
| TDI hold time              | t <sub>TDIH</sub>   | 16  | -   | -   | ns   |                 |
| TDO data delay time        | t <sub>TDOD</sub>   | -   | -   | 70  | ns   |                 |

**Table 2.69 JTAG (debug) characteristics (2)**

Conditions: VCC = 1.8 to 2.4 V

| Parameter                  | Symbol              | Min | Typ | Max | Unit | Test conditions |
|----------------------------|---------------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time       | t <sub>TCKcyc</sub> | 250 | -   | -   | ns   | Figure 2.75     |
| TCK clock high pulse width | t <sub>TCKH</sub>   | 120 | -   | -   | ns   |                 |
| TCK clock low pulse width  | t <sub>TCKL</sub>   | 120 | -   | -   | ns   |                 |
| TCK clock rise time        | t <sub>TCKr</sub>   | -   | -   | 5   | ns   |                 |
| TCK clock fall time        | t <sub>TCKf</sub>   | -   | -   | 5   | ns   |                 |
| TMS setup time             | t <sub>TMSS</sub>   | 50  | -   | -   | ns   | Figure 2.76     |
| TMS hold time              | t <sub>TMSH</sub>   | 50  | -   | -   | ns   |                 |
| TDI setup time             | t <sub>TDIS</sub>   | 50  | -   | -   | ns   |                 |
| TDI hold time              | t <sub>TDIH</sub>   | 50  | -   | -   | ns   |                 |
| TDO data delay time        | t <sub>TDOD</sub>   | -   | -   | 150 | ns   |                 |

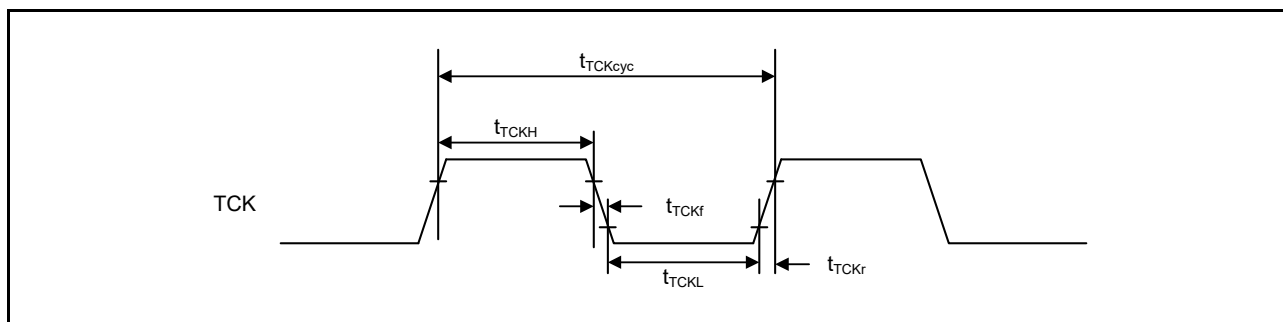


Figure 2.75 JTAG TCK timing

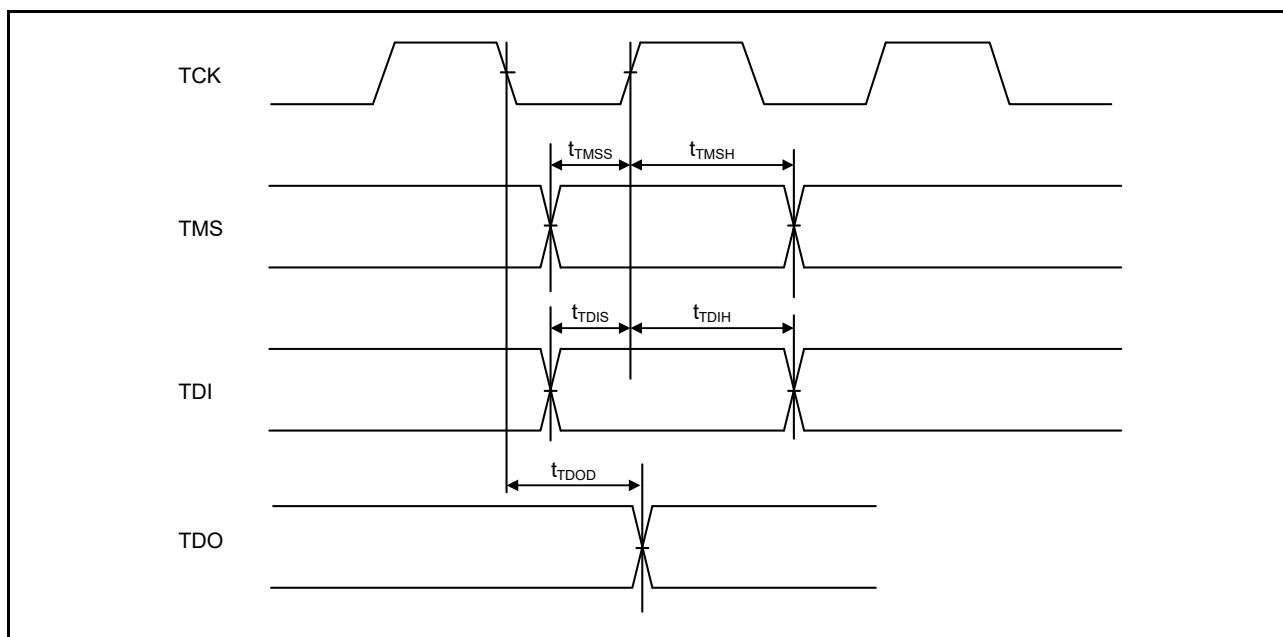


Figure 2.76 JTAG input/output timing

## 2.16.1 Serial Wire Debug (SWD)

**Table 2.70 SWD characteristics (1)**

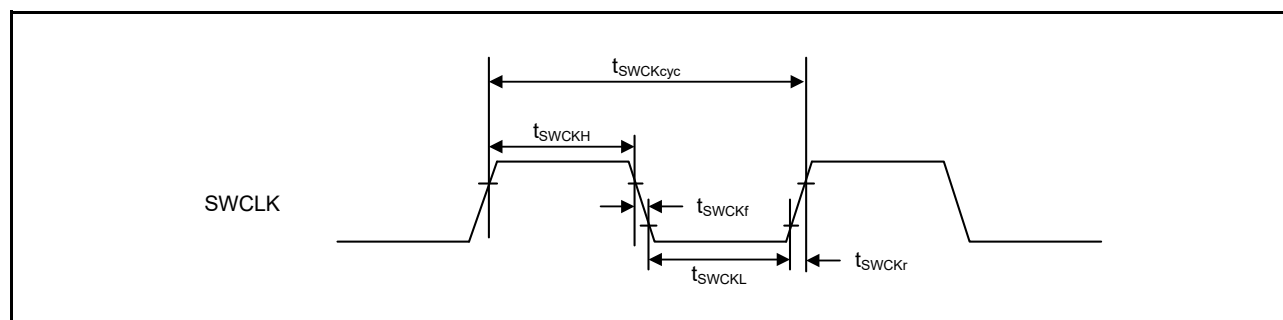
Conditions: VCC = 2.4 to 3.6 V

| Parameter                    | Symbol               | Min | Typ | Max | Unit | Test conditions |
|------------------------------|----------------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time       | $t_{\text{SWCKcyc}}$ | 80  | -   | -   | ns   | Figure 2.77     |
| SWCLK clock high pulse width | $t_{\text{SWCKH}}$   | 35  | -   | -   | ns   |                 |
| SWCLK clock low pulse width  | $t_{\text{SWCKL}}$   | 35  | -   | -   | ns   |                 |
| SWCLK clock rise time        | $t_{\text{SWCKr}}$   | -   | -   | 5   | ns   |                 |
| SWCLK clock fall time        | $t_{\text{SWCKf}}$   | -   | -   | 5   | ns   |                 |
| SWDIO setup time             | $t_{\text{SWDS}}$    | 16  | -   | -   | ns   | Figure 2.78     |
| SWDIO hold time              | $t_{\text{SWDH}}$    | 16  | -   | -   | ns   |                 |
| SWDIO data delay time        | $t_{\text{SWDD}}$    | 2   | -   | 70  | ns   |                 |

**Table 2.71 SWD characteristics (2)**

Conditions: VCC = 1.8 to 2.4 V

| Parameter                    | Symbol               | Min | Typ | Max | Unit | Test conditions |
|------------------------------|----------------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time       | $t_{\text{SWCKcyc}}$ | 250 | -   | -   | ns   | Figure 2.77     |
| SWCLK clock high pulse width | $t_{\text{SWCKH}}$   | 120 | -   | -   | ns   |                 |
| SWCLK clock low pulse width  | $t_{\text{SWCKL}}$   | 120 | -   | -   | ns   |                 |
| SWCLK clock rise time        | $t_{\text{SWCKr}}$   | -   | -   | 5   | ns   |                 |
| SWCLK clock fall time        | $t_{\text{SWCKf}}$   | -   | -   | 5   | ns   |                 |
| SWDIO setup time             | $t_{\text{SWDS}}$    | 50  | -   | -   | ns   | Figure 2.78     |
| SWDIO hold time              | $t_{\text{SWDH}}$    | 50  | -   | -   | ns   |                 |
| SWDIO data delay time        | $t_{\text{SWDD}}$    | 2   | -   | 150 | ns   |                 |

**Figure 2.77 SWD SWCLK timing**

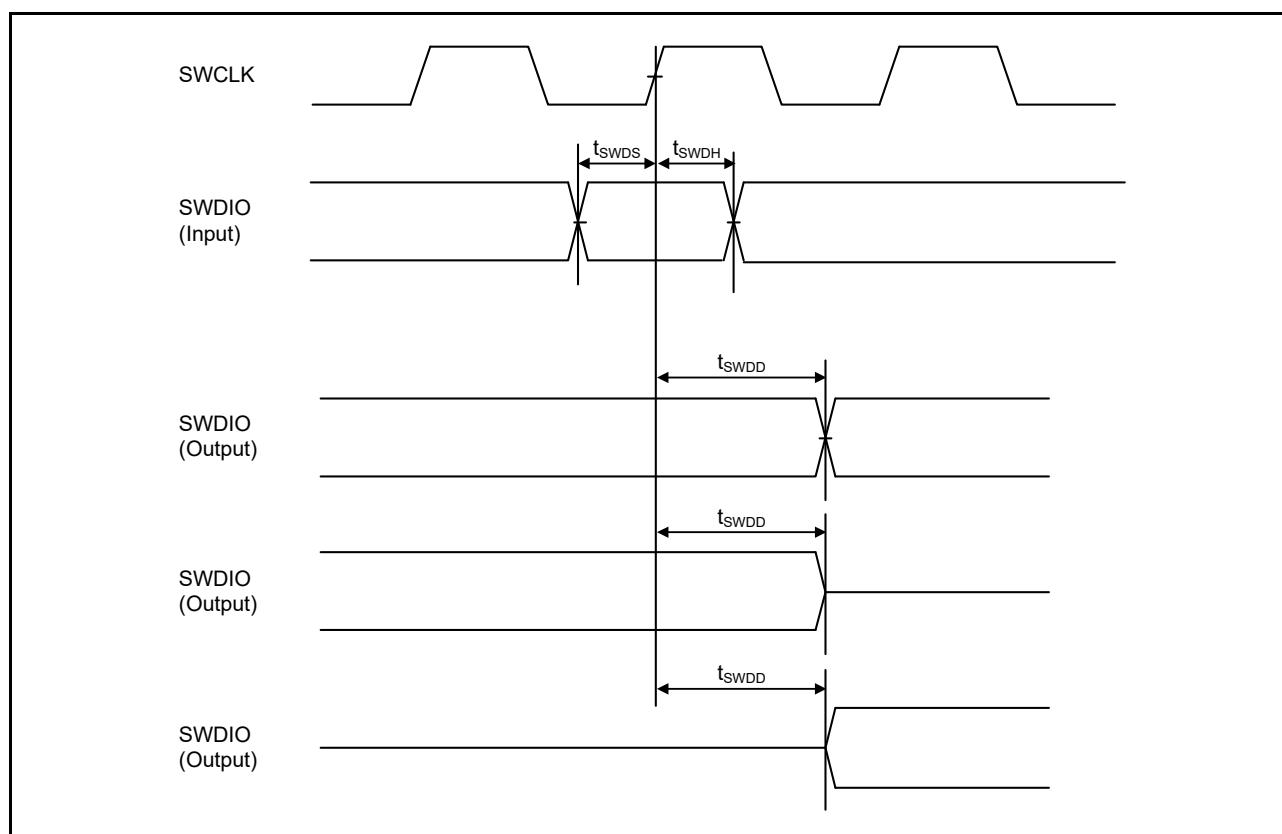


Figure 2.78 SWD input/output timing

## 2.17 BLE Characteristics

### 2.17.1 Transmission Characteristics

Table 2.72 Transmission Characteristics

Conditions:  $V_{CC} = V_{CC\_RF} = AV_{CC\_RF} = 3.3\text{ V}$ ,  $V_{SS} = V_{SS\_RF} = 0\text{ V}$ ,  $T_a = +25^\circ\text{C}$

| Parameter                        | Symbol            | Min  | Typ | Max  | Unit | Test conditions   |
|----------------------------------|-------------------|------|-----|------|------|-------------------|
| Range of frequency               | $RF_{CF}$         | 2402 | -   | 2480 | MHz  |                   |
| Data rate                        | $RF_{DATA\_2M}$   | -    | 2   | -    | Mbps |                   |
|                                  | $RF_{DATA\_1M}$   | -    | 1   | -    | Mbps |                   |
|                                  | $RF_{DATA\_500k}$ | -    | 500 | -    | kbps |                   |
|                                  | $RF_{DATA\_125k}$ | -    | 125 | -    | kbps |                   |
| Maximum transmitted output power | $RF_{POWER}$      | -    | 0   | 2    | dBm  | 0 dBm output mode |
|                                  |                   | -    | 4   | 6    | dBm  | 4 dBm output mode |
| Output frequency error           | $RF_{TXFERR}$     | -10  | -   | 10   | ppm  | *1                |

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

## 2.17.2 Reception Characteristics (2 Mbps)

**Table 2.73 Reception Characteristics**Conditions: VCC = VCC\_RF = AVCC\_RF = 3.3 V, VSS = VSS\_RF = 0 V, T<sub>a</sub> = +25°C

| Item                             | Symbol                 | Min. | Typ. | Max. | Unit | Test Conditions                    |
|----------------------------------|------------------------|------|------|------|------|------------------------------------|
| Input frequency                  | RF <sub>RXFIN_2M</sub> | 2402 | —    | 2480 | MHz  |                                    |
| Maximum input level              | RF <sub>LEVL_2M</sub>  | -10  | 4    | —    | dBm  | *1                                 |
| Receiver sensitivity             | RF <sub>STY_2M</sub>   | —    | -92  | —    | dBm  | *1                                 |
| Secondary emission strength      | RF <sub>RXSP_2M</sub>  | —    | -72  | -57  | dBm  | 30 MHz to 1 GHz                    |
|                                  |                        | —    | -54  | -47  | dBm  | 1 GHz to 12 GHz                    |
| Co-channel rejection ratio       | RF <sub>CCR_2M</sub>   | —    | -8   | —    | dB   | Prf = -67 dBm*1                    |
| Adjacent channel rejection ratio | RF <sub>ADCR_2M</sub>  | —    | 2    | —    | dB   | Prf = -67 dBm*1 ±2 MHz             |
|                                  |                        | —    | 35   | —    | dB   | ±4 MHz                             |
|                                  |                        | —    | 39   | —    | dB   | ±6 MHz                             |
| Blocking                         | RF <sub>BLK_2M</sub>   | —    | -1   | —    | dBm  | Prf = -67 dBm*1 30 MHz to 2000 MHz |
|                                  |                        | —    | -25  | —    | dBm  | 2000 MHz to 2399 MHz               |
|                                  |                        | —    | -21  | —    | dBm  | 2484 MHz to 3000 MHz               |
|                                  |                        | —    | -10  | —    | dBm  | > 3000 MHz                         |
| Allowable frequency deviation*2  | RF <sub>RXFER_2M</sub> | -120 | —    | 120  | ppm  | *1                                 |
| RSSI accuracy                    | RF <sub>RSSIS_2M</sub> | —    | ±4   | —    | dB   | -70 dBm ≤ Prf ≤ -10 dBm            |

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER ≤ 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

## 2.17.3 Reception Characteristics (1 Mbps)

**Table 2.74 Reception Characteristics**Conditions: VCC = VCC\_RF = AVCC\_RF = 3.3 V, VSS = VSS\_RF = 0 V, T<sub>a</sub> = +25°C

| Item                             | Symbol                 | Min. | Typ. | Max. | Unit | Test Conditions                 |
|----------------------------------|------------------------|------|------|------|------|---------------------------------|
| Input frequency                  | RF <sub>RXFIN_1M</sub> | 2402 | —    | 2480 | MHz  |                                 |
| Maximum input level              | RF <sub>LEVL_1M</sub>  | -10  | 4    | —    | dBm  | *1                              |
| Receiver sensitivity             | RF <sub>STY_1M</sub>   | —    | -95  | —    | dBm  | *1                              |
| Secondary emission strength      | RF <sub>RXSP_1M</sub>  | —    | -72  | -57  | dBm  | 30MHz to 1GHz                   |
|                                  |                        | —    | -54  | -47  | dBm  | 1GHz to 12GHz                   |
| Co-channel rejection ratio       | RF <sub>CCR_1M</sub>   | —    | -7   | —    | dB   | Prf = -67dBm*1                  |
| Adjacent channel rejection ratio | RF <sub>ADCR_1M</sub>  | —    | -1   | —    | dB   | Prf = -67dBm*1 ±1MHz            |
|                                  |                        | —    | 34   | —    | dB   | ±2MHz                           |
|                                  |                        | —    | 35   | —    | dB   | ±3MHz                           |
| Blocking                         | RF <sub>BLK_1M</sub>   | —    | 0    | —    | dBm  | Prf = -67dBm*1 30MHz to 2000MHz |
|                                  |                        | —    | -24  | —    | dBm  | 2000MHz to 2399MHz              |
|                                  |                        | —    | -20  | —    | dBm  | 2484MHz to 3000MHz              |
|                                  |                        | —    | -4   | —    | dBm  | > 3000MHz                       |
| Allowable frequency deviation*2  | RF <sub>RXFER_1M</sub> | -120 | —    | 120  | ppm  | *1                              |
| RSSI accuracy                    | RF <sub>RSSIS_1M</sub> | —    | ±4   | —    | dB   | -70dBm ≤ Prf ≤ -10dBm           |

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER ≤ 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

## 2.17.4 Reception Characteristics (500 kbps)

**Table 2.75 Reception Characteristics**Conditions: VCC = VCC\_RF = AVCC\_RF = 3.3 V, VSS = VSS\_RF = 0 V, T<sub>a</sub> = +25°C

| Item                             | Symbol                   | Min. | Typ. | Max. | Unit | Test Conditions                 |
|----------------------------------|--------------------------|------|------|------|------|---------------------------------|
| Input frequency                  | RF <sub>RXFIN_500k</sub> | 2402 | —    | 2480 | MHz  |                                 |
| Maximum input level              | RF <sub>LEVL_500k</sub>  | -10  | 4    | —    | dBm  | *1                              |
| Receiver sensitivity             | RF <sub>STY_500k</sub>   | —    | -100 | —    | dBm  | *1                              |
| Secondary emission strength      | RF <sub>RXSP_500k</sub>  | —    | -72  | -57  | dBm  | 30MHz to 1GHz                   |
|                                  |                          | —    | -54  | -47  | dBm  | 1GHz to 12GHz                   |
| Co-channel rejection ratio       | RF <sub>CCR_500k</sub>   | —    | -4   | —    | dB   | Prf = -72dBm*1                  |
| Adjacent channel rejection ratio | RF <sub>ADCR_500k</sub>  | —    | 6    | —    | dB   | Prf = -72dBm*1 ±1MHz            |
|                                  |                          | —    | 36   | —    | dB   | ±2MHz                           |
|                                  |                          | —    | 42   | —    | dB   | ±3MHz                           |
| Blocking                         | RF <sub>BLK_500k</sub>   | —    | 0    | —    | dBm  | Prf = -72dBm*1 30MHz to 2000MHz |
|                                  |                          | —    | -23  | —    | dBm  | 2000MHz to 2399MHz              |
|                                  |                          | —    | -20  | —    | dBm  | 2484MHz to 3000MHz              |
|                                  |                          | —    | -7   | —    | dBm  | > 3000MHz                       |
| Allowable frequency deviation*2  | RF <sub>RXFER_500k</sub> | -120 | —    | 120  | ppm  | *1                              |
| RSSI accuracy                    | RF <sub>RSSIS_500k</sub> | —    | ±4   | —    | dB   | -70dBm ≤ Prf ≤ -10dBm           |

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER ≤ 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

## 2.17.5 Reception Characteristics (125 kbps)

**Table 2.76 Reception Characteristics**Conditions: VCC = VCC\_RF = AVCC\_RF = 3.3 V, VSS = VSS\_RF = 0 V, T<sub>a</sub> = +25°C

| Item                             | Symbol                   | Min. | Typ. | Max. | Unit | Test Conditions                                 |
|----------------------------------|--------------------------|------|------|------|------|-------------------------------------------------|
| Input frequency                  | RF <sub>RXFIN_125k</sub> | 2402 | —    | 2480 | MHz  |                                                 |
| Maximum input level              | RF <sub>LEVL_125k</sub>  | -10  | 4    | —    | dBm  | *1                                              |
| Receiver sensitivity             | RF <sub>STY_125k</sub>   | —    | -105 | —    | dBm  | *1                                              |
| Secondary emission strength      | RF <sub>RXSP_125k</sub>  | —    | -72  | -57  | dBm  | 30 MHz to 1 GHz                                 |
|                                  |                          | —    | -54  | -47  | dBm  | 1 GHz to 12 GHz                                 |
| Co-channel rejection ratio       | RF <sub>CCR_125k</sub>   | —    | -2   | —    | dB   | Prf = -79 dBm*1                                 |
| Adjacent channel rejection ratio | RF <sub>ADCR_125k</sub>  | —    | 12   | —    | dB   | Prf = -79 dBm*1 ±1 MHz                          |
|                                  |                          | —    | 39   | —    | dB   | ±2 MHz                                          |
|                                  |                          | —    | 45   | —    | dB   | ±3 MHz                                          |
| Blocking                         | RF <sub>BLK_125k</sub>   | —    | 0    | —    | dBm  | Prf = -79 dBm*1 30 MHz to 2000 MHz              |
|                                  |                          | —    | -23  | —    | dBm  | 2000 MHz to 2399 MHz                            |
|                                  |                          | —    | -20  | —    | dBm  | 2484 MHz to 3000 MHz                            |
|                                  |                          | —    | -1   | —    | dBm  | > 3000MHz                                       |
| Allowable frequency deviation*2  | RF <sub>RXFER_125k</sub> | -120 | —    | 120  | ppm  | *1                                              |
| RSSI accuracy                    | RF <sub>RSSIS_125k</sub> | —    | ±4   | —    | dB   | T <sub>a</sub> = +25°C, -70 dBm ≤ Prf ≤ -10 dBm |

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER ≤ 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

## Appendix 1. Package Dimensions

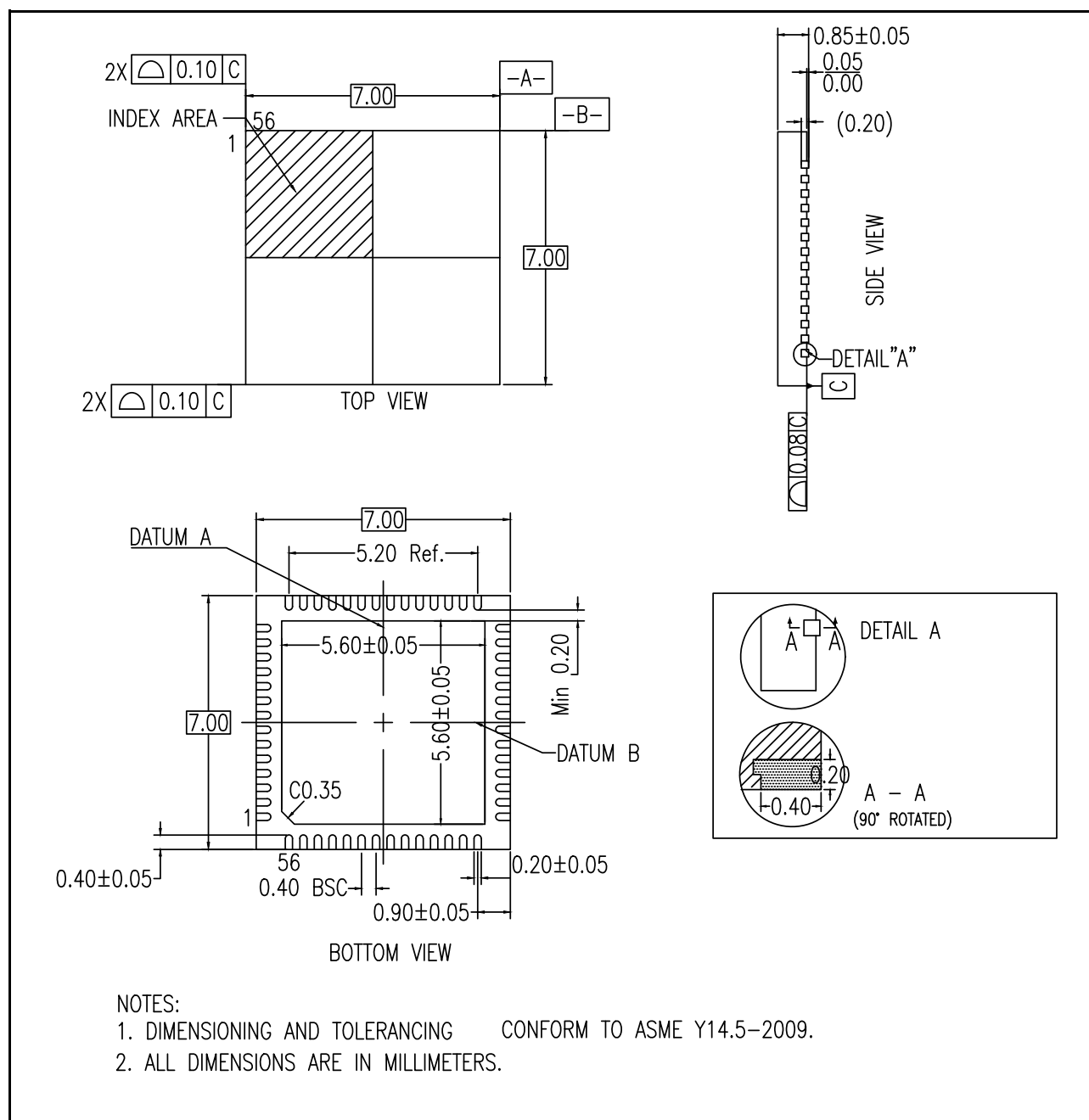
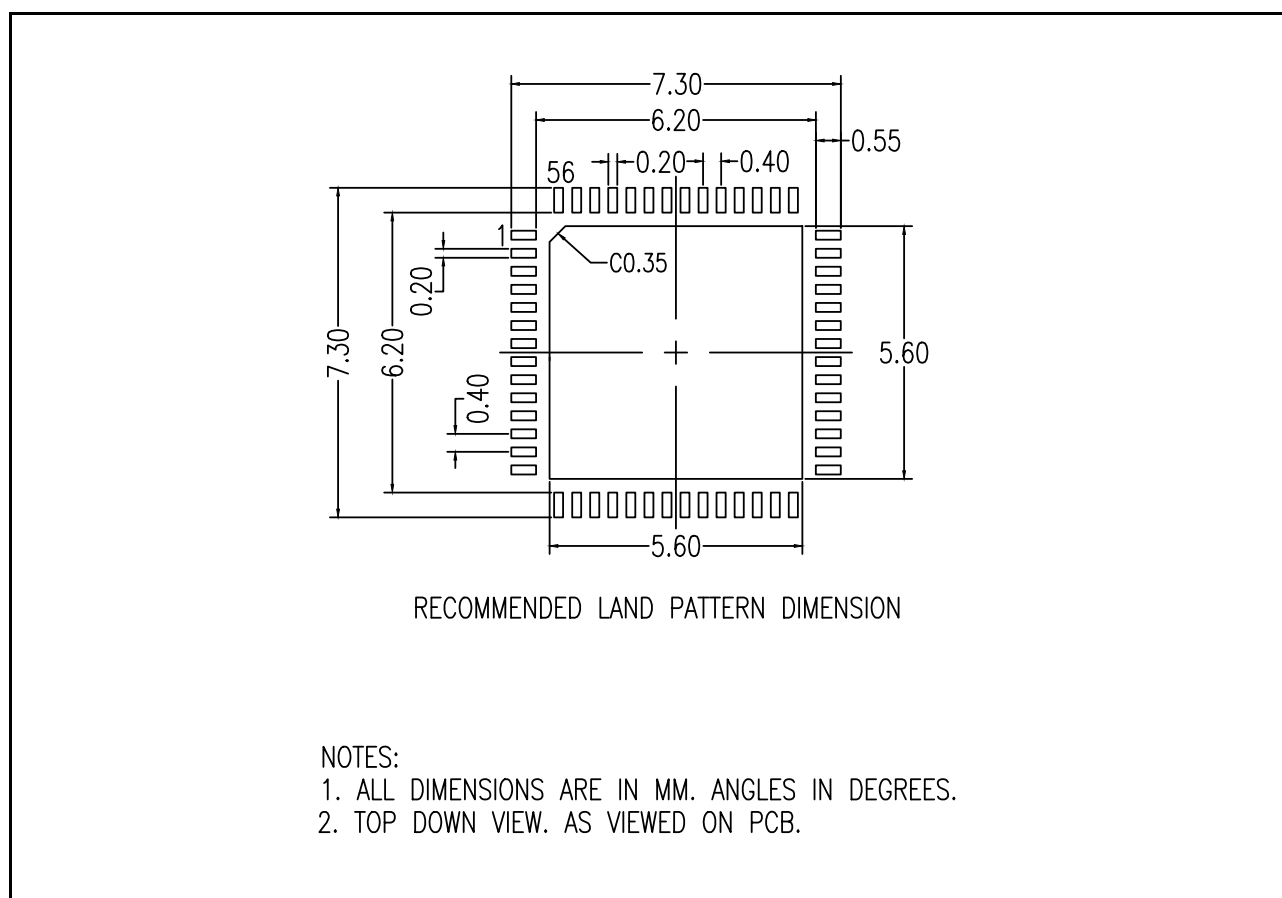


Figure 1.1 QFN 56-pin



**Figure 1.2      Land Pattern**

|                  |                       |
|------------------|-----------------------|
| Revision History | RA4W1 Group Datasheet |
|------------------|-----------------------|

| Rev. | Date         | Summary       |
|------|--------------|---------------|
| 1.00 | Mar 31, 2020 | First release |

## Proprietary Notice

All text, graphics, photographs, trademarks, logos, artwork and computer code, collectively known as content, contained in this document is owned, controlled or licensed by or to Renesas, and is protected by trade dress, copyright, patent and trademark laws, and other intellectual property rights and unfair competition laws. Except as expressly provided herein, no part of this document or content may be copied, reproduced, republished, posted, publicly displayed, encoded, translated, transmitted or distributed in any other medium for publication or distribution or for any commercial enterprise, without prior written consent from Renesas.

Arm® and Cortex® are registered trademarks of Arm Limited. CoreSight™ is a trademark of Arm Limited.

CoreMark® is a registered trademark of the Embedded Microprocessor Benchmark Consortium.

Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

Bluetooth® is a trademark of the Bluetooth SIG, Inc.

SuperFlash® is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Other brands and names mentioned in this document may be the trademarks or registered trademarks of their respective holders.

---

RA4W1 Group Datasheet

Publication Date: Rev.1.00 Mar 31, 2020

Published by: Renesas Electronics Corporation

---

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
  3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
  6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
  11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



### SALES OFFICES

### Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "http://www.renesas.com/" for the latest and detailed information.

**Renesas Electronics Corporation**  
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

**Renesas Electronics America Inc.**  
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia  
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338

# Renesas RA Family RA4W1 Group