Datasheet

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Renesas RA6M1 Group

Datasheet

32-bit MCU

Renesas Advanced (RA) Family

Renesas RA6 Series

Renesas Electronics
www.renesas.com

Rev.1.00 Oct 2019

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瑞萨电子高级(RA)系列32位MCU

Renesas RA6 Series

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Rev.1.00 Oct 2019

Leading performance 120-MHz Arm® Cortex®-M4 core, 512-KB code flash memory, 256-KB SRAM, Capacitive Touch Sensing Unit, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

■ Memory
- 512-KB code flash memory (40 MHz zero wait states)
- 8-KB data flash memory (125,000 erase/write cycles)
- 256-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver
- Serial Communications Interface (SCI) with FIFO × 7
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN) × 2
- Serial Sound Interface Enhanced (SSIE)
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8-bit bus space

■ Analog
- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 5
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Code Correction (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General-Purpose I/O Ports
- Up to 76 input/output pins
  - Up to 9 CMOS input
  - Up to 67 CMOS input/output
    - Up to 14 input/output 5 V tolerant
    - Up to 13 high current (20 mA)

■ Operating Voltage
- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 100-pin LGA (7 mm × 7 mm, 0.65 mm pitch)
- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)

RA6M1 Group
Datasheet

性能领先的120-MHzArm®Cortex®-M4内核、512-KB代码闪存、256-KBSRAM、电容式触摸感应单元、USB2.0全速、SDHI、QuadSPI、安全和安全功能以及高级模拟。

Features

■带浮点单元(FPU)的ArmCortex-M4内核带DSP指令集的Armv7E-M架构最大工作频率：120MHz支持4GB地址空间片上调试系统：JTAG、SWD和ETM　边界扫描和Arm内存保护单元(ArmMPU)

■ Memory
512KB代码闪存（40MHz零等待状态）　8KB数据闪存（125 000个擦除写入周期）　256KBSRAM　闪存(FCACHE)　内存保护单元(MPU)　内存镜像功能(MMF)　128位唯一ID

■ Connectivity
USB2.0全速(USBFS)模块片上收发器　带FIFO的串行通信接口(SCI)×7　串行外设接口(SPI)×2　I2C总线接口(IIC)×2　CAN模块(CAN)×2　增强型串行声音接口(SSIE)　SDMMC主机接口(SDHI)×2　四路串行外设接口(QSPI)　IrDA接口　采样率转换器(SRC)　外部地址空间8位总线空间

■ Analog
12位模数转换器(ADC12)，每个具有3个采样和保持电路×2　12位模数转换器(DAC12)×2　高速模拟比较器(ACMPHS)×6　可编程增益放大器(PGA)×6　温度传感器(TSN)

■ Timers
通用PWM定时器32位增强型高分辨率(GPT32EH)×4　通用PWM定时器32位增强型(GPT32E)×4　通用PWM定时器32位(GPT32)×5　异步通用定时器(AGT)×2　看门狗定时器(WDT)

■ Safety
SRAM中的错误代码校正(ECC)　SRAM奇偶校验错误检查　闪存区域保护　ADC自诊断功能　时钟频率精度测量电路(CAC)　循环冗余校验(CRC)计算器　数据操作电路(DOC)　端口GPT(POEG)的输出使能　独立看门狗定时器(IWDT)　GPIO回读电平检测　寄存器写保护　主振荡器停止检测　非法内存访问

■系统和电源管理　低功耗模式　支持日历和VBATT的实时时钟(RTC)　事件链接控制器(ELC)　DMA控制器(DMAC)×8　数据传输控制器(DTC)　按键中断功能(KINT)　上电复位　具有电压设置的低电压检测(LVD)

■安全和加密　AES128192256　3DESARC4　SHA1SHA224SHA256MD5　GHASH　RSADSAECC　真随机数生成器(TRNG)

■人机界面(HMI)　电容式触摸传感单元(CTSU)

■多个时钟源
主时钟振荡器(MOSC)(8至24MHz)　副时钟振荡器(SOSC)(32.768kHz)　高速片上振荡器(HOCO)(161820MHz)　中速片上振荡器(MOCO)(8MHz)　低速片上振荡器(LOCO)(32.768kHz)　IWDT专用片上振荡器(15kHz)　HOCOMOCOLOCO的时钟微调功能　时钟输出支持

■通用IO端口　多达76个输入输出引脚多达9个CMOS输入多达67个CMOS输入输出多达14个输入输出5V耐受多达13个大电流(20mA)

■工作电压　VCC：2.7至3.6V

■工作温度和封装　Ta=−40°C至+85°C

100引脚LGA（7mm×7mm，0.65mm间距）　Ta=−40°C至+105°C
- 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
- 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
- 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz with the following features:

- 512-KB code flash memory
- 256-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- USBFS
- SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Analog peripherals.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 120 MHz • Arm Cortex-M4 core: - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): - Armv7 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	512-KB code flash memory. See section 50, Flash Memory in User's Manual.
Data flash memory	8-KB data flash memory. See section 50, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 provides error correction capability using ECC. Parity check is performed for other areas. See section 48, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 49, Standby SRAM in User's Manual.

1. Overview

MCU集成了多个系列软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外设，以促进设计可扩展性和基于平台的高效产品开发。

该系列中的MCU包含一个运行频率高达120MHz的高性能ArmCortex®-M4内核，具有以下特性：

- 512-KB代码闪存
- 256-KB SRAM
- 电容式触控感应单元(CTSU)
- USBFS
- SDMMC主机接口
- 四路串行外设接口(QSPI)
- 安全和安全功能
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- 模拟外设。

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M4内核	最大工作频率：高达120MHz ArmCortex-M4内核：修订版：r0p1-01rel0Armv7E-M架构配置文件符合ANSIIEEEStd754-2008的单精度浮点单元。 Arm内存保护单元（ArmMPU）： Armv7ProtectedMemorySystemArchitecture8保护区域。 SysTick计时器： 由SYSTICCLK(LOCO)或ICLK驱动。

Table 1.2 Memory

Feature	功能说明
代码闪存	512KB代码闪存。请参阅用户手册中的第50节，闪存。
数据闪存	8KB数据闪存。请参阅用户手册中的第50节，闪存。
内存镜像功能(MMF)	内存镜像功能(MMF)可配置为将代码闪存中的目标应用程序映像加载地址镜像到23位未使用的内存空间（内存镜像空间地址）中的应用程序映像链接地址。您的应用程序代码已开发并链接到从该MMF目标地址运行。您的应用程序代码不需要知道它存储在代码闪存中的加载位置。请参阅用户手册中的第5节，内存镜像功能(MMF)。
Option-setting memory	选项设置存储器确定复位后MCU的状态。见第7节， 用户手册中的选项设置内存。
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。SRAM0的前32KB使用ECC提供纠错能力。对其他区域执行奇偶校验。请参阅用户手册中的第48节SRAM。
Standby SRAM	可以在深度软件待机模式下保留数据的片上SRAM。见第49节，待机 用户手册中的SRAM。

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI or USB boot mode. See section 3, Operating Modes in User's Manual.
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Independent watchdog timer reset • Watchdog timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IDWT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.

RA6M1 Group 1. Overview

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种工作模式： 单芯片模式 SCI或USB启动模式。请参阅用户手册中的第3节操作模式。
Resets	14次复位： RES引脚复位 上电复位 电压监控器0复位 电压监控器1复位 电压监控器2复位 独立看门狗定时器复位 看门狗定时器复位 深度软件待机复位 SRAM奇偶校验错误复位 SRAMECC错误复位 总线主MPU错误复位 总线从属MPU错误复位 堆栈指针错误复位 软件复位。请参阅用户手册中的第6节，重置。
低电压检测(LVD)	低电压检测(LVD)功能监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。请参阅用户手册中的第8节，低电压检测(LVD)。
Clocks	主时钟振荡器(MOSC) 子时钟振荡器(SOSC) 高速片上振荡器(HOCO) 中速片上振荡器(MOCO) 低速片上振荡器(LOCO) PLL频率合成器 IDWT专用的片上振荡器 时钟输出支持。请参阅用户手册中的第9节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在用作测量基准的时钟（测量基准时钟）生成的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据是否脉冲数在允许范围内。当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时，将产生中断请求。请参阅用户手册中的第10节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到NVICDTC模块和DMAC模块。ICU还控制NMI中断。请参阅用户手册中的第14节，中断控制器单元(ICU)。
按键中断功能(KINT)	通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚输入上升沿或下降沿，可以生成按键中断。请参阅用户手册中的第21节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，例如设置时钟分频器、控制EBCLK输出、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅用户手册中的第11节，低功耗模式。
电池备份功能	提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、备份存储器以及VCC和VBATT之间的切换。请参阅用户手册中的第12节"电池备份功能"。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。请参见用户手册中的第13节，寄存器写保护。
内存保护单元(MPU)	提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能用于内存保护。请参阅用户手册中的第16节，内存保护单元(MPU)。

Table 1.3 System (2 of 2)

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.6 External bus interface

Feature	Functional description
External buses	• CS area (EXBIU): Connected to the external devices (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 13 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General-Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual.

Table 1.3 系统(2之2)

Feature	功能说明
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，下溢可能会产生不可屏蔽的中断或中断。可以设置一个允许刷新周期来刷新计数器，作为检测系统何时失控的条件。请参阅用户手册中的第27节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或定时器下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以在复位、下溢或刷新错误时自动触发，或者通过刷新寄存器中的计数值来触发。请参阅用户手册中的第28节，独立看门狗定时器(IWDT)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的中断请求作为事件信号，将它们连接到不同的模块，实现模块之间的直接交互，无需CPU干预。请参阅用户手册中的第19节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅用户手册中的第18节，数据传输控制器(DTC)。
DMA Controller (DMAC)	提供了一个8通道DMA控制器(DMAC)模块，用于在没有CPU的情况下传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参阅用户手册中的第17节，DMA控制器(DMAC)。

Table 1.6 外部总线接口

Feature	功能说明
外部总线	CS区（EXBIU）：连接到外部设备（外部存储器接口） QSPI区（EXBIUT2）：连接到QSPI（外部设备接口）。

Table 1.7 计时器(1of2)

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有13个通道的32位定时器。PWM波形可以通过控制递增计数器、递减计数器或递增递减计数器来生成。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参阅用户手册中的第23节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	使用PortOutputEnableforGPT(POEG)功能将通用PWM定时器(GPT)输出引脚置于输出禁用状态。请参阅用户手册中的第22节，GPT(POEG)的端口输出启用。
Asynchronous General-Purpose Timer (AGT)	异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参阅用户手册中的第25节，异步通用定时器(AGT)。

Table 1.7 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can section 30, Serial Communications Interface (SCI)be configured independently using an on-chip baud rate generator. See in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 31, IrDA Interface in User's Manual.
I2C bus interface (IIC)	The 2-channel I2C bus interface (IIC) conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions. See section 32, I2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 34, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I2S (Inter-Integrated Sound) 2ch, 4ch, 6ch, 8ch, Word Select (WS) Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 37, Serial Sound Interface Enhanced (SSIE) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 35, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 33, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed Module (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 29, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.7 计时器（2个中的2个）

Feature	功能说明
实时时钟(RTC)	实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，由寄存器设置控制。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。 二进制计数模式可用于公历（西方）以外的日历。 请参阅用户手册中的第26节，实时时钟(RTC)。

Table 1.8 通信接口（2个中的1个）

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)可配置为五个异步和同步串行接口： 异步接口（UART和异步通信接口适配器(ACIA)） 8位时钟同步接口 简单IIC（仅限主机） 简单SPI 智能卡接口。智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。每个SCI都有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度（第30节，串行通信接口(SCI)）。参见用户手册。
IrDA Interface (IrDA)	IrDA接口与基于IrDA（InfraredDataAssociation）标准1.0的SCI1协同发送和接收IrDA数据通信波形。请参阅用户手册中的第31节，IrDA接口。
I2C总线接口(IIC)	2通道I2C总线接口(IIC)符合并提供NXPI2C（内部集成电路）总线接口功能的子集。请参阅用户手册中的第32节，I2C总线接口(IIC)。
串行外设接口(SPI)	两个独立的串行外围接口(SPI)通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。请参阅用户手册中的第34节，串行外设接口(SPI)。
串行声音接口增强(SSIE)	串行声音接口增强(SSIE)外设提供与数字音频设备接口的功能，用于通过串行总线传输I2S（内部集成声音）2ch、4ch、6ch、8ch、字选择(WS)继续单声道TDM音频数据.SSIE支持高达50MHz的音频时钟频率，并可作为从属或主接收器、发送器或收发器运行，以适应各种应用。SSIE在接收器和发送器中包含32级FIFO缓冲区，并支持中断和DMA驱动的数据接收和发送。请参阅用户手册中的第37节，增强的串行声音接口(SSIE)。
四路串行外设接口(QSPI)	QuadSerialPeripheralInterface(QSPI)是一种存储器控制器，用于连接串行 具有SPI兼容接口的ROM（非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM）。请参阅用户手册中的第35节，四通道串行外设接口(QSPI)。
控制器局域网(CAN)模块	控制器局域网(CAN)模块提供了在电磁噪声应用中使用基于消息的协议在多个从机和主机之间接收和传输数据的功能。CAN模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。请参阅用户手册中的第33节，控制器局域网(CAN)模块。
USB2.0全速模块(USBFS)模块	USB2.0全速(USBFS)模块可以作为主机控制器或设备控制器运行。该模块支持全速和低速（仅限主机控制器）传输，如 通用串行总线规范2.0。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据您的系统为管道1到9分配任何端点编号。请参阅用户手册中的第29节，USB2.0全速模块(USBFS)。

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit and 4-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 39, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	Up to two successive approximation 12-bit A/D Converters (ADC12) are provided. In unit 0, up to 11 analog input channels are selectable. In unit 1, up to eight analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 42, 12-Bit A/D Converter (ADC12) in User's Manual.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 43, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 44, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 45, High-Speed Analog Comparator (ACMPHS) in User's Manual.

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 46, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.11 Data processing (1 of 2)

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 36, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 47, Data Operation Circuit (DOC) in User's Manual.

Table 1.8 通信接口（2个中的2个）

Feature	功能说明
SDMMC主机接口(SDHI)	SDHI和多媒体卡(MMC)接口模块提供将各种外部存储卡连接到MCU所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。MMC接口支持提供eMMC4.51(JEDEC)的1位和4位MMC总线 标准JESD84-B451)设备访问。该接口还提供向后兼容性并支持高速SDR传输模式。请参阅用户手册中的第39节，SDMMC主机接口(SDHI)。

Table 1.9 Analog

Feature	功能说明
12-bit A/D Converter (ADC12)	最多提供两个逐次逼近型12位模数转换器(ADC12)。在单元0中，最多可选择11个模拟输入通道。在单元1中，可以选择多达8个模拟输入通道、温度传感器输出和内部参考电压进行转换。AD转换精度可从12位、10位和8位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的折衷。请参阅用户手册中的第42节，12位AD转换器(ADC12)。
12-bit D/A Converter (DAC12)	一个12位DA转换器(DAC12)转换数据并包括一个输出放大器。请参阅用户手册中的第43节，12位DA转换器(DAC12)。
温度传感器(TSN)	片上温度传感器(TSN)可以确定和监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压呈线性关系。输出电压提供给ADC12进行转换，也可供最终应用使用。请参阅用户手册中的第44节，温度传感器(TSN)。
高速模拟比较器(ACMPHS)	高速模拟比较器(ACMPHS)将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及带有或不带有内部PGA的外部源提供给比较器。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。请参阅用户手册中的第45节，高速模拟比较器(ACMPHS)。

Table 1.10 人机界面

Feature	功能说明
电容式触控感应单元(CTSU)	电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。请参阅用户手册中的第46节，电容式触摸传感单元(CTSU)。

Table 1.11 数据处理(1of2)

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种生成CRC的多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅用户手册中的第36节，循环冗余校验(CRC)计算器。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。见第47节， 用户手册中的数据操作电路(DOC)。

Table 1.11 Data processing (2 of 2)

Feature	Functional description
Sampling Rate Converter (SRC)	The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 38, Sampling Rate Converter (SRC) in User's Manual.

Table 1.12 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and ECC. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5 - 128-bit unique ID.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

RA6M1 Group 1. Overview

Table 1.11 数据处理（2之2）

Feature	功能说明
采样率转换器(SRC)	采样率转换器(SRC)转换各种音频解码器（如WMA、MP3和AAC）产生的数据的采样率。支持16位立体声和单声道数据。请参阅用户手册中的第38节，采样率转换器(SRC)。

Table 1.12 Security

Feature	功能说明
安全加密引擎7(SCE7)	• Security algorithms: 对称算法：AES、3DES和ARC4非对称算法：RSA、DSA和ECC。 其他支持功能： TRNG（真随机数生成器）哈希值生成：SHA1、SHA224、SHA256、GHASH和MD5128位唯一ID。

1.2 框图

图1.1显示了MCU超集的框图，该组中的一些单独的设备具有功能的子集。

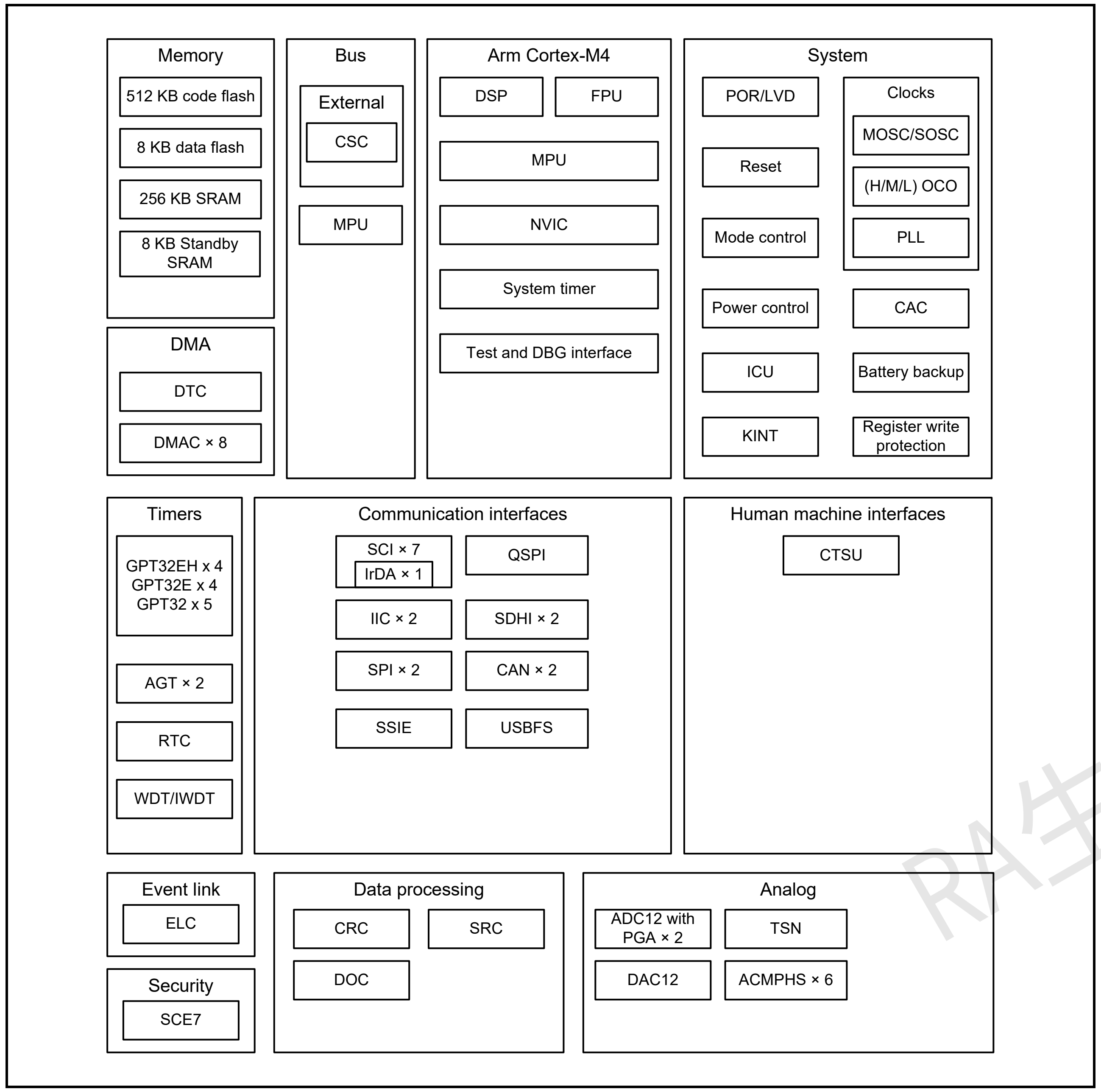


Figure 1.1 Block diagram

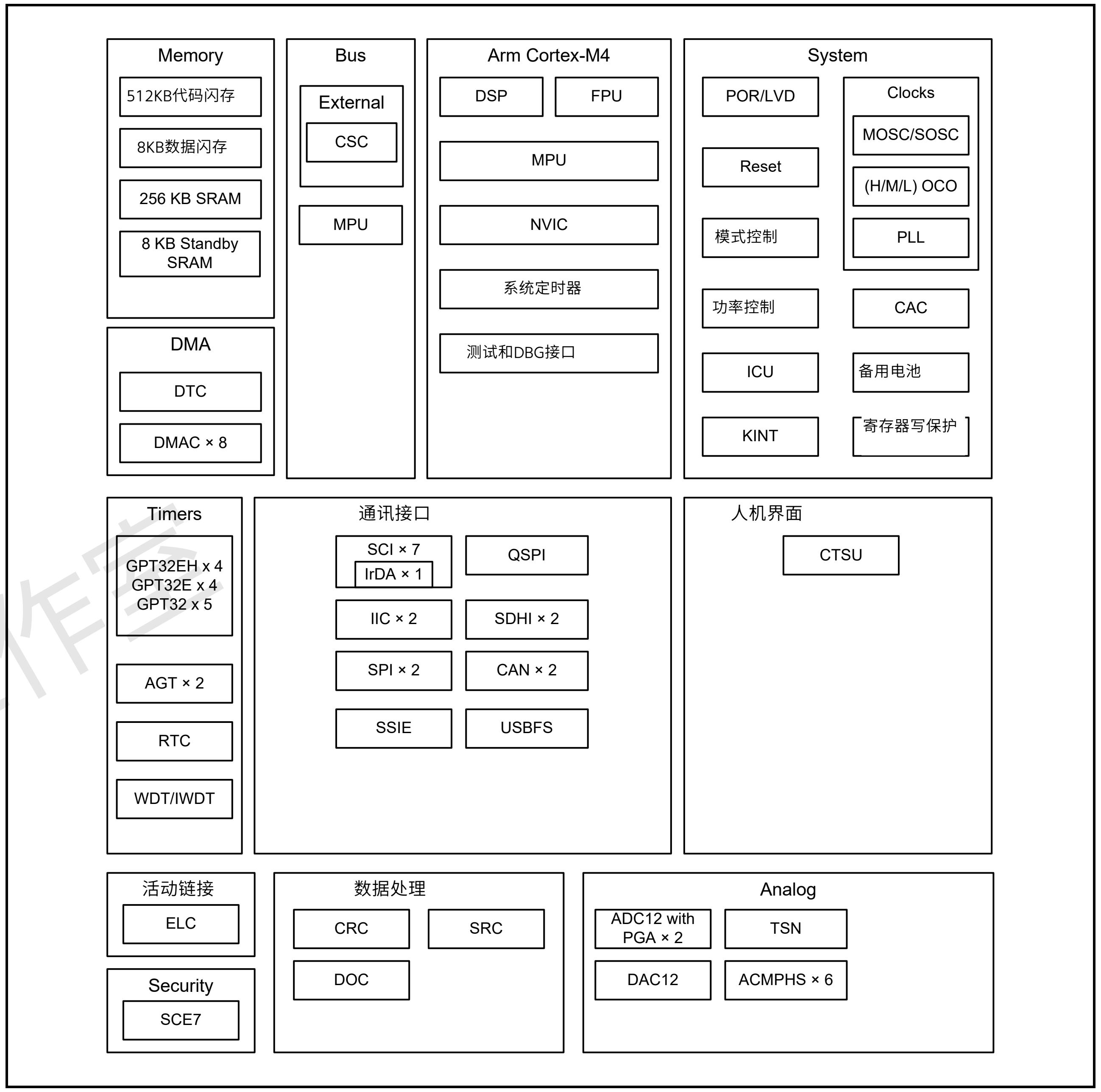


Figure 1.1 框图

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.13 shows a list of products.

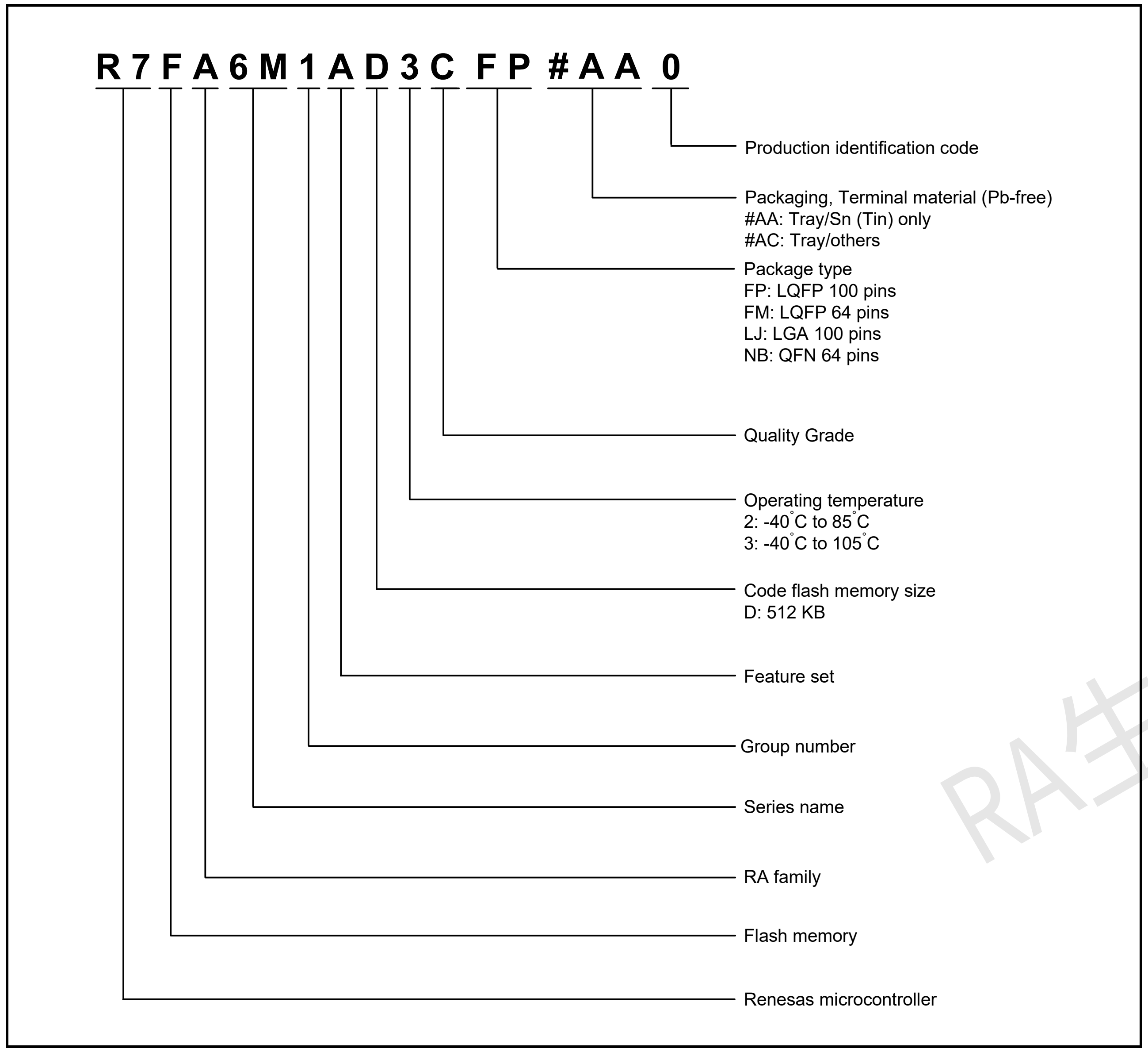


Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6M1AD2CLJ	R7FA6M1AD2CLJ#AC0	PTLG0100JA-A	512 KB	8 KB	256 KB	-40 to +85°C
R7FA6M1AD3CFP	R7FA6M1AD3CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FA6M1AD3CFM	R7FA6M1AD3CFM#AA0	PLQP0064KB-C				-40 to +105°C
R7FA6M1AD3CNB	R7FA6M1AD3CNB#AC0	PWQN0064LA-A				-40 to +105°C

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.13显示了产品列表。

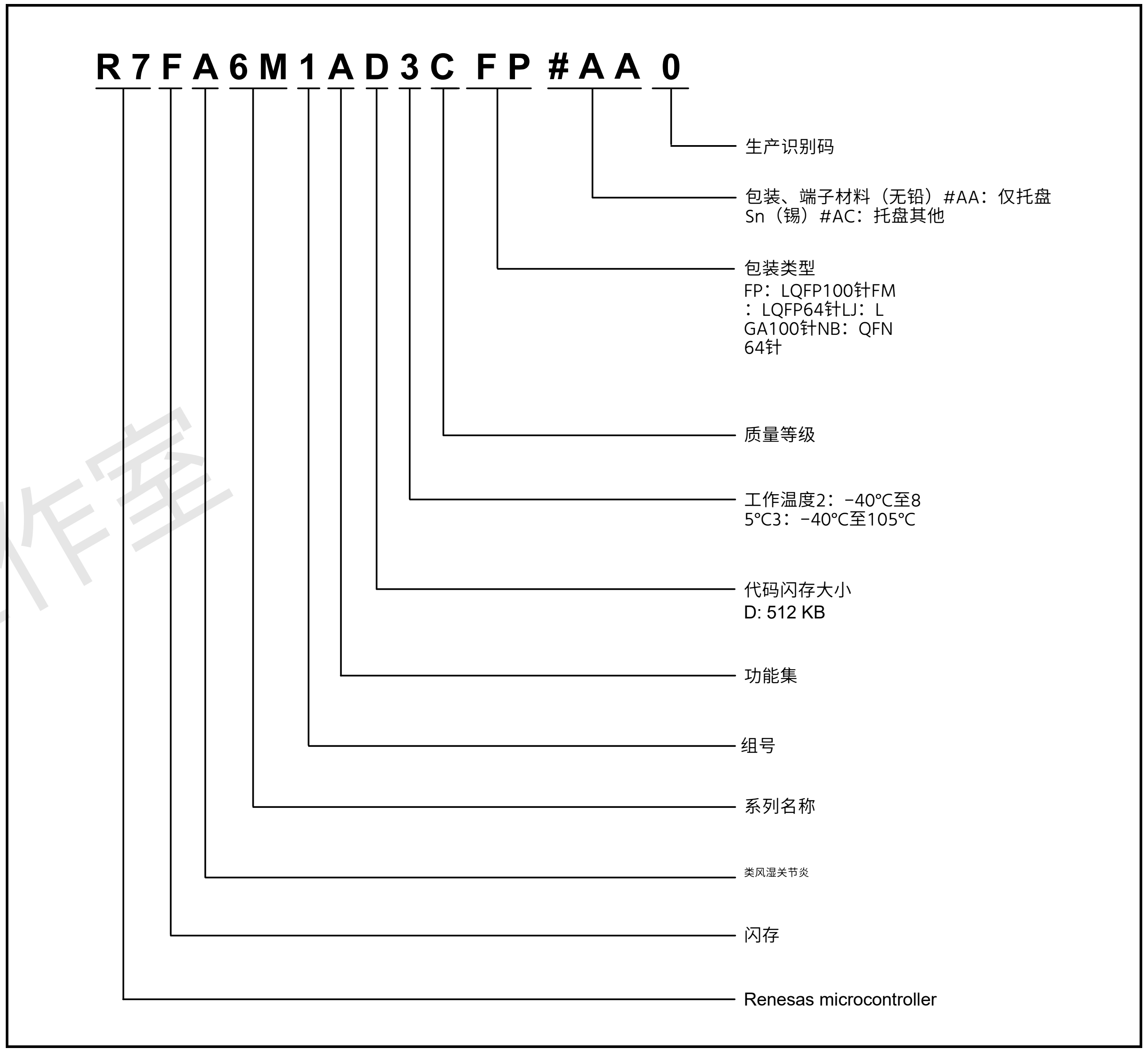


Figure 1.2 零件编号方案

Table 1.13 产品列表

产品部件号	可订购部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA6M1AD2CLJ	R7FA6M1AD2CLJ#AC0	PTLG0100JA-A	512 KB	8 KB	256 KB	-40 to +85°C
R7FA6M1AD3CFP	R7FA6M1AD3CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FA6M1AD3CFM	R7FA6M1AD3CFM#AA0	PLQP0064KB-C				-40 to +105°C
R7FA6M1AD3CNB	R7FA6M1AD3CNB#AC0	PWQN0064LA-A				-40 to +105°C

1.4 Function Comparison

Table 1.14 Functional comparison

Function		Part numbers R7FA6M1AD2CLJ	R7FA6M1AD3CFP	R7FA6M1AD3CFM	R7FA6M1AD3CNB
Pin count		100	100	64	64
Package		LGA	LQFP	LQFP	QFN
Code flash memory		512 KB			
Data flash memory		8 KB			
SRAM		256 KB			
	Parity	224 KB			
	ECC	32 KB			
Standby SRAM		8 KB			
System	CPU clock	120 MHz			
	Backup registers	512 B			
	ICU	Yes			
	KINT	8			
Event link	ELC	Yes			
DMA	DTC	Yes			
	DMAC	8			
BUS	External bus	8-bit bus		No	
Timers	GPT32EH	4			
	GPT32E	4		3	
	GPT32	5		4	
	AGT	2			
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	7			
	IIC	2			
	SPI	2			
	SSIE	1		No	
	QSPI	1			
	SDHI	2		No	
	CAN	2			
	USBFS	Yes			
Analog	ADC12	19		10	
	DAC12	2			
	ACMPHS	6			
	TSN	Yes			
HMI	CTSU	12		7	
Data processing	CRC	Yes			
	DOC	Yes			
	SRC	Yes			
Security		SCE7			

1.4 功能比较

Table 1.14 功能比较

Function		零件号 R7FA6M1AD2CLJ	R7FA6M1AD3CFP	R7FA6M1AD3CFM	R7FA6M1AD3CNB
针数		100	100	64	64
Package		LGA	LQFP	LQFP	QFN
代码闪存		512 KB			
数据闪存		8 KB			
SRAM		256 KB			
	Parity	224 KB			
	ECC	32 KB			
Standby SRAM		8 KB			
System	中央处理器时钟	120 MHz			
	备份寄存器	512 B			
	ICU	Yes			
	KINT	8			
活动链接	ELC	Yes			
DMA	DTC	Yes			
	DMAC	8			
BUS	外部总线	8-bit bus		No	
Timers	GPT32EH	4			
	GPT32E	4		3	
	GPT32	5		4	
	AGT	2			
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	7			
	IIC	2			
	SPI	2			
	SSIE	1		No	
	QSPI	1			
	SDHI	2		No	
	CAN	2			
	USBFS	Yes			
Analog	ADC12	19		10	
	DAC12	2			
	ACMPHS	6			
	TSN	Yes			
HMI	CTSU	12		7	
数据处理	CRC	Yes			
	DOC	Yes			
	SRC	Yes			
Security		SCE7			

1.5 Pin Functions

Table 1.15 Pin functions (1 of 4)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect this pin to the system power supply. Connect it to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL0	Input	Connect this pin to VSS through a 0.1-μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VCL	Input	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ13	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
	SWO	Output	Serial wire trace output pin
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active-low
	WR0	Output	Strobe signal indicating that writing to the external bus interface space is in progress, active-low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low
	CS0, CS1, CS4 to CS7	Output	Select signals for CS areas, active-low
	A00 to A12	Output	Address bus
	D00 to D07	I/O	Data bus
	A00/D00 to A07/D07	I/O	Address/data multiplexed bus

1.5 引脚功能

Table 1.15 引脚功能(1of4)

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。这用作各个模块和内部稳压器的数字电源，并用于监控PORLVD的电压。将此引脚连接到系统电源。通过一个0.1μF电容将其连接到VSS。将电容器靠近引脚放置。
	VCL0	Input	通过一个用于稳定内部电源的0.1μF平滑电容器将此引脚连接到VSS。将电容器靠近引脚放置。
	VCL	Input	
	VSS	Input	接地引脚。连接到系统电源(0V)。
	VBATT	Input	备用电源引脚
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过输入 EXTAL pin.
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	EBCLK	Output	为外部设备输出外部总线时钟
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ13	Input	可屏蔽中断请求引脚
KINT	KR00 to KR07	Input	通过向按键中断输入引脚输入下降沿可以产生按键中断
On-chip emulator	TMS	I/O	片上仿真器或边界扫描引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	该引脚输出与跟踪数据同步的时钟
	TDATA0 to TDATA3	Output	跟踪数据输出
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
	SWO	Output	串行线迹输出引脚
外部总线接口	RD	Output	指示正在从外部总线接口空间读取的选通信号，低电平有效
	WR0	Output	指示正在写入外部总线接口空间的选通信号，低电平有效
	ALE	Output	选择地址数据复用总线时的地址锁存信号
	WAIT	Input	用于访问外部空间的等待请求信号的输入引脚，低电平有效
	CS0, CS1, CS4 to CS7	Output	CS区域的选择信号，低电平有效
	A00 to A12	Output	地址总线
	D00 to D07	I/O	数据总线
	A00/D00 to A07/D07	I/O	Address/data multiplexed bus

Table 1.15 Pin functions (2 of 4)

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC12A, GTIOC0B to GTIOC12B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK4, SCK8, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD4, RXD8, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD4, TXD8, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS4_RTS4, CTS8_RTS8, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0 to SCL4, SCL8, SCL9	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDA0 to SDA4, SDA8, SDA9	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCK0 to SCK4, SCK8, SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO4, MISO8, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI4, MOSI8, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0 to SS4, SS8, SS9	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCL0, SCL1	I/O	Input/output pins for the clock
	SDA0, SDA1	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)

Table 1.15 引脚功能(2of4)

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOC0A to GTIOC12A, GTIOC0B to GTIOC12B	I/O	输入捕捉、输出比较或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEE0, AGTEE1	Input	外部事件输入使能信号
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出引脚
	AGTO0, AGTO1	Output	脉冲输出引脚
	AGTOA0, AGTOA1	Output	输出比较匹配A输出引脚
	AGTOB0, AGTOB1	Output	输出比较匹配B输出引脚
RTC	RTCOUT	Output	用于1Hz或64Hz时钟的输出引脚
	RTCIC0 to RTCIC2	Input	时间捕捉事件输入引脚
SCI	SCK0 to SCK4, SCK8, SCK9	I/O	时钟输入输出引脚（时钟同步模式）
	RXD0 to RXD4, RXD8, RXD9	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXD0 to TXD4, TXD8, TXD9	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTS0_RTS0 to CTS4_RTS4, CTS8_RTS8, CTS9_RTS9	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效
	SCL0 to SCL4, SCL8, SCL9	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDA0 to SDA4, SDA8, SDA9	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCK0 to SCK4, SCK8, SCK9	I/O	时钟输入输出引脚（简单SPI模式）
	MISO0 to MISO4, MISO8, MISO9	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSI0 to MOSI4, MOSI8, MOSI9	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SS0 to SS4, SS8, SS9	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCL0, SCL1	I/O	时钟的输入输出引脚
	SDA0, SDA1	I/O	数据输入输出引脚
SSIE	SSIBCK0	I/O	SSIE串行位时钟引脚
	SSILRCK0/SSIFS0	I/O	LR时钟帧同步管脚
	SSITXD0	Output	串行数据输出引脚
	SSIRXD0	Input	串行数据输入引脚
	AUDIO_CLK	Input	音频外部时钟引脚（输入过采样时钟）

Table 1.15 Pin functions (3 of 4)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	Receive data
	CTX0, CTX1	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT3, SD1DAT0 to SD1DAT3	I/O	SD and MMC data bus pins
	SD0CD	Input	SD card detection pins
	SD0WP	Input	SD write-protect signals
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

Table 1.15 引脚功能(3of4)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	用于从主机输出数据的输入或输出引脚
	MISOA, MISOB	I/O	从机数据输出的输入或输出引脚
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚
QSPI	QSPCLK	Output	QSPI时钟输出引脚
	QSSL	Output	QSPI从机输出引脚
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	接收数据
	CTX0, CTX1	Output	传输数据
USBFS	VCC_USB	Input	电源引脚
	VSS_USB	Input	接地引脚
	USB_DP	I/O	USB片上收发器的D+IO引脚。将此引脚连接到USB总线的D+引脚
	USB_DM	I/O	USB片上收发器的DIO引脚。将此引脚连接到USB总线的Dpin
	USB_VBUS	Input	USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为设备控制器运行时，可以检测到VBUS引脚状态（连接或断开）。
	USB_EXICEN	Output	用于外部电源(OTG)芯片的低功耗控制信号
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号
	USB_OVRCURA, USB_OVRCURB	Input	将外部过电流检测信号连接到这些引脚。连接OTG电源芯片时，将VBUS比较器信号连接到这些引脚。
	USB_ID	Input	在操作期间将MicroAB连接器ID输入信号连接到此引脚 OTG mode
SDHI	SD0CLK, SD1CLK	Output	SD时钟输出引脚
	SD0CMD, SD1CMD	I/O	命令输出引脚和响应输入信号引脚
	SD0DAT0 to SD0DAT3, SD1DAT0 to SD1DAT3	I/O	SD和MMC数据总线引脚
	SD0CD	Input	SD卡检测引脚
	SD0WP	Input	SD write-protect signals
模拟电源	AVCC0	Input	模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH0	Input	ADC12（单元0）的模拟参考电压电源引脚。当不使用ADC12（单元0）和AN000到AN002的采样保持电路时，将此引脚连接到VCC。
	VREFL0	Input	ADC12的模拟参考接地引脚。不使用ADC12（单元0）和AN000至AN002的采样保持电路时，将此引脚连接到VSS
	VREFH	Input	ADC12（单元1）和DA的模拟参考电压电源引脚 转换器。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VCC。
	VREFL	Input	ADC12和DA转换器的模拟参考接地引脚。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VSS。

Table 1.15 Pin functions (4 of 4)

Function	Signal	I/O	Description
ADC12	AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020	Input	Input pins for the analog signals to be processed by the ADC12
	AN100 to AN102, AN105 to AN107, AN116, AN117	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
	ADTRG1	Input	
	PGAVSS000, PGAVSS100	Input	Differential input pins
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter
ACMPHS	VCOUT	Output	Comparator output pin
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator
	IVCMP0 to IVCMP3	Input	Analog voltage input pins for comparator
CTSU	TS01 to TS12	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
I/O ports	P000 to P007	Input	General-purpose input pins
	P008, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P205 to P214	I/O	General-purpose input/output pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P504, P508	I/O	General-purpose input/output pins
	P600 to P602, P608 to P610	I/O	General-purpose input/output pins
	P708	I/O	General-purpose input/output pin

Table 1.15 引脚功能（4个，共4个）

Function	Signal	I/O	Description
ADC12	AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020	Input	ADC12处理的模拟信号的输入引脚
	AN100 to AN102, AN105 to AN107, AN116, AN117	Input	
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚
	ADTRG1	Input	
	PGAVSS000, PGAVSS100	Input	差分输入引脚
DAC12	DA0, DA1	Output	DA转换器处理的模拟信号的输出引脚
ACMPHS	VCOUT	Output	比较器输出引脚
	IVREF0 to IVREF3	Input	比较器的参考电压输入引脚
	IVCMP0 to IVCMP3	Input	比较器的模拟电压输入引脚
CTSU	TS01 to TS12	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	-	触摸驱动器的辅助电源引脚
I/O ports	P000 to P007	Input	通用输入引脚
	P008, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201, P205 to P214	I/O	General-purpose input/output pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P504, P508	I/O	General-purpose input/output pins
	P600 to P602, P608 to P610	I/O	General-purpose input/output pins
	P708	I/O	General-purpose input/output pin

1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments.

R7FA6M1AD2CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	XCOUT	VCL0	P403	P400	P000	10
9	USB_DM	USB_DP	P411	VSS	P213/ XTAL	XCIN	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	P207	P413	P415	P708	P404	P003	P004	P002	8
7	P205	P214	P206	P408	P414	P406	P006	P007	P008	P005	7
6	P209	P208	P210	P211	P410	P402	P508	AVSS0	VREFL0	VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	VREFL	VREFH	5
4	VCC	P304	P305	P306	P115	P601	P503	P100	P015	P014	4
3	VSS	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	VSS	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO	P112	P608	VCC	VCL	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.3 Pin assignment for 100-pin LGA (top view)

1.6 引脚分配

图1.3至图1.6显示了引脚分配。

R7FA6M1AD2CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	XCOUT	VCL0	P403	P400	P000	10
9	USB_DM	USB_DP	P411	VSS	P213/ XTAL	XCIN	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	P207	P413	P415	P708	P404	P003	P004	P002	8
7	P205	P214	P206	P408	P414	P406	P006	P007	P008	P005	7
6	P209	P208	P210	P211	P410	P402	P508	AVSS0	VREFL0	VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	VREFL	VREFH	5
4	VCC	P304	P305	P306	P115	P601	P503	P100	P015	P014	4
3	VSS	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	VSS	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO	P112	P608	VCC	VCL	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.3 100引脚LGA的引脚分配（俯视图）

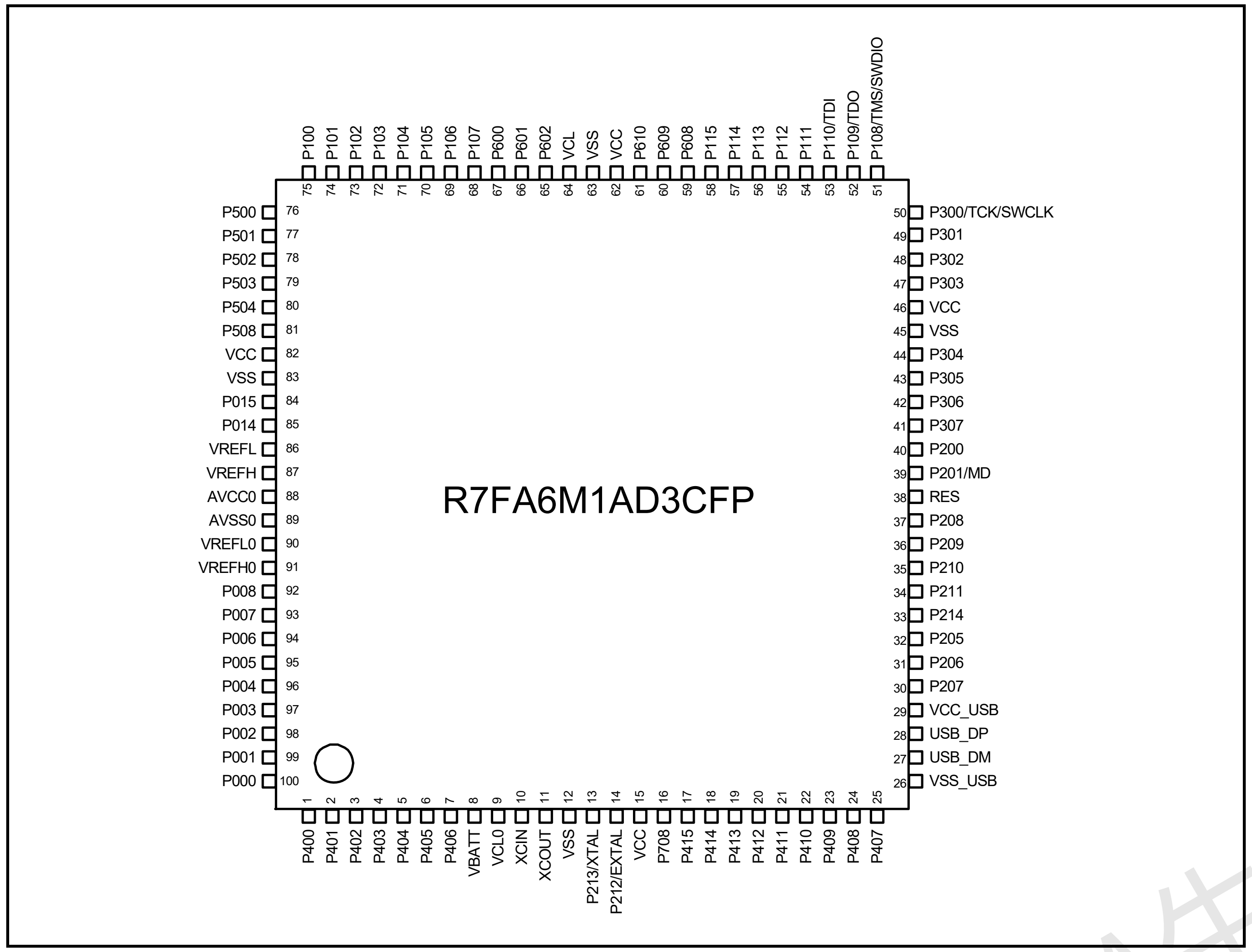


Figure 1.4 Pin assignment for 100-pin LQFP (top view)

RA6M1 Group 1. Overview

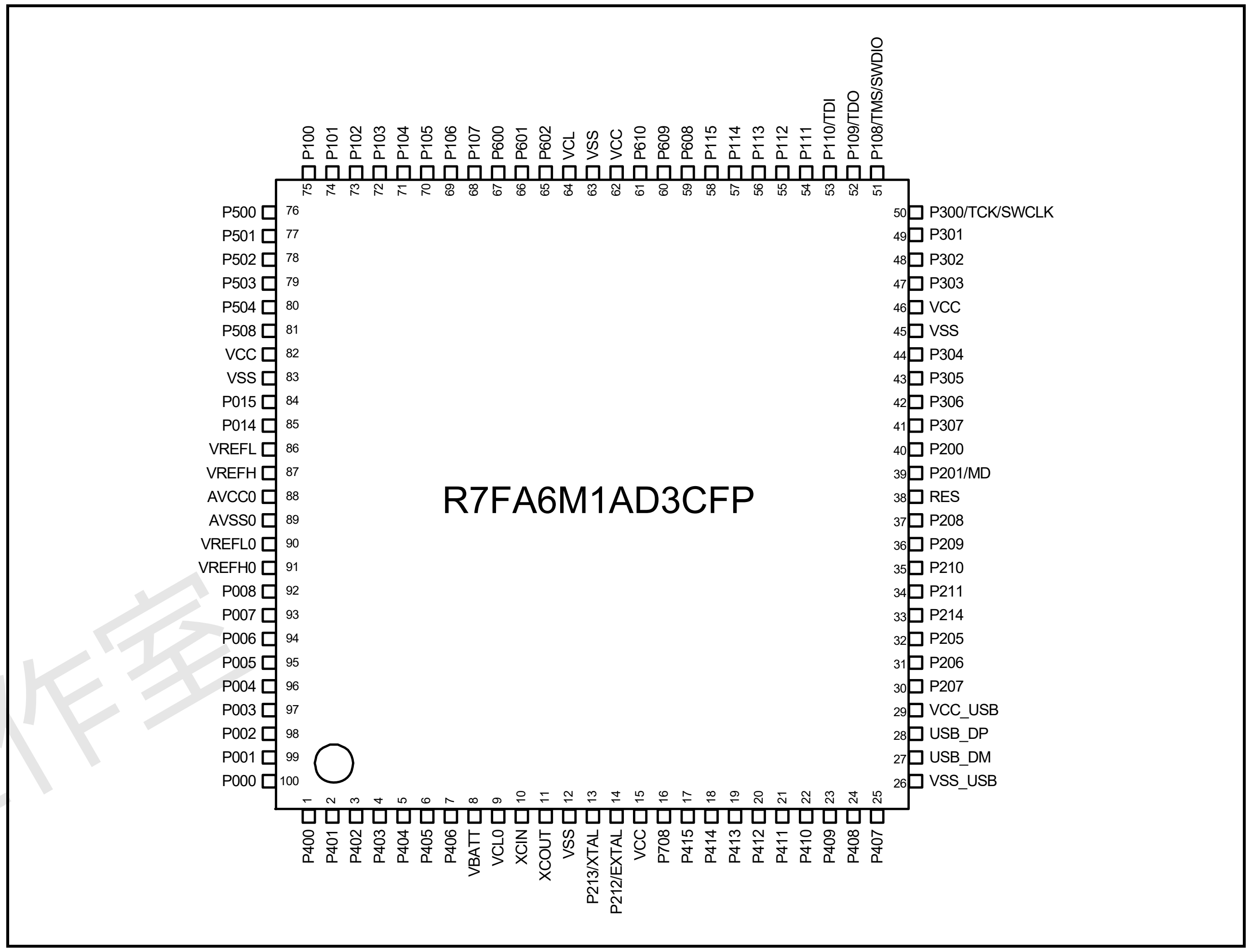


Figure 1.4 100引脚LQFP的引脚分配（顶视图）

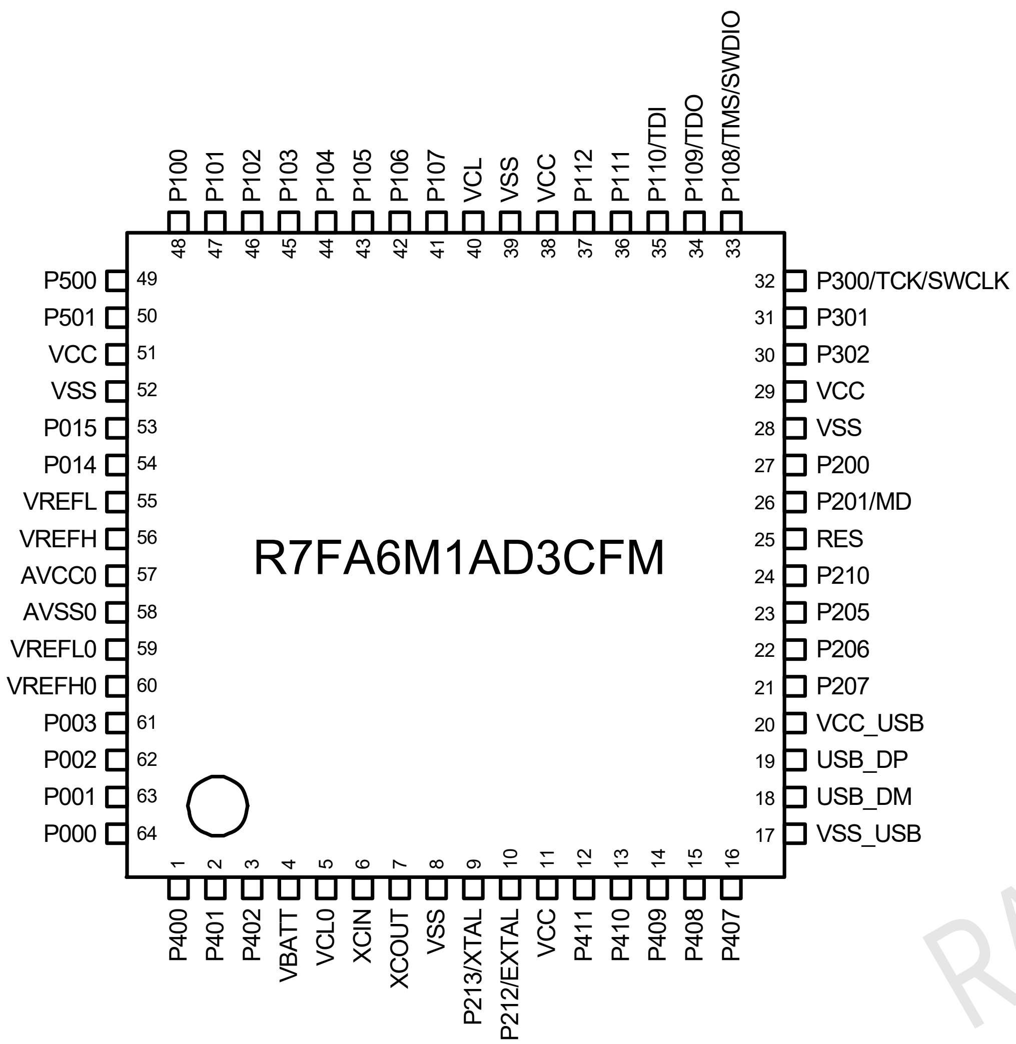


Figure 1.5 Pin assignment for 64-pin LQFP (top view)

RA6M1 Group
1. Overview

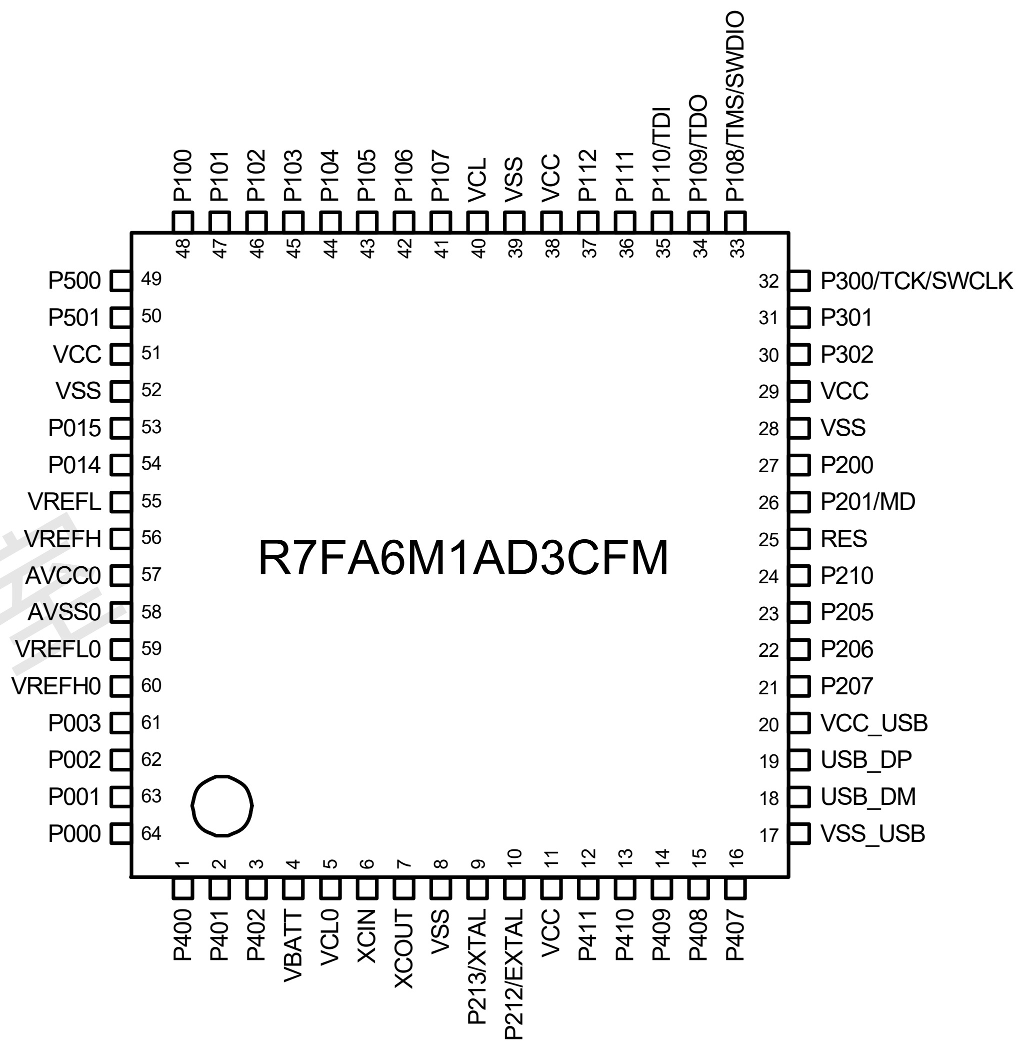


Figure 1.5 64引脚LQFP的引脚分配（顶视图）

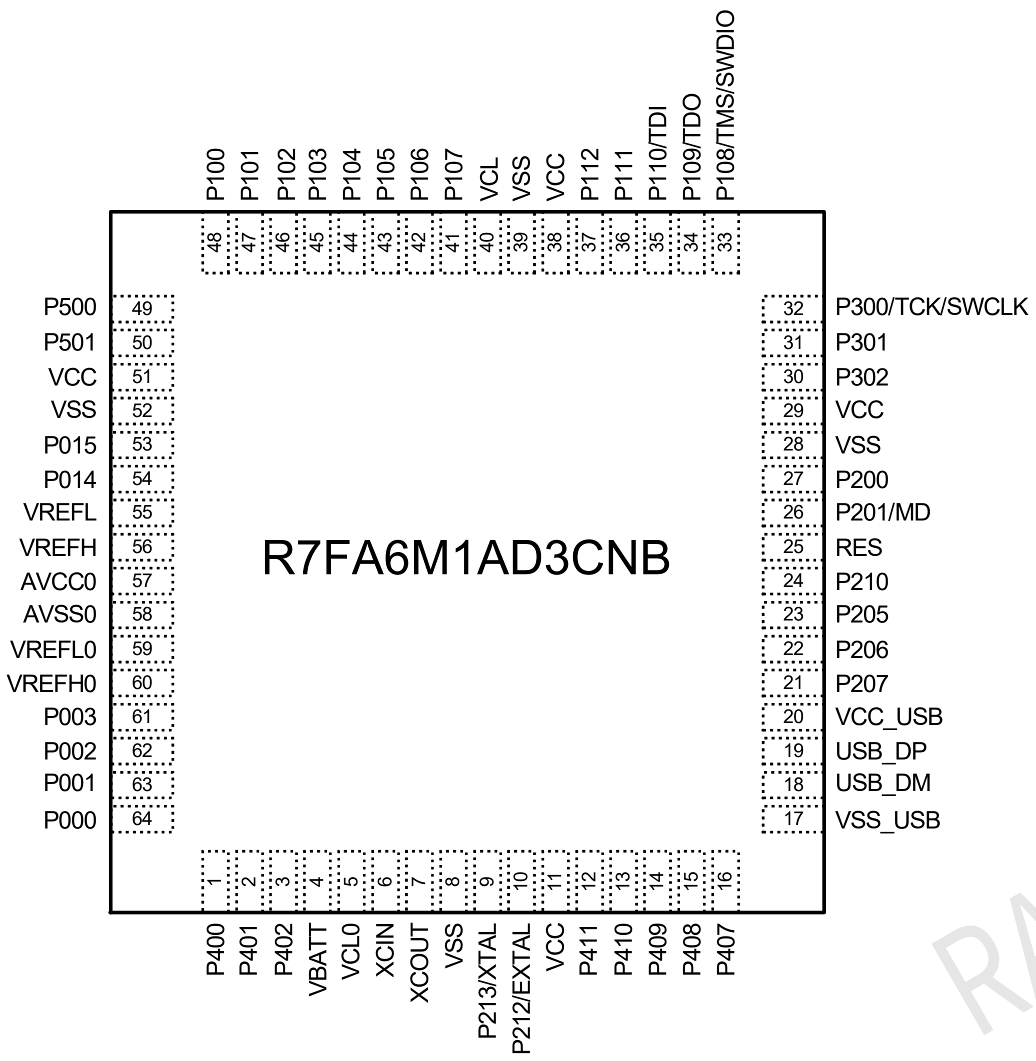


Figure 1.6 Pin assignment for 64-pin QFN (top view)

RA6M1 Group 1. Overview

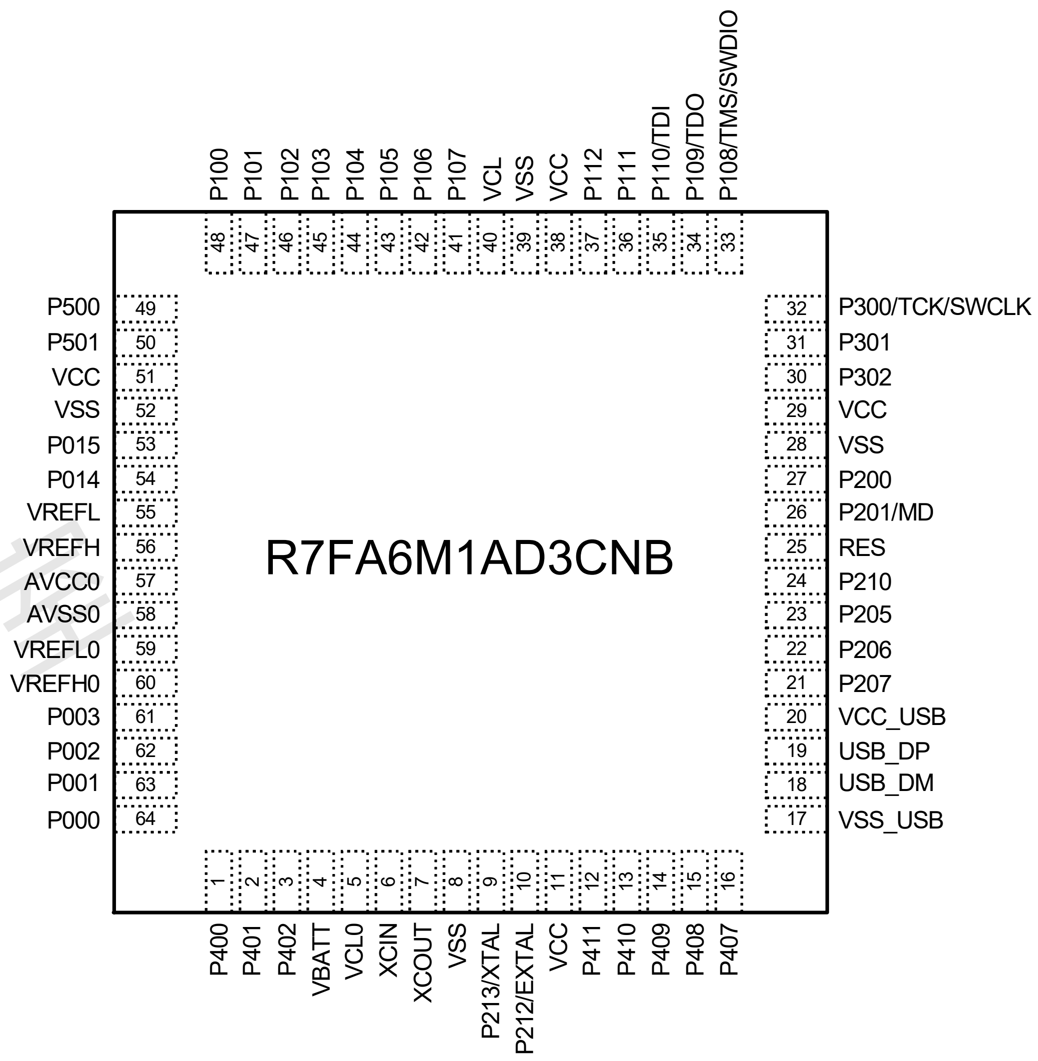


Figure 1.6 64引脚QFN的引脚分配（顶视图）

1.7 Pin Lists

Pin number				Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	Timers				Communication interfaces							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
J10	1	1	1	-	IRQ0	P400	-	AGTIO1	-	GTIOC6A	-	-	SCK4	-	SCL0_A	-	AUDIO_CLK	-	ADTRG1	-	-
J9	2	2	2	-	IRQ5-DS	P401	-	-	GTETRGA	GTIOC6B	-	CTX0	CTS4_RTS4/SS4	-	SDA0_A	-	-	-	-	-	-
F6	3	3	3	CACREF	IRQ4-DS	P402	-	AGTIO0/AGTIO1	-	-	RTCIC0	CRX0	-	-	-	-	AUDIO_CLK	-	-	-	-
H10	4	-	-	-	-	P403	-	AGTIO0/AGTIO1	-	GTIOC3A	RTCIC1	-	-	-	-	-	SSIBCK0_A	-	-	-	-
G8	5	-	-	-	-	P404	-	-	-	GTIOC3B	RTCIC2	-	-	-	-	-	SSILRCK0/SSIFS0_A	-	-	-	-
H9	6	-	-	-	-	P405	-	-	-	GTIOC1A	-	-	-	-	-	-	SSITXD0_A	-	-	-	-
F7	7	-	-	-	-	P406	-	-	-	GTIOC1B	-	-	-	-	-	-	SSIRXD0_A	-	-	-	-
G9	8	4	4	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G10	9	5	5	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F9	10	6	6	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F10	11	7	7	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	12	8	8	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E9	13	9	9	XTAL	IRQ2	P213	-	-	GTETRGC	GTIOC0A	-	-	-	TXD1/MOSI1/SDA1	-	-	-	-	ADTRG1	-	-
E10	14	10	10	EXTAL	IRQ3	P212	-	AGTEE1	GTETRGD	GTIOC0B	-	-	-	RXD1/MISO1/SCL1	-	-	-	-	-	-	-
D10	15	11	11	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F8	16	-	-	CACREF	IRQ11	P708	-	-	-	-	-	-	-	RXD1/MISO1/SCL1	-	SSLA3_B	AUDIO_CLK	-	-	-	TS12
E8	17	-	-	-	IRQ8	P415	-	-	-	GTIOC0A	-	USB_VBUSEN	-	-	-	SSLA2_B	-	SD0CD	-	-	TS11
E7	18	-	-	-	IRQ9	P414	-	-	-	GTIOC0B	-	-	-	-	-	SSLA1_B	-	SD0WP	-	-	TS10
D8	19	-	-	-	-	P413	-	-	GTOUUP	-	-	-	CTS0_RTS0/SS0	-	-	SSLA0_B	-	SD0CLK_A	-	-	TS09
C10	20	-	-	-	-	P412	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPCKA_B	-	SD0CMD_A	-	-	TS08
C9	21	12	12	-	IRQ4	P411	-	AGTOA1	GTOVUP	GTIOC9A	-	-	TXD0/MOSI0/SDA0	CTS3_RTS3/SS3	-	MOSIA_B	-	SD0DAT0_A	-	-	TS07
E6	22	13	13	-	IRQ5	P410	-	AGTOB1	GTOVLO	GTIOC9B	-	-	RXD0/MISO0/SCL0	SCK3	-	MISOA_B	-	SD0DAT1_A	-	-	TS06
B10	23	14	14	-	IRQ6	P409	-	-	GTOWUP	GTIOC10A	-	USB_EXICEN	-	TXD3/MOSI3/SDA3	-	-	-	-	-	-	TS05
D7	24	15	15	-	IRQ7	P408	-	-	GTOWLO	GTIOC10B	-	USB_ID	-	RXD3/MISO3/SCL3	SCL0_B	-	-	-	-	-	TS04
A10	25	16	16	-	-	P407	-	AGTIO0	-	-	RTCOUT	USB_VBUS	CTS4_RTS4/SS4	-	SDA0_B	-	-	-	ADTRG0	-	TS03
B8	26	17	17	VSS_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A9	27	18	18	-	-	-	-	-	-	-	-	USB_DM	-	-	-	-	-	-	-	-	-
B9	28	19	19	-	-	-	-	-	-	-	-	USB_DP	-	-	-	-	-	-	-	-	-
A8	29	20	20	VCC_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	30	21	21	-	-	P207	-	-	-	-	-	-	-	-	-	QSSL	-	-	-	-	TS02
C7	31	22	22	-	IRQ0-DS	P206	WAIT	-	GTIU	-	-	USB_VBUSEN	RXD4/MISO4/SCL4	-	SDA1_A	-	-	SD0DAT2_A	-	-	TS01
A7	32	23	23	CLKOUT	IRQ1-DS	P205	-	AGTO1	GTIV	GTIOC4A	-	USB_OVRCURA-DS	TXD4/MOSI4/SDA4	CTS9_RTS9/SS9	SCL1_A	-	-	SD0DAT3_A	-	-	TSCAP
B7	33	-	-	TRCLK	-	P214	-	-	GTIU	-	-	-	-	-	-	QSPCLK	-	SD0CLK_B	-	-	-
D6	34	-	-	TRDATA0	-	P211	CS7	-	GTIV	-	-	-	-	-	-	QIO0	-	SD0CMD_B	-	-	-
C6	35	24	24	TRDATA1	-	P210	CS6	-	GTIW	-	-	-	-	-	-	QIO1	-	SD0CD	-	-	-
A6	36	-	-	TRDATA2	-	P209	CS5	-	GTOVUP	-	-	-	-	-	-	QIO2	-	SD0WP	-	-	-
B6	37	-	-	TRDATA3	-	P208	CS4	-	GTOVLO	-	-	-	-	-	-	QIO3	-	SD0DAT0_B	-	-	-
D5	38	25	25	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B5	39	26	26	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A5	40	27	27	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C5	41	-	-	-	-	P307	A12	-	GTOUUP	-	-	-	-	-	-	QIO0	-	-	-	-	-
D4	42	-	-	-	-	P306	A11	-	GTOULO	-	-	-	-	-	-	QSSL	-	-	-	-	-
C4	43	-	-	-	IRQ8	P305	A10	-	GTOWUP	-	-	-	-	-	-	QSPCLK	-	-	-	-	-
B4	44	-	-	-	IRQ9	P304	A09	-	GTOWLO	GTIOC7A	-	-	-	-	-	-	-	-	-	-	-
A3	45	28	28	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A4	46	29	29	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B3	47	-	-	-	-	P303	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-
B2	48	30	30	-	IRQ5	P302	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-
C2	49	31	31	-	IRQ6	P301	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-
A2	50	32	32	TCK/SWCLK	-	P300	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-
A1	51	33	33	TMS/SWDIO	-	P108	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-

1.7 引脚列表

针号				电源系统，时钟，调试，CAC	Interrupt	I/O port	外部总线	Timers				通讯接口							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
J10	1	1	1	-	IRQ0	P400	-	AGTIO1	-	GTIOC6A	-	-	SCK4	-	SCL0_A	-	AUDIO_CLK	-	ADTRG1	-	-
J9	2	2	2	-	IRQ5-DS	P401	-	-	GTETRGA	GTIOC6B	-	CTX0	CTS4_RTS4/SS4	-	SDA0_A	-	-	-	-	-	-
F6	3	3	3	CACREF	IRQ4-DS	P402	-	AGTIO0/AGTIO1	-	-	RTCIC0	CRX0	-	-	-	-	AUDIO_CLK	-	-	-	-
H10	4	-	-	-	-	P403	-	AGTIO0/AGTIO1	-	GTIOC3A	RTCIC1	-	-	-	-	-	SSIBCK0_A	-	-	-	-
G8	5	-	-	-	-	P404	-	-	-	GTIOC3B	RTCIC2	-	-	-	-	-	SSILRCK0/SSIFS0_A	-	-	-	-
H9	6	-	-	-	-	P405	-	-	-	GTIOC1A	-	-	-	-	-	-	SSITXD0_A	-	-	-	-
F7	7	-	-	-	-	P406	-	-	-	GTIOC1B	-	-	-	-	-	-	SSIRXD0_A	-	-	-	-
G9	8	4	4	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G10	9	5	5	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F9	10	6	6	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F10	11	7	7	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	12	8	8	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E9	13	9	9	XTAL	IRQ2	P213	-	-	GTETRGC	GTIOC0A	-	-	-	TXD1/MOSI1/SDA1	-	-	-	-	ADTRG1	-	-
E10	14	10	10	EXTAL	IRQ3	P212	-	AGTEE1	GTETRGD	GTIOC0B	-	-	-	RXD1/MISO1/SCL1	-	-	-	-	-	-	-
D10	15	11	11	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F8	16	-	-	CACREF	IRQ11	P708	-	-	-	-	-	-	-	RXD1/MISO1/SCL1	-	SSLA3_B	AUDIO_CLK	-	-	-	TS12
E8	17	-	-	-	IRQ8	P415	-	-	-	GTIOC0A	-	USB_VBUSEN	-	-	-	SSLA2_B	-	SD0CD	-	-	TS11
E7	18	-	-	-	IRQ9	P414	-	-	-	GTIOC0B	-	-	-	-	-	SSLA1_B	-	SD0WP	-	-	TS10
D8	19	-	-	-	-	P413	-	-	GTOUUP	-	-	-	CTS0_RTS0/SS0	-	-	SSLA0_B	-	SD0CLK_A	-	-	TS09
C10	20	-	-	-	-	P412	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPCKA_B	-	SD0CMD_A	-	-	TS08
C9	21	12	12	-	IRQ4	P411	-	AGTOA1	GTOVUP	GTIOC9A	-	-	TXD0/MOSI0/SDA0	CTS3_RTS3/SS3	-	MOSIA_B	-	SD0DAT0_A	-	-	TS07
E6	22	13	13	-	IRQ5	P410	-	AGTOB1	GTOVLO	GTIOC9B	-	-	RXD0/MISO0/SCL0	SCK3	-	MISOA_B	-	SD0DAT1_A	-	-	TS06
B10	23	14	14	-	IRQ6	P409	-	-	GTOWUP	GTIOC10A	-	USB_EXICEN	-	TXD3/MOSI3/SDA3	-	-	-	-	-	-	TS05
D7	24	15	15	-	IRQ7	P408	-	-	GTOWLO	GTIOC10B	-	USB_ID	-	RXD3/MISO3/SCL3	SCL0_B	-	-	-	-	-	TS04
A10	25	16	16	-	-	P407	-	AGTIO0	-	-	RTCOUT	USB_VBUS	CTS4_RTS4/SS4	-	SDA0_B	-	-	-	ADTRG0	-	TS03
B8	26	17	17	VSS_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A9	27	18	18	-	-	-	-	-	-	-	-	USB_DM	-	-	-	-	-	-	-	-	-
B9	28	19	19	-	-	-	-	-	-	-	-	USB_DP	-	-	-	-	-	-	-	-	-
A8	29	20	20	VCC_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	30	21	21	-	-	P207	-	-	-	-	-	-	-	-	-	QSSL	-	-	-	-	TS02
C7	31	22	22	-	IRQ0-DS	P206	WAIT	-	GTIU	-	-	USB_VBUSEN	RXD4/MISO4/SCL4	-	SDA1_A	-	-	SD0DAT2_A	-	-	TS01
A7	32	23	23	CLKOUT	IRQ1-DS	P205	-	AGTO1	GTIV	GTIOC4A	-	USB_OVRCURA-DS	TXD4/MOSI4/SDA4	CTS9_RTS9/SS9	SCL1_A	-	-	SD0DAT3_A	-	-	TSCAP
B7	33	-	-	TRCLK	-	P214	-	-	GTIU	-	-	-	-	-	-	QSPCLK	-	SD0CLK_B	-	-	-
D6	34	-	-	TRDATA0	-	P211	CS7	-	GTIV	-	-	-	-	-	-	QIO0	-	SD0CMD_B	-	-	-
C6	35	24	24	TRDATA1	-	P210	CS6	-	GTIW	-	-	-	-	-	-	QIO1	-	SD0CD	-	-	-
A6	36	-	-	TRDATA2	-	P209	CS5	-	GTOVUP	-	-	-	-	-	-	QIO2	-	SD0WP	-	-	-
B6	37	-	-	TRDATA3	-	P208	CS4	-	GTOVLO	-	-	-	-	-	-	QIO3	-	SD0DAT0_B	-	-	-
D5	38	25	25	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B5	39	26	26	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A5	40	27	27	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C5	41	-	-	-	-	P307	A12	-	GTOUUP	-	-	-	-	-	-	QIO0	-	-	-	-	-
D4	42	-	-	-	-	P306	A11	-	GTOULO	-	-	-	-	-	-	QSSL	-	-	-	-	-
C4	43	-	-	-	IRQ8	P305	A10	-	GTOWUP	-	-	-	-	-	-	QSPCLK	-	-	-	-	-
B4	44	-	-	-	IRQ9	P304	A09	-	GTOWLO	GTIOC7A	-	-	-	-	-	-	-	-	-	-	-
A3	45	28	28	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A4	46	29	29	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B3	47	-	-	-	-	P303	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-
B2	48	30	30	-	IRQ5	P302	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-
C2	49	31	31	-	IRQ6	P301	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-
A2	50	32	32	TCK/SWCLK	-	P300	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-
A1	51	33	33	TMS/SWDIO	-	P108	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-

Pin number				Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	Timers				Communication interfaces							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
B1	52	34	34	CLKOUT/TDO/SWO	-	P109	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-
C3	53	35	35	TDI	IRQ3	P110	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	VCOUT	-
D3	54	36	36	-	IRQ4	P111	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-
C1	55	37	37	-	-	P112	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-
E5	56	-	-	-	-	P113	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-
D2	57	-	-	-	-	P114	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-
E4	58	-	-	-	-	P115	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-
D1	59	-	-	-	-	P608	A00	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-
E3	60	-	-	-	-	P609	CS1	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-
E2	61	-	-	-	-	P610	CS0	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-
E1	62	38	38	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F2	63	39	39	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F1	64	40	40	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F3	65	-	-	-	-	P602	EBCLK	-	-	GTIOC7B	-	-	-	TXD9	-	-	-	-	-	-	-
F4	66	-	-	-	-	P601	WR0	-	-	GTIOC6A	-	-	-	RXD9	-	-	-	-	-	-	-
F5	67	-	-	CLKOUT/CACREF	-	P600	RD	-	-	GTIOC6B	-	-	-	SCK9	-	-	-	-	-	-	-
G3	68	41	41	-	KR07	P107	D07[A07/D07]	AGTOA0	-	GTIOC8A	-	-	CTS8_RTS8/SS8	-	-	QIO3	-	-	-	-	-
G2	69	42	42	-	KR06	P106	D06[A06/D06]	AGTOB0	-	GTIOC8B	-	-	SCK8	-	-	SSLA3_A/QIO2	-	-	-	-	-
G1	70	43	43	-	IRQ0/KR05	P105	D05[A05/D05]	-	GTETRGA	GTIOC1A	-	-	TXD8/MOSI8/SDA8	-	-	SSLA2_A/QIO1	-	-	-	-	-
H1	71	44	44	-	IRQ1/KR04	P104	D04[A04/D04]	-	GTETRGB	GTIOC1B	-	-	RXD8/MISO8/SCL8	-	-	SSLA1_A/QIO0	-	-	-	-	-
H3	72	45	45	-	KR03	P103	D03[A03/D03]	-	GTOWUP	GTIOC2A_A	-	CTX0	CTS0_RTS0/SS0	-	-	SSLA0_A	-	-	-	-	-
J1	73	46	46	-	KR02	P102	D02[A02/D02]	AGTO0	GTOWLO	GTIOC2B_A	-	CRX0	SCK0	-	-	RSPCKA_A	-	-	ADTRG0	-	-
H2	74	47	47	-	IRQ1/KR01	P101	D01[A01/D01]	AGTEE0	GTETRGB	GTIOC5A	-	-	TXD0/MOSI0/SDA0	CTS1_RTS1/SS1	SDA1_B	MOSIA_A	-	-	-	-	-
H4	75	48	48	-	IRQ2/KR00	P100	D00[A00/D00]	AGTIO0	GTETRGA	GTIOC5B	-	-	RXD0/MISO0/SCL0	SCK1	SCL1_B	MISOA_A	-	-	-	-	-
K1	76	49	49	-	-	P500	-	AGTOA0	GTIU	GTIOC11A	-	USB_VBUSEN	-	-	-	QSPCLK	-	SD1CLK_A	AN016	IVREF0	-
J2	77	50	50	-	IRQ11	P501	-	AGTOB0	GTIV	GTIOC11B	-	USB_OVRCURA	-	-	-	QSSL	-	SD1CMD_A	AN116	IVREF1	-
K2	78	-	-	-	IRQ12	P502	-	-	GTIW	GTIOC12A	-	USB_OVRCURB	-	-	-	QIO0	-	SD1DAT0_A	AN017	IVCMP0	-
G4	79	-	-	-	-	P503	-	-	GTETRGC	GTIOC12B	-	USB_EXICEN	-	-	-	QIO1	-	SD1DAT1_A	AN117	-	-
G5	80	-	-	-	-	P504	ALE	-	GTETRGD	-	-	USB_ID	-	-	-	QIO2	-	SD1DAT2_A	AN018	-	-
G6	81	-	-	-	-	P508	-	-	-	-	-	-	-	-	-	-	-	SD1DAT3_A	AN020	-	-
K3	82	51	51	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	83	52	52	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J4	84	53	53	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-
K4	85	54	54	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-
J5	86	55	55	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K5	87	56	56	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H5	88	57	57	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H6	89	58	58	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J6	90	59	59	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K6	91	60	60	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J7	92	-	-	-	IRQ12-DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-
H7	93	-	-	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS100/AN107	-	-
G7	94	-	-	-	IRQ11-DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-
K7	95	-	-	-	IRQ10-DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-
J8	96	-	-	-	IRQ9-DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-
H8	97	61	61	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS000/AN007	-	-
K8	98	62	62	-	IRQ8-DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-

RA6M1 Group
1. Overview

针号				电源系统，时钟，调试，CAC	Interrupt	I/O port	外部总线	Timers				通讯接口							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
B1	52	34	34	CLKOUT/TDO/SWO	-	P109	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-
C3	53	35	35	TDI	IRQ3	P110	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	VCOUT	-
D3	54	36	36	-	IRQ4	P111	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-
C1	55	37	37	-	-	P112	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-
E5	56	-	-	-	-	P113	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-
D2	57	-	-	-	-	P114	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-
E4	58	-	-	-	-	P115	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-
D1	59	-	-	-	-	P608	A00	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-
E3	60	-	-	-	-	P609	CS1	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-
E2	61	-	-	-	-	P610	CS0	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-
E1	62	38	38	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F2	63	39	39	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F1	64	40	40	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F3	65	-	-	-	-	P602	EBCLK	-	-	GTIOC7B	-	-	-	TXD9	-	-	-	-	-	-	-
F4	66	-	-	-	-	P601	WR0	-	-	GTIOC6A	-	-	-	RXD9	-	-	-	-	-	-	-
F5	67	-	-	CLKOUT/CACREF	-	P600	RD	-	-	GTIOC6B	-	-	-	SCK9	-	-	-	-	-	-	-
G3	68	41	41	-	KR07	P107	D07[A07/D07]	AGTOA0	-	GTIOC8A	-	-	CTS8_RTS8/SS8	-	-	QIO3	-	-	-	-	-
G2	69	42	42	-	KR06	P106	D06[A06/D06]	AGTOB0	-	GTIOC8B	-	-	SCK8	-	-	SSLA3_A/QIO2	-	-	-	-	-
G1	70	43	43	-	IRQ0/KR05	P105	D05[A05/D05]	-	GTETRGA	GTIOC1A	-	-	TXD8/MOSI8/SDA8	-	-	SSLA2_A/QIO1	-	-	-	-	-
H1	71	44	44	-	IRQ1/KR04	P104	D04[A04/D04]	-	GTETRGB	GTIOC1B	-	-	RXD8/MISO8/SCL8	-	-	SSLA1_A/QIO0	-	-	-	-	-
H3	72	45	45	-	KR03	P103	D03[A03/D03]	-	GTOWUP	GTIOC2A_A	-	CTX0	CTS0_RTS0/SS0	-	-	SSLA0_A	-	-	-	-	-
J1	73	46	46	-	KR02	P102	D02[A02/D02]	AGTO0	GTOWLO	GTIOC2B_A	-	CRX0	SCK0	-	-	RSPCKA_A	-	-	ADTRG0	-	-
H2	74	47	47	-	IRQ1/KR01	P101	D01[A01/D01]	AGTEE0	GTETRGB	GTIOC5A	-	-	TXD0/MOSI0/SDA0	CTS1_RTS1/SS1	SDA1_B	MOSIA_A	-	-	-	-	-
H4	75	48	48	-	IRQ2/KR00	P100	D00[A00/D00]	AGTIO0	GTETRGA	GTIOC5B	-	-	RXD0/MISO0/SCL0	SCK1	SCL1_B	MISOA_A	-	-	-	-	-
K1	76	49	49	-	-	P500	-	AGTOA0	GTIU	GTIOC11A	-	USB_VBUSEN	-	-	-	QSPCLK	-	SD1CLK_A	AN016	IVREF0	-
J2	77	50	50	-	IRQ11	P501	-	AGTOB0	GTIV	GTIOC11B	-	USB_OVRCURA	-	-	-	QSSL	-	SD1CMD_A	AN116	IVREF1	-
K2	78	-	-	-	IRQ12	P502	-	-	GTIW	GTIOC12A	-	USB_OVRCURB	-	-	-	QIO0	-	SD1DAT0_A	AN017	IVCMP0	-
G4	79	-	-	-	-	P503	-	-	GTETRGC	GTIOC12B	-	USB_EXICEN	-	-	-	QIO1	-	SD1DAT1_A	AN117	-	-
G5	80	-	-	-	-	P504	ALE	-	GTETRGD	-	-	USB_ID	-	-	-	QIO2	-	SD1DAT2_A	AN018	-	-
G6	81	-	-	-	-	P508	-	-	-	-	-	-	-	-	-	-	-	SD1DAT3_A	AN020	-	-
K3	82	51	51	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	83	52	52	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J4	84	53	53	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-
K4	85	54	54	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-
J5	86	55	55	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K5	87	56	56	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H5	88	57	57	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H6	89	58	58	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J6	90	59	59	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K6	91	60	60	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J7	92	-	-	-	IRQ12-DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-
H7	93	-	-	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS100/AN107	-	-
G7	94	-	-	-	IRQ11-DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-
K7	95	-	-	-	IRQ10-DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-
J8	96	-	-	-	IRQ9-DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-
H8	97	61	61	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS000/AN007	-	-
K8	98	62	62	-	IRQ8-DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-

Pin number				Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	Timers				Communication interfaces							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
K9	99	63	63	-	IRQ7-DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-
K10	100	64	64	-	IRQ6-DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-

Note: Some pin names have the added suffix of _A and _B. When assigning the GPT, IIC, SPI, SSIE, and SDHI functionality, select the functional pins with the same suffix.

RA6M1 Group 1. Overview

针号				电源系统，时钟，调试，CAC	Interrupt	I/O port	外部总线	Timers				通讯接口							Analog		HMI
LGA100	LQFP100	LQFP64	QFN64					AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,8 (30 MHz)	SCI1,3,9 (30 MHz)	IIC	SPI, QSPI	SSIE	SDHI	ADC12	DAC12, ACMPHS	CTSU
K9	99	63	63	-	IRQ7-DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-
K10	100	64	64	-	IRQ6-DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-

Note: 一些引脚名称添加了_A和_B的后缀。在分配GPT、IIC、SPI、SSIE和SDHI功能时，选择具有相同后缀的功能管脚。

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$.

Figure 2.1 shows the timing conditions.

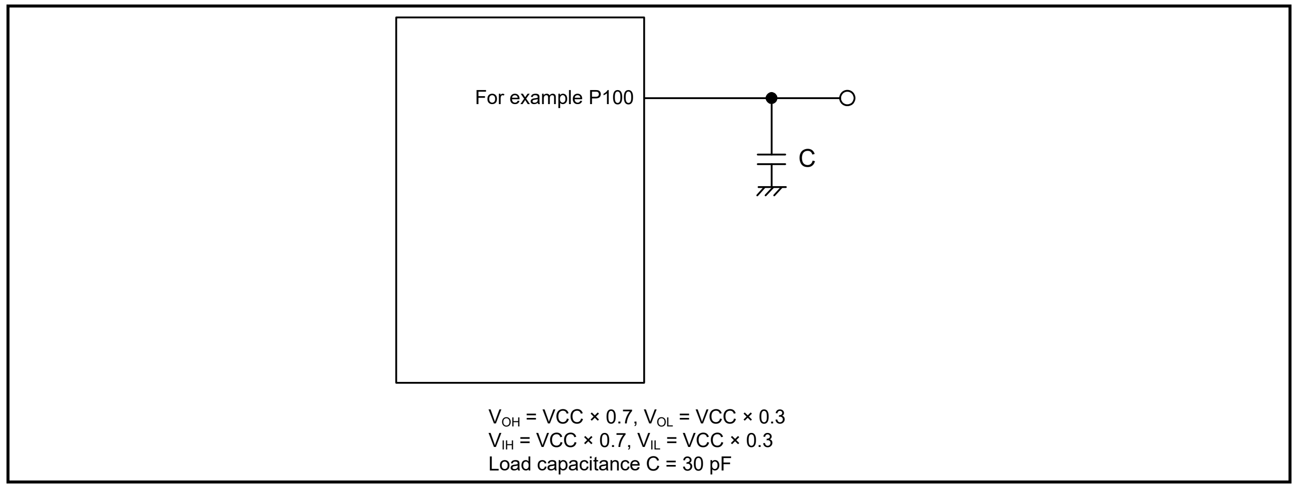


Figure 2.1 Input or output timing measurement conditions

The measurement conditions for the timing specification of each peripheral are recommended for the best peripheral operation. However, make sure to adjust the driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT power supply voltage	VBATT	-0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	-0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	-0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
Analog power supply voltage	AVCC0 *2	-0.3 to +4.0	V
Analog input voltage (except for P000 to P007)	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P007) when PGA differential input is disabled	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002, P004 to P006) when PGA differential input is enabled	V_{AN}	-1.3 to AVCC0 + 0.3	V
Analog input voltage (P003, P007) when PGA differential input is enabled	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3, *4, *5	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

2. 电气特性

除非另有规定，MCU的电气特性在以下条件下定义：

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$.

图2.1显示了时序条件。

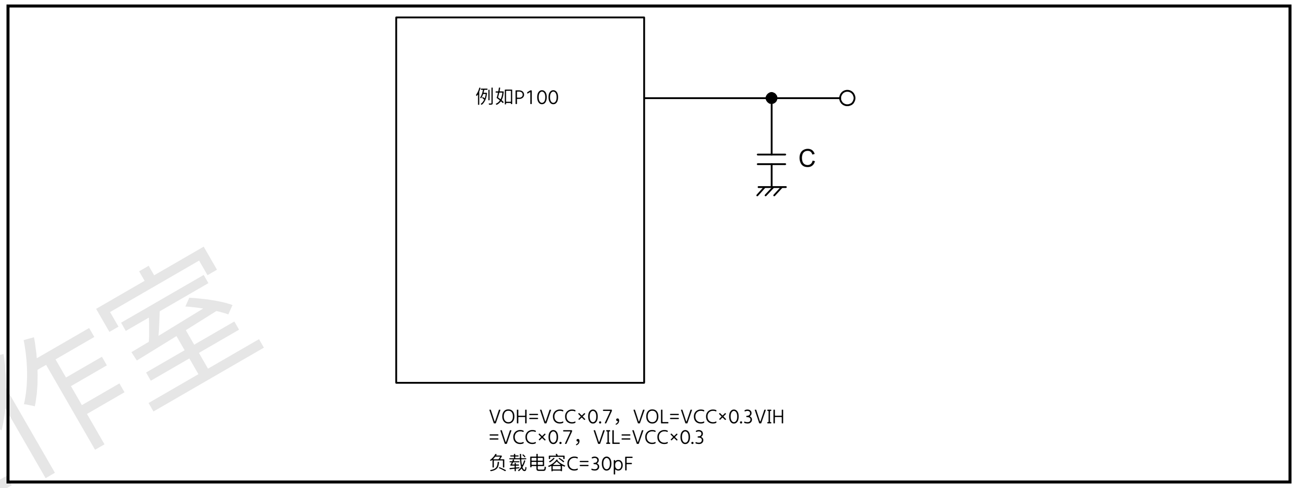


Figure 2.1 输入或输出定时测量条件

推荐每个外设时序规范的测量条件，以实现最佳外设操作。但是，请确保调整每个引脚的驱动能力以满足您系统的条件。

用于相同功能的每个功能引脚必须选择相同的驱动能力。如果各功能管脚的IO驱动能力混用，则无法保证各功能的AC规格。

2.1 绝对最大额定值

Table 2.1 绝对最大额定值

Parameter	Symbol	Value	Unit
电源电压	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT电源电压	VBATT	-0.3 to +4.0	V
输入电压（除了5V容限端口*1）	V_{in}	-0.3 to VCC + 0.3	V
输入电压（5V容限端口*1）	V_{in}	-0.3 to + VCC + 4.0 (max. 5.8)	V
参考电源电压	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
模拟电源电压	AVCC0 *2	-0.3 to +4.0	V
模拟输入电压（P000至P007除外）	V_{AN}	-0.3 to AVCC0 + 0.3	V
PGA差分输入禁用时的模拟输入电压（P000至P 007）	V_{AN}	-0.3 to AVCC0 + 0.3	V
启用PGA差分输入时的模拟输入电压（P000至P002 、P004至P006）	V_{AN}	-1.3 to AVCC0 + 0.3	V
PGA差分输入启用时的模拟输入电压(P003 P007)	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3, *4, *5	T_{opr}	-40 to +85 -40 to +105	°C
贮存温度	T_{stg}	-55 to +125	°C

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Note 1. Ports P205, P206, P400, P401, P407 to P415, and P708 are 5 V tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1, T_j/T_a Definition.
Note 4. Contact Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB is not used	2.7	-	3.6	V
		When USB is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB		-	VCC	-	V
	VSS_USB		-	0	-	V
VBATT power supply voltage	VBATT		1.8	-	3.6	V
Analog power supply voltages	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter, or the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) -40 to +105°C.

Parameter		Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	100-pin LQFP 64-pin LQFP	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode.
	64-pin QFN			117		
	100-pin LGA			105		

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W),
where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI (except RSPCK)	V_{IH}	VCC × 0.8	-	-	V
			V_{IL}	-	-	VCC × 0.2	
		D00 to D07	V_{IH}	VCC × 0.7	-	-	
			V_{IL}	-	-	VCC × 0.3	
		IIC (SMBus)*1	V_{IH}	2.1	-	-	
			V_{IL}	-	-	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	0.8	

Note 1. 端口P205、P206、P400、P401、P407至P415和P708可承受5V电压。
Note 2. 将AVCC0和VCC_USB连接到VCC。
Note 3. 请参阅第2.2.1节，TjTa定义。
Note 4. 有关Ta=+85°C至+105°C时降额操作的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。
Note 5. 工作温度上限为+85°C或+105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分 Numbering.

Table 2.2 推荐工作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC	不使用USB时	2.7	-	3.6	V
		使用USB时	3.0	-	3.6	V
	VSS		-	0	-	V
USB电源电压	VCC_USB		-	VCC	-	V
	VSS_USB		-	0	-	V
VBATT电源电压	VBATT		1.8	-	3.6	V
模拟电源电压	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. 将AVCC0连接到VCC。不使用AD转换器、DA转换器或比较器时，请勿离开AVCC0、VREFHVREFH0、AVSS0和VREFLVREFL0引脚打开。将AVCC0和VREFHVREFH0引脚分别连接到VCC，将AVSS0和VREFLVREFL0引脚分别连接到VSS。

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics
条件：工作温度(Ta)-40至+105°C的产品。

Parameter		Symbol	Typ	Max	Unit	测试条件
允许结温	100-pin LQFP 64-pin LQFP	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode.
	64-pin QFN			117		
	100-pin LGA			105		

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+ICCmax×VCC。工作温度上限为+85°C或+105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分

Numbering.

2.2.2 I O V I H

Table 2.4 IOVIH VIL(1of2)

Parameter			Symbol	Min	Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外设功能引脚	EXTAL（外部时钟输入）、WAIT、SPI（RSPCK除外）	V_{IH}	VCC × 0.8	-	-	V
			V_{IL}	-	-	VCC × 0.2	
		D00 to D07	V_{IH}	VCC × 0.7	-	-	
			V_{IL}	-	-	VCC × 0.3	
		IIC (SMBus)*1	V_{IH}	2.1	-	-	
			V_{IL}	-	-	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
			V_{IL}	-	-	0.8	

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*1			V_{IH}	VCC × 0.7	-	-	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2			V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		5 V-tolerant ports*3, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	When using the battery backup function	When VBATT power supply is selected	V_{IH}	VBATT × 0.8	-	VBATT + 0.3	
					V_{IL}	-	-	VBATT × 0.2	
					ΔV_T	VBATT × 0.05	-	-	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or VBATT + 0.3 V	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
			When not using the battery backup function		V_{IH}	VCC × 0.8	-	VCC + 0.3	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		Other input pins*4			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
	Ports	5 V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.2	
		Other input pins*6			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	

Note 1. SCL1_B, SDA1_B (total 2 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A (total 6 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P708 (total 15 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P708 (total 14 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the breakdown voltage.

Table 2.4 IOVIH VIL(2of2)

Parameter					Symbol	Min	Typ	Max	Unit
施密特触发器输入电压	外设功能引脚	IIC (except for SMBus)*1			V_{IH}	VCC × 0.7	-	-	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2			V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		5 V-tolerant ports*3, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	使用电池备份功能时	选择VBATT电源时	V_{IH}	VBATT × 0.8	-	VBATT + 0.3	
					V_{IL}	-	-	VBATT × 0.2	
					ΔV_T	VBATT × 0.05	-	-	
				选择VCC电源时	V_{IH}	VCC × 0.8	-	更高的电压VCC+0.3V或VBATT+0.3 V	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
			不使用电池备份功能时		V_{IH}	VCC × 0.8	-	VCC + 0.3	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		其他输入引脚*4			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
	Ports	5 V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.2	
		其他输入引脚*6			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	

Note 1. SCL1_B, SDA1_B (total 2 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A (total 6 pins).
Note 3. RES和与P205、P206、P400、P401、P407到P415、P708相关的外围功能引脚（共15个引脚）。
Note 4. 除表中已描述的外围功能引脚外的所有输入引脚。
Note 5. P205, P206, P400, P401, P407 to P415, P708 (total 14 pins).
Note 6. 除表中已描述的端口外的所有输入引脚。
Note 7. 当VCC小于2.7V时，耐5V端口的输入电压应小于3.6V，否则可能发生击穿，因为5V耐压端口是电控的，不会违反击穿电压。

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008, P201	-	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P008, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value of total of all pins)	Maximum of all output pins		$\Sigma I_{OH (max)}$	-	-	-80	mA
			$\Sigma I_{OL (max)}$	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. Except for P000 to P007, P200, which are input ports.

2.2.3 我爱我哦

Table 2.5 我爱我哦

Parameter			Symbol	Min	Typ	Max	Unit
允许输出电流（每个引脚的平均值）	Ports P008, P201	-	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	端口P205、P206、P407至P415、P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	其他输出引脚*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
允许输出电流（每个引脚的最大值）	Ports P008, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	端口P205、P206、P407至P415、P602, P708 (total 13 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	其他输出引脚*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
允许输出电流（所有引脚总和的最大值）	所有输出引脚的最大值		$\Sigma I_{OH (max)}$	-	-	-80	mA
			$\Sigma I_{OL (max)}$	-	-	80	mA

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流是指在100µs内测得的电流平均值。

Note 1. 这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 3. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 4. 除了P000至P007、P200为输入端口。

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*1		V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	Ports P205, P206, P407 to P415, P602, P708 (total of 13 pins)*2		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P002, P004 to P006, P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)			-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to P7 (except for ports P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P401		C_{in}	-	-	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Other input pins			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. P0nPFS.ASEL(n = 3 or 7) = 1
Note 4. P0nPFS.ASEL(n = 3 or 7) = 0

2.2.4 IOVOH VOL和其他特性

Table 2.6 IOVOH、VOL和其他特性

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
输出电压	IIC		V_{OL}	-	-	0.4	V	我OL=3.0毫安
			V_{OL}	-	-	0.6		我OL=6.0毫安
	IIC*1		V_{OL}	-	-	0.4		IOL=15.0mA(ICFER.FMPE=1)
			V_{OL}	-	0.4	-		IOL=20.0mA(ICFER.FMPE=1)
	端口P205、P206、P407至P415、P602、P708（共13针）*2		V_{OH}	VCC - 1.0	-	-		我OH=−20毫安VCC=3.3V
			V_{OL}	-	-	1.0		我OL=20毫安VCC=3.3V
	其他输出引脚		V_{OH}	VCC - 0.5	-	-		IOH=−1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
输入漏电流	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	端口P000至P002、P004至P006、P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5 V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	其他端口（端口P000至P007、P200除外）			-	-	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0至P7（端口除外 P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
输入电容	USB_DP、USB_DM和端口 P003, P007, P014, P015, P400, P401		C_{in}	-	-	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	其他输入引脚			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。
Note 3. P0nPFS.ASEL(n = 3 or 7) = 1
Note 4. P0nPFS.ASEL(n = 3 or 7) = 0

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	87	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	17	-		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	24	-		
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	12	-		
		Sleep mode*5, *6			-	9	33.5		
		Increase during BGO operation	Data flash P/E		-	6	-		
			Code flash P/E		-	8	-		
	Low-speed mode*5				-	1.2	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	1.0	-		ICLK = 32.768 kHz
	Software Standby mode				-	1.3	13		Ta ≤ 85°C
					-	1.3	21		Ta ≤ 105°C
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	28	65	μA	Ta ≤ 85°C
					-	28	93		Ta ≤ 105°C
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		-	11.6	28		Ta ≤ 85°C
					-	11.6	32		Ta ≤ 105°C
			Power-on reset circuit low power function enabled		-	4.9	21		Ta ≤ 85°C
					-	4.9	26		Ta ≤ 105°C
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	4.4	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	1.4	-		-
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		-	0.9	-		VBATT = 1.8 V, VCC = 0 V
					-	1.1	-		VBATT = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.0	-		VBATT = 1.8 V, VCC = 0 V
					-	1.6	-		VBATT = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1 unit)				-	100	150	μA	-
	Temperature sensor				-	0.1	0.2	mA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)*7				-	2	8	μA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	μA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.5	μA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.5	μA	-
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)			AI_{REFH}	-	70	120	μA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.4	mA	-
			With AMP ouput		-	0.1	0.4	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion				-	0.07	0.8	μA	-
	ADC12 unit 1 in standby modes				-	0.07	0.8	μA	-

2.2.5 工作和待机电流

Table 2.7 工作和待机电流(1of2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
供电电流*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	87	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	17	-		
		正常模式	启用所有外设时钟，同时(1)代码从闪存执行*4		-	24	-		
			禁用所有外设时钟，同时(1)代码从闪存执行*5、*6		-	12	-		
		Sleep mode*5, *6			-	9	33.5		
		BGO运行期间增加	数据闪存PE		-	6	-		
			代码闪存PE		-	8	-		
	Low-speed mode*5				-	1.2	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	1.0	-		ICLK = 32.768 kHz
	软件待机模式				-	1.3	13		Ta ≤ 85°C
					-	1.3	21		Ta ≤ 105°C
	深度软件待机模式	为备用SRAM和USB恢复检测单元供电			-	28	65	μA	Ta ≤ 85°C
					-	28	93		Ta ≤ 105°C
		未向SRAM或USB恢复检测单元供电	上电复位电路低功耗功能禁用		-	11.6	28		Ta ≤ 85°C
					-	11.6	32		Ta ≤ 105°C
			上电复位电路低功耗功能启用		-	4.9	21		Ta ≤ 85°C
					-	4.9	26		Ta ≤ 105°C
		RTC和AGT运行时增加	使用低速片上振荡器(LOCO)时		-	4.4	-		-
			当使用用于低时钟负载的晶体振荡器时		-	1.0	-		-
			当使用标准时钟负载的晶体振荡器时		-	1.4	-		-
	VCC关闭时RTC运行（具有电池备份功能，只有RTC和副时钟振荡器运行）		当使用用于低时钟负载的晶体振荡器时		-	0.9	-		VBATT = 1.8 V, VCC = 0 V
					-	1.1	-		VBATT = 3.3 V, VCC = 0 V
			当使用用标准时钟负载的晶体振荡器时		-	1.0	-		VBATT = 1.8 V, VCC = 0 V
					-	1.6	-		VBATT = 3.3 V, VCC = 0 V
模拟电源电流	在12位AD转换期间			AI_{CC}	-	0.8	1.1	mA	-
	在使用SHamp进行12位AD转换期间				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1 unit)				-	100	150	μA	-
	温度感应器				-	0.1	0.2	mA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.2	mA	-
			带AMP输出		-	0.6	1.1	mA	-
	等待AD、DA转换（所有单位）				-	0.9	1.6	mA	-
	ADC12、DAC12处于待机模式（所有单元）*7				-	2	8	μA	-
参考电源电流(VREFH0)	在12位AD转换期间（单元0）			AI_{REFH0}	-	70	120	μA	-
	等待12位AD转换（单元0）				-	0.07	0.5	μA	-
	ADC12处于待机模式（单元0）				-	0.07	0.5	μA	-
参考电源电流(VREFH)	在12位AD转换期间（单元1）			AI_{REFH}	-	70	120	μA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.4	mA	-
			带AMP输出		-	0.1	0.4	mA	-
	等待12位AD（单元1）、DA（所有单元）转换				-	0.07	0.8	μA	-
	ADC12单元1处于待机模式				-	0.07	0.8	μA	-

Table 2.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
USB operating current	Low speed	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
	Full speed	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)
I_{CC} Max. = 0.53 x f + 23 (maximum operation in High-speed mode)
I_{CC} Typ. = 0.08 x f + 2.4 (normal operation in High-speed mode)
I_{CC} Typ. = 0.1 x f + 1.1 (Low-speed mode)
I_{CC} Max. = 0.09 x f + 23 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D Converter 1 Module Stop bit) are in the module-stop state.
See section 42.6.8, Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107 in User's Manual.

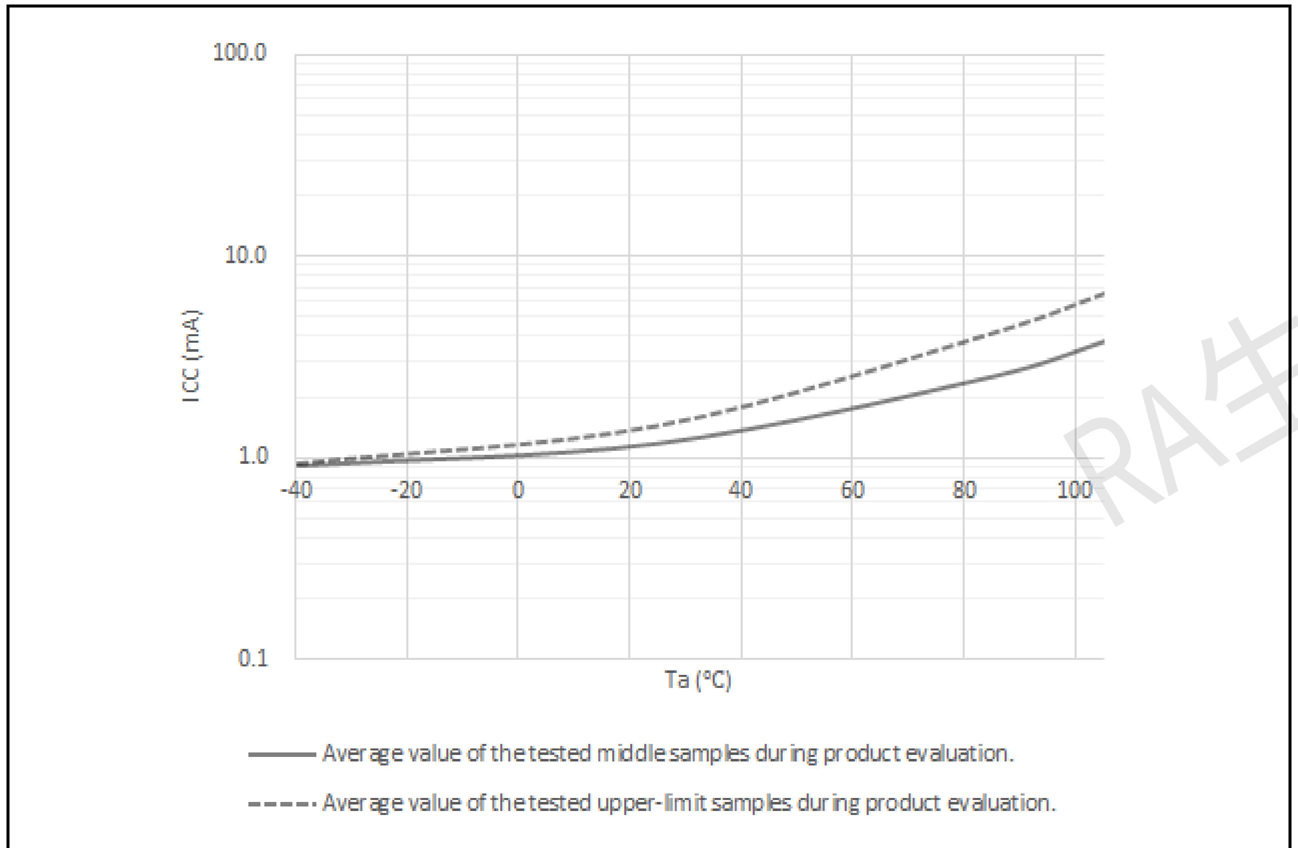


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

Table 2.7 工作和待机电流(2of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
USB工作电流	低速	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
	全速	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB

Note 1. 电源电流值是在所有输出引脚空载且所有输入上拉MOS晶体管处于关闭状态的情况下。
Note 2. 使用提供给外围功能的时钟进行测量。这不包括BGO操作。
Note 3. ICC取决于f(ICLK)如下。（ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK=2:2:1:1:2:1:1）
我CC最大。=0.53xf+23（高速模式下的最大操作）
我CC典型。=0.08xf+2.4（高速模式下的正常操作）
I_{CC} Typ. = 0.1 x f + 1.1 (Low-speed mode)
I_{CC} Max. = 0.09 x f + 23 (Sleep mode).
Note 4. 这不包括BGO操作。
Note 5. 在该状态下停止向外围设备提供时钟信号。这不包括BGO操作。
Note 6. FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频(3.75MHz)。
Note 7. 当MCU处于软件待机模式或MSTPCRD.MSTPD16（12位AD转换器0模块停止位）和MSTPCRD.MSTPD15（12位AD转换器1模块停止位）处于模块停止状态。
请参阅第42.6.8节，AN000至AN002、AN007、AN100至AN102和AN107的可用功能和寄存器设置
User's Manual.

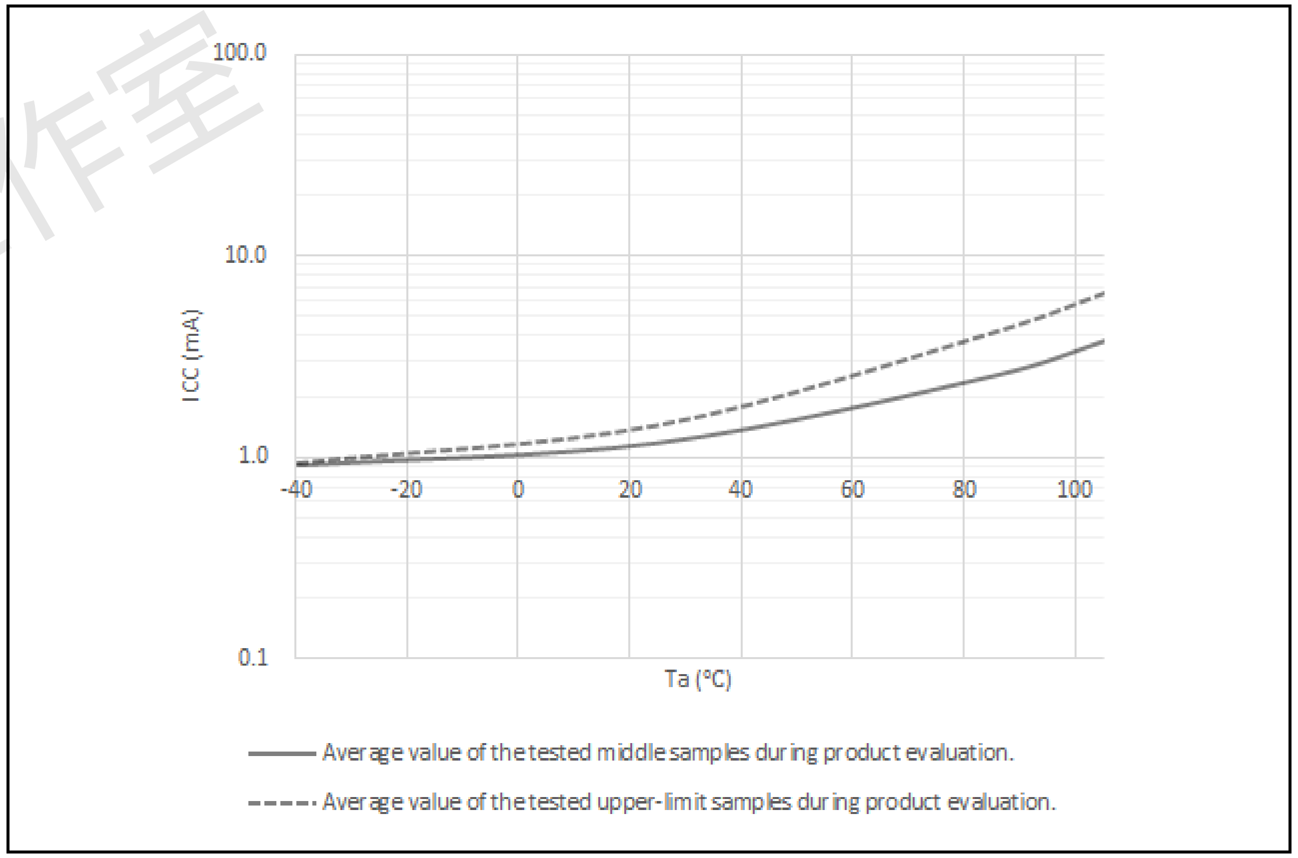


Figure 2.2 软件待机模式下的温度依赖性（参考数据）

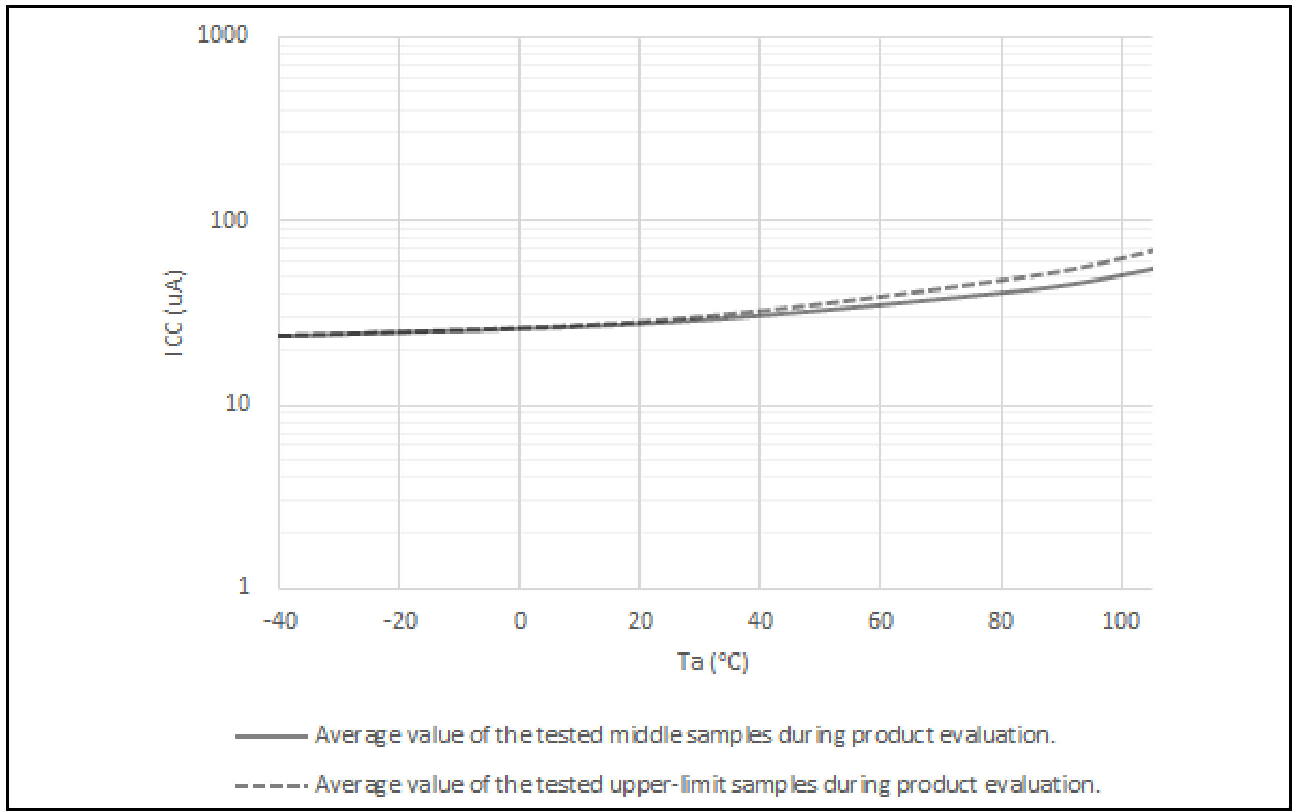


Figure 2.3 **Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)**

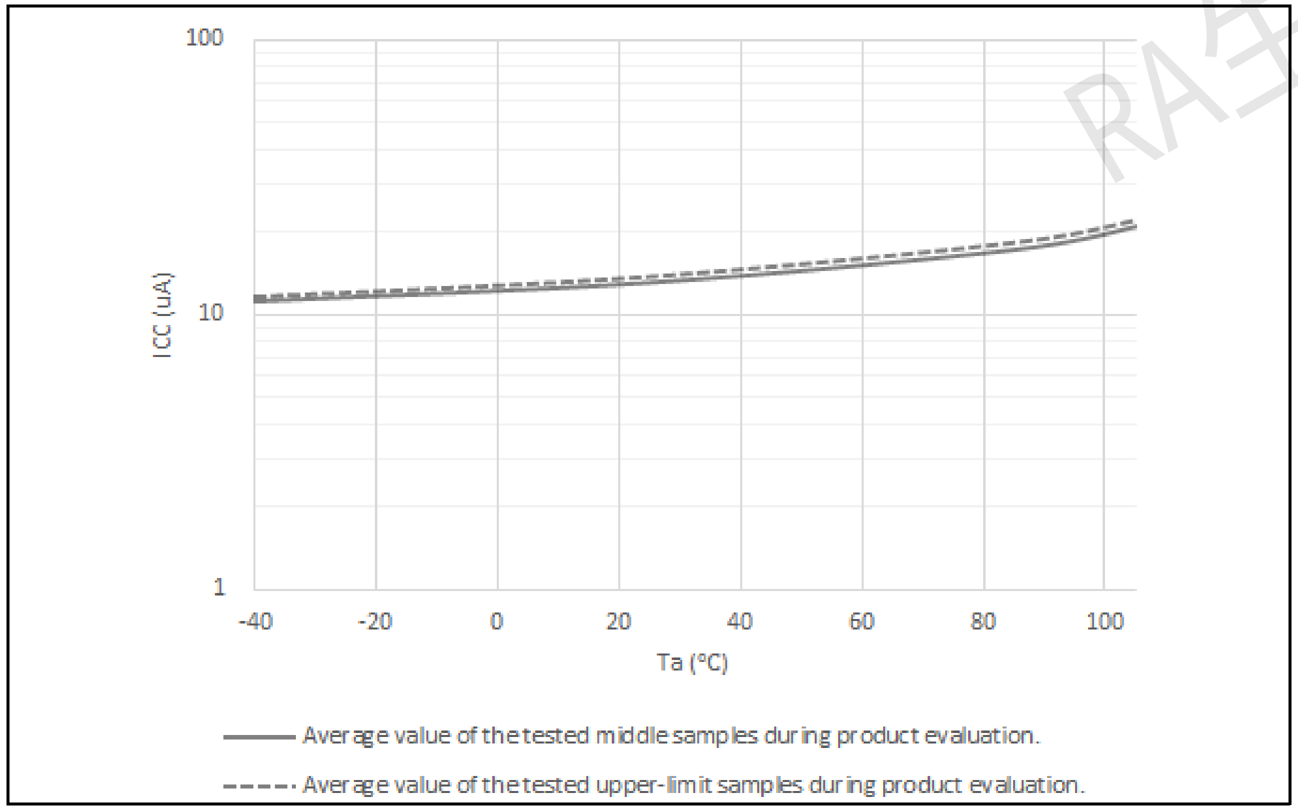


Figure 2.4 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)**

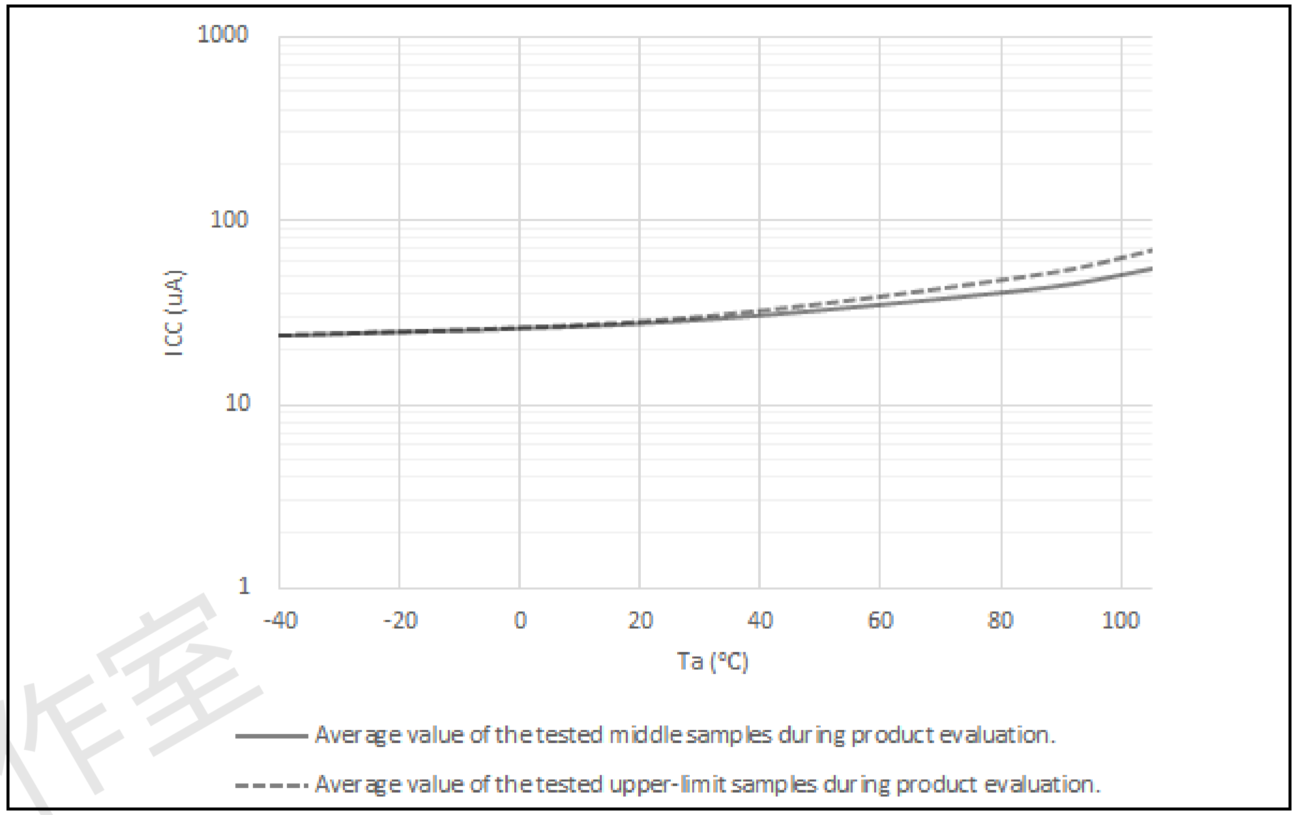


Figure 2.3 **深度软件待机模式下的温度依赖性，为待机SRAM供电和USB恢复检测单元（参考数据）**

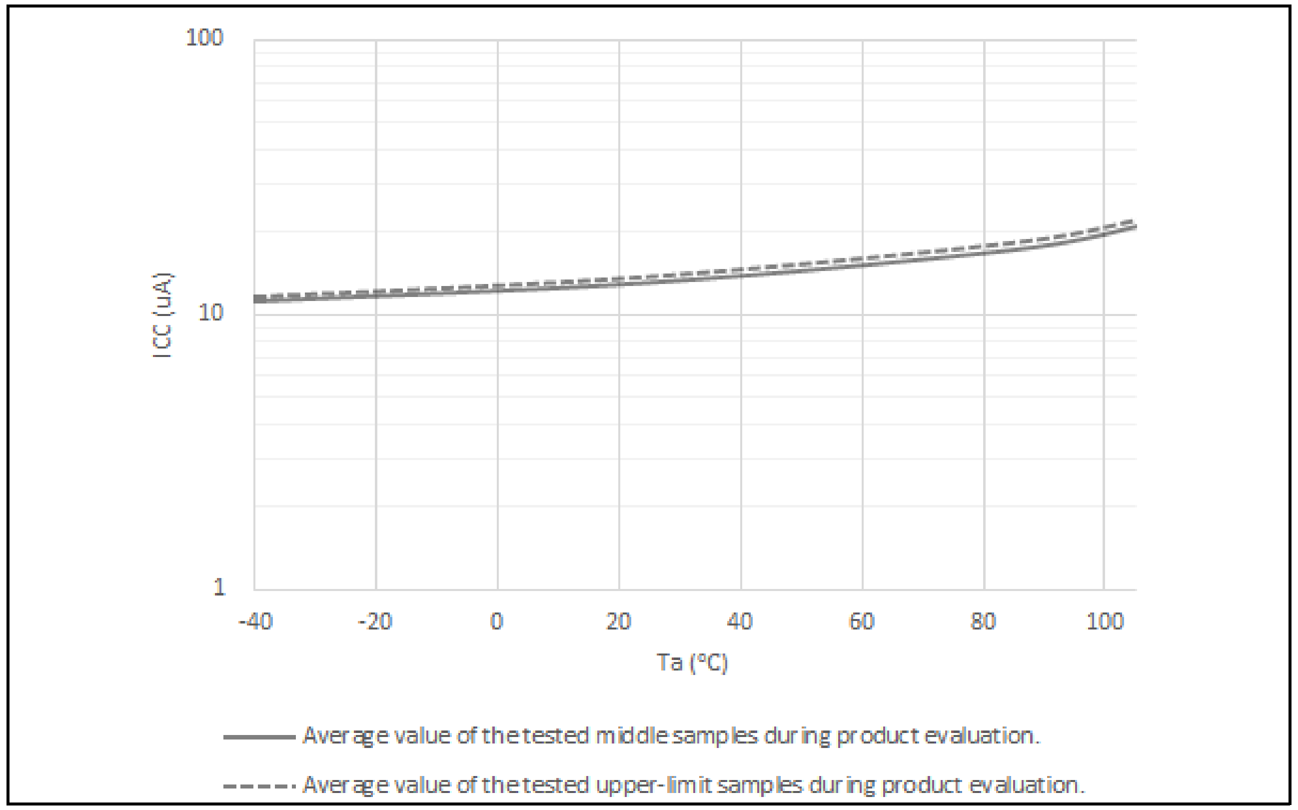


Figure 2.4 **深度软件待机模式下的温度依赖性、未向SRAM或USB恢复检测单元供电、上电复位电路低功耗功能禁用（参考数据）**

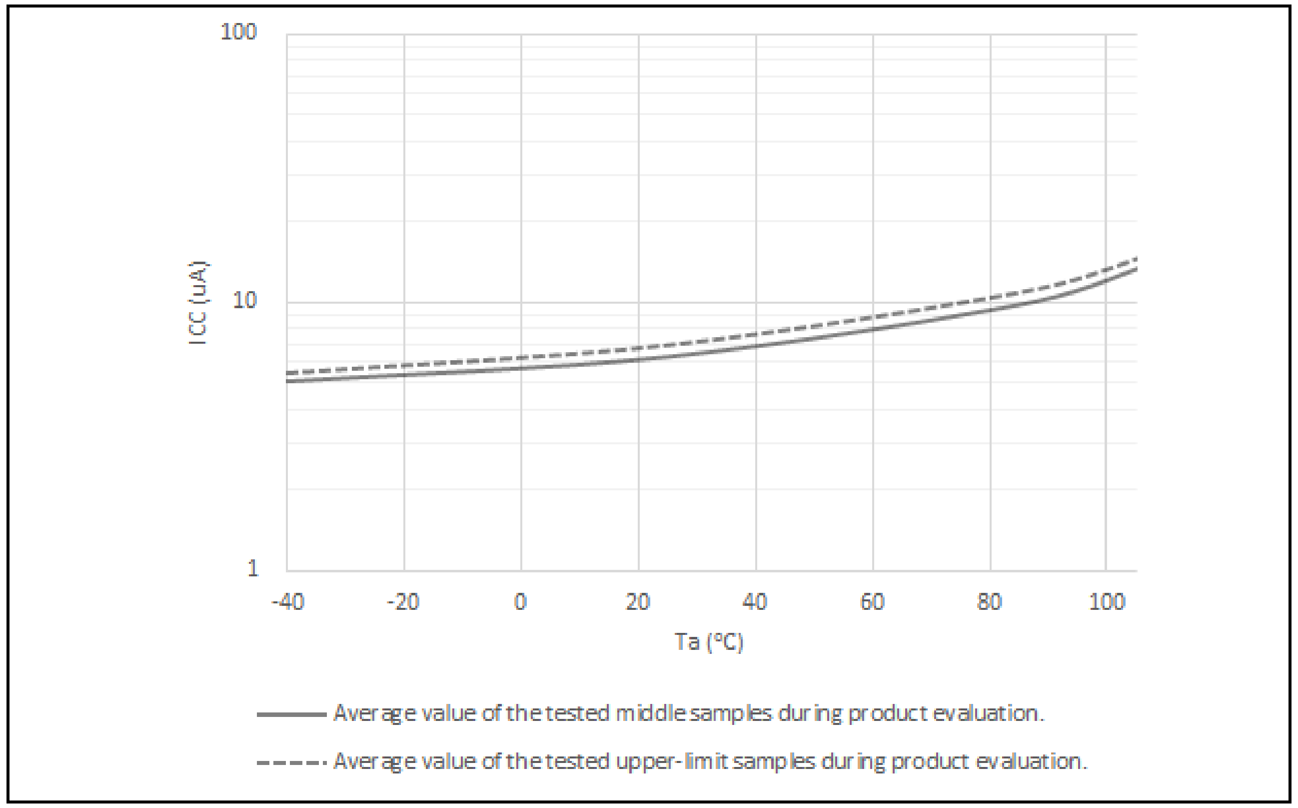


Figure 2.5 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)**

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.8 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V	-
	Voltage monitor 0 reset enabled at startup		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

Table 2.9 Rise and fall gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.2
		-	-	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.08
		-	-	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.06
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

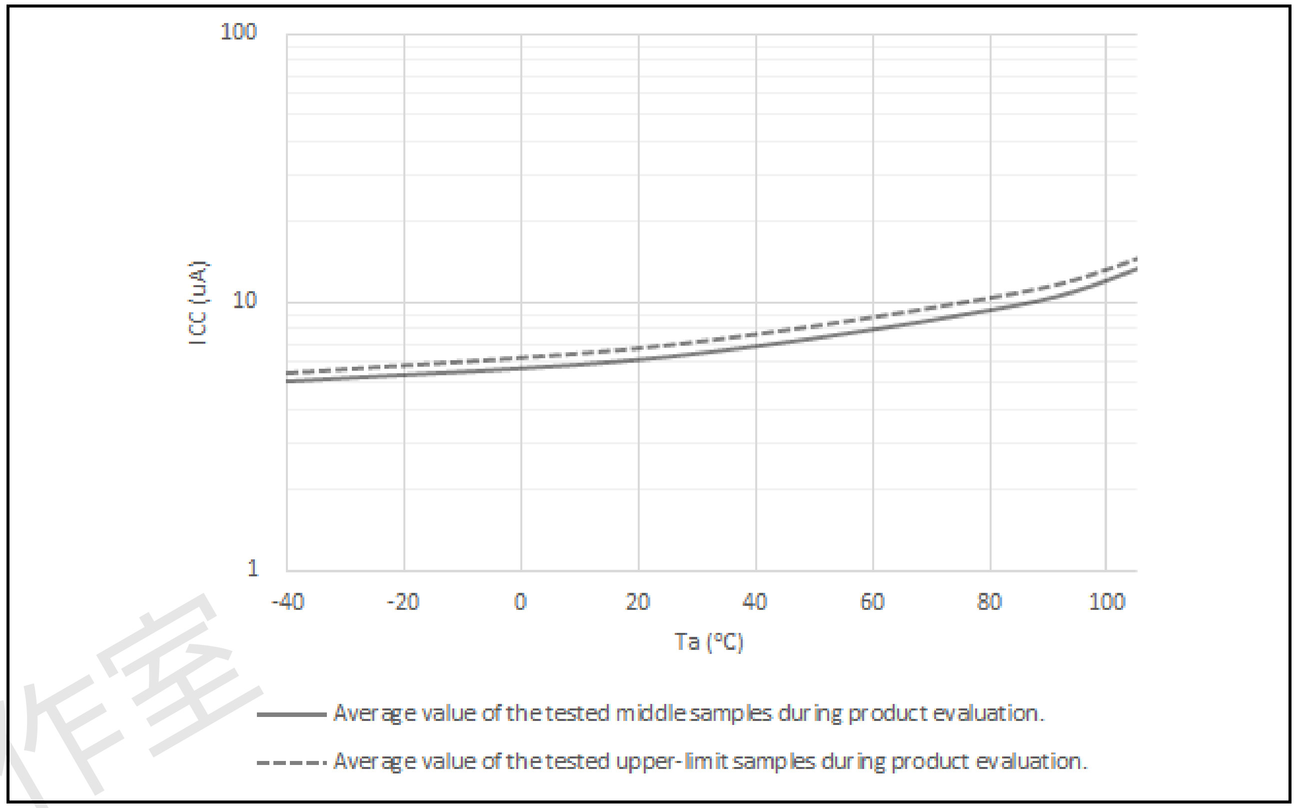


Figure 2.5 **深度软件待机模式下的温度依赖性、未向SRAM或USB恢复检测单元供电、启用上电复位电路低功耗功能（参考数据）**

2.2.6 VCC上升和下降梯度和纹波频率

Table 2.8 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	-	20	ms/V	-
	启动时启用电压监视器0复位		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. 在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。
Note 2. 这适用于使用VBATT时。

Table 2.9 升降梯度和纹波频率特性

纹波电压必须在VCC上限(3.6V)和下限(2.7V)之间的范围内满足允许的纹波频率fr(VCC)。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.2
		-	-	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.08
		-	-	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq$ VCC × 0.06
允许电压变化上升下降梯度	dt/dVCC	1.0	-	-	ms/V	当VCC变化超过VCC±10%

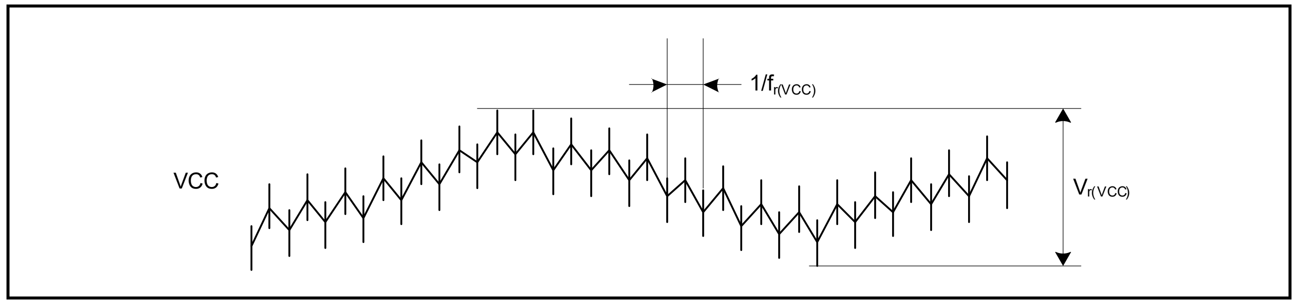


Figure 2.6 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)	f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2		-	-	120	
	Peripheral module clock (PCLKB)*2		-	-	60	
	Peripheral module clock (PCLKC)*2		-*3	-	60	
	Peripheral module clock (PCLKD)*2		-	-	120	
	Flash interface clock (FCLK)*2		-*1	-	60	
	External bus clock (BCLK)*2		-	-	120	
	EBCLK pin output		-	-	60	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2,*3		-*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	
	External bus clock (BCLK)		-	-	1	
	EBCLK pin output		-	-	1	

Note 1. Programming or erasing the flash memory is disabled in Low-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

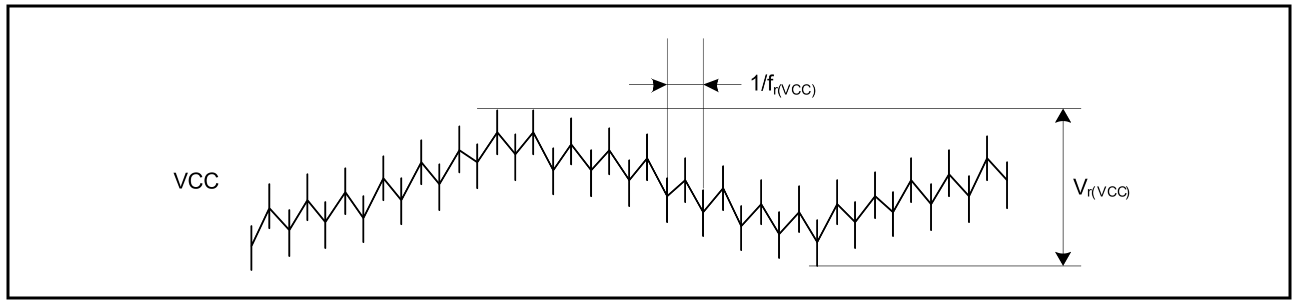


Figure 2.6 纹波波形

2.3 交流特性

2.3.1 Frequency

Table 2.10 高速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK*2)	f	-	-	120	MHz
	外设模块时钟(PCLKA)*2		-	-	120	
	外设模块时钟(PCLKB)*2		-	-	60	
	外设模块时钟(PCLKC)*2		-*3	-	60	
	外设模块时钟(PCLKD)*2		-	-	120	
	闪存接口时钟(FCLK)*2		-*1	-	60	
	外部总线时钟(BCLK)*2		-	-	120	
	EBCLK引脚输出		-	-	60	

Note 1. 在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. 使用ADC12时，PCLKC频率必须至少为1MHz。

Table 2.11 低速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	-	-	1	MHz
	外设模块时钟(PCLKA)*2		-	-	1	
	外设模块时钟(PCLKB)*2		-	-	1	
	外设模块时钟(PCLKC)*2 *3		-*3	-	1	
	外设模块时钟(PCLKD)*2		-	-	1	
	Flash接口时钟(FCLK)*1 *2		-	-	1	
	外部总线时钟(BCLK)		-	-	1	
	EBCLK引脚输出		-	-	1	

Note 1. 编程或擦除闪存在低速模式下被禁用。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. 使用ADC12时，PCLKC频率必须设置为至少1MHz。

Table 2.12 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	29.4	-	36.1	kHz
	Peripheral module clock (PCLKA)*2		-	-	36.1	
	Peripheral module clock (PCLKB)*2		-	-	36.1	
	Peripheral module clock (PCLKC)*2,*3		-	-	36.1	
	Peripheral module clock (PCLKD)*2		-	-	36.1	
	Flash interface clock (FCLK)*1, *2		29.4	-	36.1	
	External bus clock (BCLK)*2		-	-	36.1	
	EBCLK pin output		-	-	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time		t_{Bcyc}	16.6	-	-	ns	Figure 2.7
EBCLK pin output high pulse width		t_{CH}	3.3	-	-	ns	
EBCLK pin output low pulse width		t_{CL}	3.3	-	-	ns	
EBCLK pin output rise time		t_{Cr}	-	-	5.0	ns	
EBCLK pin output fall time		t_{Cf}	-	-	5.0	ns	
EXTAL external clock input cycle time		t_{EXcyc}	41.66	-	-	ns	Figure 2.8
EXTAL external clock input high pulse width		t_{EXH}	15.83	-	-	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	-	-	ns	
EXTAL external clock rise time		t_{EXr}	-	-	5.0	ns	
EXTAL external clock fall time		t_{EXf}	-	-	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	-	24	MHz	-
Main clock oscillation stabilization wait time (crystal) *1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.9
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	-
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	-	-	60.4	μs	Figure 2.10
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	-
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	-	-	15.0	μs	-
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		-40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	-	-	64.7	μs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-

Table 2.12 Subosc-speed模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	29.4	-	36.1	kHz
	外设模块时钟(PCLKA)*2		-	-	36.1	
	外设模块时钟(PCLKB)*2		-	-	36.1	
	外设模块时钟(PCLKC)*2 *3		-	-	36.1	
	外设模块时钟(PCLKD)*2		-	-	36.1	
	Flash接口时钟(FCLK)*1 *2		29.4	-	36.1	
	外部总线时钟(BCLK)*2		-	-	36.1	
	EBCLK引脚输出		-	-	36.1	

Note 1. 在Subosc速度模式下，禁止对闪存进行编程或擦除。
Note 2. 关于ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率。
Note 3. ADC12不能使用。

2.3.2 时钟时序

Table 2.13 除副时钟振荡器外的时钟时序（2个中的1个）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
EBCLK引脚输出周期时间		t_{Bcyc}	16.6	-	-	ns	Figure 2.7
EBCLK引脚输出高脉冲宽度		t_{CH}	3.3	-	-	ns	
EBCLK引脚输出低脉冲宽度		t_{CL}	3.3	-	-	ns	
EBCLK引脚输出上升时间		t_{Cr}	-	-	5.0	ns	
EBCLK引脚输出下降时间		t_{Cf}	-	-	5.0	ns	
EXTAL外部时钟输入周期时间		t_{EXcyc}	41.66	-	-	ns	Figure 2.8
EXTAL外部时钟输入高脉冲宽度		t_{EXH}	15.83	-	-	ns	
EXTAL外部时钟输入低脉冲宽度		t_{EXL}	15.83	-	-	ns	
EXTAL外部时钟上升时间		t_{EXr}	-	-	5.0	ns	
EXTAL外部时钟下降时间		t_{EXf}	-	-	5.0	ns	
主时钟振荡器频率		f_{MAIN}	8	-	24	MHz	-
主时钟振荡稳定等待时间（晶振）*1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.9
LOCO时钟振荡频率		f_{LOCO}	29.4912	32.768	36.0448	kHz	-
LOCO时钟振荡稳定等待时间		t_{LOCOWT}	-	-	60.4	μs	Figure 2.10
ILOCO时钟振荡频率		f_{ILOCO}	13.5	15	16.5	kHz	-
MOCO时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO时钟振荡稳定等待时间		t_{MOCOWT}	-	-	15.0	μs	-
HOCO时钟振荡器振荡频率	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		-40≤Ta≤105°C副时钟频率精度为±50ppm。
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO时钟振荡稳定等待时间*2		t_{HOCOWT}	-	-	64.7	μs	-
FLL稳定等待时间		t_{FLLWT}	-	-	1.8	ms	-
锁相环时钟频率		f_{PLL}	120	-	240	MHz	-

Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
PLL clock oscillation stabilization wait time	t_{PLLWT}	-	-	174.9	μs	Figure 2.11

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*1	s	Figure 2.12

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

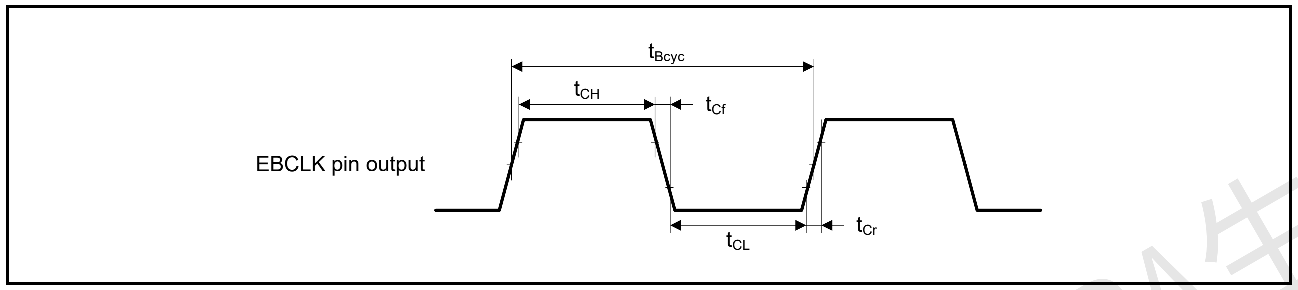


Figure 2.7 EBCLK output timing

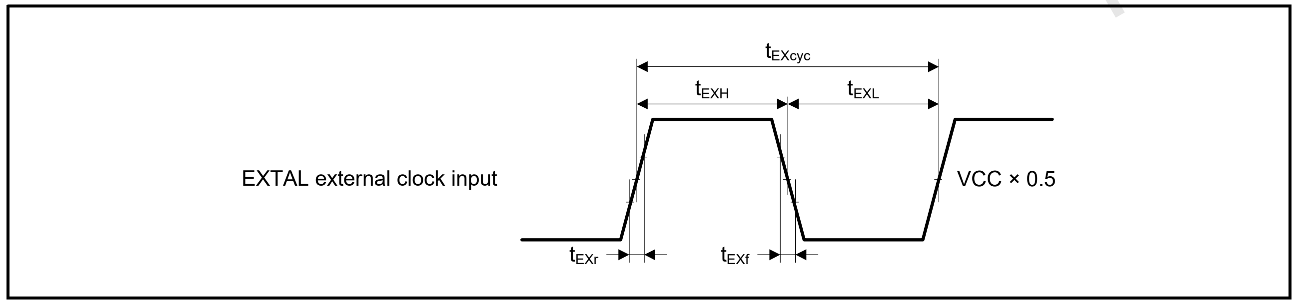


Figure 2.8 EXTAL external clock input timing

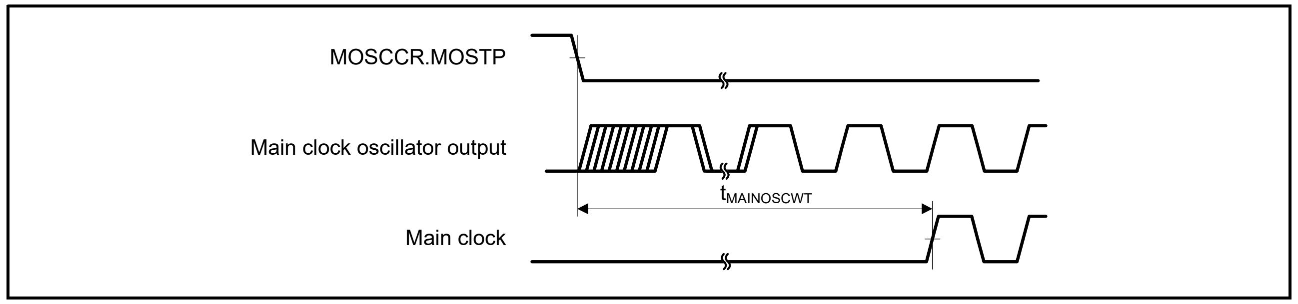


Figure 2.9 Main clock oscillation start timing

Table 2.13 除副时钟振荡器外的时钟时序(2of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
PLL时钟振荡稳定等待时间	t_{PLLWT}	-	-	174.9	μs	Figure 2.11

Note 1. 设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

Note 2. 这是从复位状态释放到HOCO振荡频率(fHOCO)达到保证工作范围的时间。

Table 2.14 副时钟振荡器的时钟时序

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
副时钟振荡稳定等待时间	$t_{SUBOSCWT}$	-	-	-*1	s	Figure 2.12

Note 1. 设置副时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。更改SOSCCR.SOSTP位的设置以启动副时钟操作后，只有在副时钟振荡稳定时间过去并留有足够余量后才开始使用副时钟振荡器。建议使用两倍于显示值的值。

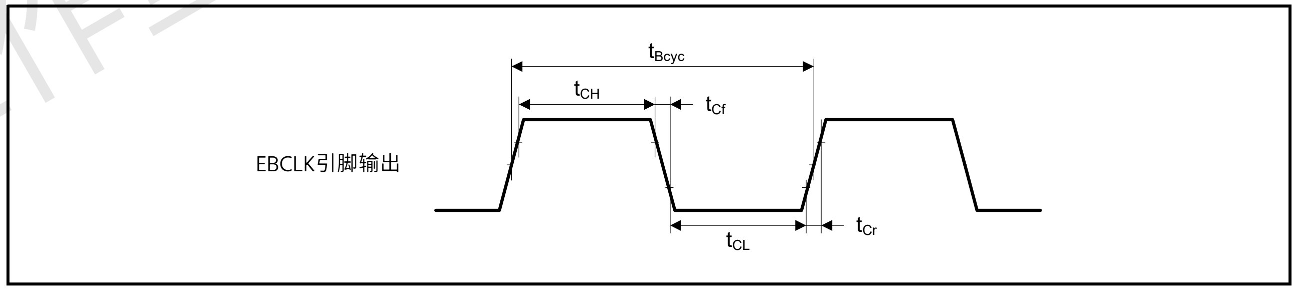


Figure 2.7 EBCLK输出时序

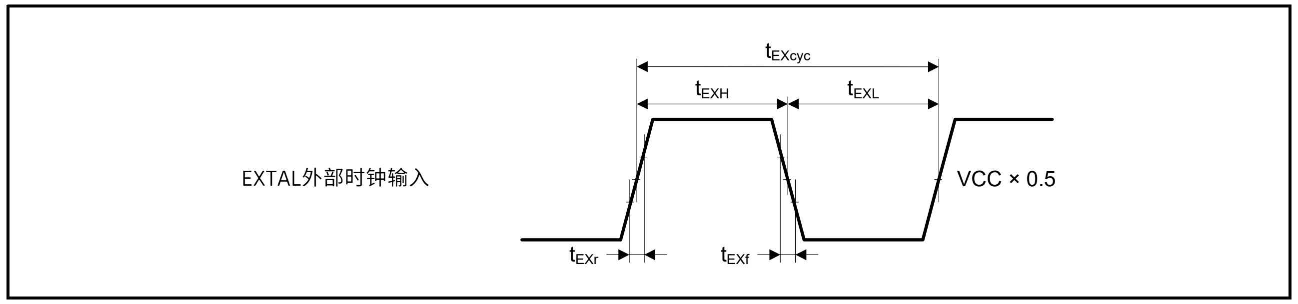


Figure 2.8 EXTAL外部时钟输入时序

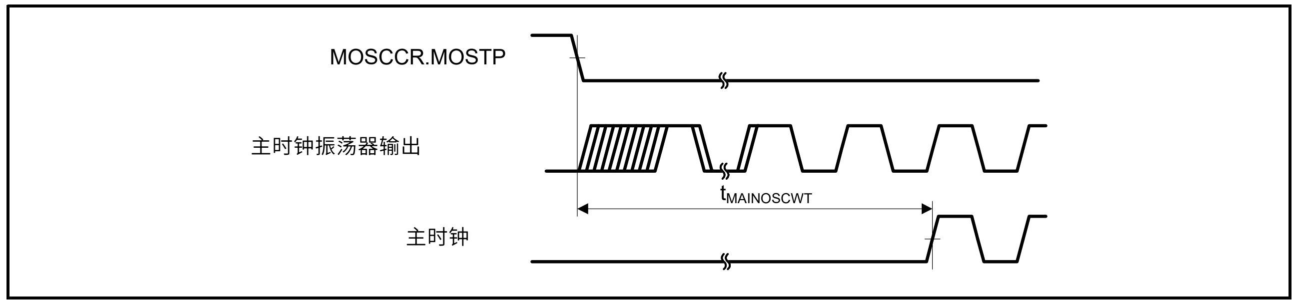


Figure 2.9 主时钟振荡开始时序

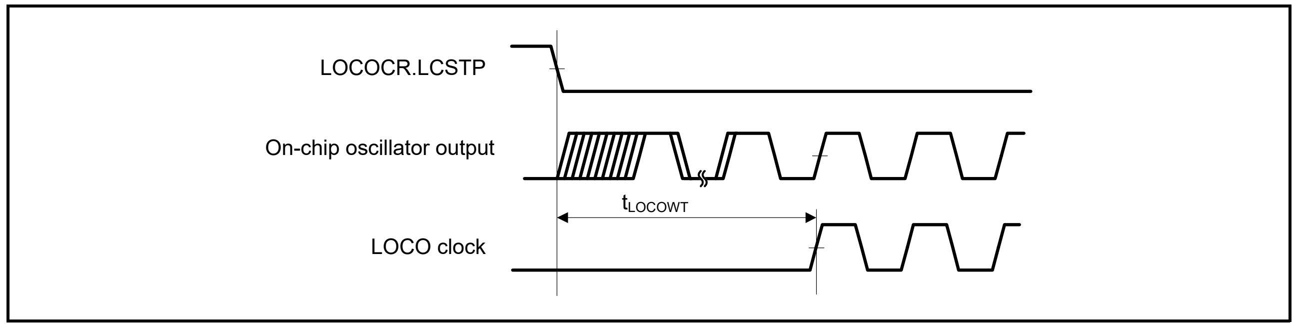


Figure 2.10 LOCO clock oscillation start timing

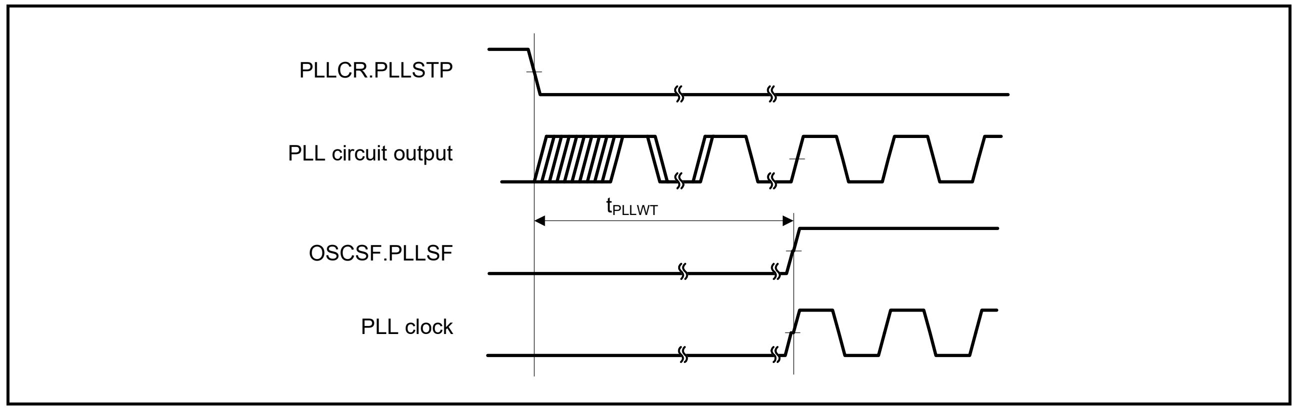


Figure 2.11 PLL clock oscillation start timing

Note: Only operate the PLL after the main clock oscillation has stabilized.

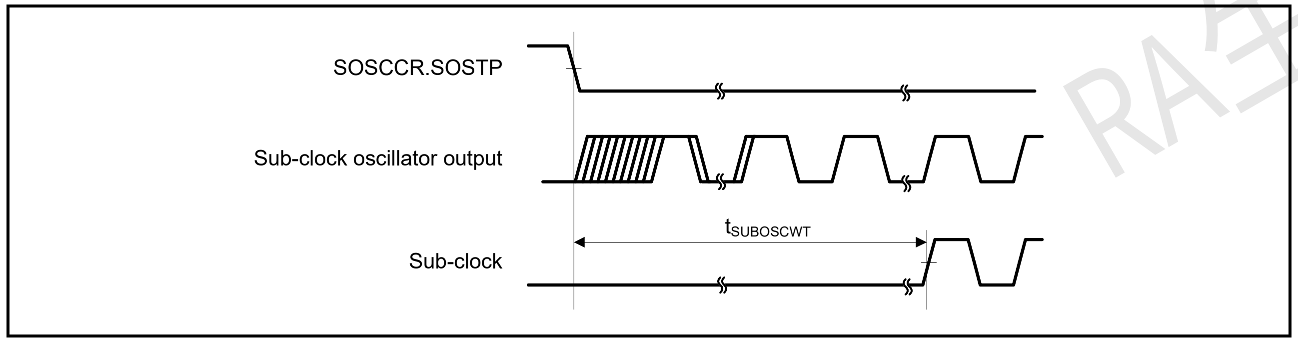


Figure 2.12 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.13
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 2.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	μs	
Wait time after RES cancellation		t_{RESWT}	-	29	32	μs	Figure 2.13

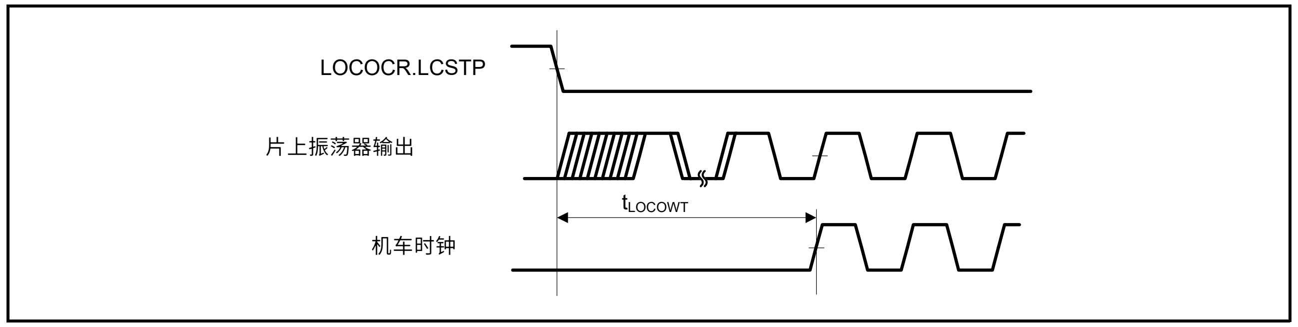


Figure 2.10 LOCO时钟振荡开始时序

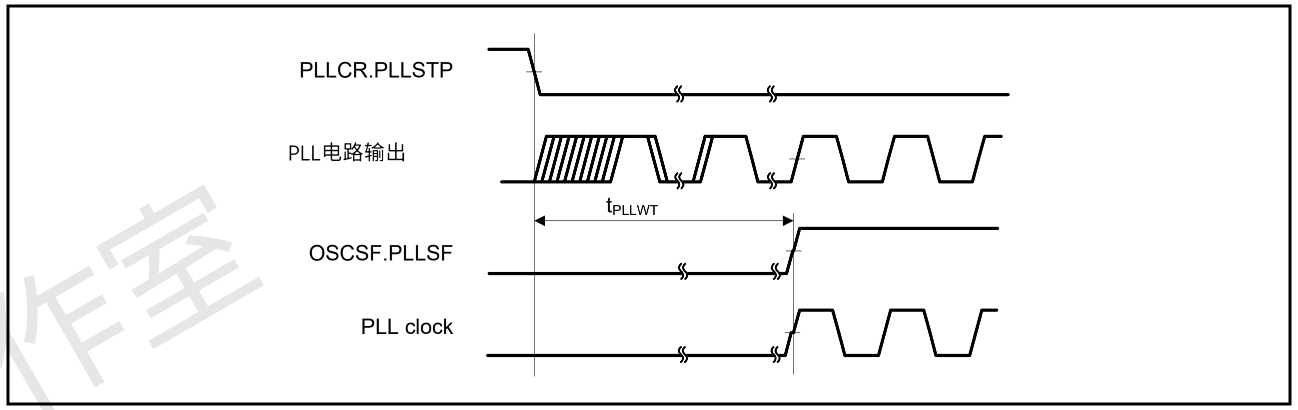


Figure 2.11 PLL时钟振荡开始时序

Note: 仅在主时钟振荡稳定后操作PLL。

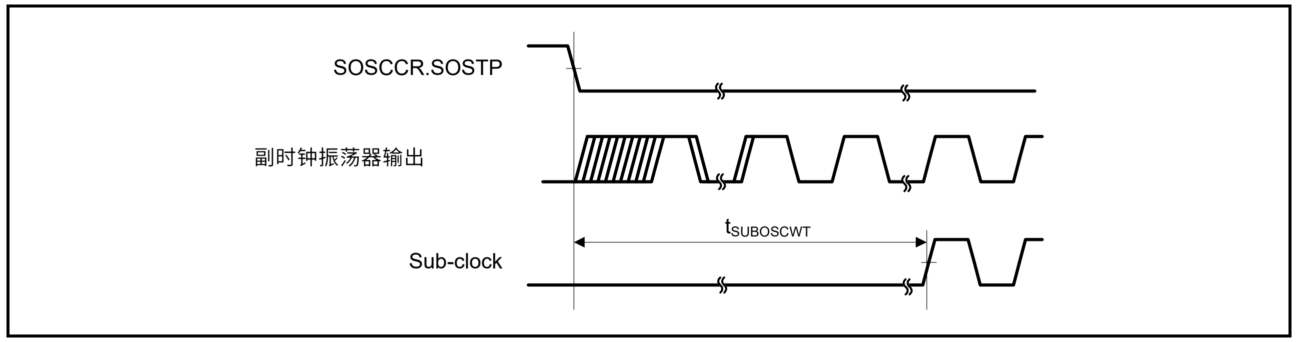


Figure 2.12 副时钟振荡开始时序

2.3.3 重置时间

Table 2.15 重置时间(1of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.13
	深度软件待机模式	t_{RESWD}	0.6	-	-	ms	Figure 2.14
	软件待机模式，Subosc速度模式	t_{RESWS}	0.3	-	-	ms	
	所有其他	t_{RESW}	200	-	-	μs	
RES取消后的等待时间		t_{RESWT}	-	29	32	μs	Figure 2.13

Table 2.15 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)	t_{RESW2}	-	320	390	μs	-

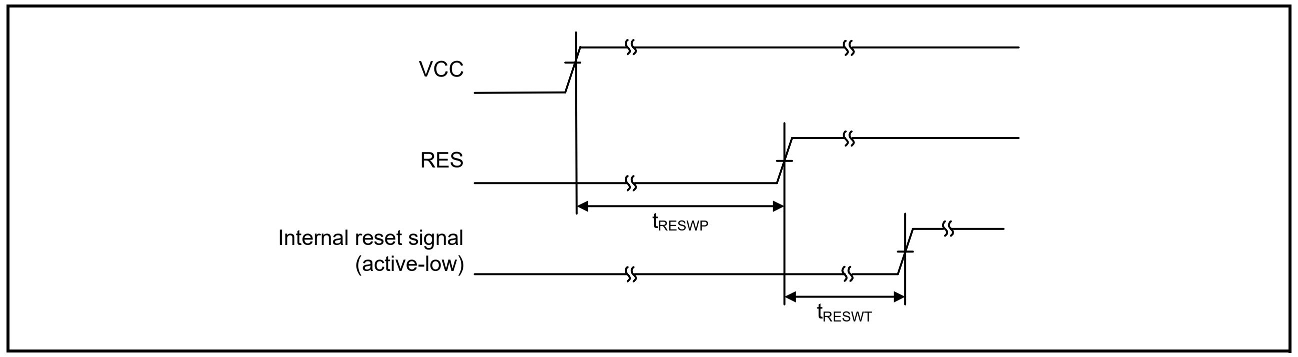


Figure 2.13 Power-on reset timing

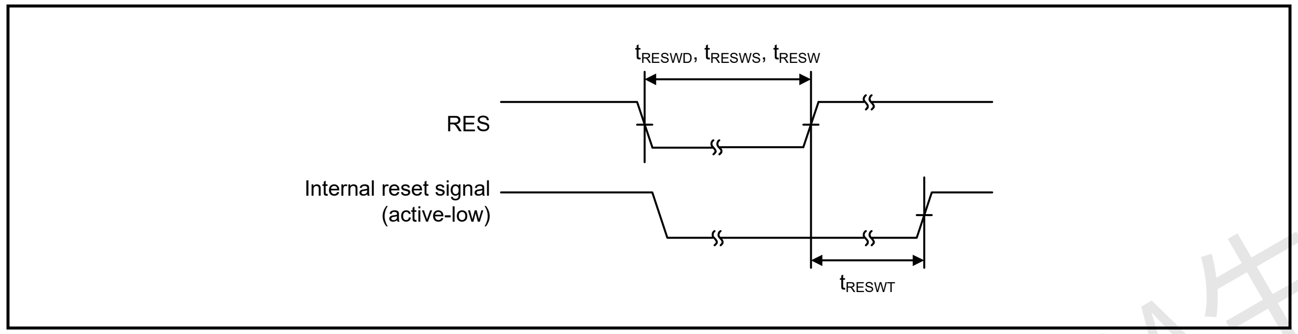


Figure 2.14 Reset input timing

2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 2.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	μs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	μs	
	System clock source is sub-clock oscillator*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	System clock source is HOCO*6		t_{SBYHO}	-	240*9, *10	300 *9, *10	μs	
	System clock source is MOCO*7		t_{SBYMO}	-	220*9	300*9	μs	

Table 2.15 重置时间（2之2）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
内部复位取消后的等待时间（IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主MPU错误复位、总线从MPU错误复位、堆栈指针错误复位）	t_{RESW2}	-	320	390	μs	-

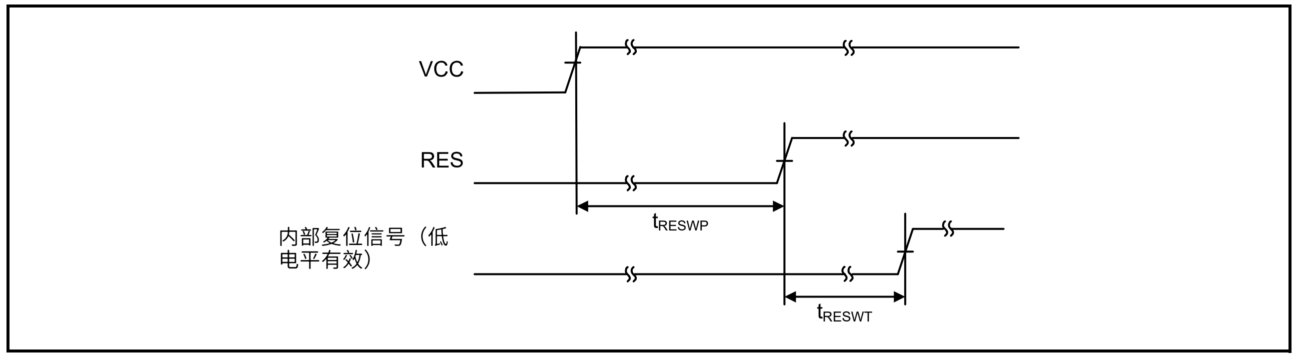


Figure 2.13 上电复位时序

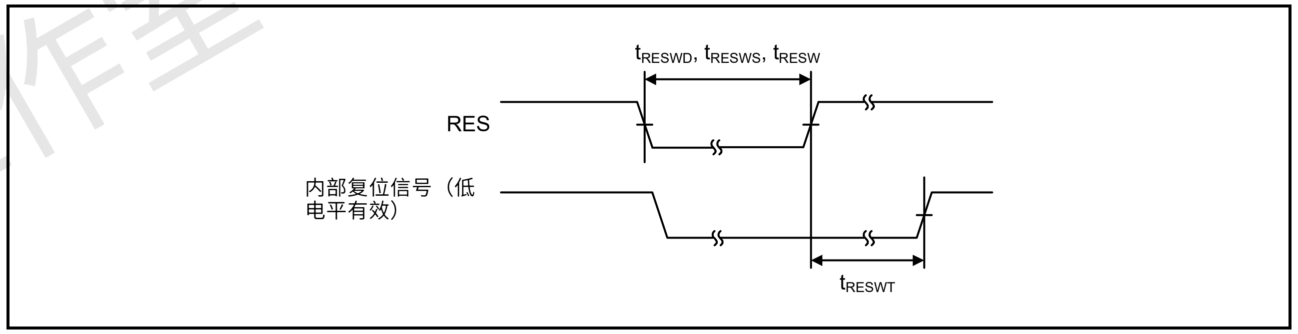


Figure 2.14 复位输入时序

2.3.4 唤醒时间

Table 2.16 从低功耗模式恢复的时间（2个中的1个）

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	图2.15所有振荡器的分频比为1。
		系统时钟源是带有主时钟振荡器的PLL*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器*4	t_{SBYEX}	-	230*9	280*9	μs	
		系统时钟源是带有主时钟振荡器*5的PLL	t_{SBYPE}	-	570*9	700*9	μs	
	系统时钟源为副时钟振荡器*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	系统时钟源为LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	系统时钟源为HOCO*6		t_{SBYHO}	-	240*9, *10	300 *9, *10	μs	
	系统时钟源为MOCO*7		t_{SBYMO}	-	220*9	300*9	μs	

Table 2.16 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode		t_{DSBY}	-	0.65	1.0	ms	Figure 2.16
Wait time after cancellation of Deep Software Standby mode		t_{DSBYWT}	34	-	35	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	-	35*9, *10	70 *9, *10	μs	Figure 2.17
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	-	11*9	14*9	μs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 6. The HOCO frequency is 20 MHz.
Note 7. The MOCO frequency is 8 MHz.
Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 μs (typical), 34 μs (maximum)
STCONR.STCON[1:0] = 11b:16 μs (typical), 104 μs (maximum).
Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 μs (typical) or 18 μs (maximum) is added as the HOCO wait time.

Table 2.16 从低功耗模式恢复的时间（2个中的2个）

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
从深度软件待机模式恢复时间		t_{DSBY}	-	0.65	1.0	ms	Figure 2.16
取消深度软件待机模式后的等待时间		t_{DSBYWT}	34	-	35	t_{cyc}	
从软件待机模式恢复到贪睡模式	系统时钟源为HOCO(20MHz)时的高速模式	t_{SNZ}	-	35*9, *10	70 *9, *10	μs	Figure 2.17
	系统时钟源为MOCO(8MHz)时的高速模式	t_{SNZ}	-	11*9	14*9	μs	

Note 1. 恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=振荡器作为系统时钟源的恢复时间+任何需要比系统时钟源更长稳定时间的振荡器的最长振荡稳定时间+2个LOCO周期（当LOCO运行时）+3个SOSC周期（当Subosc正在振荡且MSTPC0=0（CAC模块停止）时）。

Note 2. 当晶振频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 3. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 4. 当外部时钟频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为00h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=00h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=00h))

Note 5. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为00h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=00h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=00h))

Note 6. HOCO频率为20MHz。
Note 7. MOCO频率为8MHz。
Note 8. 在Subosc速度模式下，副时钟振荡器或LOCO在软件待机模式下继续振荡。
Note 9. 当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：
STCONR.STCON[1:0] = 00b:16 μs (typical), 34 μs (maximum)
STCONR.STCON[1:0] = 11b:16 μs (typical), 104 μs (maximum).
注10.当SNZCR.RXDREQEN位设置为0时，添加16μs（典型值）或18μs（最大值）作为HOCO等待时间。

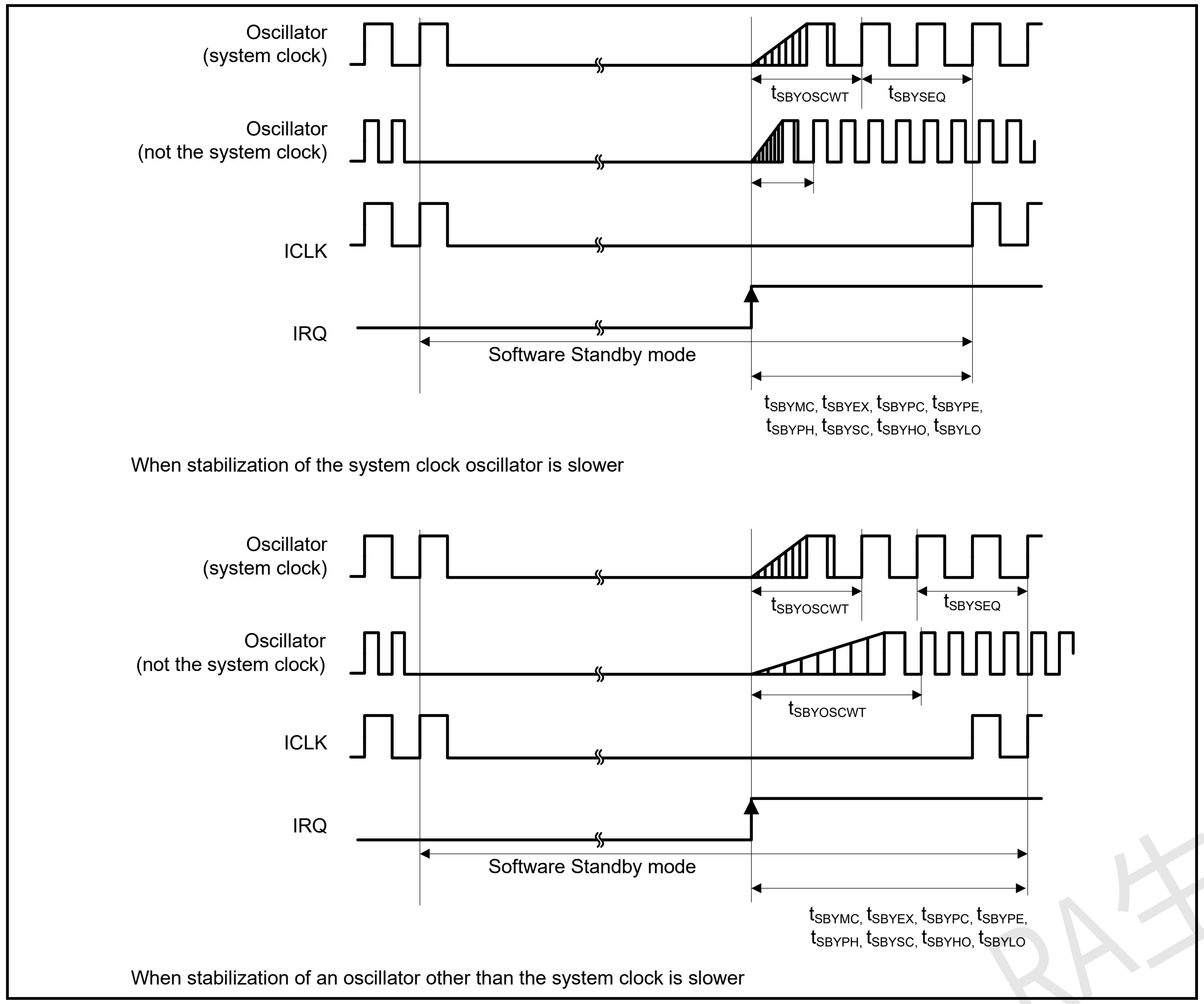


Figure 2.15 Software Standby mode cancellation timing

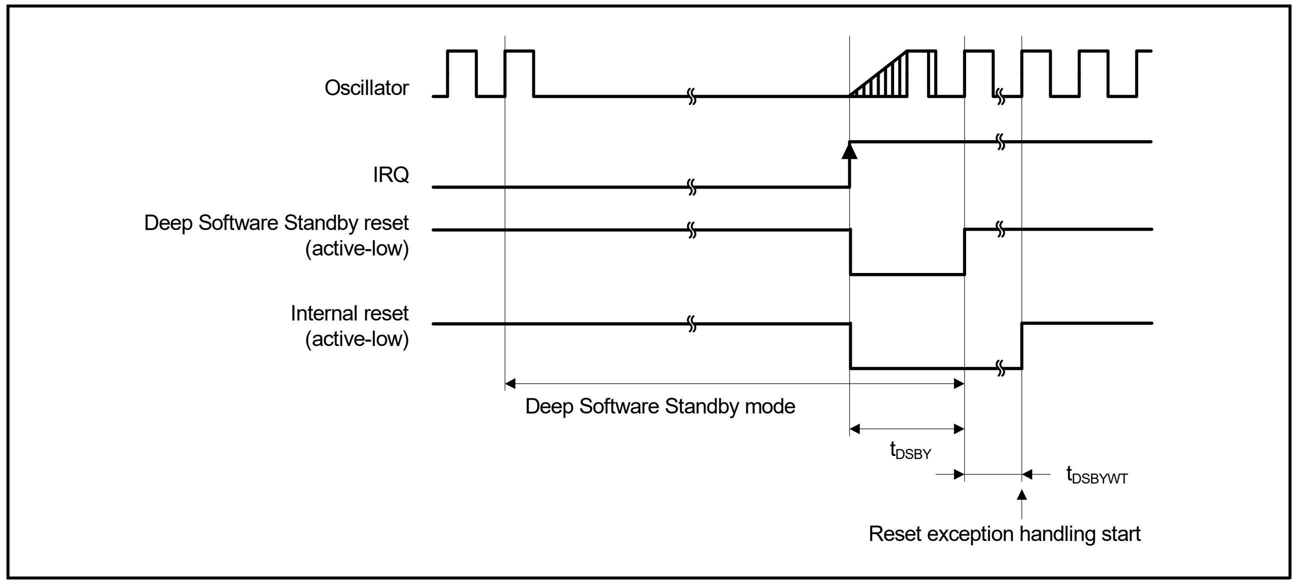


Figure 2.16 Deep Software Standby mode cancellation timing

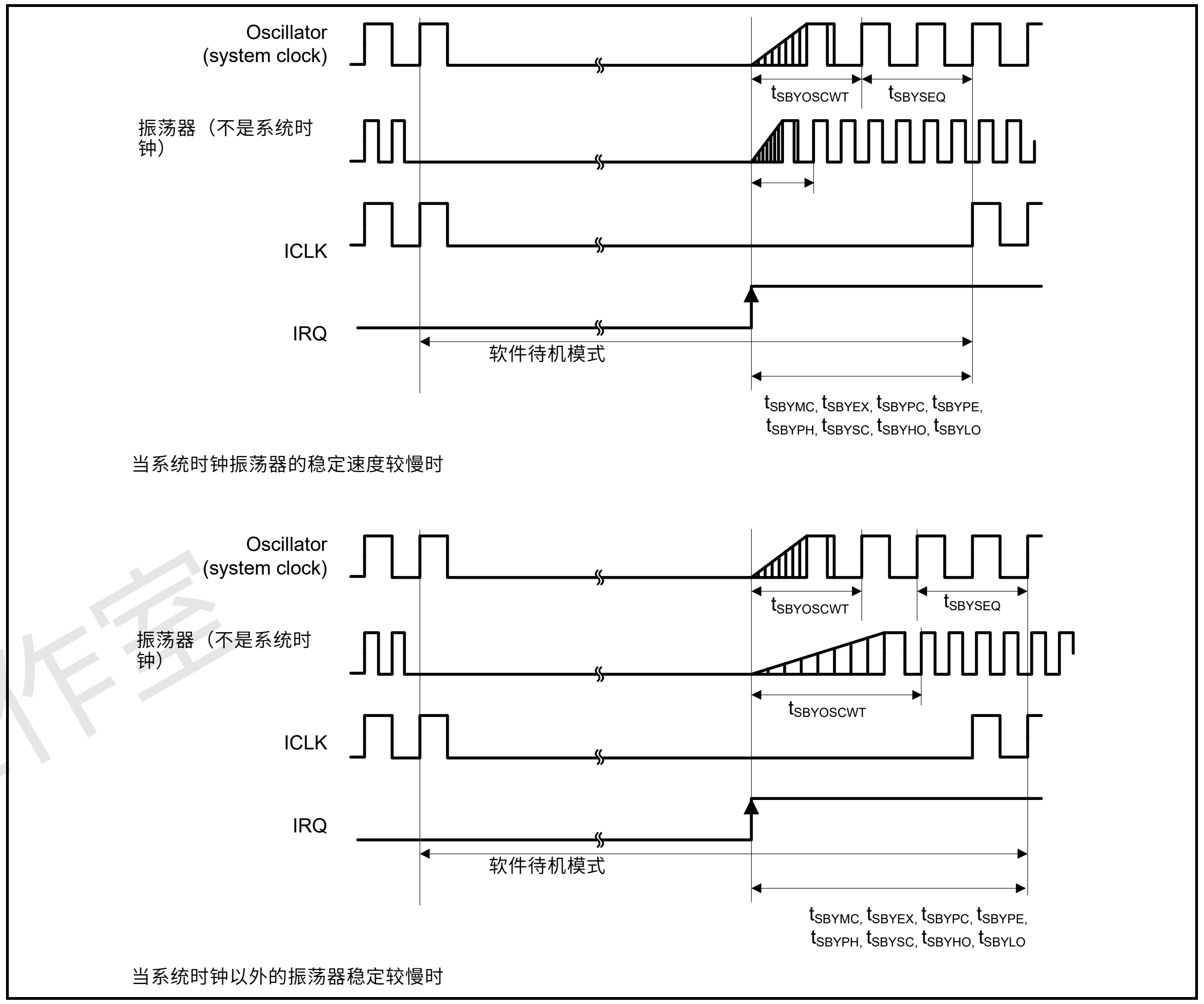


Figure 2.15 软件待机模式取消时序

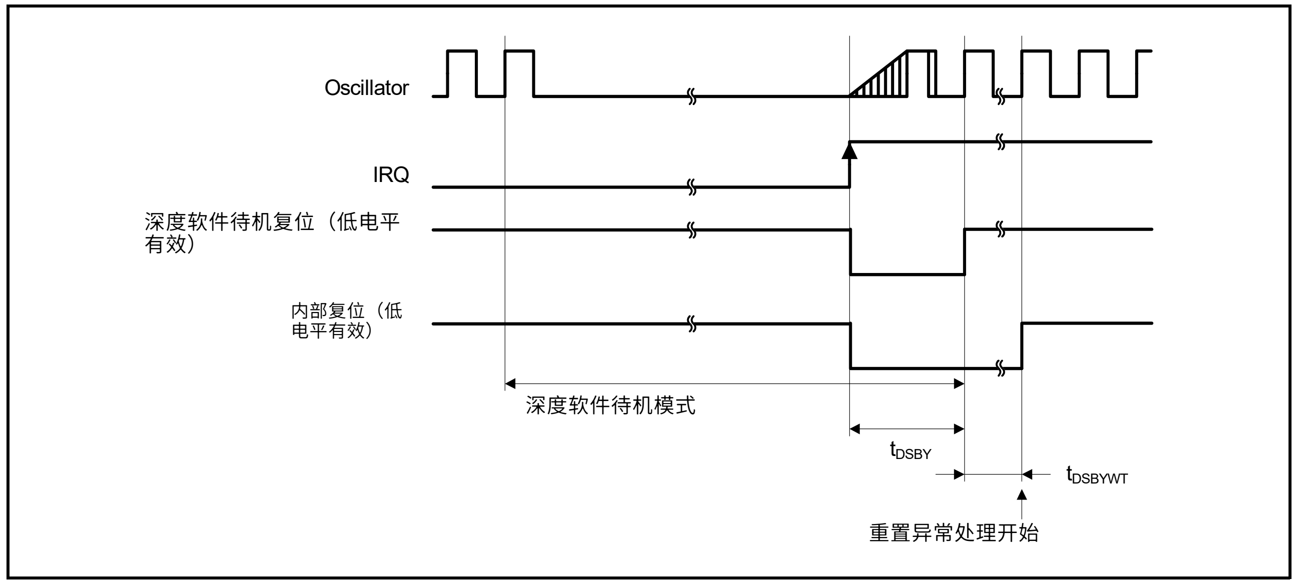
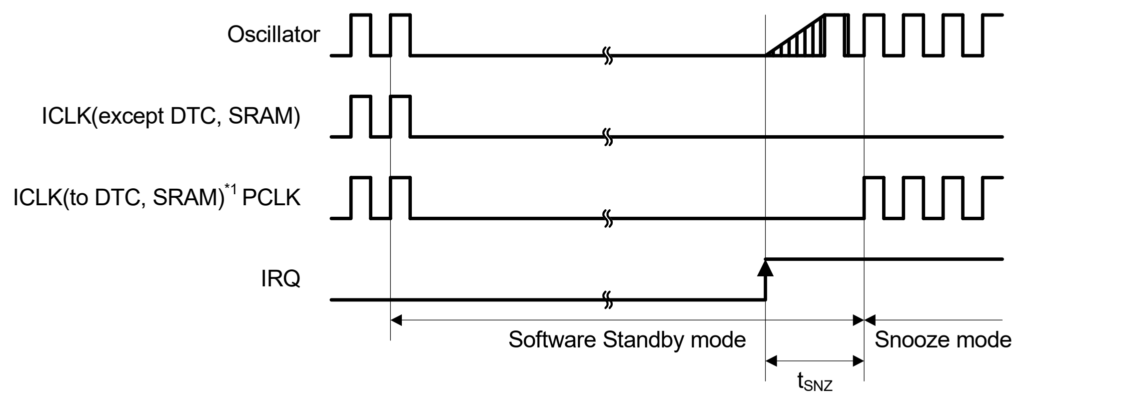


Figure 2.16 深度软件待机模式取消时序



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.17 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

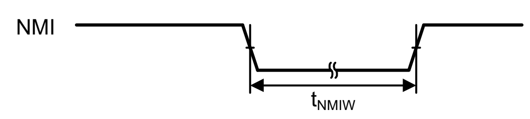


Figure 2.18 NMI interrupt input timing

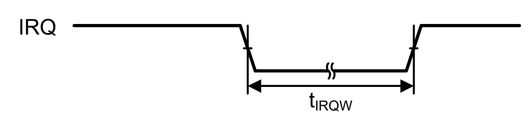
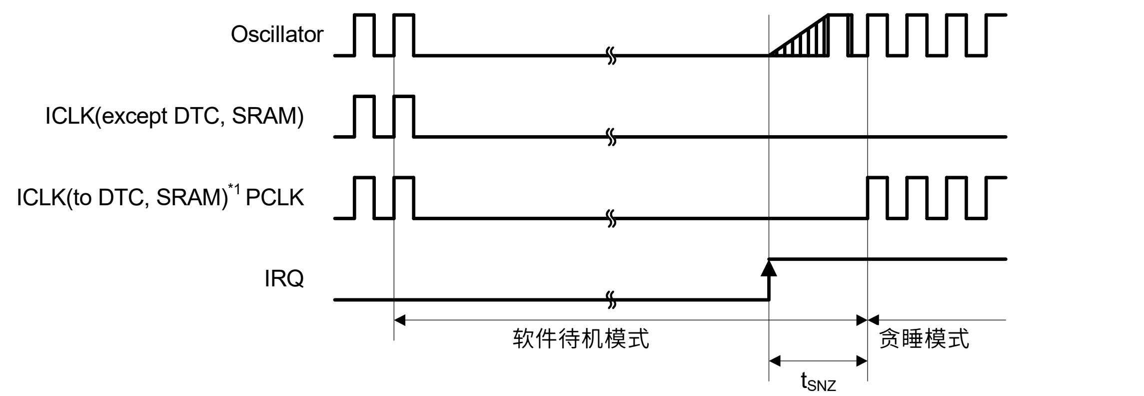


Figure 2.19 IRQ interrupt input timing



注1.当SNZCR.SNZDTCEN设置为1时，ICLK提供给DTC和SRAM。

Figure 2.17 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI和IRQ噪声滤波器

Table 2.17 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	-	-	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	-	-	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。
Note 1. tPcyc表示PCLKB周期。
Note 2. tNMICK表示NMI数字滤波器采样时钟的周期。
Note 3. tIRQCK表示IRQi数字滤波器采样时钟的周期。

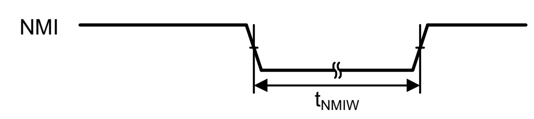


Figure 2.18 NMI中断输入时序

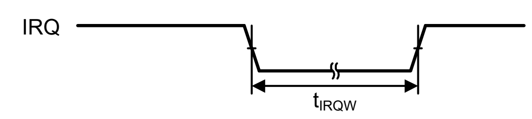


Figure 2.19 IRQ中断输入时序

2.3.6 Bus Timing

Table 2.18 Bus timing
Conditions:
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz.
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0.
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.
EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	12.5	ns	Figure 2.20 to Figure 2.25
CS delay	t_{CSD}	-	12.5	ns	
ALE delay time	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
Read data setup time	t_{RDS}	12.5	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR0 delay	t_{WRD}	-	12.5	ns	
Write data delay	t_{WDD}	-	12.5	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	12.5	-	ns	Figure 2.26
WAIT hold time	t_{WTH}	0	-	ns	

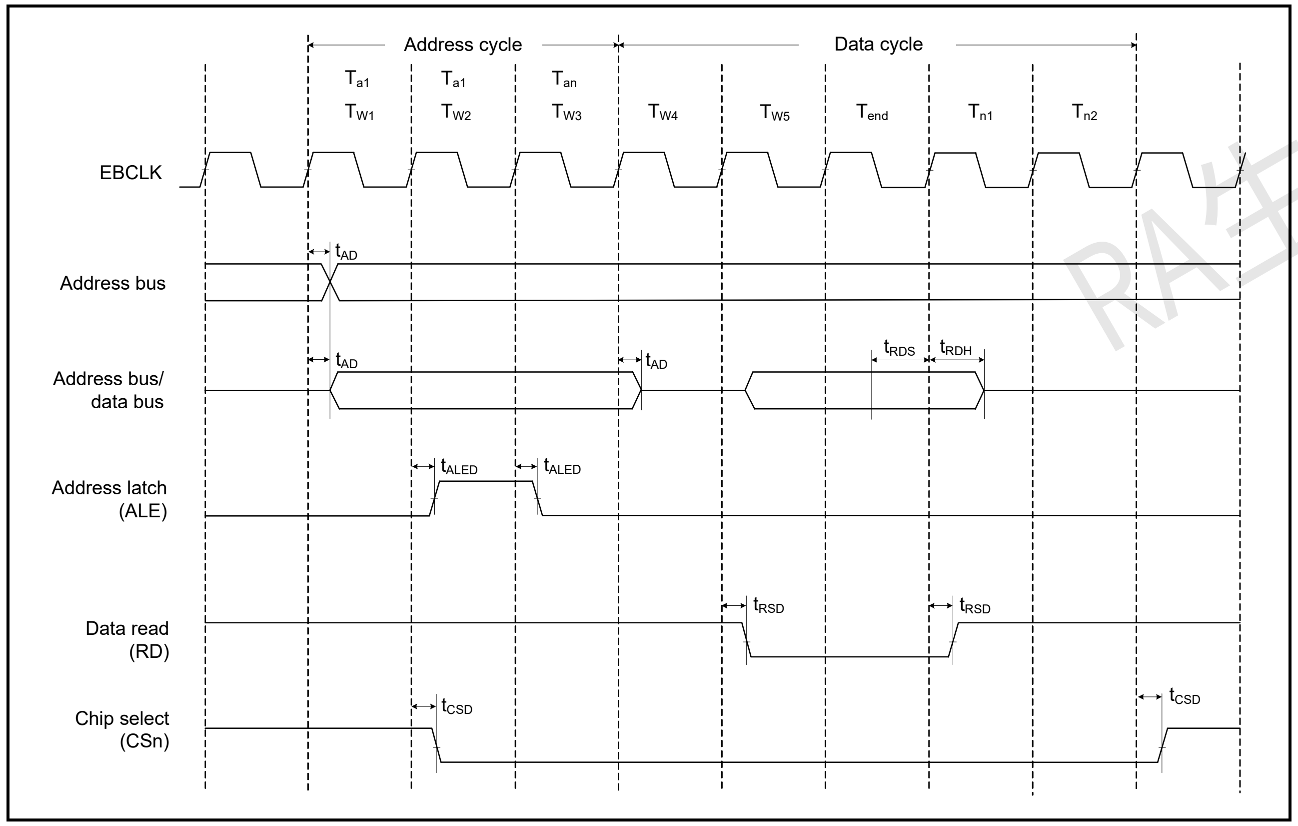


Figure 2.20 Address/data multiplexed bus read access timing

2.3.6 巴士时间

Table 2.18 公交车计时
Conditions:
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz.
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0.
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF。
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟	t_{AD}	-	12.5	ns	图2.20至 Figure 2.25
CS delay	t_{CSD}	-	12.5	ns	
ALE延迟时间	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
读取数据建立时间	t_{RDS}	12.5	-	ns	
读取数据保持时间	t_{RDH}	0	-	ns	
WR0 delay	t_{WRD}	-	12.5	ns	
写数据延迟	t_{WDD}	-	12.5	ns	
写数据保持时间	t_{WDH}	0	-	ns	
等待设置时间	t_{WTS}	12.5	-	ns	Figure 2.26
WAIT保持时间	t_{WTH}	0	-	ns	

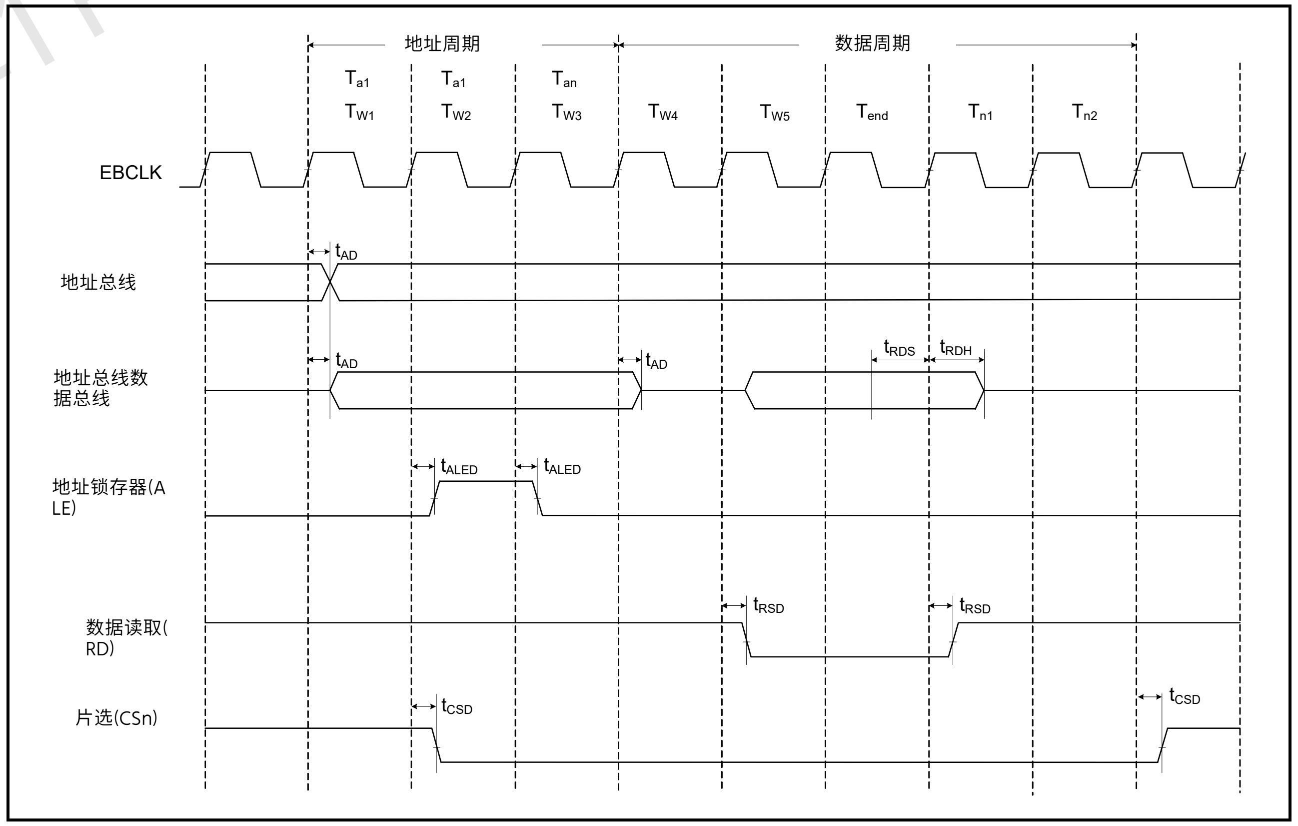


Figure 2.20 地址数据复用总线读访问时序

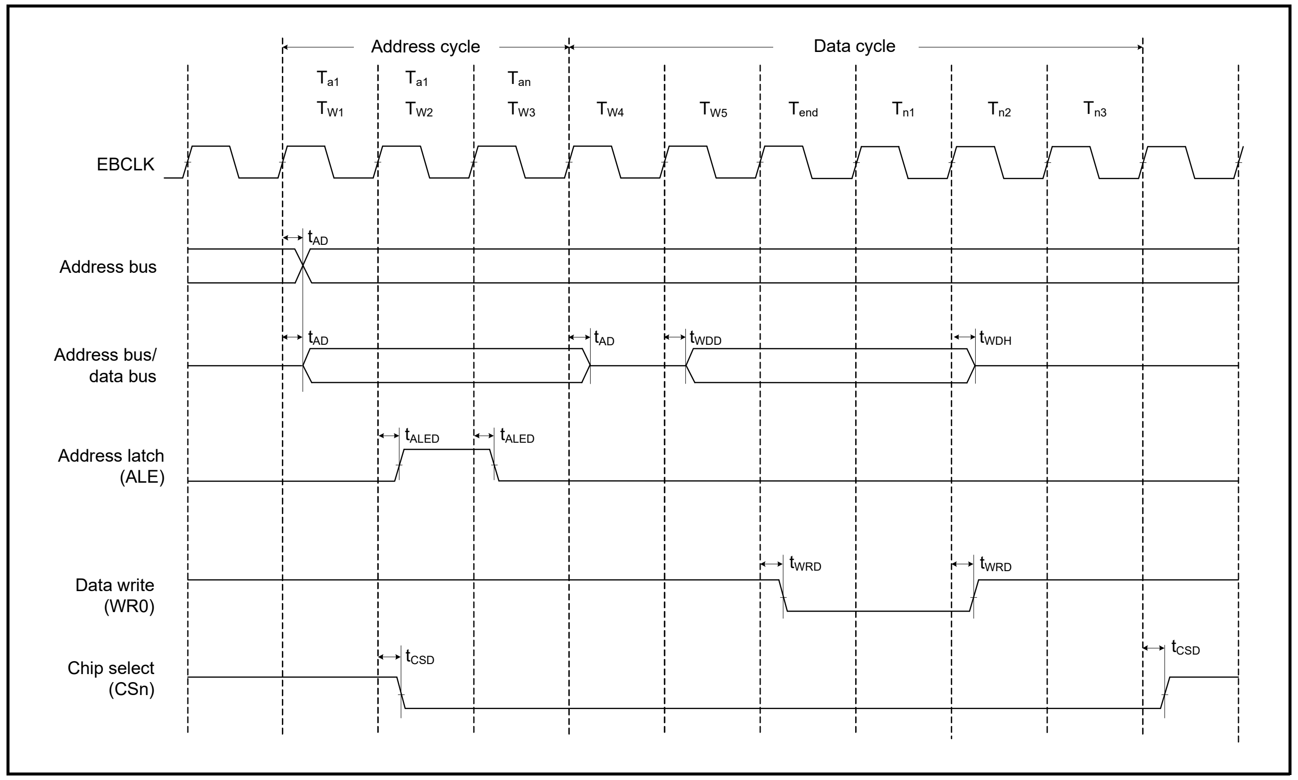


Figure 2.21 Address/data multiplexed bus write access timing

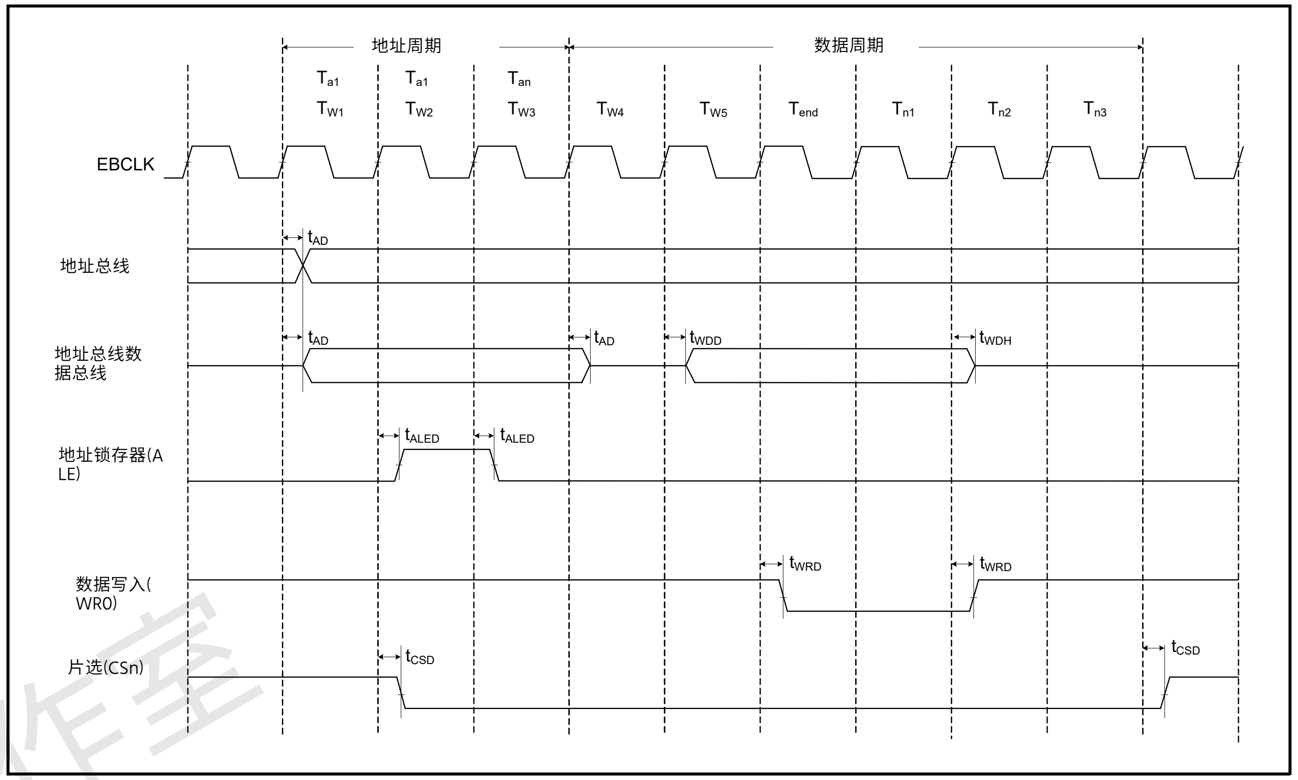


Figure 2.21 地址数据复用总线写访问时序

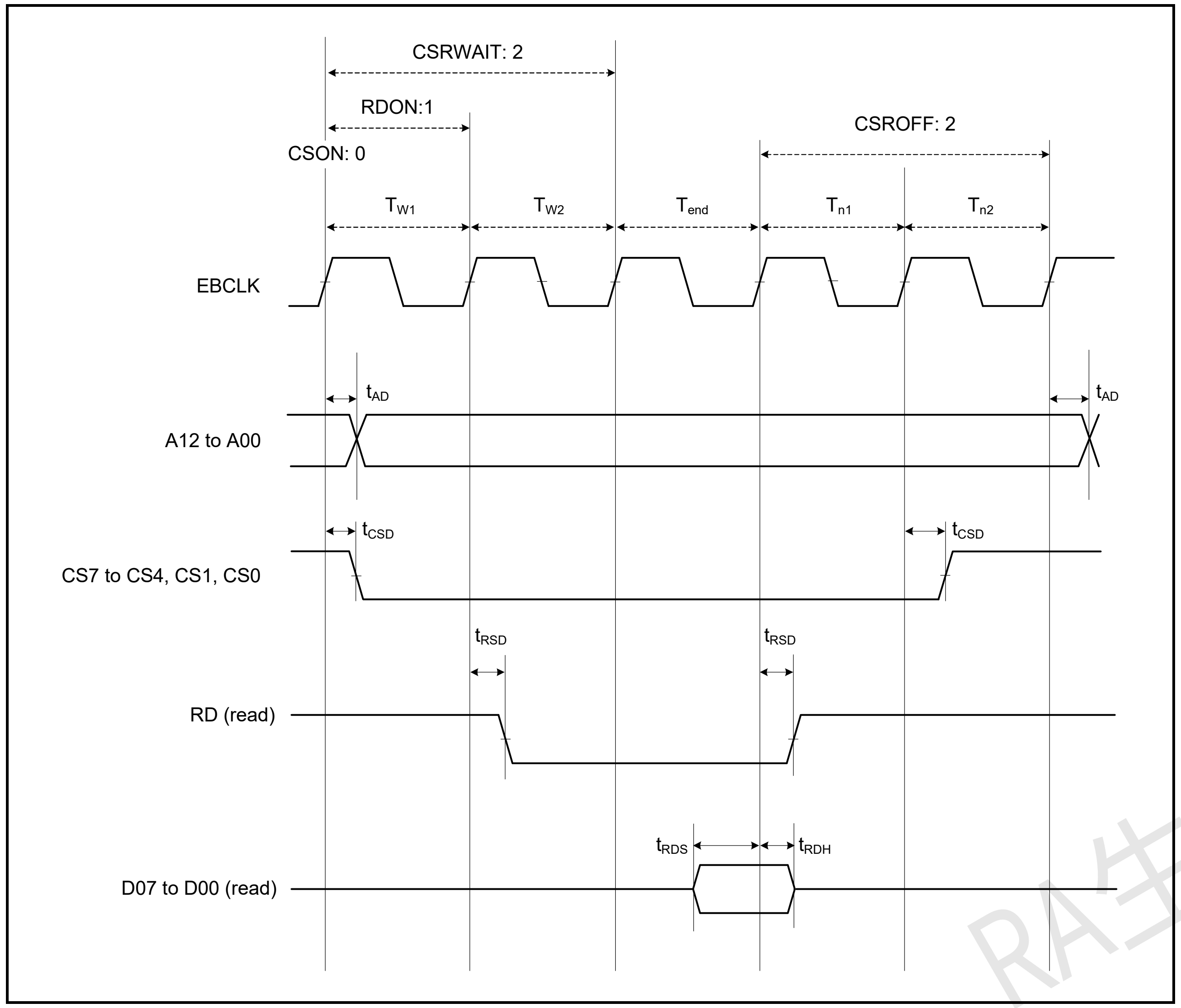


Figure 2.22 External bus timing for normal read cycle with bus clock synchronized

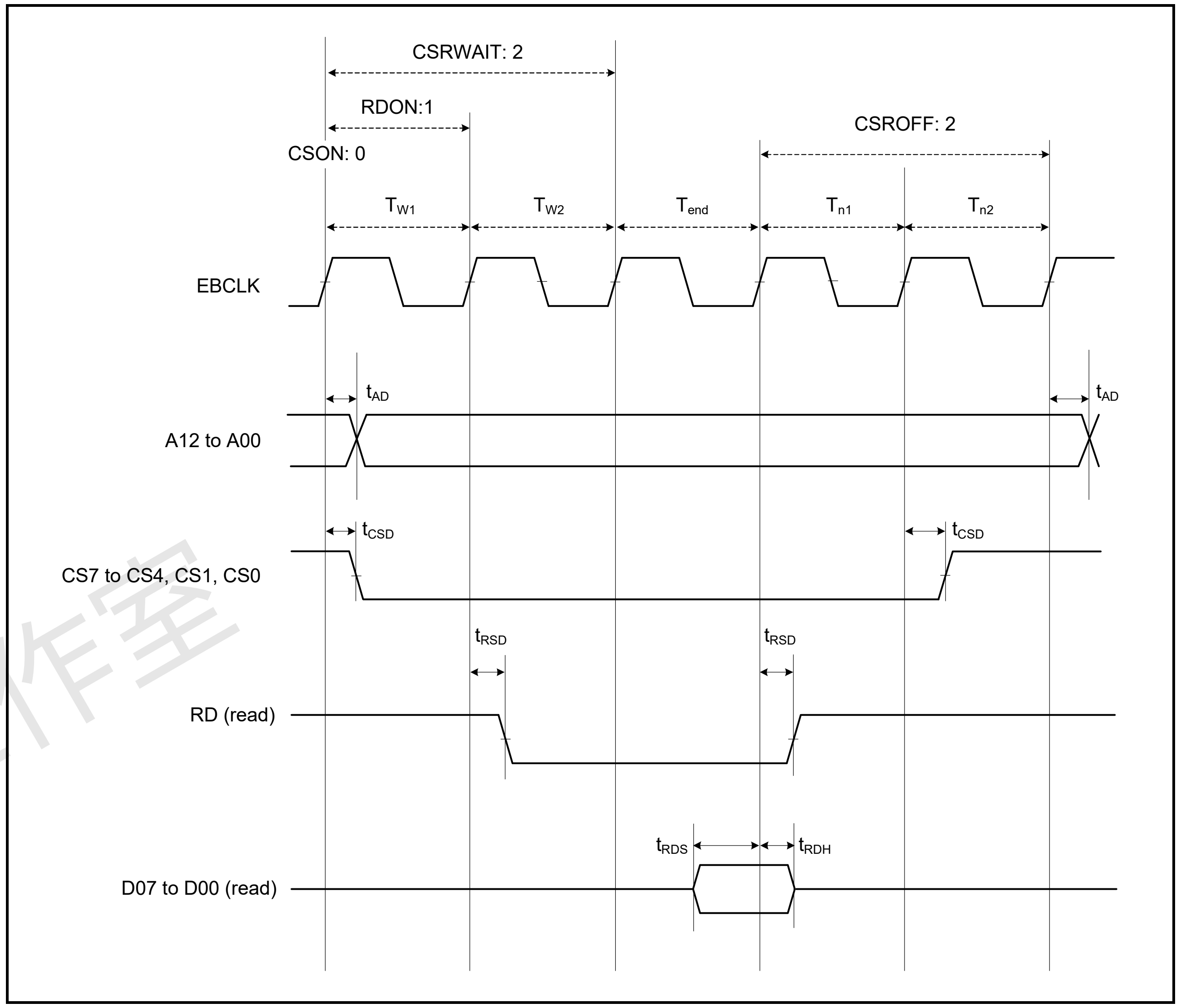
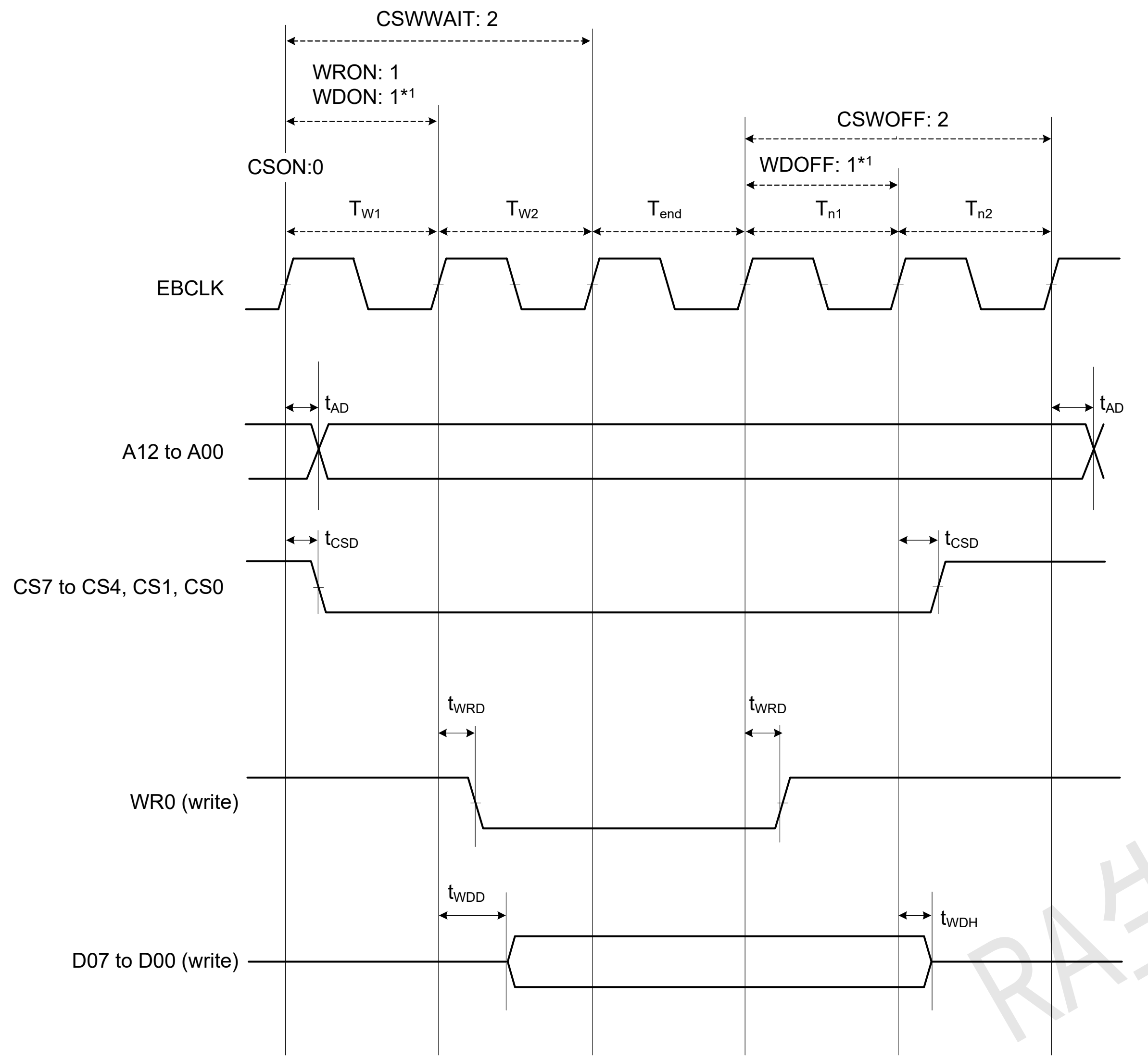
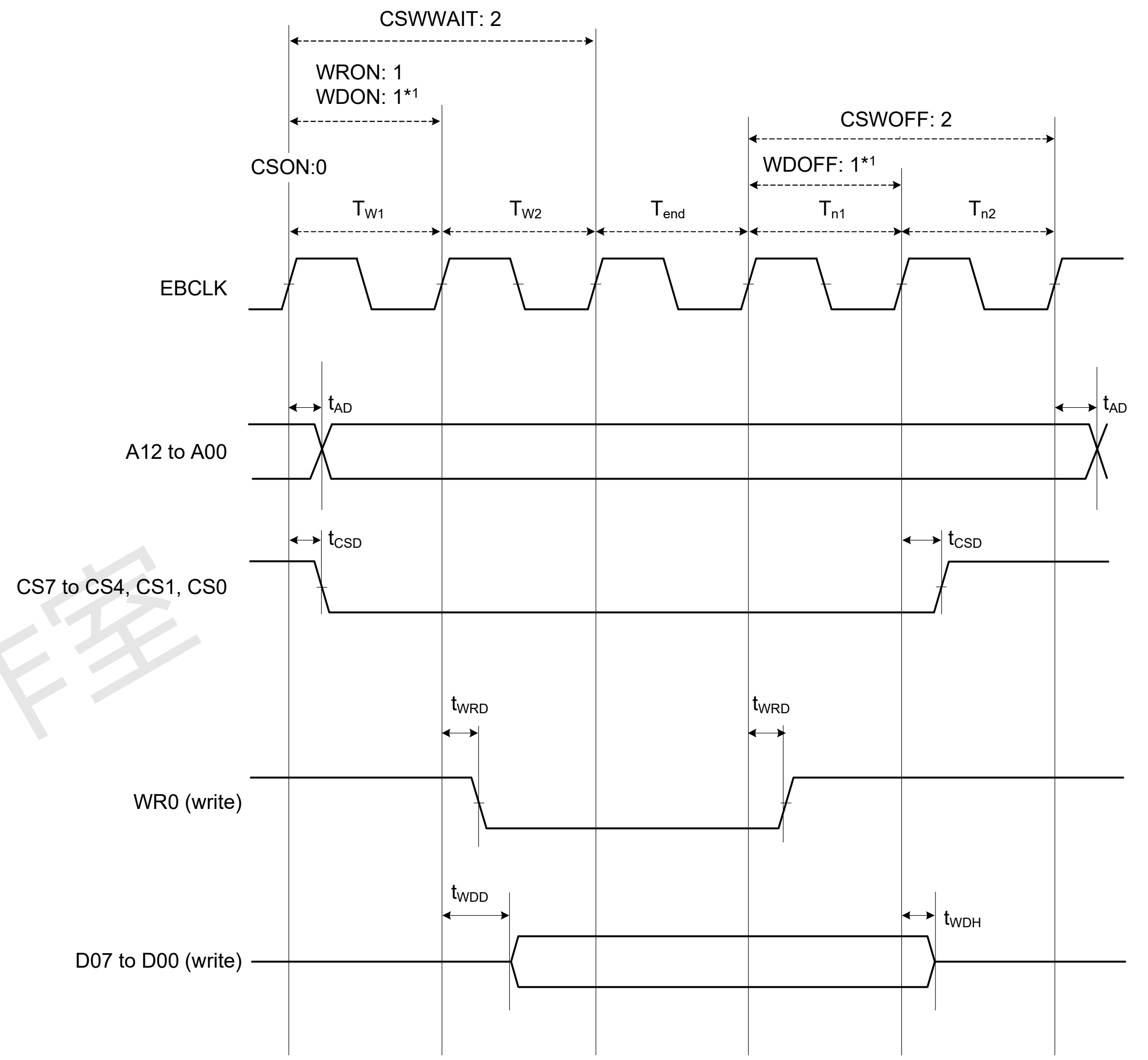


Figure 2.22 正常读取周期的外部总线时序与总线时钟同步



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.23 External bus timing for normal write cycle with bus clock synchronized



注1.始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 2.23 与总线时钟同步的正常写周期的外部总线时序

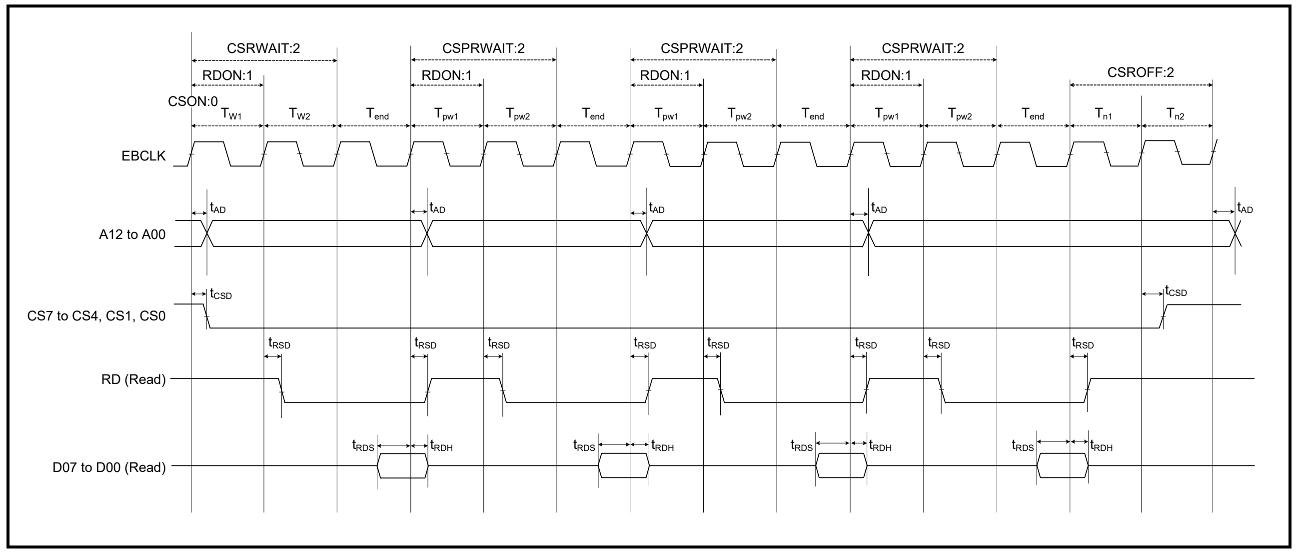
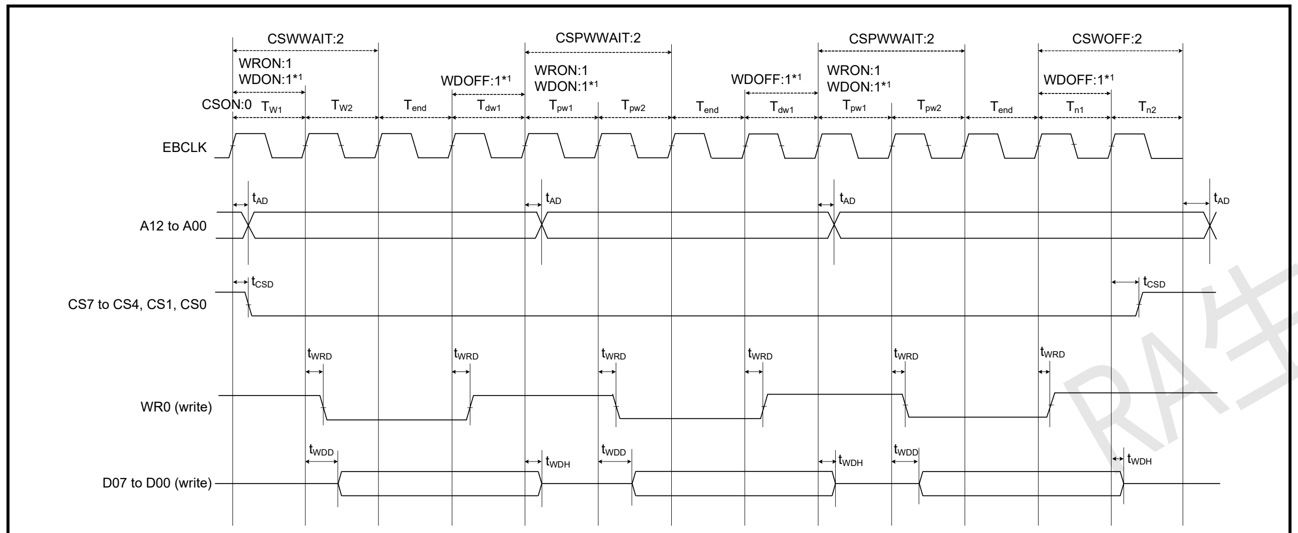


Figure 2.24 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.25 External bus timing for page write cycle with bus clock synchronized

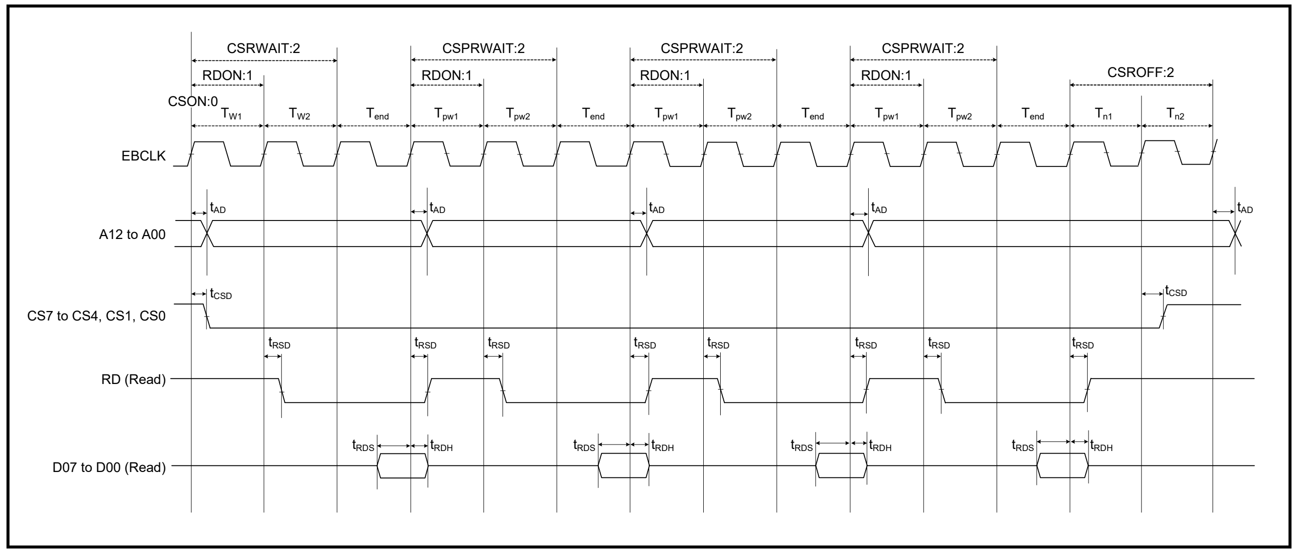
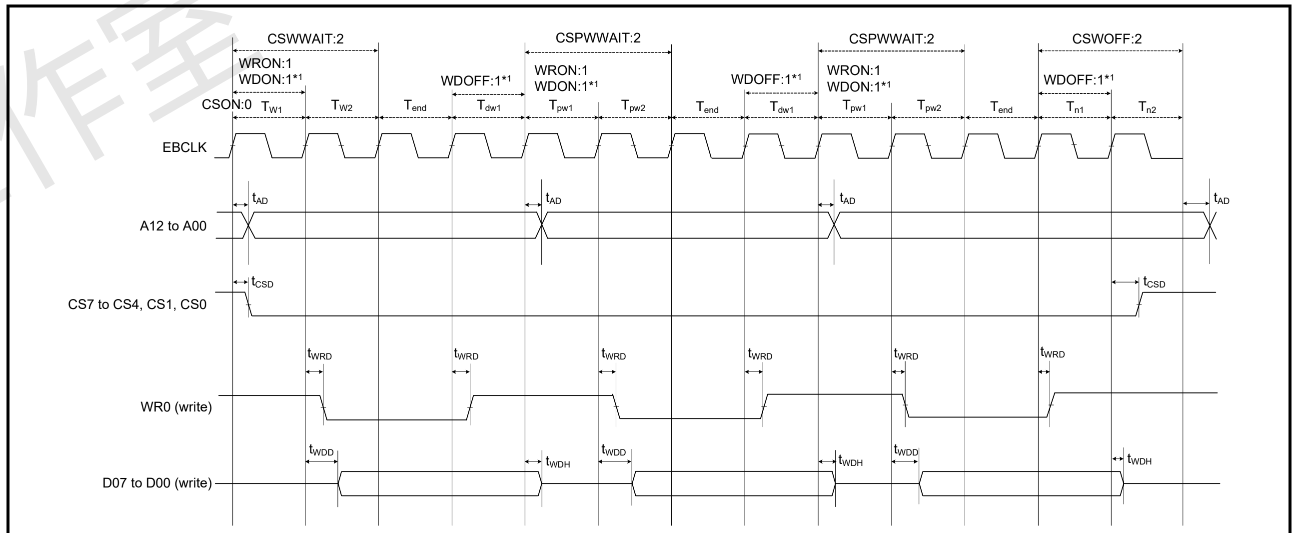


Figure 2.24 页面读取周期的外部总线时序与总线时钟同步



Note 1. 始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 2.25 页面写入周期的外部总线时序与总线时钟同步

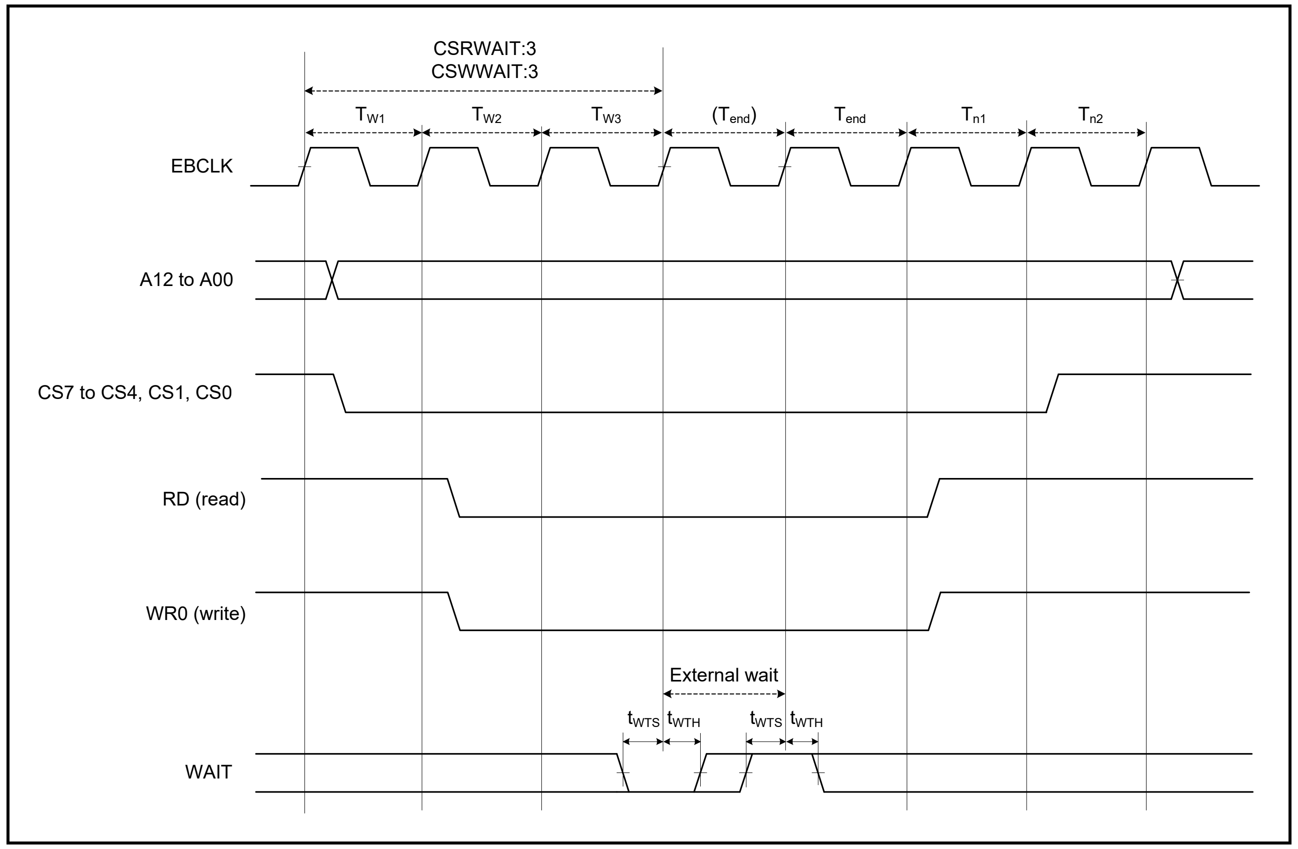


Figure 2.26 External bus timing for external wait control

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)
GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.27
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 2.28
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.29
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*1	-	4	ns	Figure 2.30
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 12, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 12, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.31
GPT (PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*2	-	2.0	ns	Figure 2.32

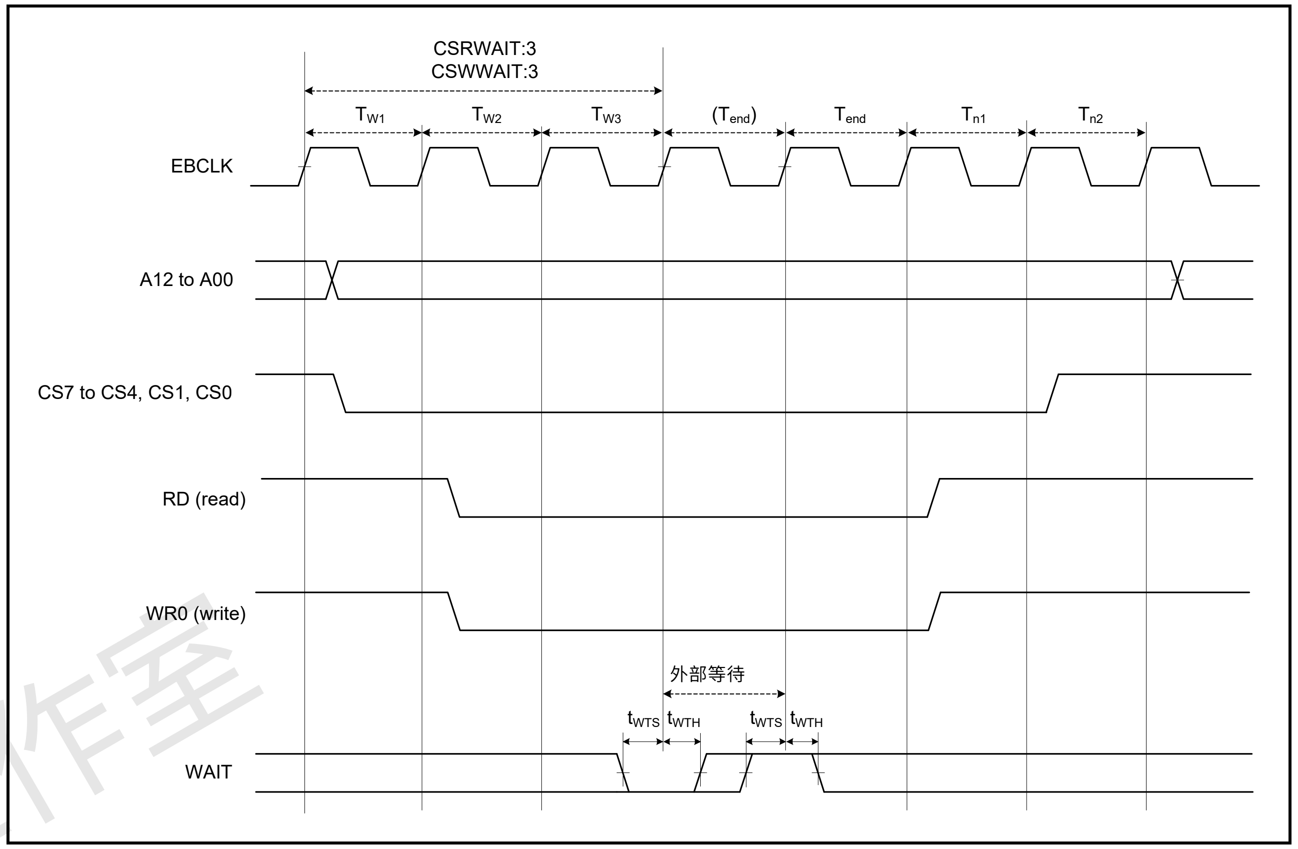


Figure 2.26 外部等待控制的外部总线时序

2.3.7 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序

Table 2.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序（1of2）
GPT32条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。AGT条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.27
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	-	t_{Pcyc}	Figure 2.28
GPT32	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.29
		双刃		2.5	-		
	GTIOCxY输出偏移（x =0到7，Y=A或B）	中间驱动缓冲器	t_{GTISK}*1	-	4	ns	Figure 2.30
		高驱动缓冲器		-	4		
	GTIOCxY输出偏差（x= 8到12，Y=A或B）	中间驱动缓冲器		-	4		
		高驱动缓冲器		-	4		
	GTIOCxY输出偏移（x= 0到12，Y=A或B）	中间驱动缓冲器		-	6		
		高驱动缓冲器		-	6		
	OPS输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.31
GPT（PWM 延迟生成 Circuit)	GTIOCxY_Z输出偏移（x=0到3，Y=A或B，Z=A）		t_{HRSK}*2	-	2.0	ns	Figure 2.32

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)

GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
AGT	AGTIO, AGTEE input cycle	t_{ACYC}*3	100	-	ns	Figure 2.33
	AGTIO, AGTEE input high width, low width	t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width	t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.34
KINT	KRn(n = 00 to 07) pulse width	t_{KR}	250	-	ns	Figure 2.35

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. The load is 30 pF.
Note 3. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

Figure 2.27 I/O ports input timing

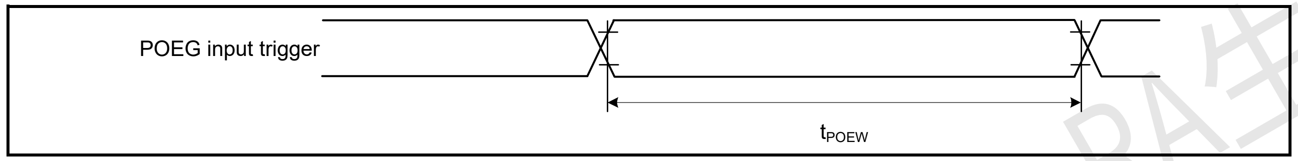


Figure 2.28 POEG input trigger timing

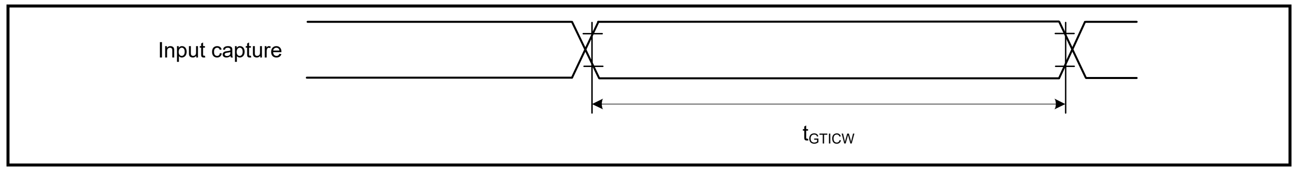


Figure 2.29 GPT32 input capture timing

Table 2.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序(2of2)

GPT32条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。AGT条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
AGT	AGTIO、AGTEE输入周期	t_{ACYC}*3	100	-	ns	Figure 2.33
	AGTIO、AGTEE输入高宽、低宽	t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO、AGTO、AGTOA、AGTOB输出周期	t_{ACYC2}	62.5	-	ns	
ADC12	ADC12触发输入脉冲宽度	t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.34
KINT	KRn(n=00到07)脉冲宽度	t_{KR}	250	-	ns	Figure 2.35

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. 当使用相同的驱动程序IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。
Note 2. 负载为30pF。
Note 3. 输入周期的约束：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。

Figure 2.27 IO端口输入时序

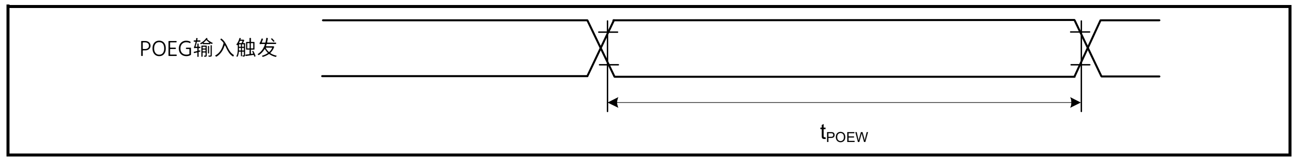


Figure 2.28 POEG输入触发时序

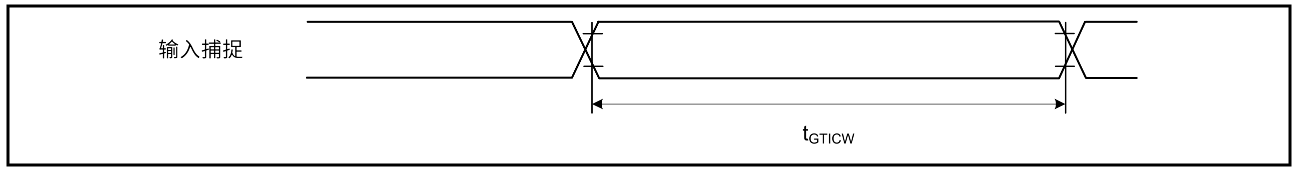


Figure 2.29 GPT32输入捕捉时序

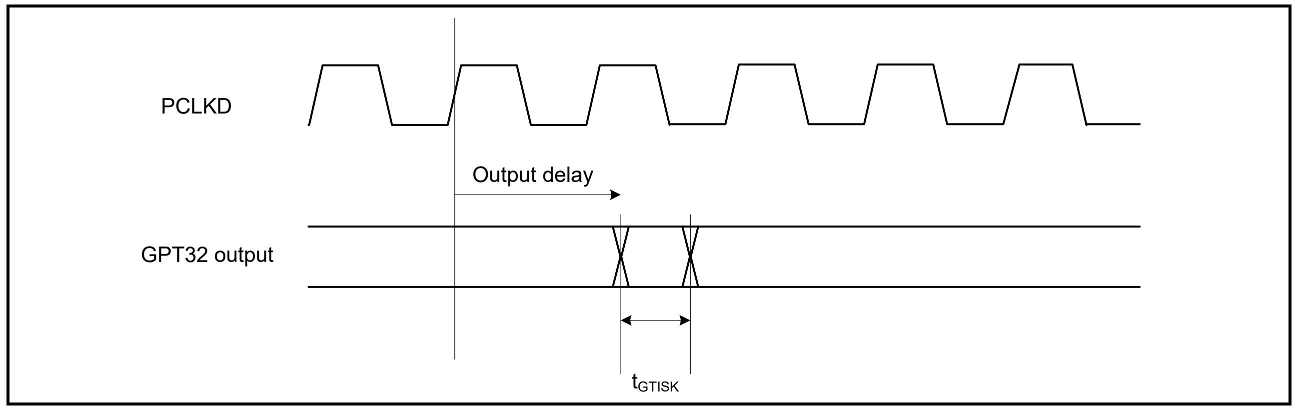


Figure 2.30 GPT32 output delay skew

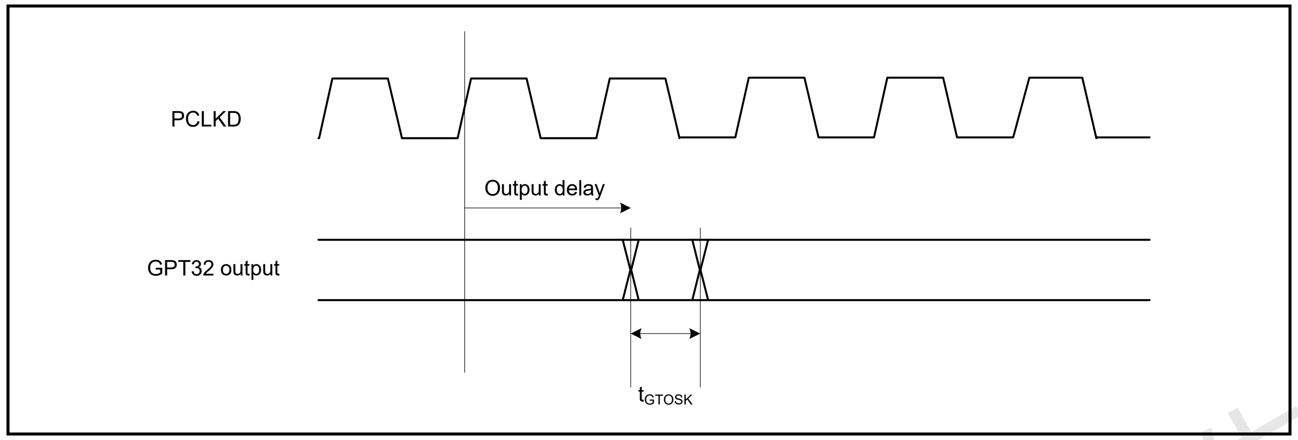


Figure 2.31 GPT32 output delay skew for OPS

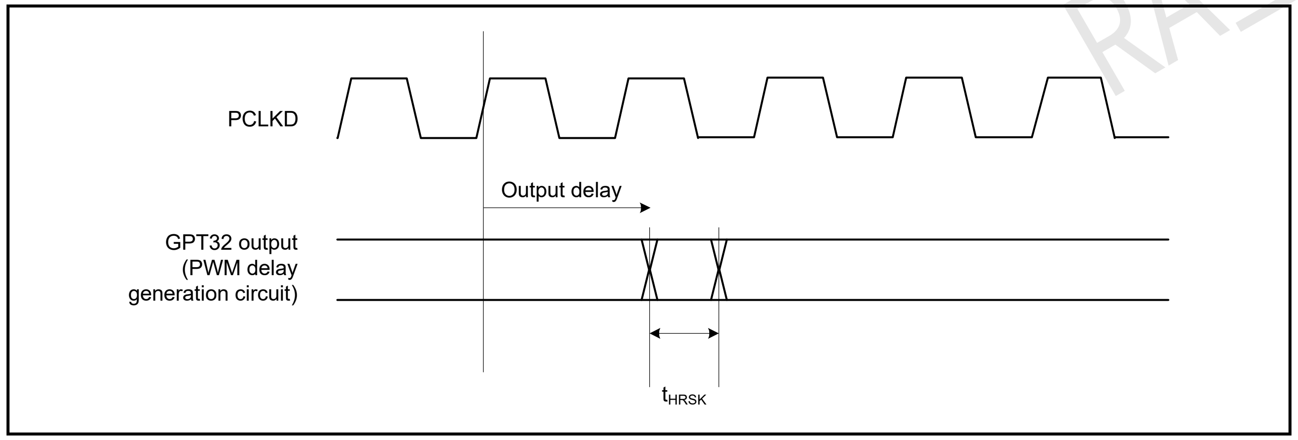


Figure 2.32 GPT32 (PWM delay generation circuit) output delay skew

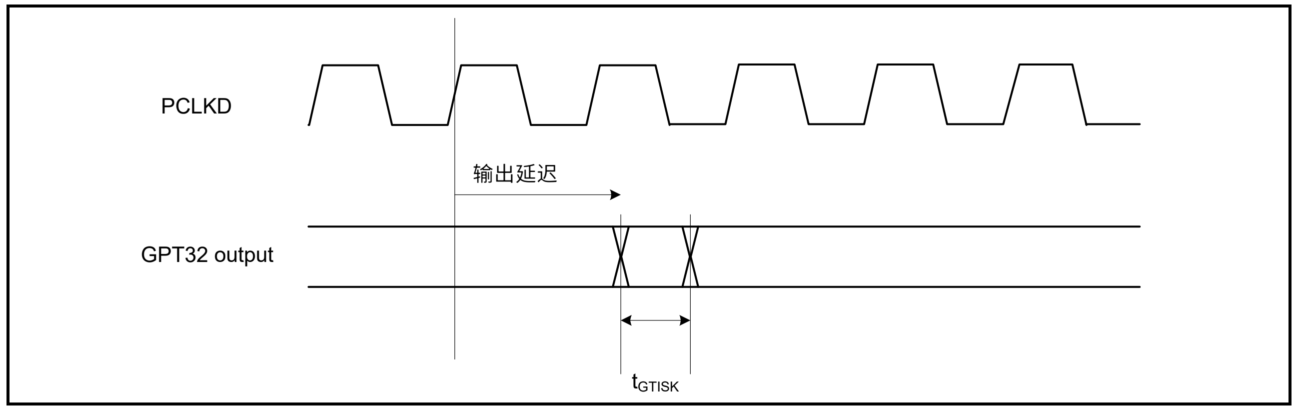


Figure 2.30 GPT32输出延迟偏移

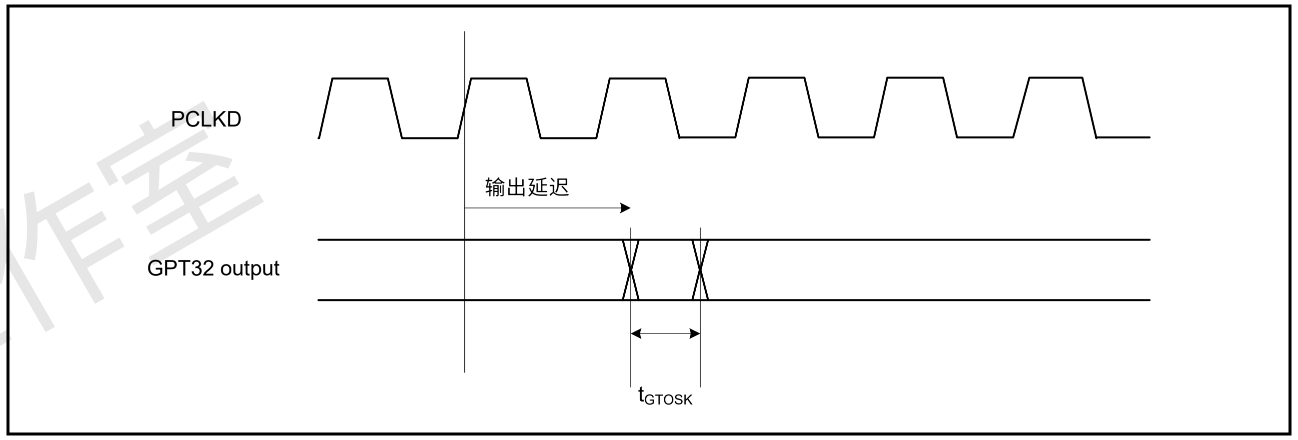


Figure 2.31 用于OPS的GPT32输出延迟偏移

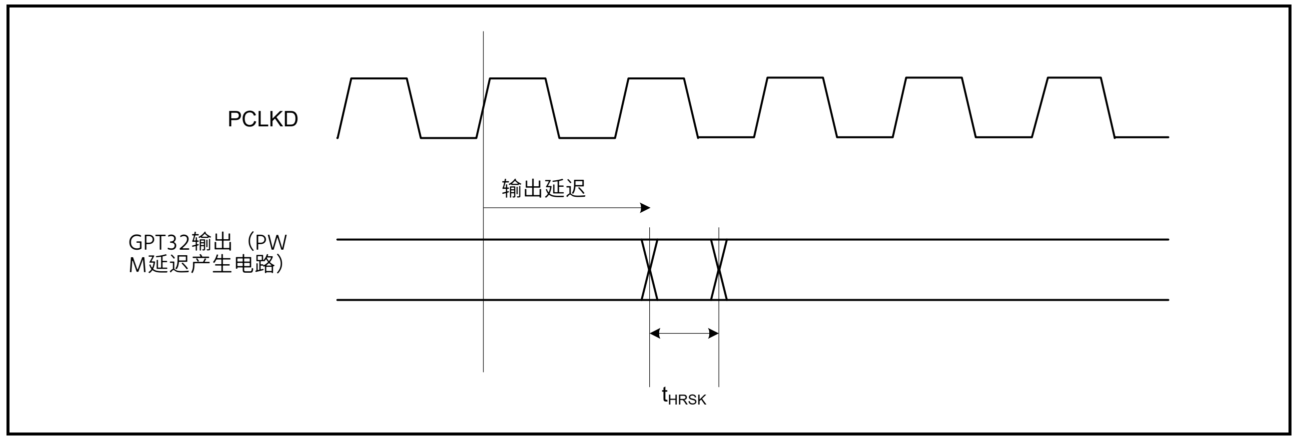


Figure 2.32 GPT32（PWM延迟产生电路）输出延迟歪斜

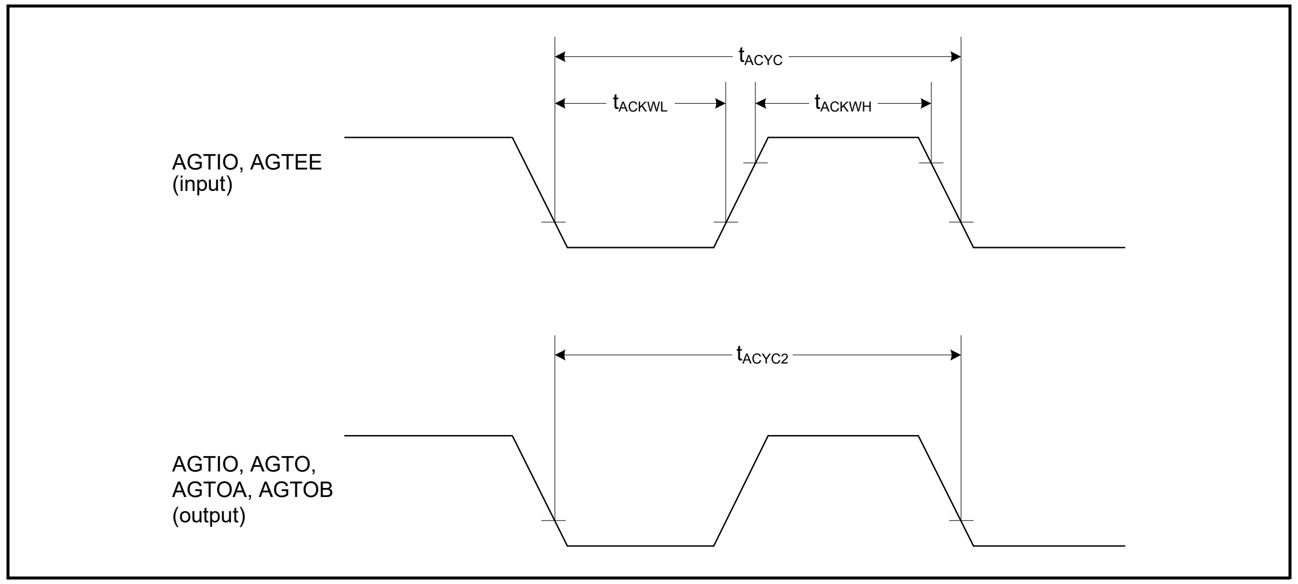


Figure 2.33 AGT input/output timing

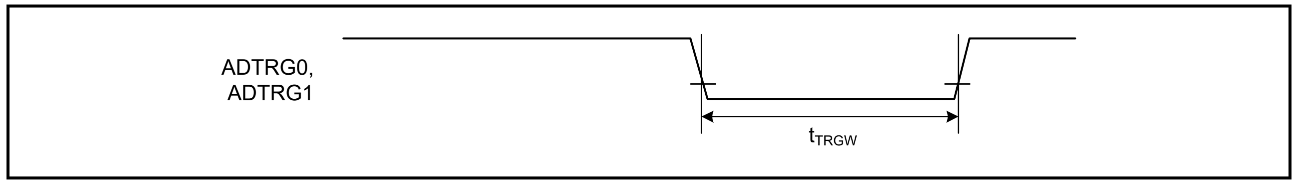


Figure 2.34 ADC12 trigger input timing

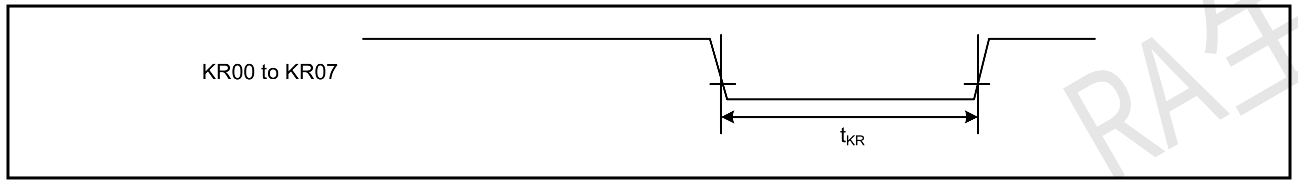


Figure 2.35 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > t_{cac}$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

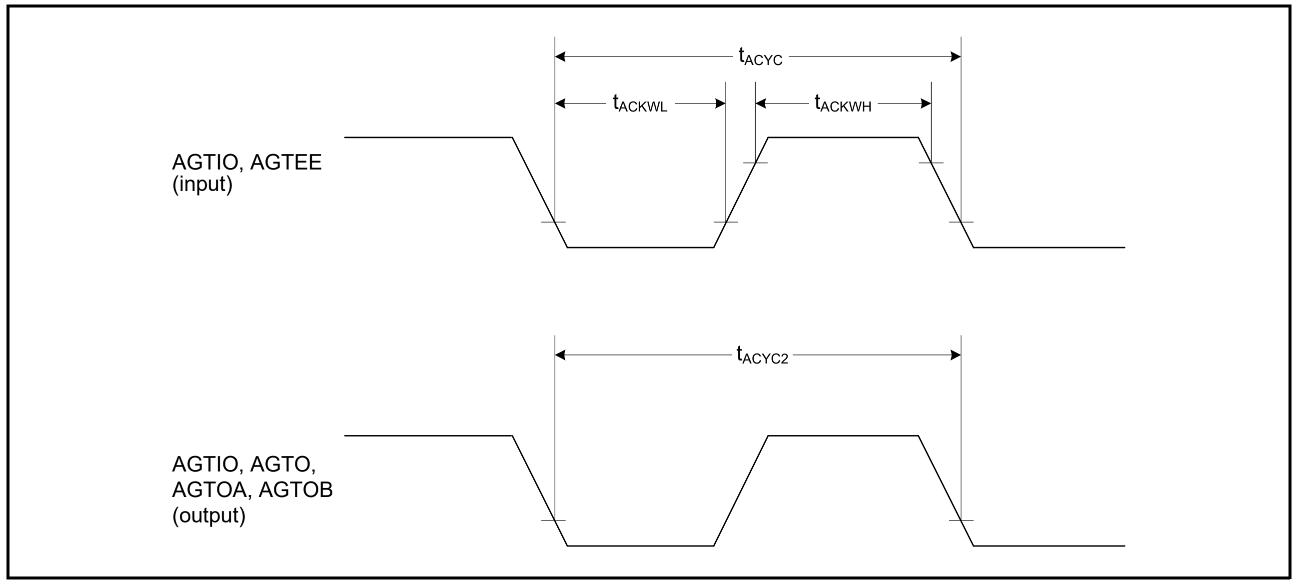


Figure 2.33 AGT input/output timing

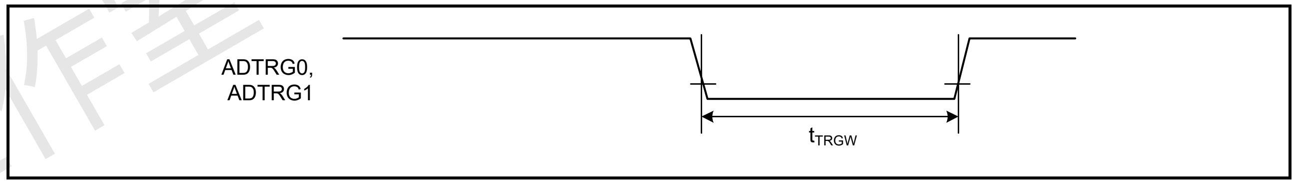


Figure 2.34 ADC12触发输入时序

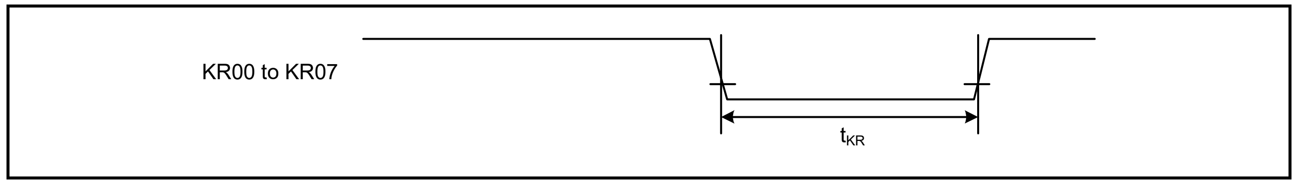


Figure 2.35 按键中断输入时序

2.3.8 PWM延迟产生电路时序

Table 2.20 PWM延迟产生电路时序

Parameter	Min	Typ	Max	Unit	测试条件
运行频率	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. 此值标准化1-LSB分辨率中的行之间的差异。

2.3.9 CAC时序

Table 2.21 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \le t_{cac}$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > t_{cac}$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.36
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 2.37
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

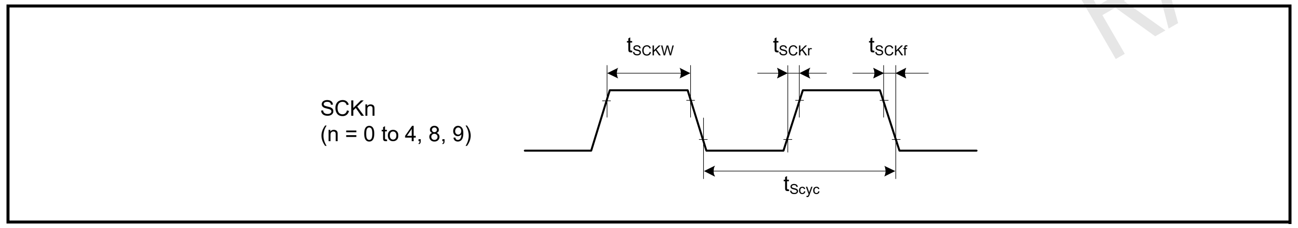


Figure 2.36 SCK clock input/output timing

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. tcac:CAC计数时钟源周期。

2.3.10 SCI时序

Table 2.22 SCI时序（1）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK4，SCK8, SCK9.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	测试条件
SCI	输入时钟周期	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.36
		时钟同步		6	-		
	输入时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间		t_{SCKr}	-	5	ns	
	输入时钟下降时间		t_{SCKf}	-	5	ns	
	输出时钟周期	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		时钟同步		4	-		
	输出时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		t_{SCKr}	-	5	ns	
	输出时钟下降时间		t_{SCKf}	-	5	ns	
	传输数据延迟	时钟同步	t_{TXD}	-	25	ns	Figure 2.37
	接收数据建立时间	时钟同步	t_{RXS}	15	-	ns	
	接收数据保持时间	时钟同步	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

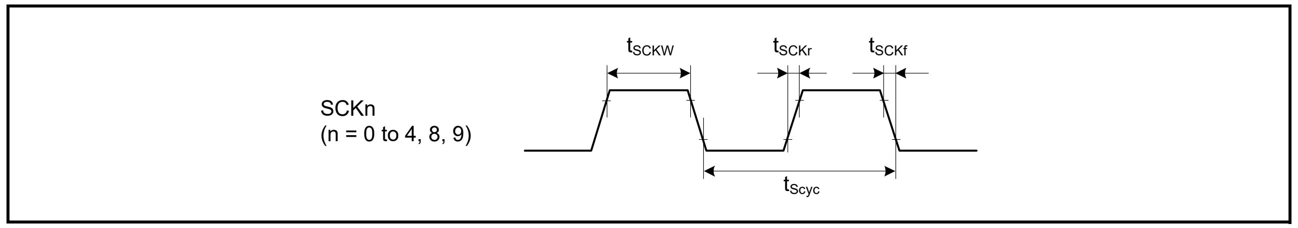


Figure 2.36 SCK时钟输入输出时序

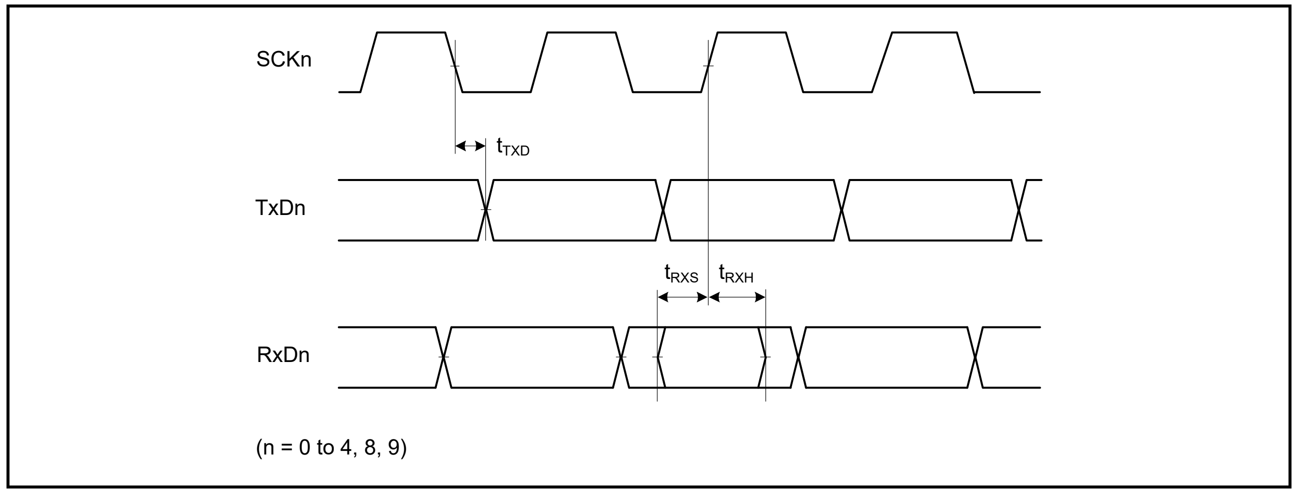


Figure 2.37 SCI input/output timing in clock synchronous mode

Table 2.23 SCI timing (2)
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 2.38
	SCK clock cycle input (slave)	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	t_{SU}	33.3	-	ns	Figure 2.39 to Figure 2.42
	Data input hold time	t_H	33.3	-	ns	
	SS input setup time	t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	t_{OD}	-	33.3	ns	
	Data output hold time	t_{OH}	-10	-	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	-	16.6	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	Slave access time	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 2.42
	Slave output release time	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

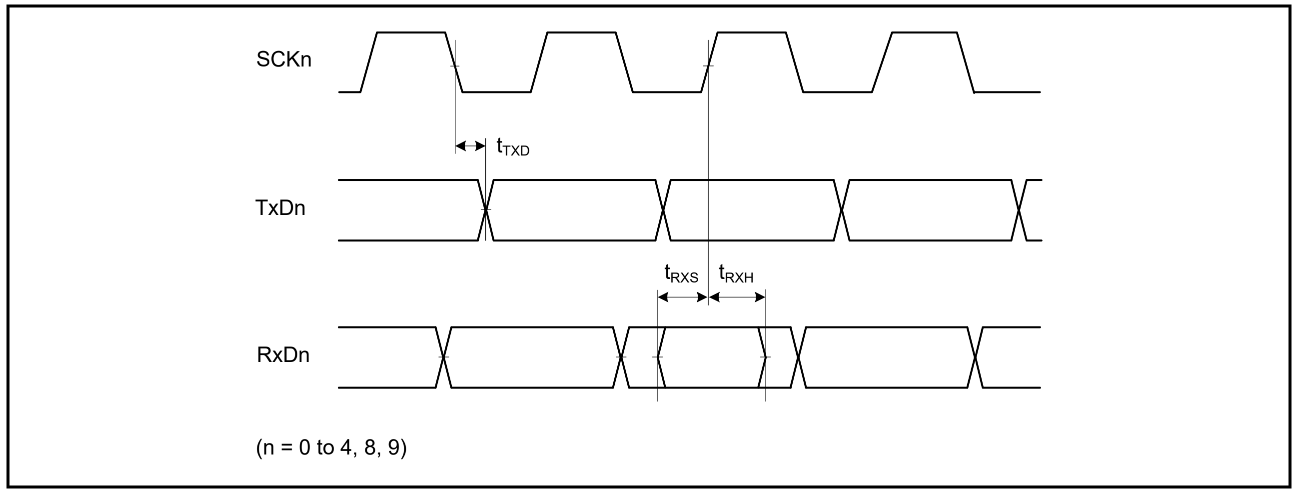


Figure 2.37 时钟同步模式下的SCI输入输出时序

Table 2.23 SCI时序（2）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK4，SCK8, SCK9.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple SPI	SCK时钟周期输出（主机）	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 2.38
	SCK时钟周期输入（从机）	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK时钟高脉冲宽度	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	数据输入建立时间	t_{SU}	33.3	-	ns	图2.39至 Figure 2.42
	数据输入保持时间	t_H	33.3	-	ns	
	SS输入建立时间	t_{LEAD}	1	-	t_{SPcyc}	
	SS输入保持时间	t_{LAG}	1	-	t_{SPcyc}	
	数据输出延迟	t_{OD}	-	33.3	ns	
	数据输出保持时间	t_{OH}	-10	-	ns	
	数据上升和下降时间	t_{Dr}, t_{Df}	-	16.6	ns	
	SS输入上升和下降时间	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	从站访问时间	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 2.42
	从机输出释放时间	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

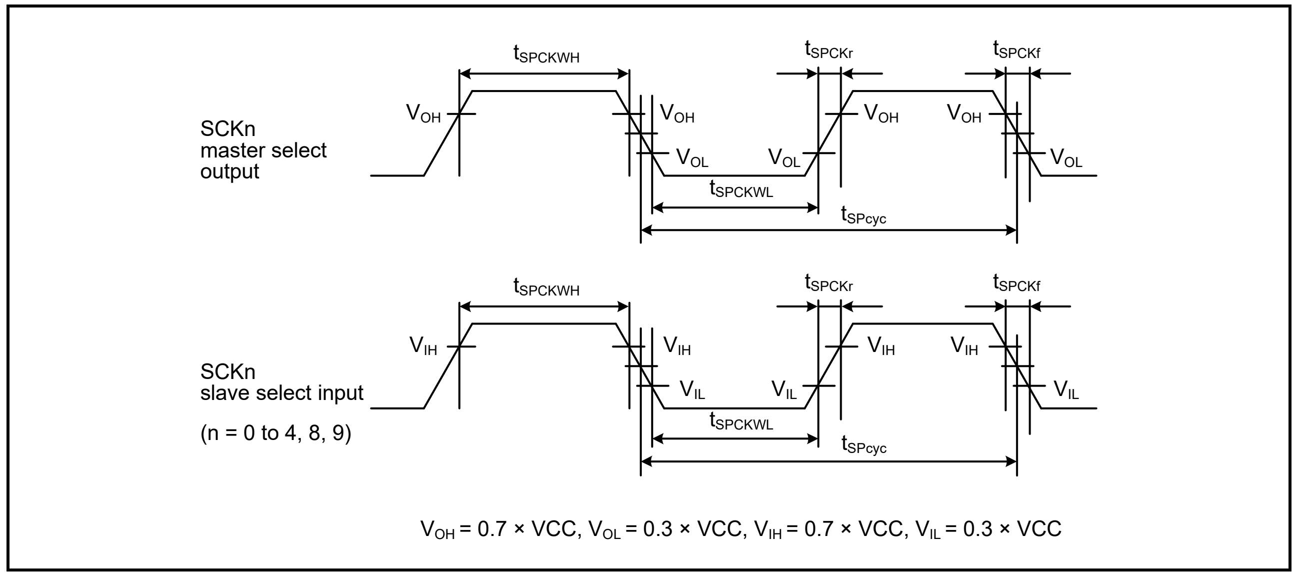


Figure 2.38 SCI simple SPI mode clock timing

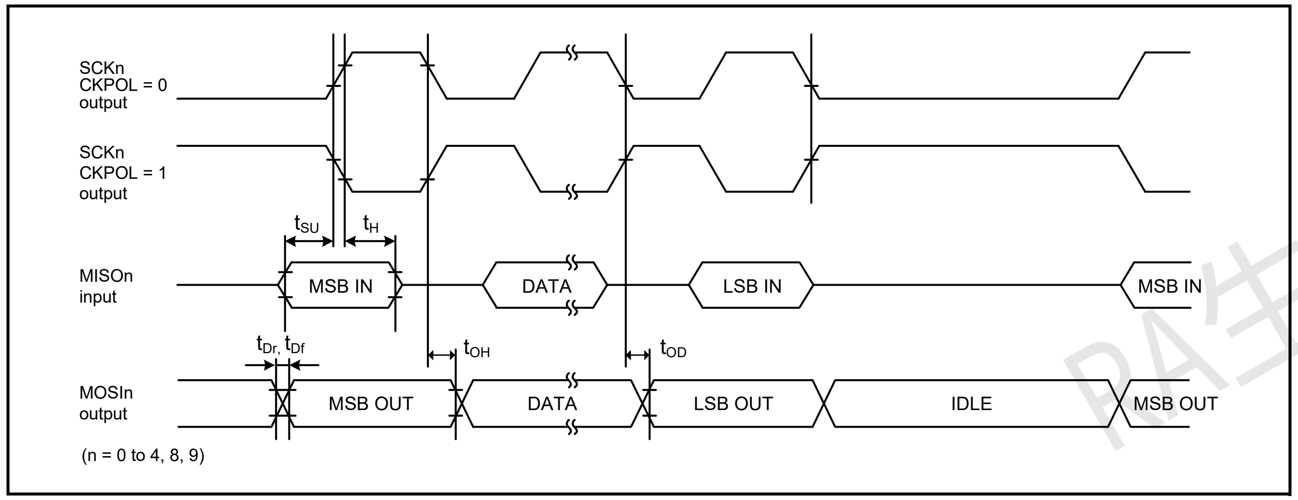


Figure 2.39 SCI simple SPI mode timing for master when CKPH = 1

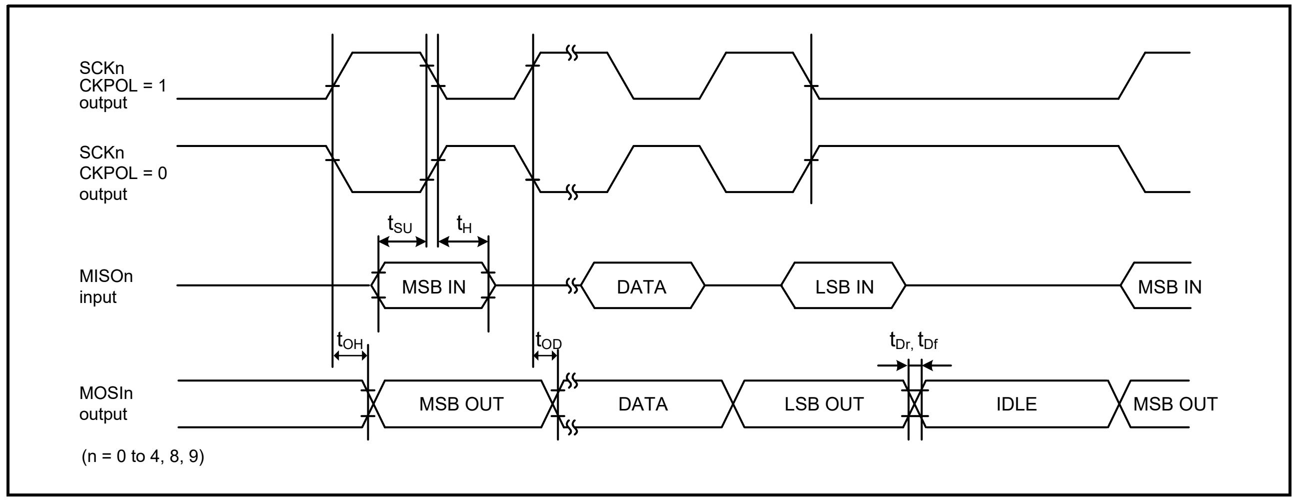


Figure 2.40 SCI simple SPI mode timing for master when CKPH = 0

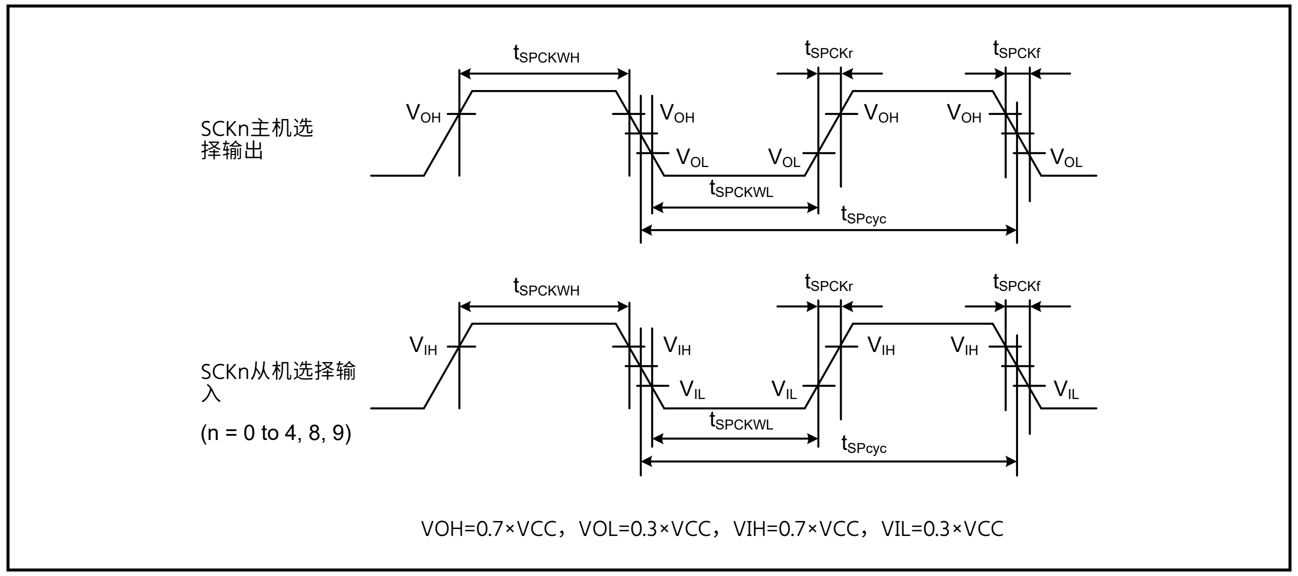


Figure 2.38 SCI简单SPI模式时钟时序

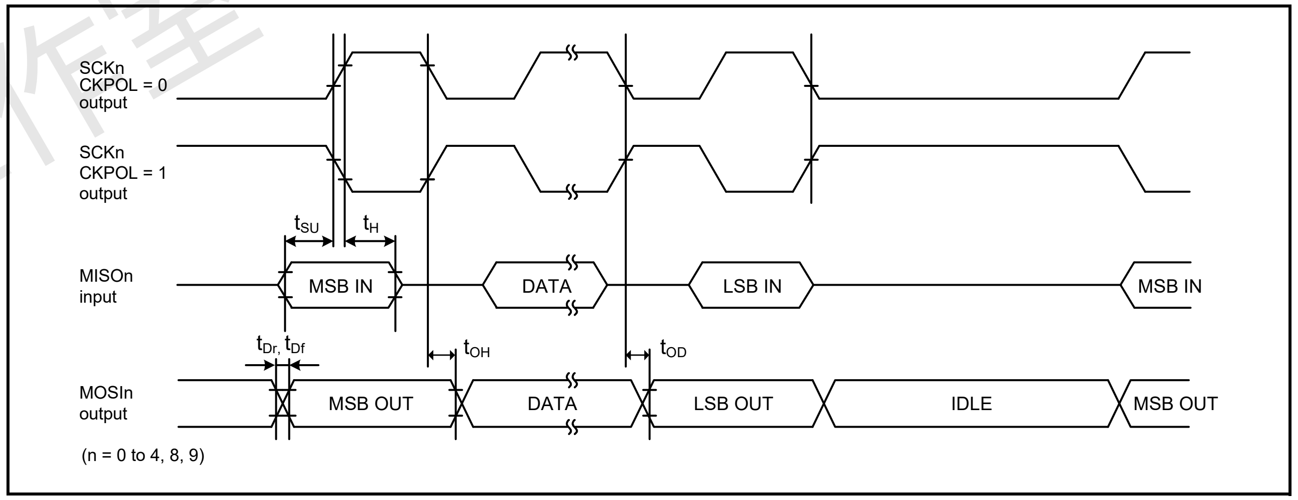


Figure 2.39 CKPH=1时主机的SCI简单SPI模式时序

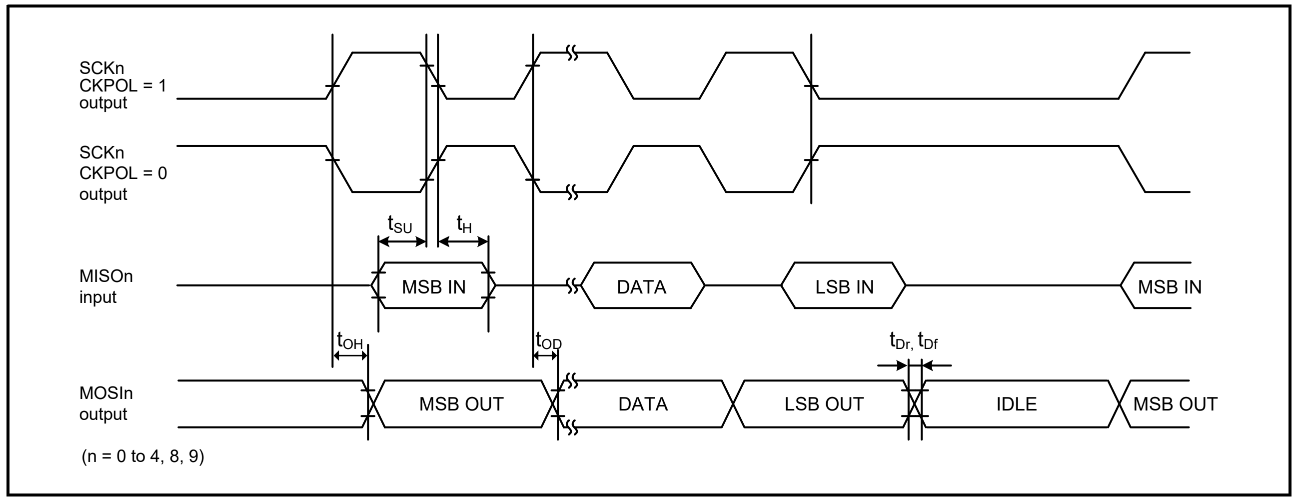


Figure 2.40 CKPH=0时主机的SCI简单SPI模式时序

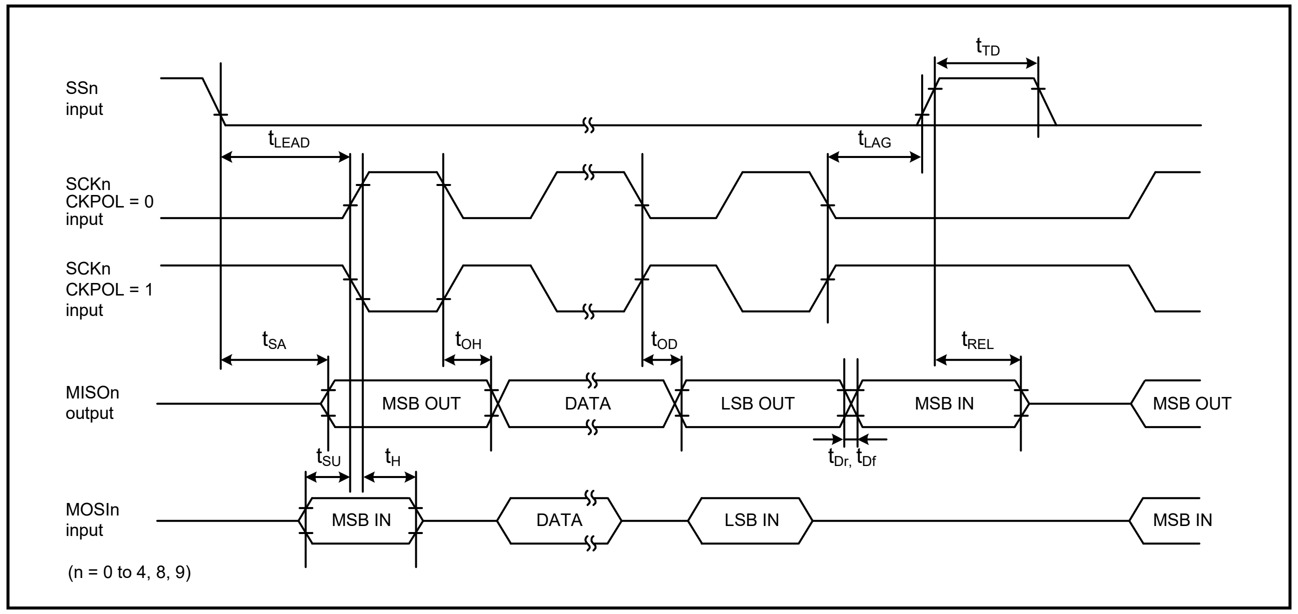


Figure 2.41 SCI simple SPI mode timing for slave when CKPH = 1

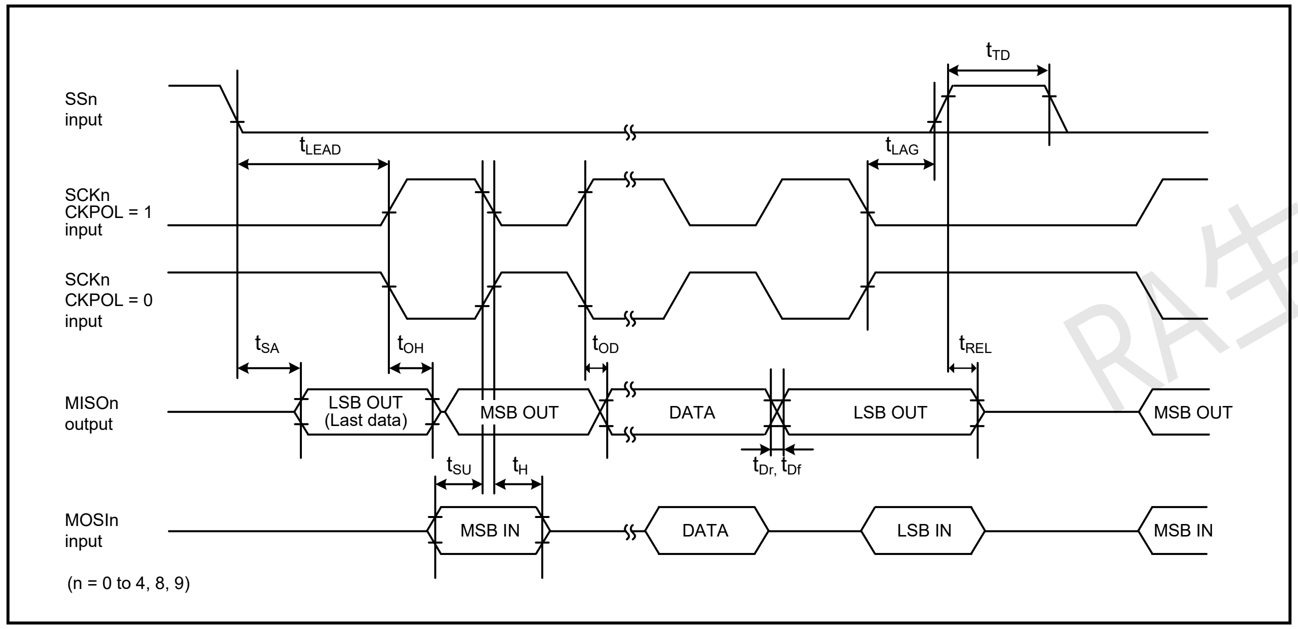


Figure 2.42 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.43
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

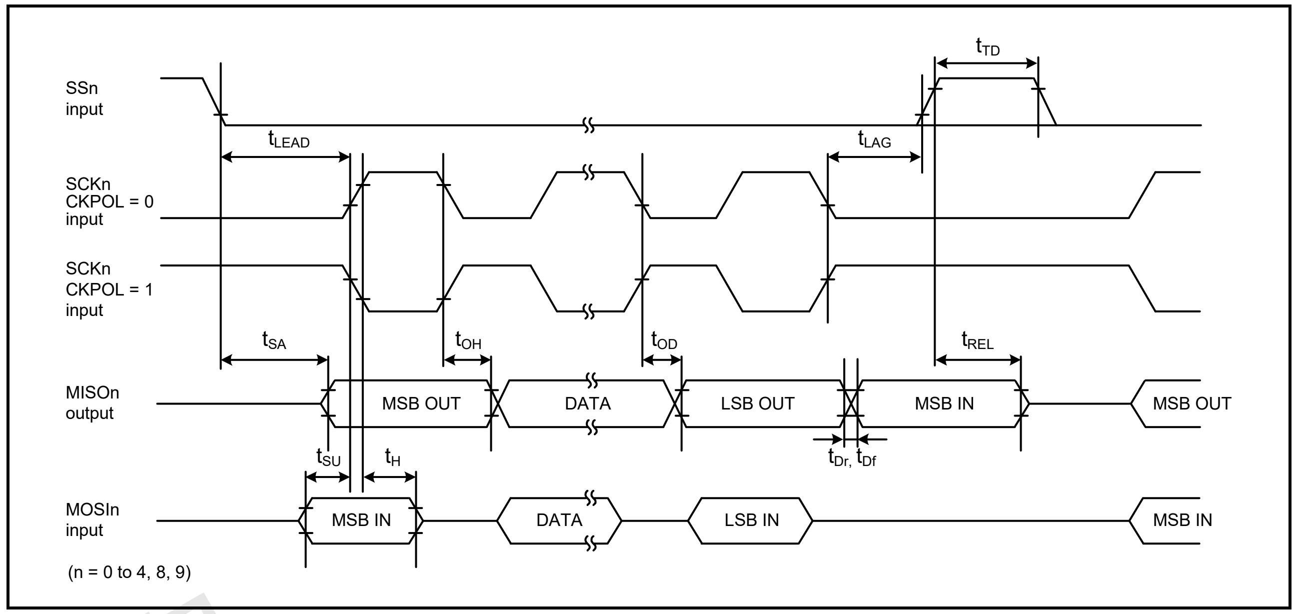


Figure 2.41 CKPH=1时从机的SCI简单SPI模式时序

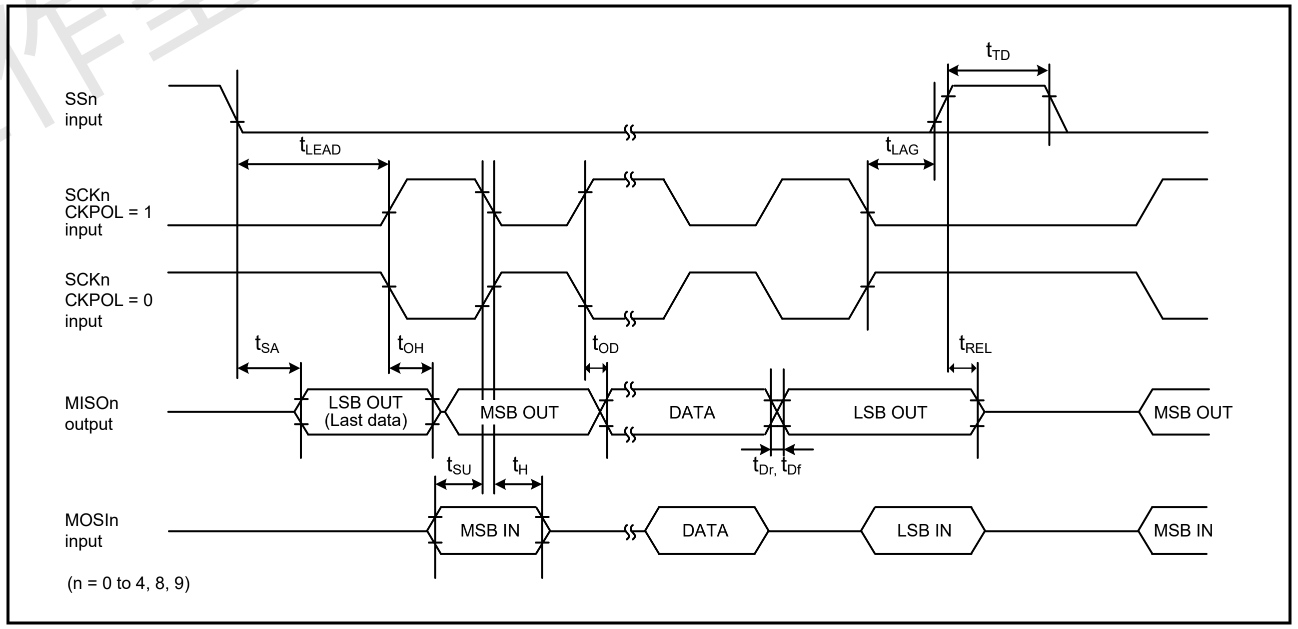


Figure 2.42 CKPH=0时从机的SCI简单SPI模式时序

Table 2.24 SCI计时(3)(1of2)

条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	-	1000	ns	Figure 2.43
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	250	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Table 2.24 SCI timing (3) (2 of 2)
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.43
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. Cb indicates the total capacity of the bus line.

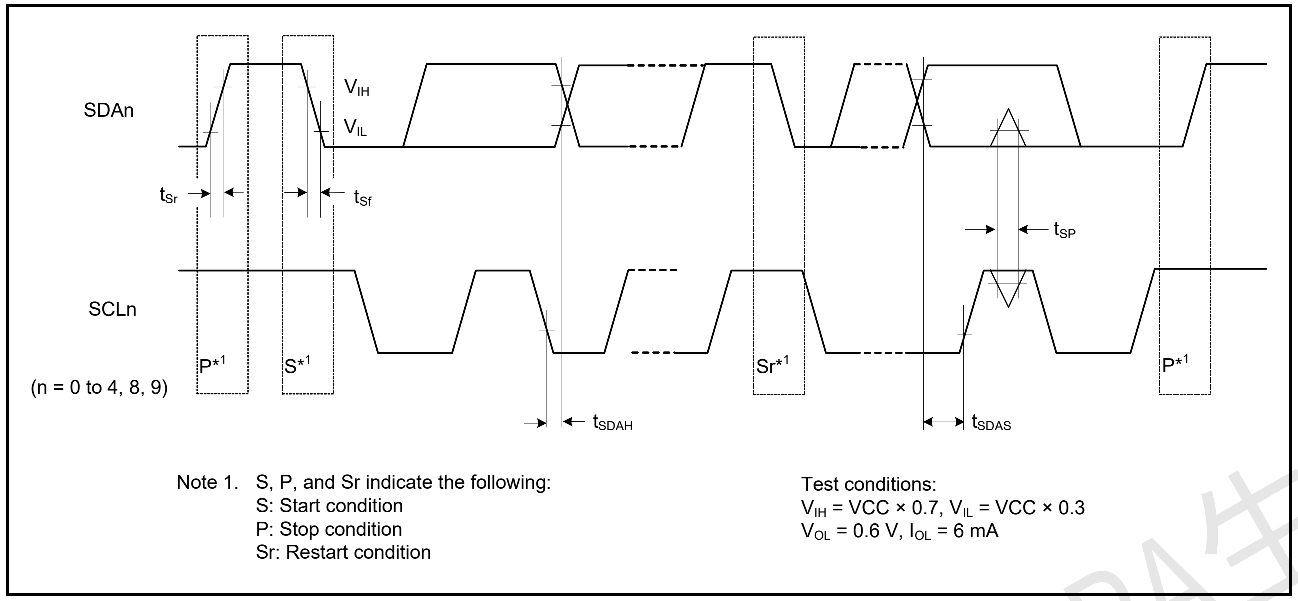


Figure 2.43 SCI simple IIC mode timing

Table 2.24 SCI计时(3)(2of2)
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	-	300	ns	Figure 2.43
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	100	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note 1. Cb表示公交线路的总容量。

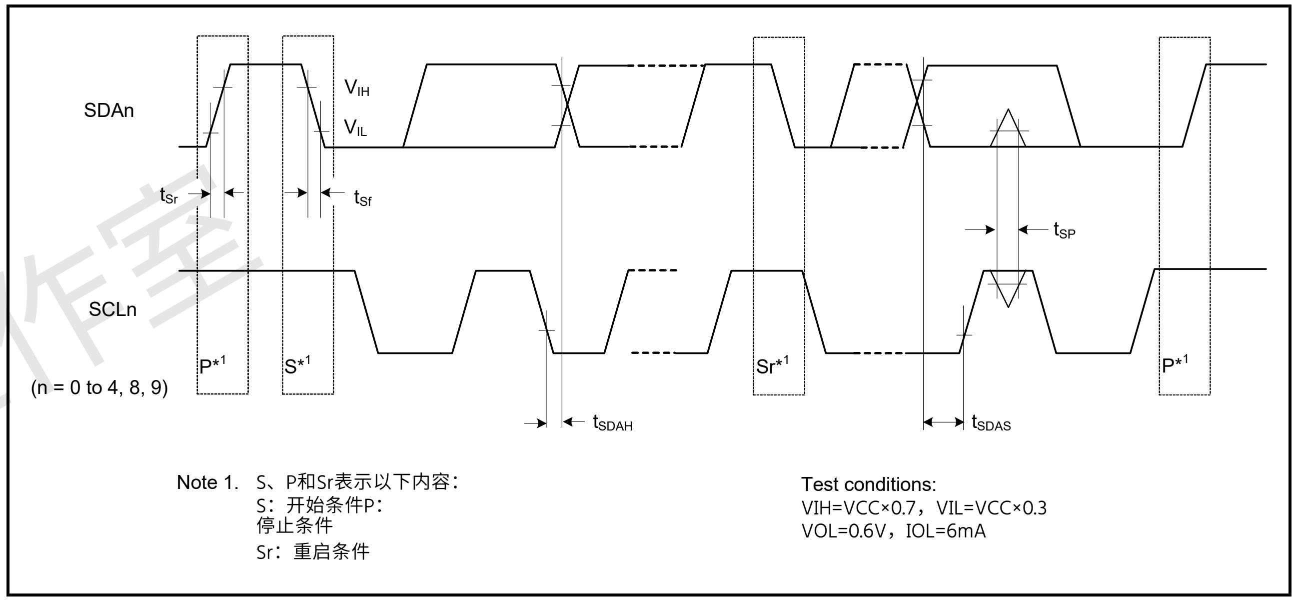


Figure 2.43 SCI简单IIC模式时序

2.3.11 SPI Timing

Table 2.25 SPI timing

Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the Port Drive Capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.44 C = 30 pF
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	μs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 2.45 to Figure 2.50 C = 30 pF
		Slave		5	-		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 10$*3	$N \times t_{SPcyc} + 100$*3	ns	
		Slave		$6 \times t_{Pcyc}$	-	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 10$ *4	$N \times t_{SPcyc} + 100$*4	ns	
		Slave		$6 \times t_{Pcyc}$	-	ns	
	Data output delay	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$6 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	μs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	μs	
	Slave access time		t_{SA}	-	$2 \times t_{Pcyc} + 28$	ns	Figure 2.49 and Figure 2.50 C = 30pF
	Slave output release time		t_{REL}	-	$2 \times t_{Pcyc} + 28$		

Note 1. t_{Pcyc}: PCLKA cycle.

2.3.11 SPI时序

Table 2.25 SPI时序

Conditions:
对于RSPCKA和RSPCKB引脚，通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK时钟周期	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.44 C = 30 pF
		Slave		4	4096		
	RSPCK时钟高脉冲宽度	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK时钟低脉冲宽度	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK时钟上升和下降时间	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	μs	
	数据输入建立时间	Master	t_{SU}	4	-	ns	图2.45至 Figure 2.50 C = 30 pF
		Slave		5	-		
	数据输入保持时间	主控（PCLKA分频比设置为1/2）	t_{HF}	0	-	ns	
		主控（PCLKA分频比设置为1/2以外的值）	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL设置时间	Master	t_{LEAD}	$N \times t_{SPcyc} - 10$*3	$N \times t_{SPcyc} + 100$*3	ns	
		Slave		$6 \times t_{Pcyc}$	-	ns	
	SSL保持时间	Master	t_{LAG}	$N \times t_{SPcyc} - 10$ *4	$N \times t_{SPcyc} + 100$*4	ns	
		Slave		$6 \times t_{Pcyc}$	-	ns	
	数据输出延迟	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	数据输出保持时间	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	连续传输延迟	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$6 \times t_{Pcyc}$			
	MOSI和MISO上升和下降时间	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	μs	
	SSL上升和下降时间	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	μs	
	从站访问时间		t_{SA}	-	$2 \times t_{Pcyc} + 28$	ns	图2.49和 Figure 2.50 C = 30pF
	从机输出释放时间		t_{REL}	-	$2 \times t_{Pcyc} + 28$		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

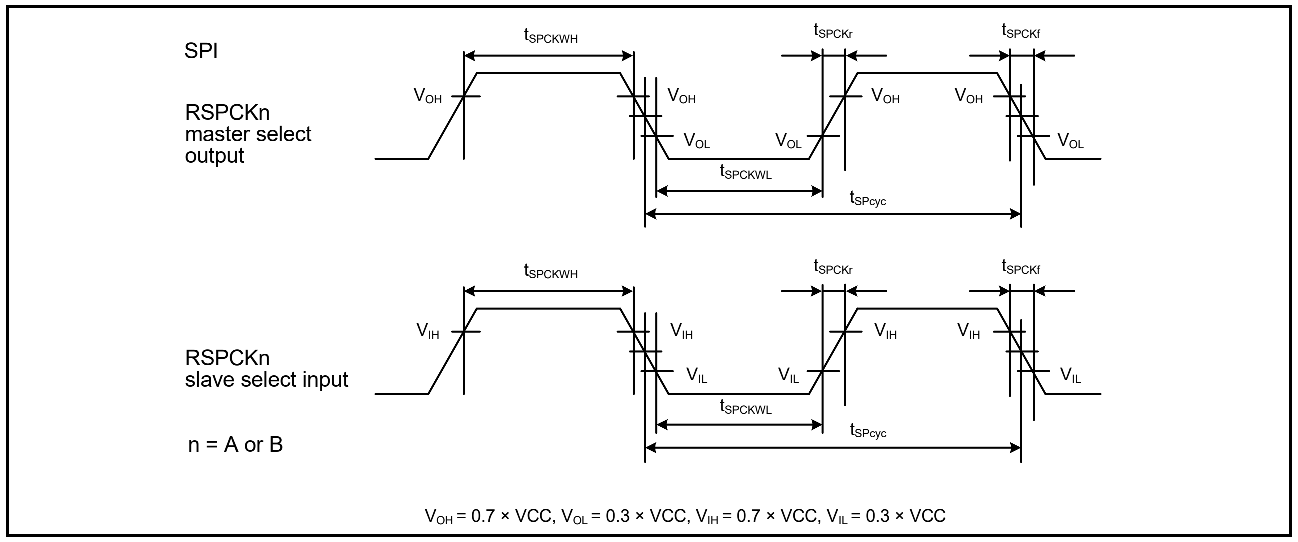


Figure 2.44 SPI clock timing

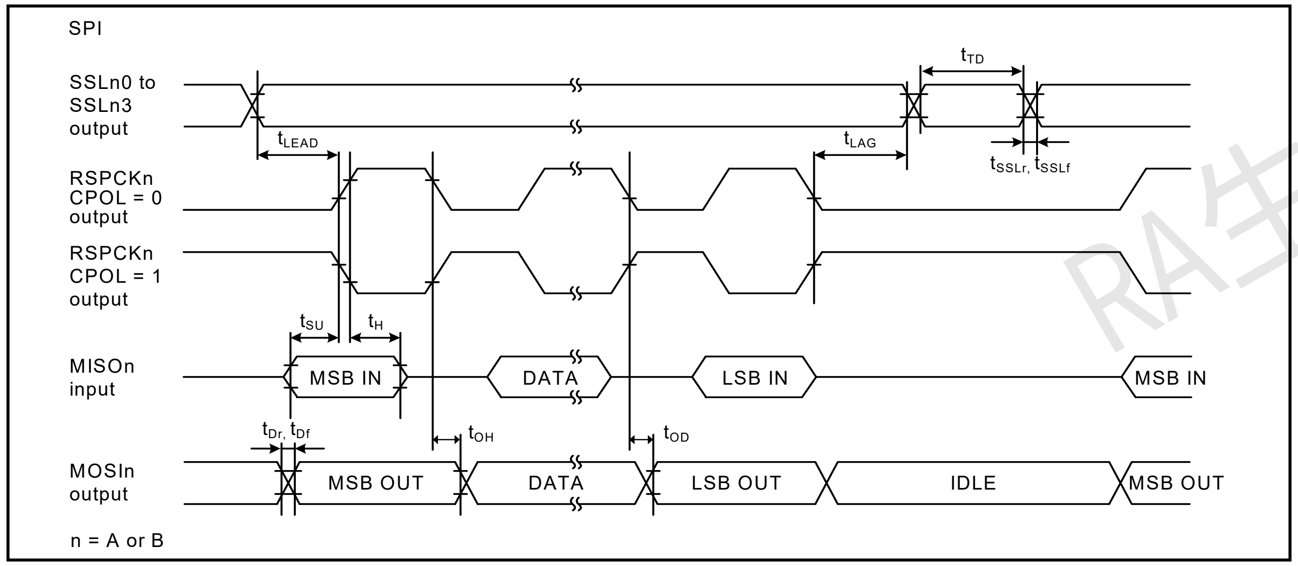


Figure 2.45 SPI timing for master when CPHA = 0

RA6M1 Group 2、电气特性

Note 2. 必须使用名称后附有字母的引脚，例如"_A"、"_B"，以表示组成员身份。对于SPI接口，测量每组的电气特性的交流部分。

Note 3. N由SPCKD寄存器设置为从1到8的整数。
Note 4. N由SSLND寄存器设置为从1到8的整数。

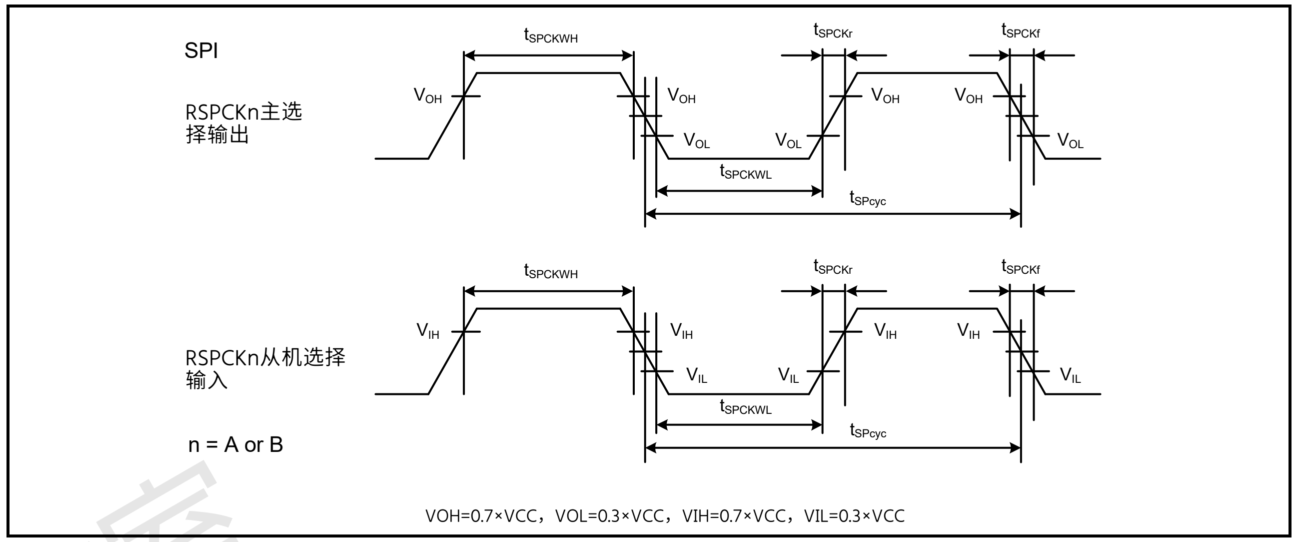


Figure 2.44 SPI时钟时序

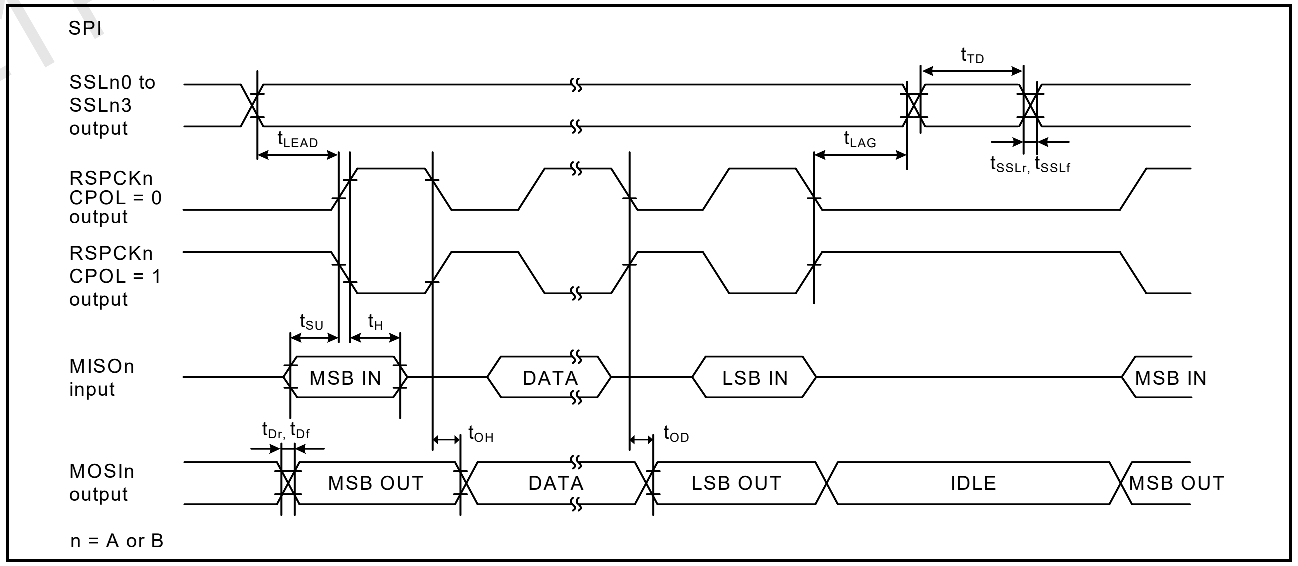


Figure 2.45 CPHA=0时主机的SPI时序

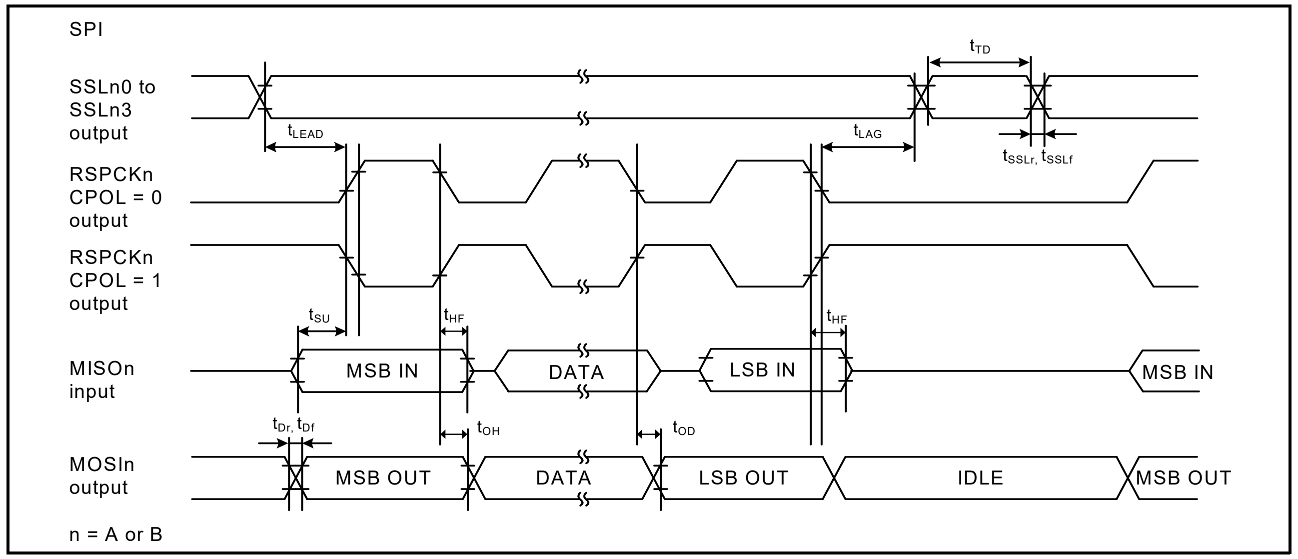


Figure 2.46 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

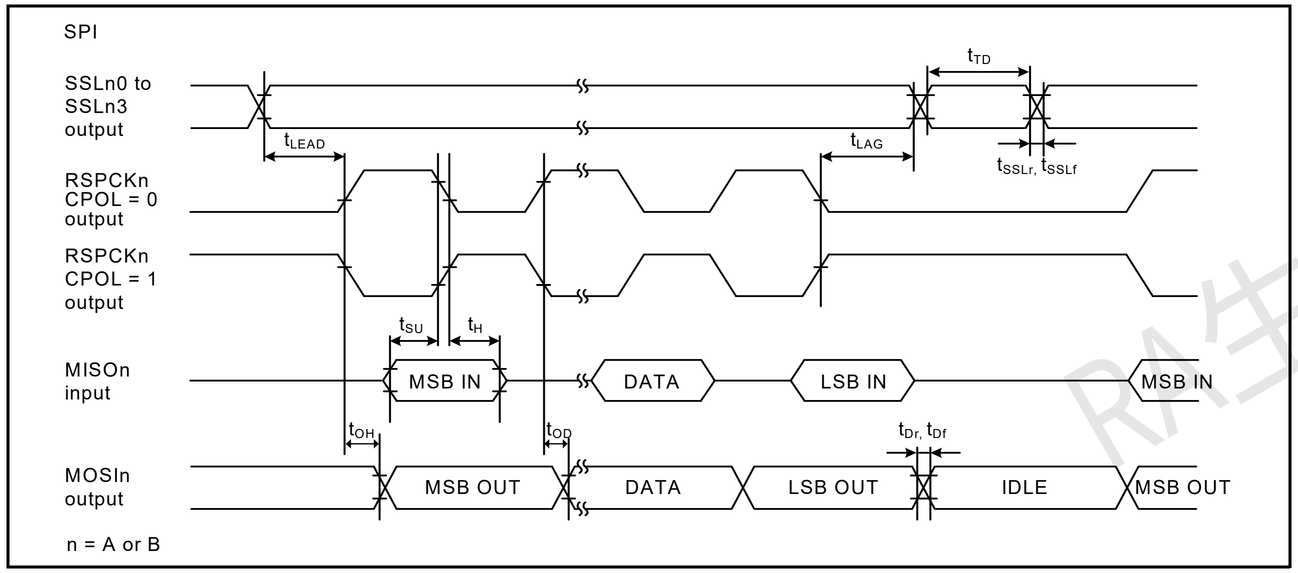


Figure 2.47 SPI timing for master when CPHA = 1

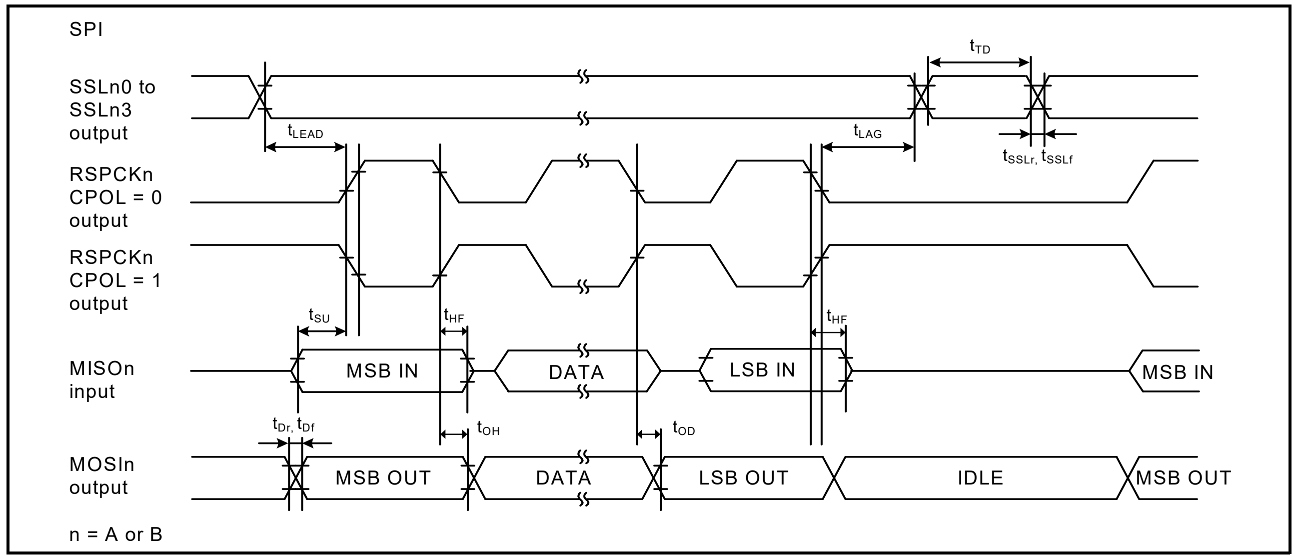


Figure 2.46 **当CPHA=0且比特率设置为PCLKA2时主设备的SPI时序**

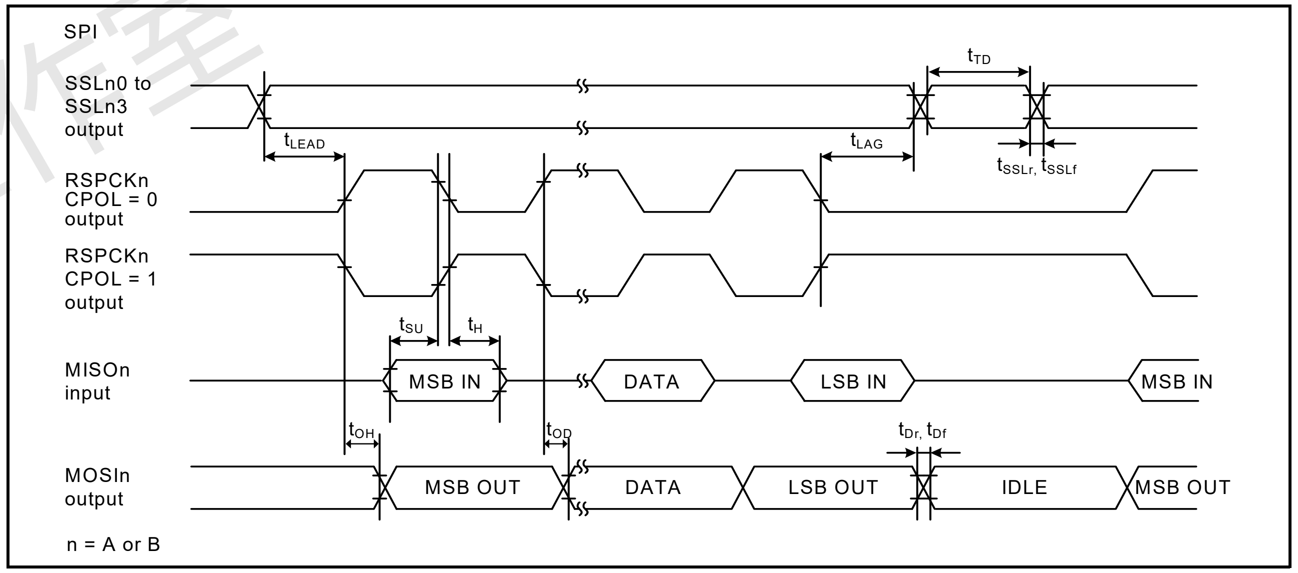


Figure 2.47 **CPHA=1时主机的SPI时序**

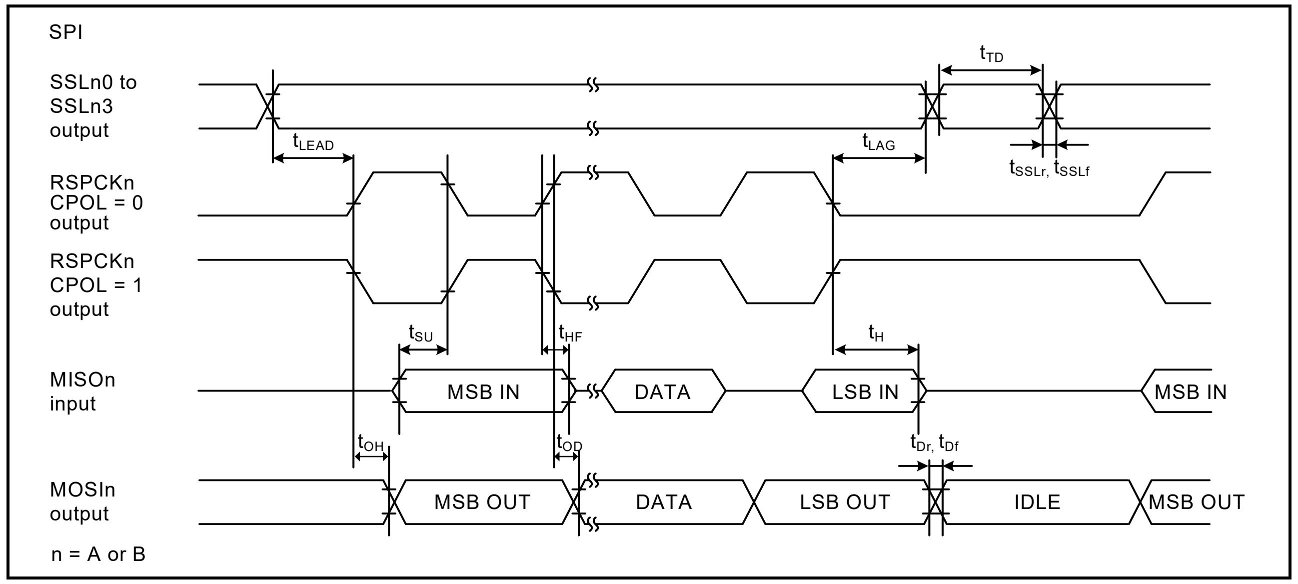


Figure 2.48 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

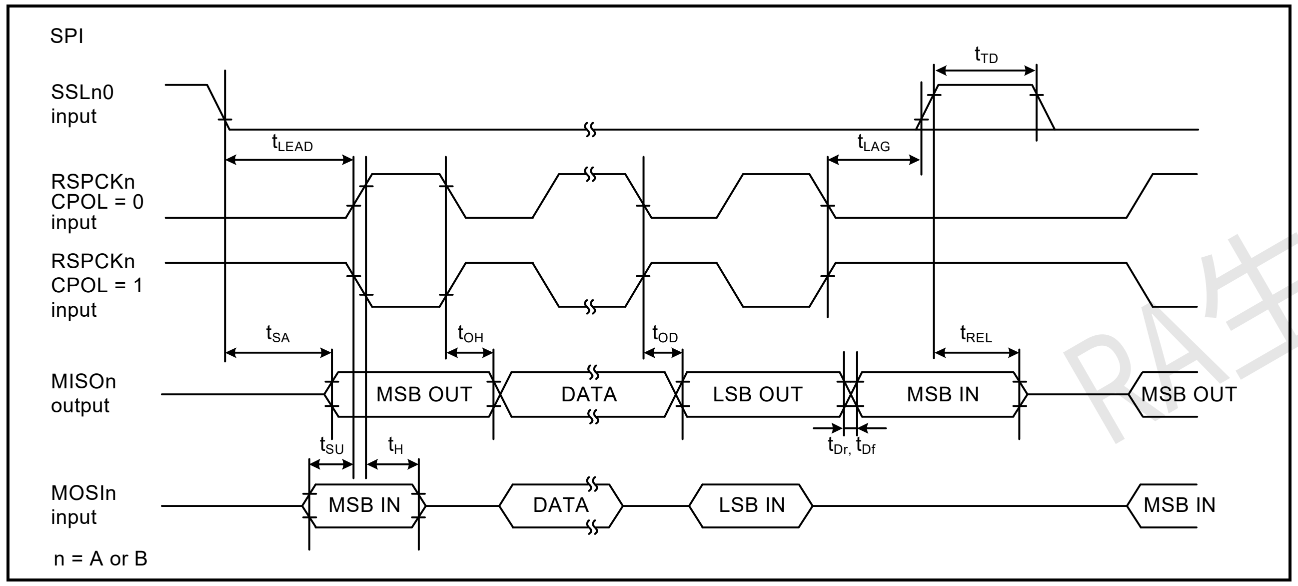


Figure 2.49 SPI timing for slave when CPHA = 0

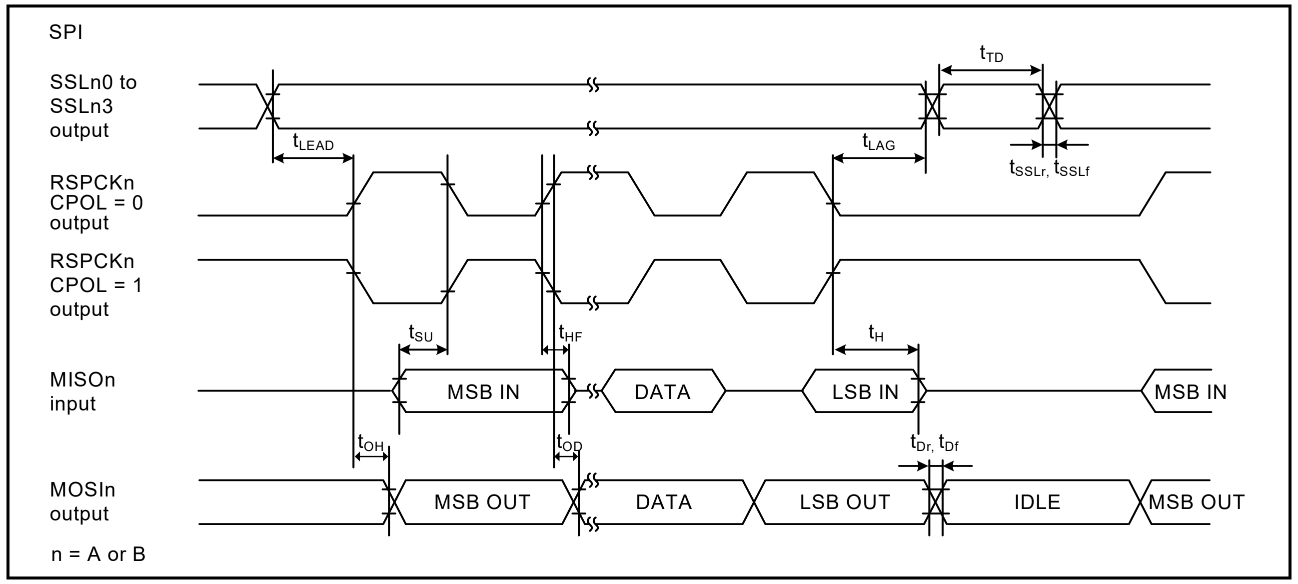


Figure 2.48 当CPHA=1且比特率设置为PCLKA2时，主机的RSPI时序

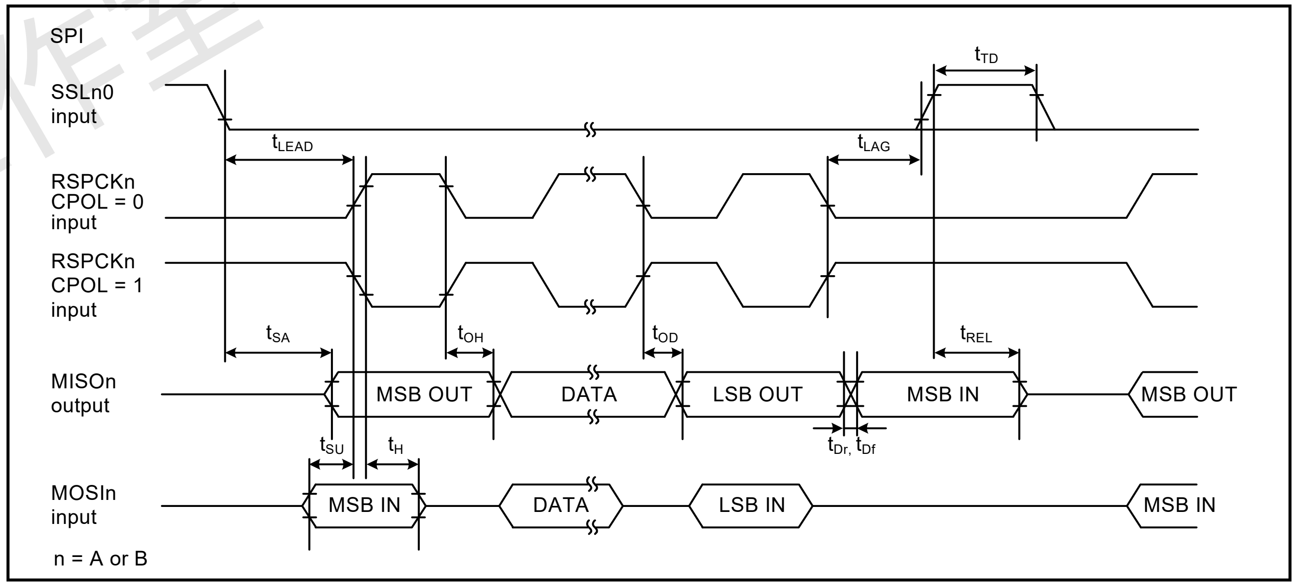


Figure 2.49 CPHA=0时从机的SPI时序

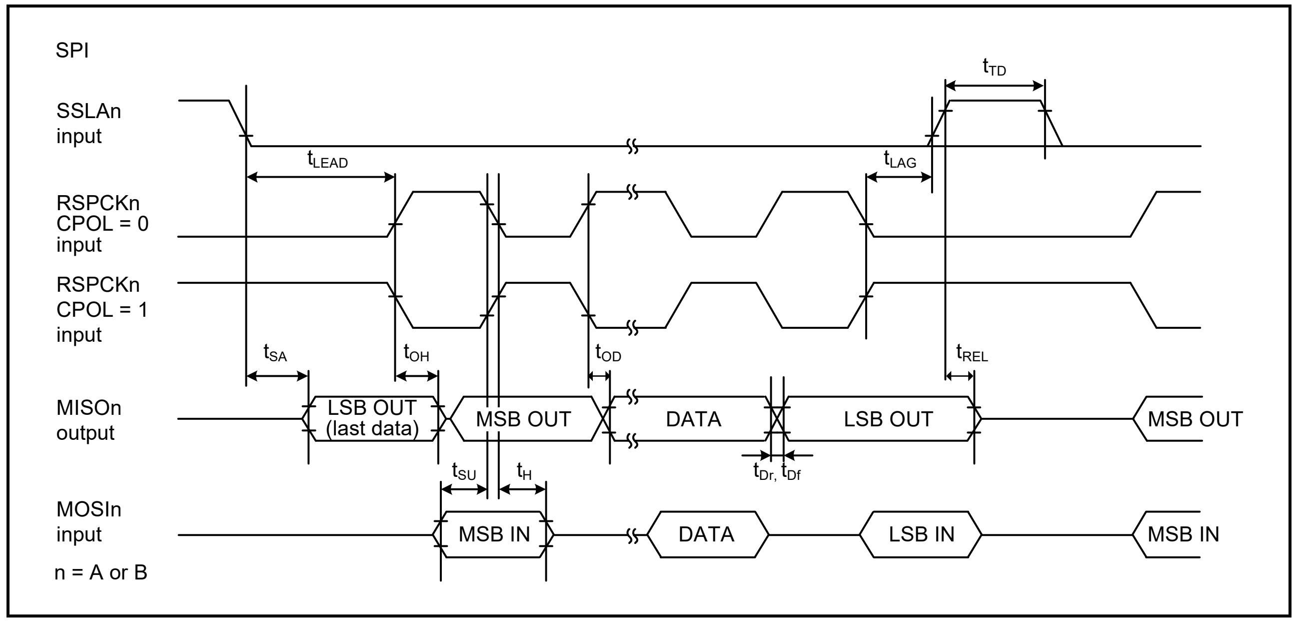


Figure 2.50 SPI timing for slave when CPHA = 1

2.3.12 QSPI Timing

Table 2.26 QSPI timing
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit[*1]	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.51
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	Data input setup time	t_{Su}	8	-	ns	Figure 2.52
	Data input hold time	t_{IH}	0	-	ns	
	QSSL setup time	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 [*2]	(N+0.5) x t_{Qscyc} +100 [*2]	ns	
	QSSL hold time	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 [*3]	(N+0.5) x t_{Qscyc} +100 [*3]	ns	
	Data output delay	t_{OD}	-	4	ns	
	Data output hold time	t_{OH}	-3.3	-	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set to 0 or 1 in SFMSLD.
Note 3. N is set to 0 or 1 in SFMSHD.

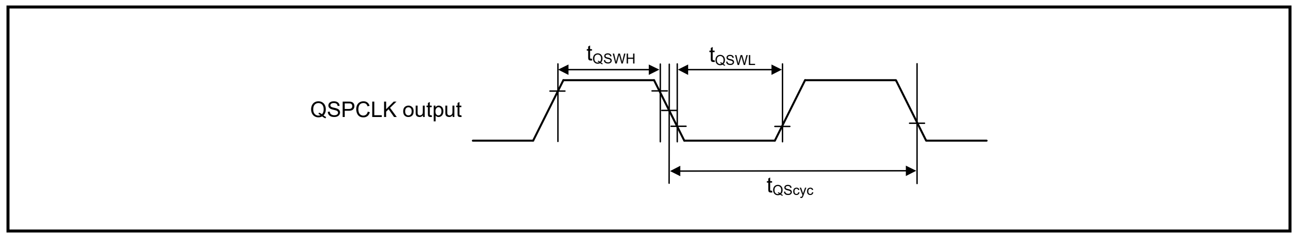


Figure 2.51 QSPI clock timing

RA6M1 Group

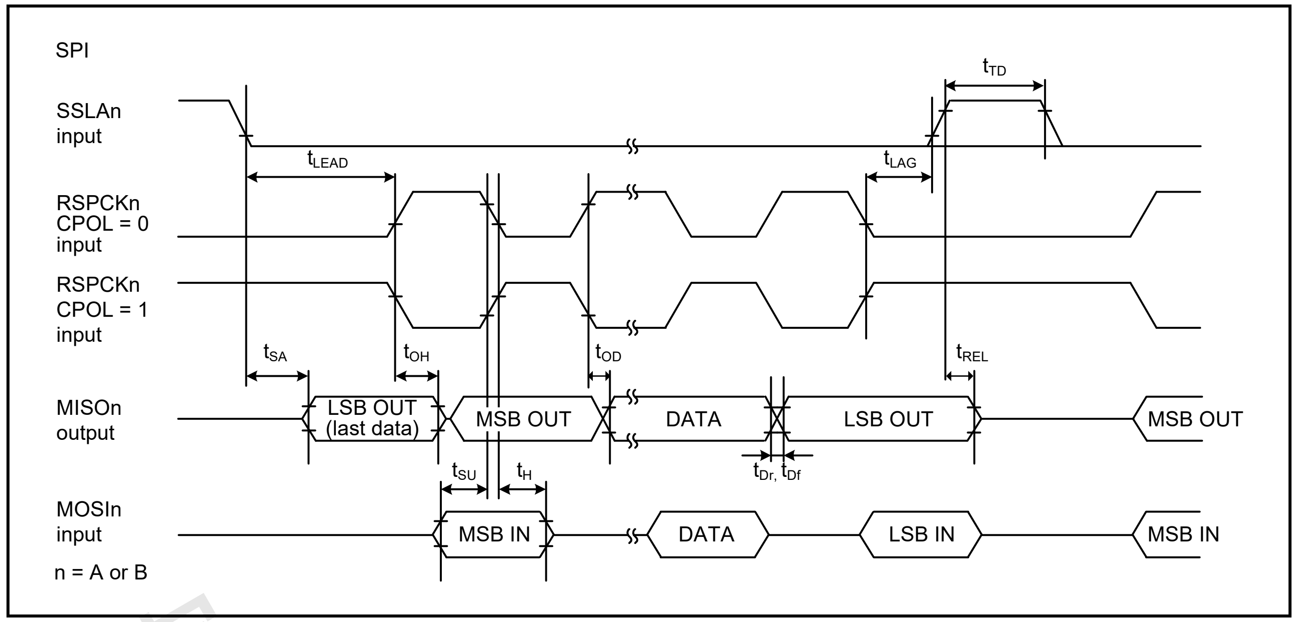


Figure 2.50 CPHA=1时从机的SPI时序

2.3.12 QSPI Timing

Table 2.26 QSPI timing
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		Symbol	Min	Max	Unit[*1]	测试条件
QSPI	QSPCK时钟周期	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.51
	QSPCK时钟高脉冲宽度	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK时钟低脉冲宽度	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	数据输入建立时间	t_{Su}	8	-	ns	Figure 2.52
	数据输入保持时间	t_{IH}	0	-	ns	
	QSSL设置时间	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 [*2]	(N+0.5) x t_{Qscyc} +100 [*2]	ns	
	QSSL保持时间	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 [*3]	(N+0.5) x t_{Qscyc} +100 [*3]	ns	
	数据输出延迟	t_{OD}	-	4	ns	
	数据输出保持时间	t_{OH}	-3.3	-	ns	
	连续传输延迟	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N在SFMSLD中设置为0或1。
Note 3. N在SFMSHD中设置为0或1。

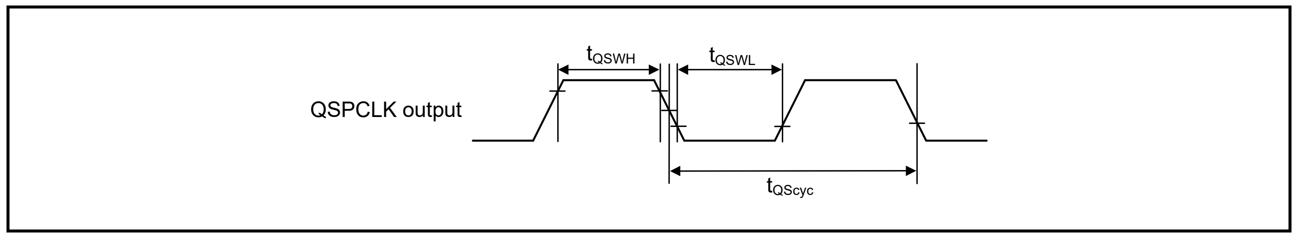


Figure 2.51 QSPI时钟时序

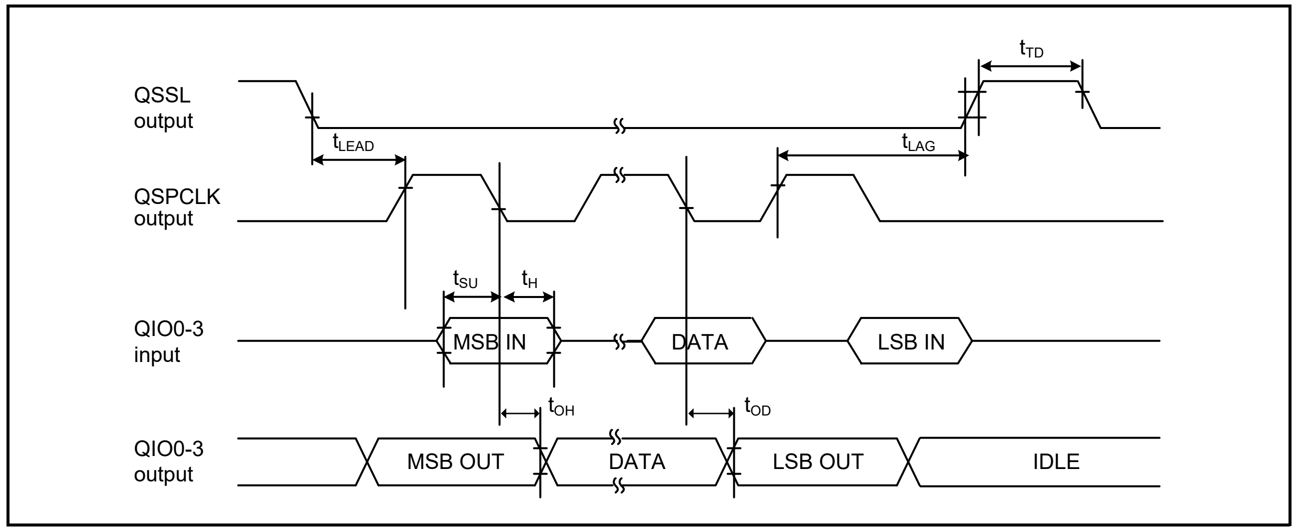


Figure 2.52 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.53
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

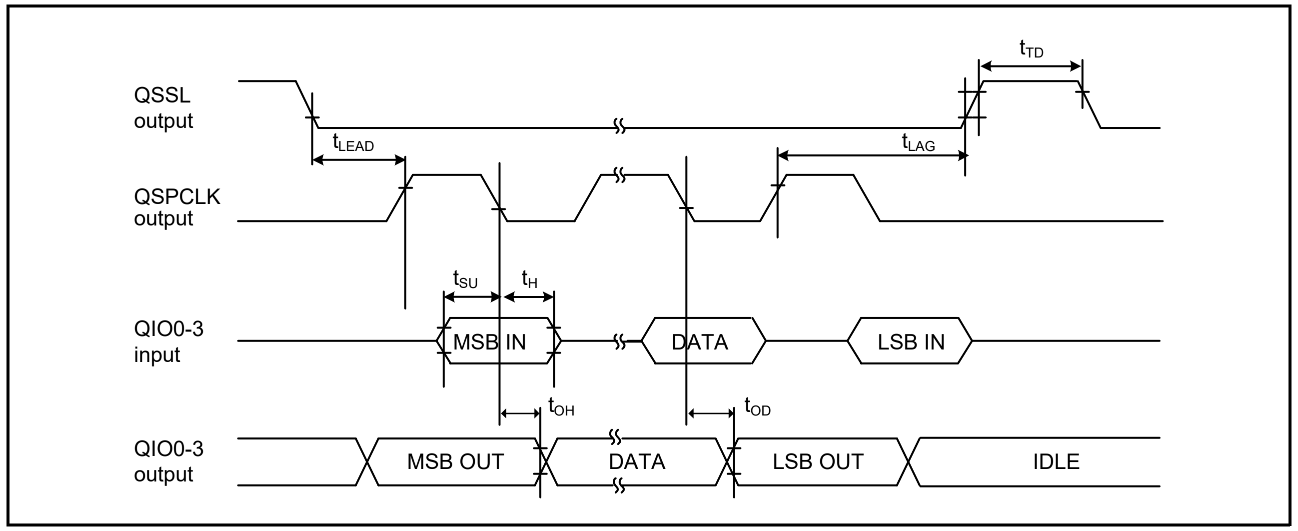


Figure 2.52 发送和接收时序

2.3.13 IIC Timing

表2.27IIC时序(1)(1of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.53
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	-	ns	
	STOP条件输入建立时间	t_{STOS}	1000	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Table 2.27 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A.

(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.53
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0_A, SDA0_A.

Note 3. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

表2.27IIC时序(1)(2of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.53
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	300	-	ns	
	STOP条件输入建立时间	t_{STOS}	300	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。

Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。

Note 2. 仅支持SCL0_A、SDA0_A。

Note 3. 必须使用名称后附有字母的引脚，例如"_A"、"_B"，以表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Table 2.28 IIC timing (2)

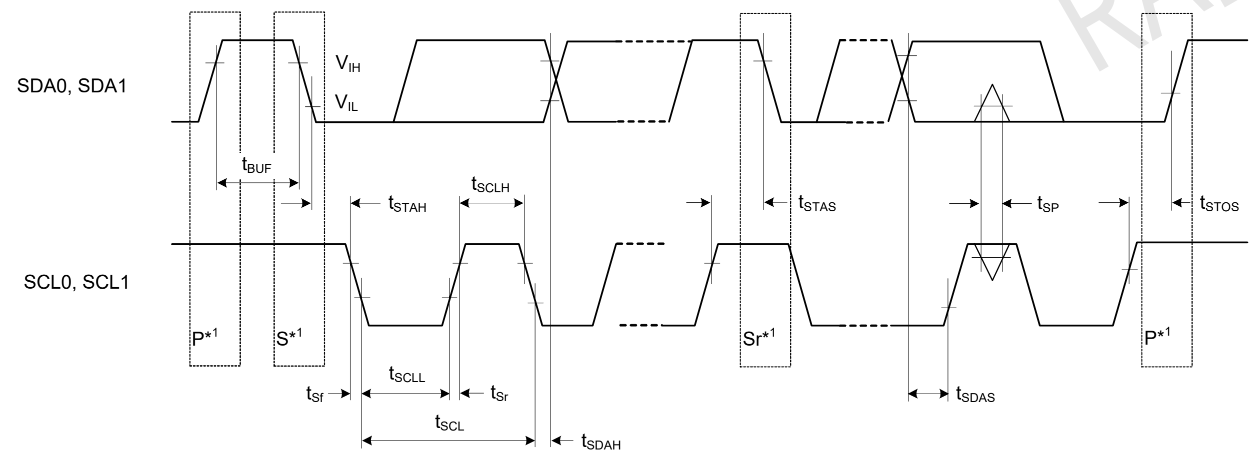
Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min[*1,*2]	Max	Unit	Test conditions
IIC (Fast mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.53
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Cb indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA (ICFER.FMPE = 0)
V_{OL} = 0.4 V, I_{OL} = 15 mA (ICFER.FMPE = 1)

Figure 2.53 I2C bus interface input/output timing

Table 2.28 IIC timing (2)

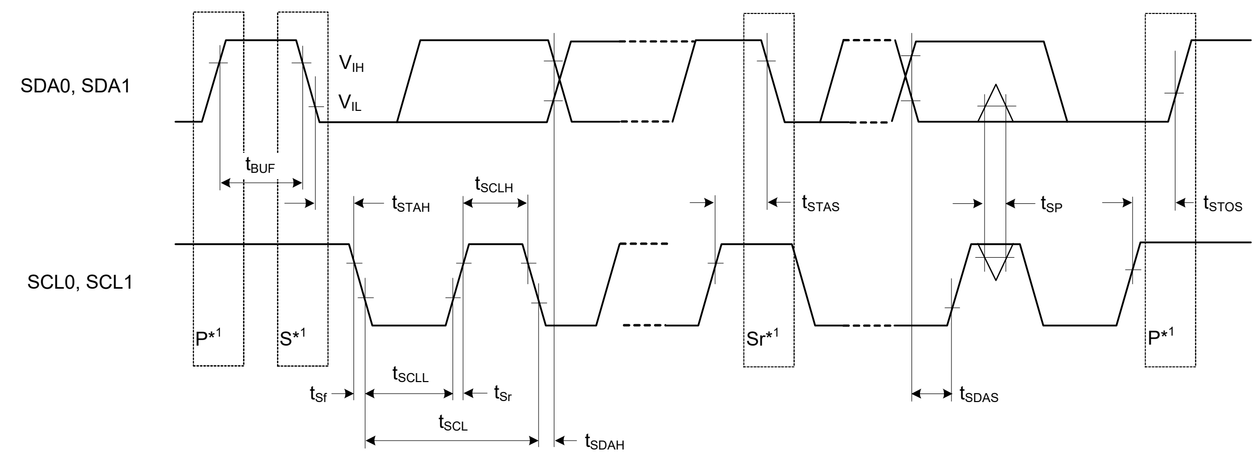
PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

Parameter		Symbol	Min[*1,*2]	Max	Unit	测试条件
IIC (Fast mode+) ICFER.FMPE = 1	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.53
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	120	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	120	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	禁用唤醒功能时的启动条件输入保持时间	t_{STAH}	t_{IICcyc} + 120	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	重启条件输入建立时间	t_{STAS}	120	-	ns	
	停止条件输入建立时间	t_{STOS}	120	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。

Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。

Note 2. Cb表示公交线路的总容量。



Note 1. S、P和Sr表示以下内容：
S：开始条件P：
停止条件
Sr：重启条件

Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA(ICFER.FMPE=0)VOL=
0.4V，IOL=15mA(ICFER.FMPE=1)

Figure 2.53 I2C总线接口输入输出时序

2.3.14 SSIE Timing

Table 2.29 SSIE timing

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance “_A” or “_B” to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification Min.	Max.	Unit	Comments
SSIBCK0	Cycle	Master	t_O	80	-	ns	Figure 2.54
		Slave	t_I	80	-	ns	
	High level/low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK0/SSIFS0, SSITXD0, SSIRXD0	Input set up time	Master	t_{SR}	12	-	ns	Figure 2.56, Figure 2.57
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.56, Figure 2.57
	Output delay time from SSILRCK0/SSIFS0 change	Slave	t_{DTRW}	-	20	ns	Figure 2.58*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.55
	High level/low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 pin.

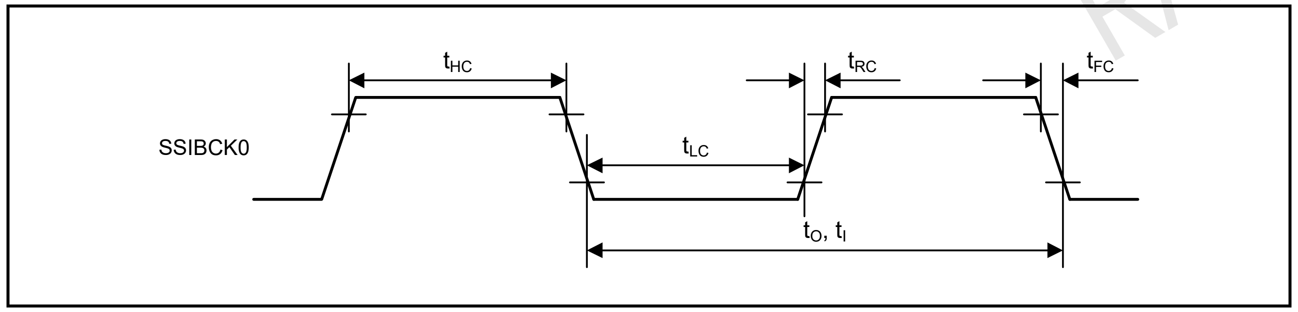


Figure 2.54 SSIE clock input/output timing

2.3.14 SSIE Timing

表2.29SSIE时序(1)通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用名称后附有字母的引脚，例如“_A”或“_B”来表示组成员身份。对于SSIE接口，测量每组的电气特性的交流部分。

Parameter			Symbol	目标规格 Min.	Max.	Unit	Comments
SSIBCK0	Cycle	Master	t_O	80	-	ns	Figure 2.54
		Slave	t_I	80	-	ns	
	高电平低电平	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	上升时间下降时间	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK0/SSIFS0, SSITXD0, SSIRXD0	输入建立时间	Master	t_{SR}	12	-	ns	Figure 2.56, Figure 2.57
		Slave		12	-	ns	
	输入保持时间	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	输出延迟时间	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.56, Figure 2.57
	从输出延迟时间 SSILRCK0/SSIFS0 change	Slave	t_{DTRW}	-	20	ns	Figure 2.58*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.55
	高电平低电平		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. 对于从模式传输，SSIE有一条路径，通过该路径从SSILRCK0SSIFS0引脚输入的信号用于生成传输数据，并将传输数据逻辑输出到SSITXD0引脚。

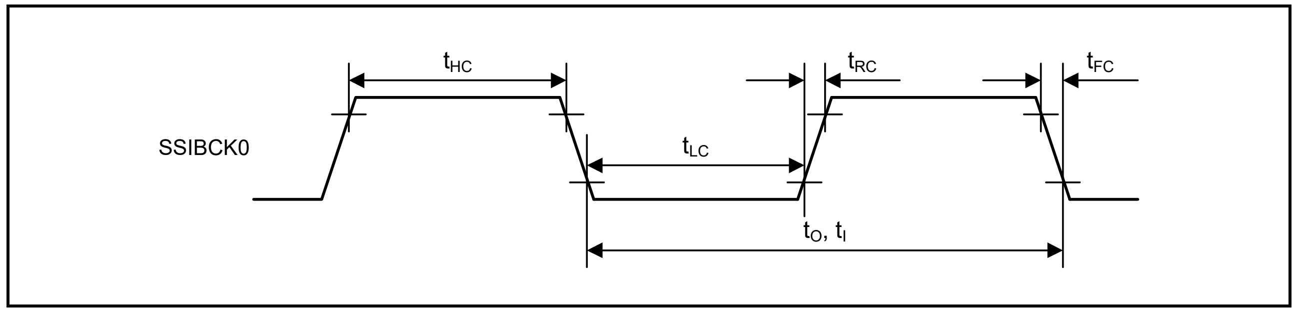


Figure 2.54 SSIE时钟输入输出时序

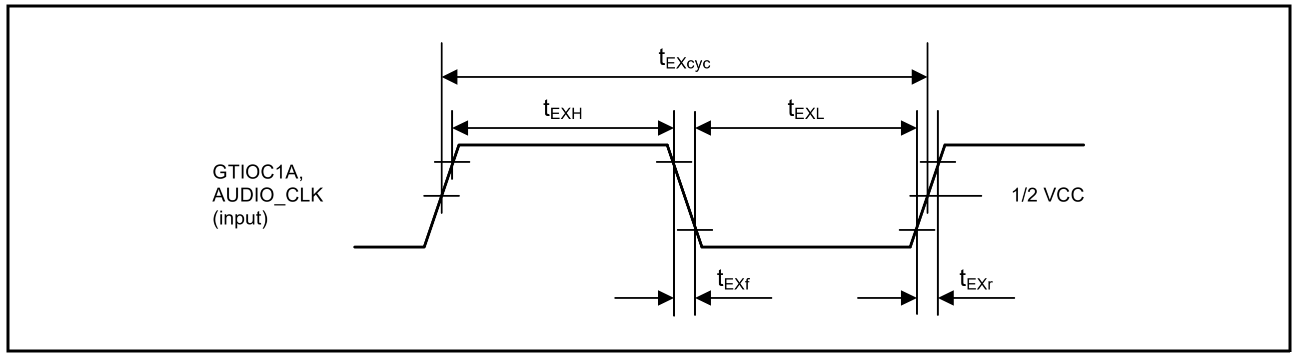


Figure 2.55 Clock input timing

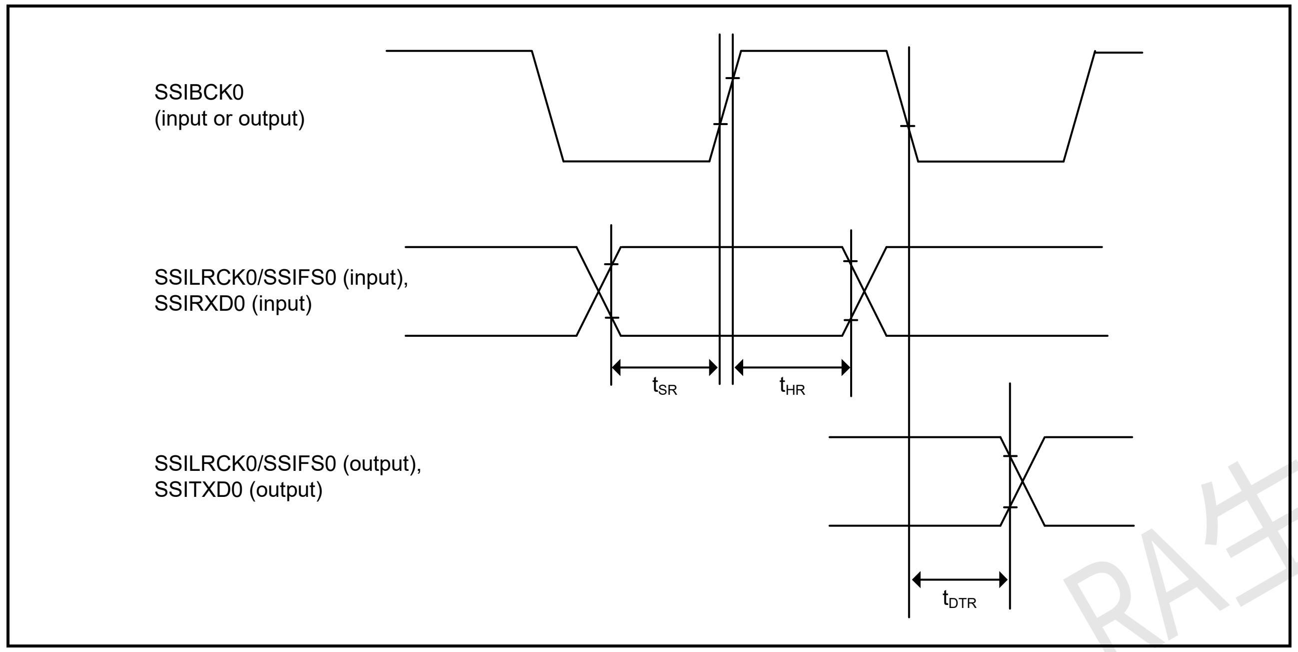


Figure 2.56 SSIE data transmit and receive timing when SSICR.BCKP = 0

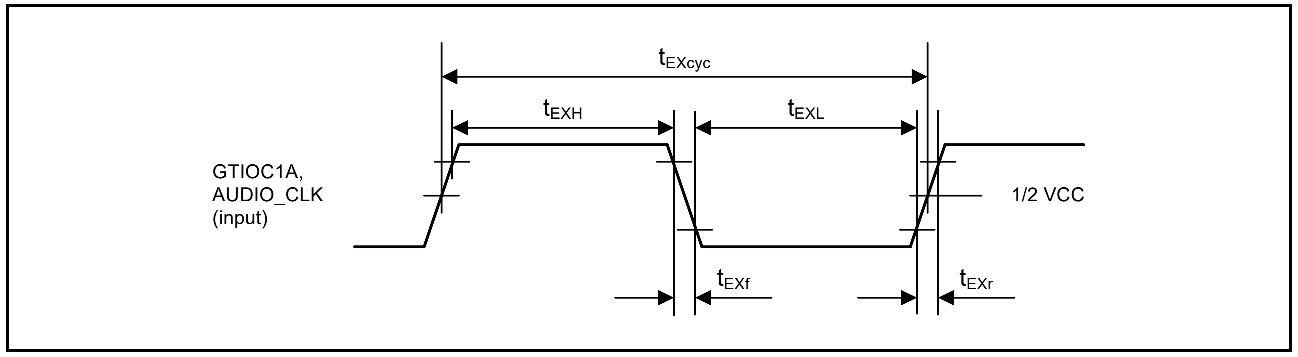


Figure 2.55 时钟输入时序

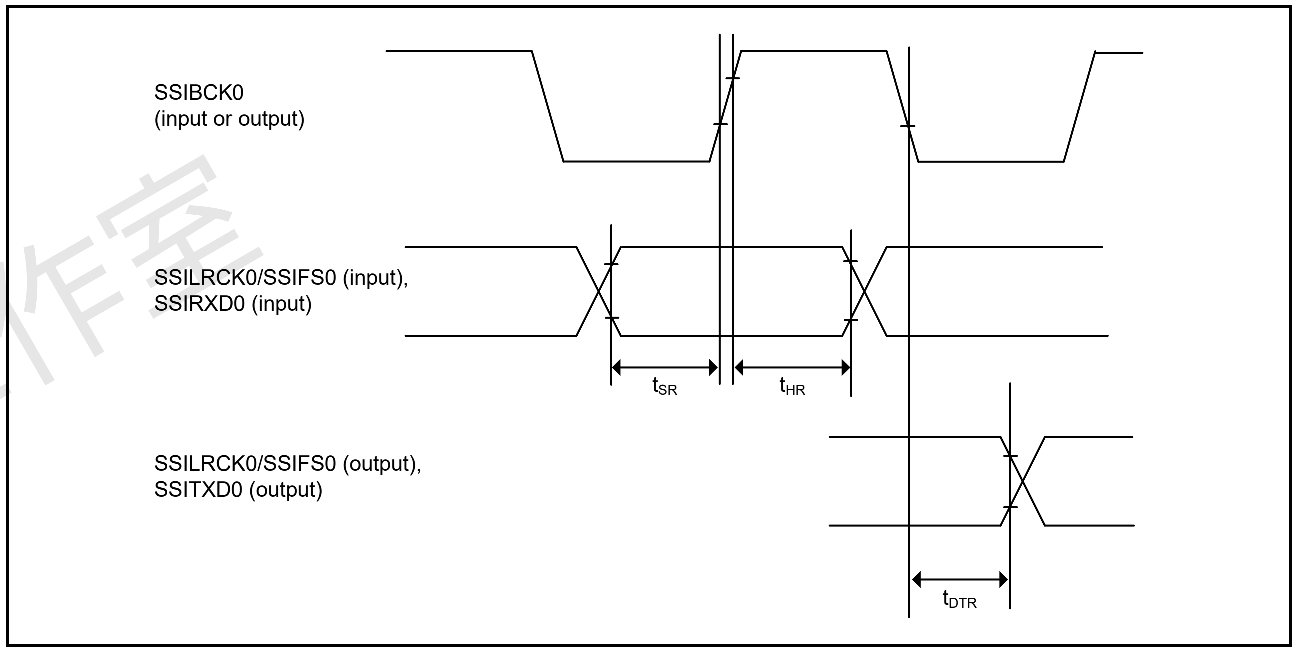


Figure 2.56 SSICR.BCKP=0时的SSIE数据发送和接收时序

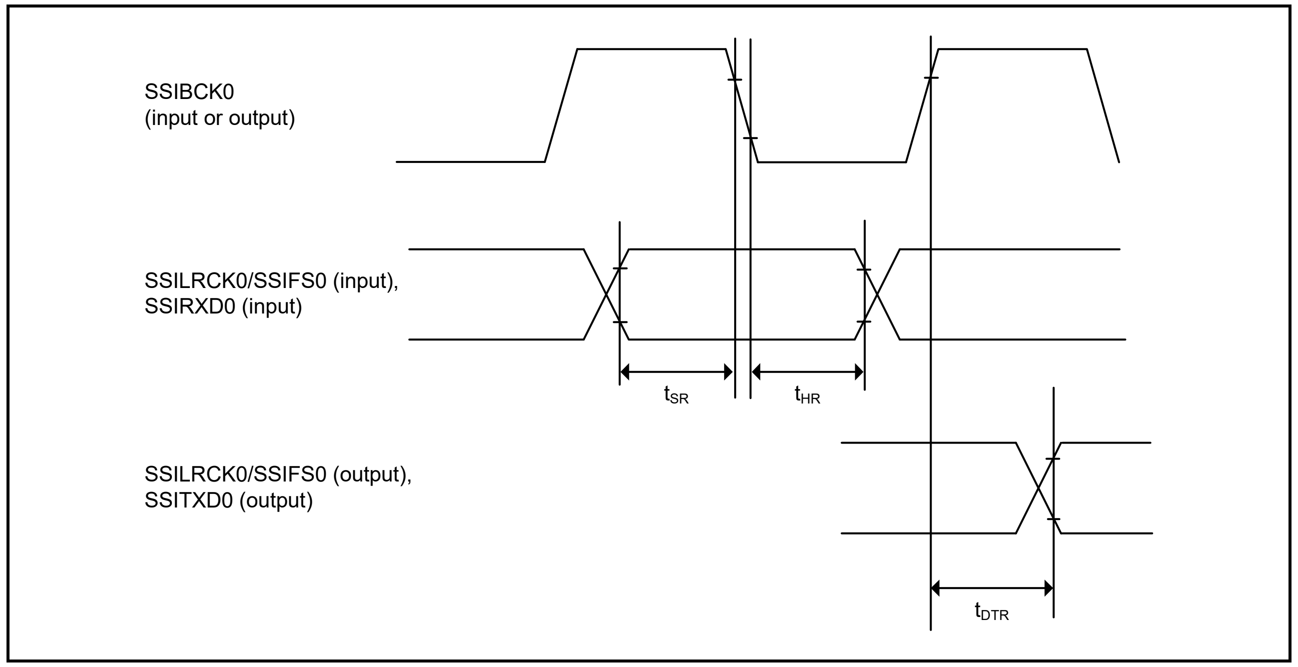


Figure 2.57 SSIE data transmit and receive timing when SSICR.BCKP = 1

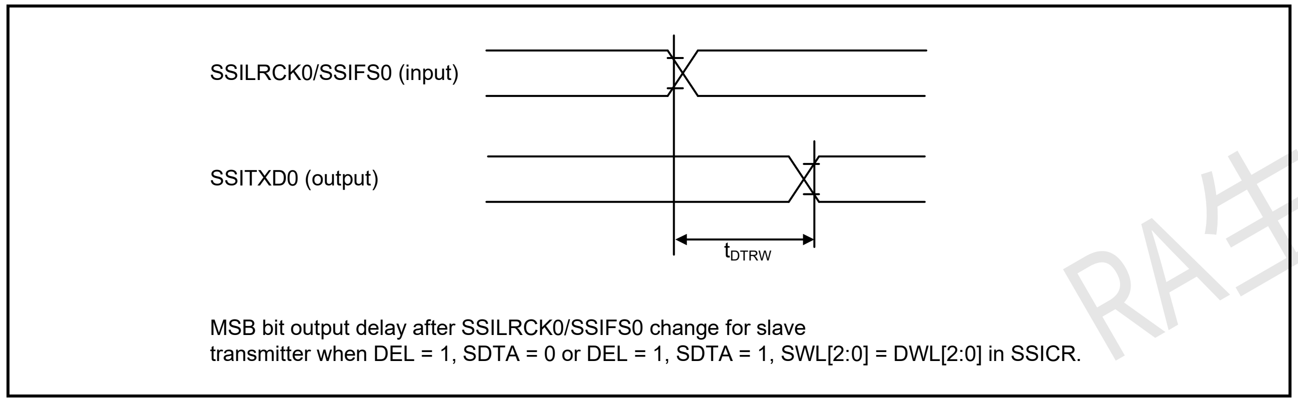


Figure 2.58 SSIE data output delay after SSILRCK0/SSIFS0 change

2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Parameter	Symbol	Min	Max	Unit	Test conditions*1
SDCLK clock cycle	T_{SDCYC}	20	-	ns	Figure 2.59
SDCLK clock high pulse width	T_{SDWH}	6.5	-	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	-	ns	
SDCLK clock rise time	T_{SDLH}	-	3	ns	
SDCLK clock fall time	T_{SDHL}	-	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	-6	5	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4	-	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	2	-	ns	

Note 1. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

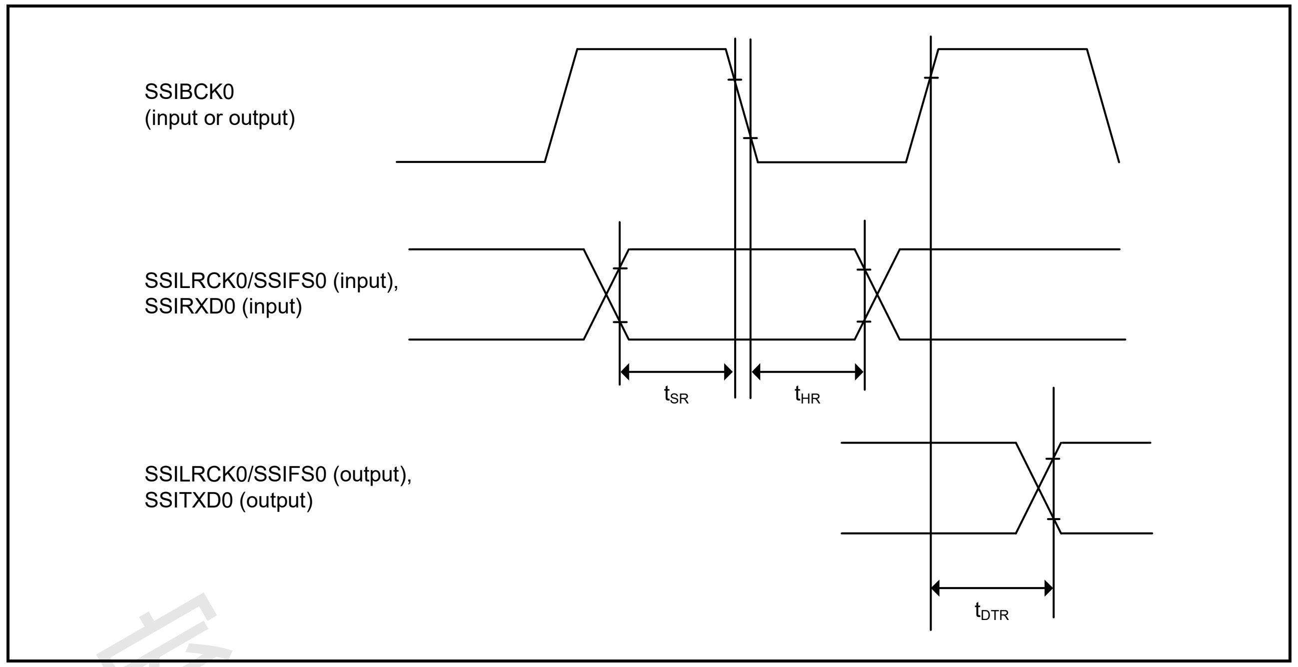


Figure 2.57 SSICR.BCKP=1时的SSIE数据发送和接收时序

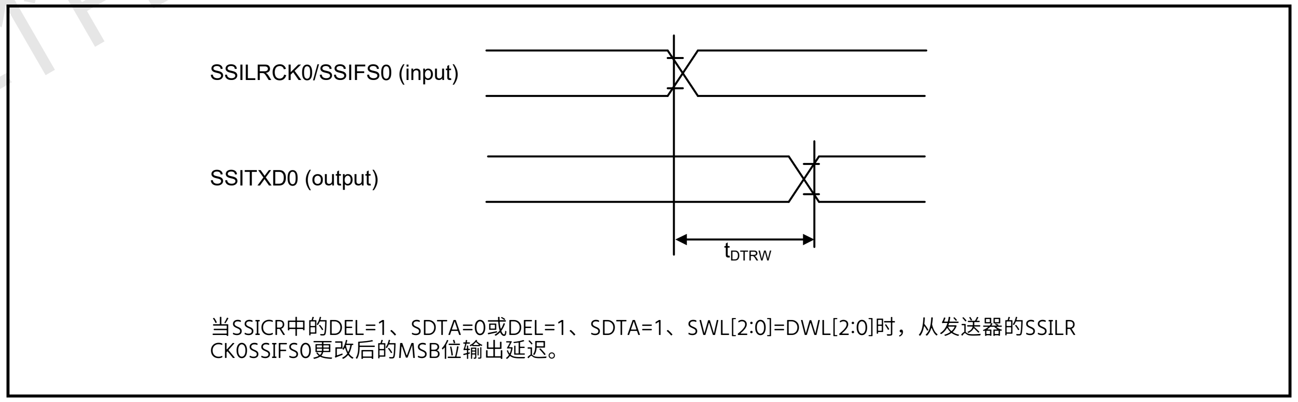


Figure 2.58 SSILRCK0SSIFS0更改后的SSIE数据输出延迟

2.3.15 SDMMC主机接口时序

Table 2.30 SDMMC主机接口信号时序
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
时钟占空比为50%。

Parameter	Symbol	Min	Max	Unit	Test conditions*1
SDCLK 时钟周期	T_{SDCYC}	20	-	ns	Figure 2.59
SDCLK 时钟高脉冲宽度	T_{SDWH}	6.5	-	ns	
SDCLK 时钟低脉冲宽度	T_{SDWL}	6.5	-	ns	
SDCLK 时钟上升时间	T_{SDLH}	-	3	ns	
SDCLK 时钟下降时间	T_{SDHL}	-	3	ns	
SDCMDSDDAT输出数据延迟	T_{SDODLY}	-6	5	ns	
SDCMDSDDAT输入数据设置	T_{SDIS}	4	-	ns	
SDCMDSDDAT输入数据保持	T_{SDIH}	2	-	ns	

注1.必须使用名称后附有字母的引脚，例如"_A"、"_B"，以表示组成员身份。
对于SDMMC主机接口，测量每组的电气特性的交流部分。

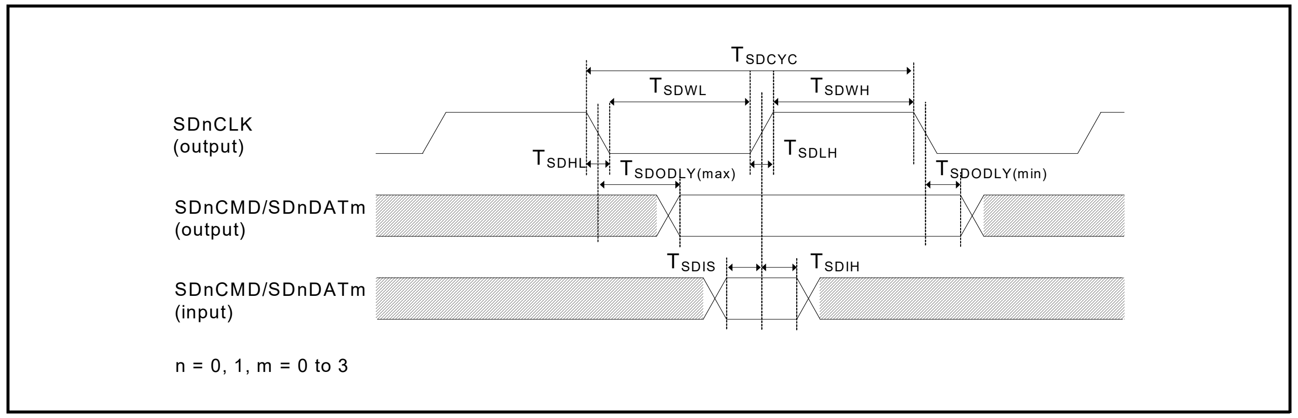


Figure 2.59 SD/MMC Host Interface signal timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.31 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.60
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

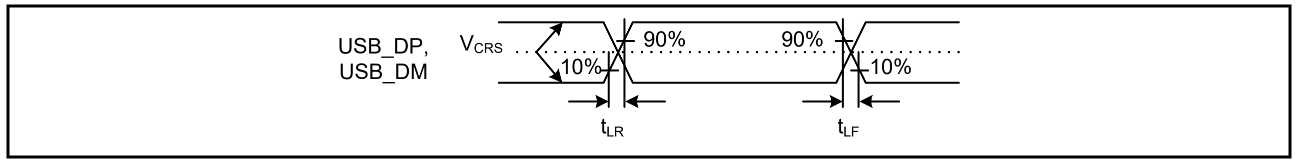


Figure 2.60 USB_DP and USB_DM output timing in low-speed mode

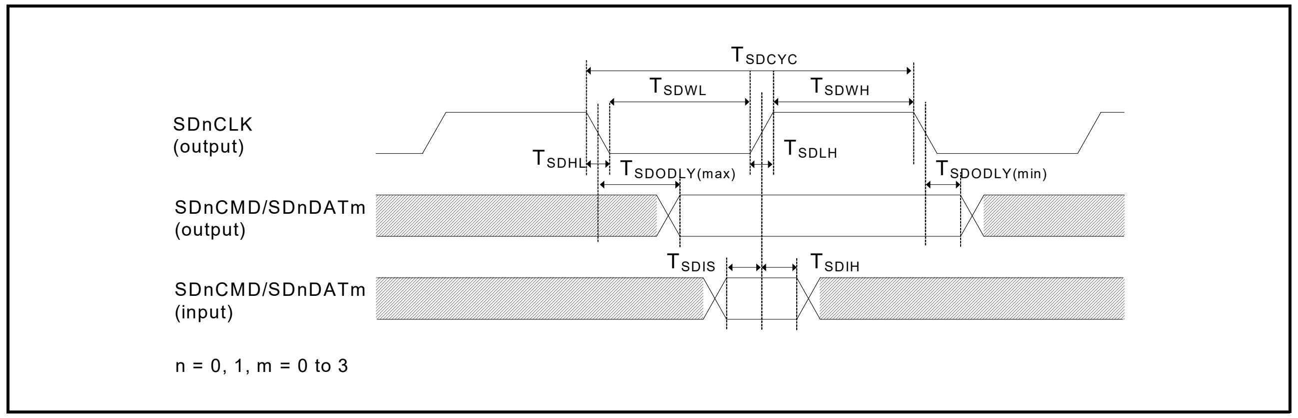


Figure 2.59 SDMMC主机接口信号时序

2.4 USB特性

2.4.1 USBFS Timing

Table 2.31 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.60
	上升时间	t_{LR}	75	-	300	ns	
	秋季时间	t_{LF}	75	-	300	ns	
	上升下降时间比	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
上拉和下拉特性	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

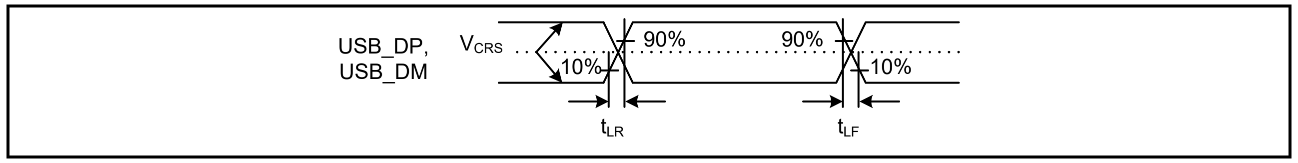


Figure 2.60 低速模式下的USB_DP和USB_DM输出时序

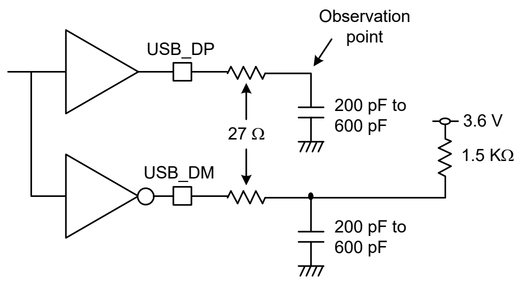


Figure 2.61 Test circuit in low-speed mode

Table 2.32 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.62
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

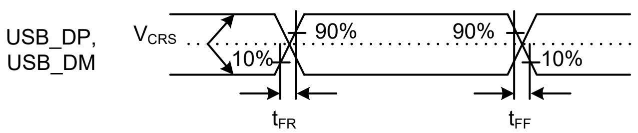


Figure 2.62 USB_DP and USB_DM output timing in full-speed mode

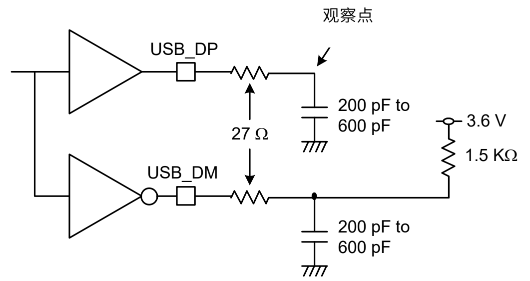


Figure 2.61 低速模式下的测试电路

Table 2.32 USBFS全速特性（USB_DP和USB_DM引脚特性）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.62
	上升时间	t_{LR}	4	-	20	ns	
	秋季时间	t_{LF}	4	-	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
上拉和下拉特性	设备控制器模式下的DM上拉电阻	R_{pu}	0.900	-	1.575	kΩ	空闲状态期间
			1.425	-	3.090	kΩ	在发送和接收期间
	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

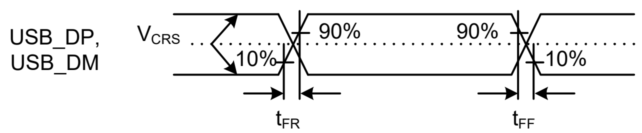


Figure 2.62 全速模式下的USB_DP和USB_DM输出时序

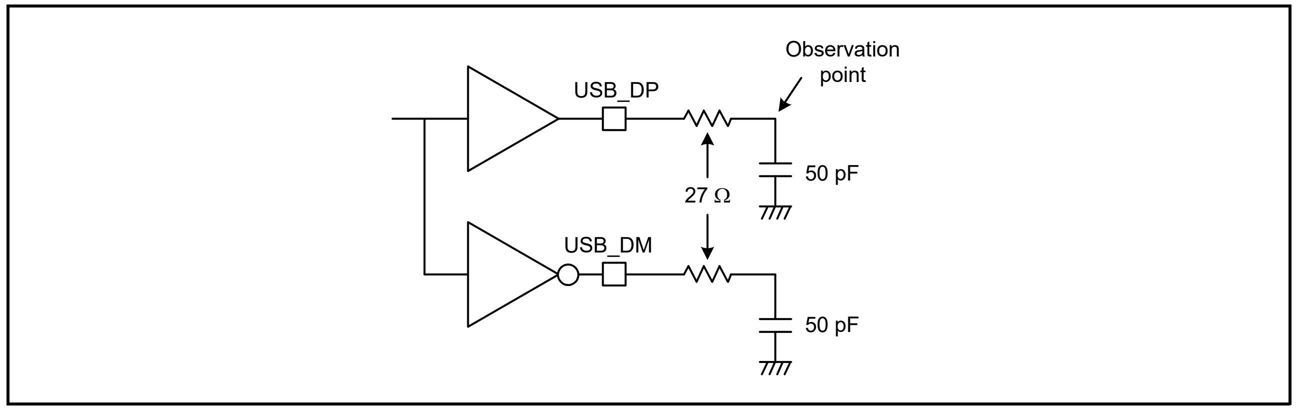


Figure 2.63 Test circuit in full-speed mode

2.5 ADC12 Characteristics

Table 2.33 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
	Dynamic range		0.25	-	VREFH0 - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN003, AN005, AN006)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-

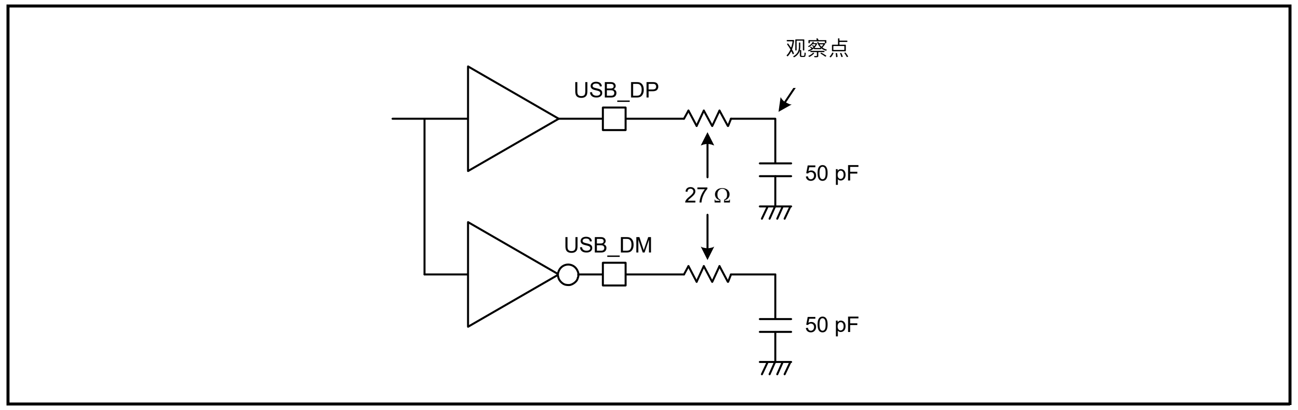


Figure 2.63 全速模式下的测试电路

2.5 ADC12 Characteristics

Table 2.33 单元0(1of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路*3（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	通道采样 24种状态的专用采样保持电路 15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	μs	-
	动态范围		0.25	-	VREFH0 - 0.25	V	-
未使用通道专用采样保持电路（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	μs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
High-precision channels (AN003, AN005, AN006)	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	μs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-

Table 2.33 A/D conversion characteristics for unit 0 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN003, AN005, AN006)	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.75 (0.533)*2	-	-	μs	Sampling in 32 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN018, AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 2.35.

Table 2.34 A/D conversion characteristics for unit 1 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-

Table 2.33 单元0(2of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
High-precision channels (AN003, AN005, AN006)	INL积分非线性误差		-	±1.0	±2.5	LSB	-
High-precision channels (AN007)	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.75 (0.533)*2	-	-	μs	在32个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
普通精度通道（AN016至AN018、AN020）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.88 (0.667)*2	-	-	μs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在AD转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

Note 2. 括号中的值表示采样时间。

Note 3. 在单元0和单元1中同时使用通道专用的采样保持电路时，请参见表2.35。

Table 2.34 单元1的AD转换特性（2个中的1个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路*3（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	通道采样 24种状态的专用采样保持电路15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	μs	-
	动态范围		0.25	-	VREFH - 0.25	V	-

Table 2.34 A/D conversion characteristics for unit 1 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN105, AN106)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.75 (0.533)*2	-	-	μs	Sampling in 32 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116, AN117)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.
Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 2.35.

Table 2.34 单元1的AD转换特性（2个中的2个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
未使用通道专用采样保持电路（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	μs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
High-precision channels (AN105, AN106)	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	μs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
High-precision channels (AN107)	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.75 (0.533)*2	-	-	μs	在32个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116, AN117)	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.88 (0.667)*2	-	-	μs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在AD转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。
Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。
Note 2. 括号中的值表示采样时间。
Note 3. 在单元0和单元1中同时使用通道专用的采样保持电路时，请参见表2.35。

Table 2.35 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit 0 and unit 1

Conditions: PCLKC = 30/60 MHz

Parameter		Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	• PCLKC = 60 MHz • Sampling in 15 states
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	• PCLKC = 30 MHz • Sampling in 7 states
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	+4.5/-6.5	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	+4.5/-6.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 2.36 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	μs	-

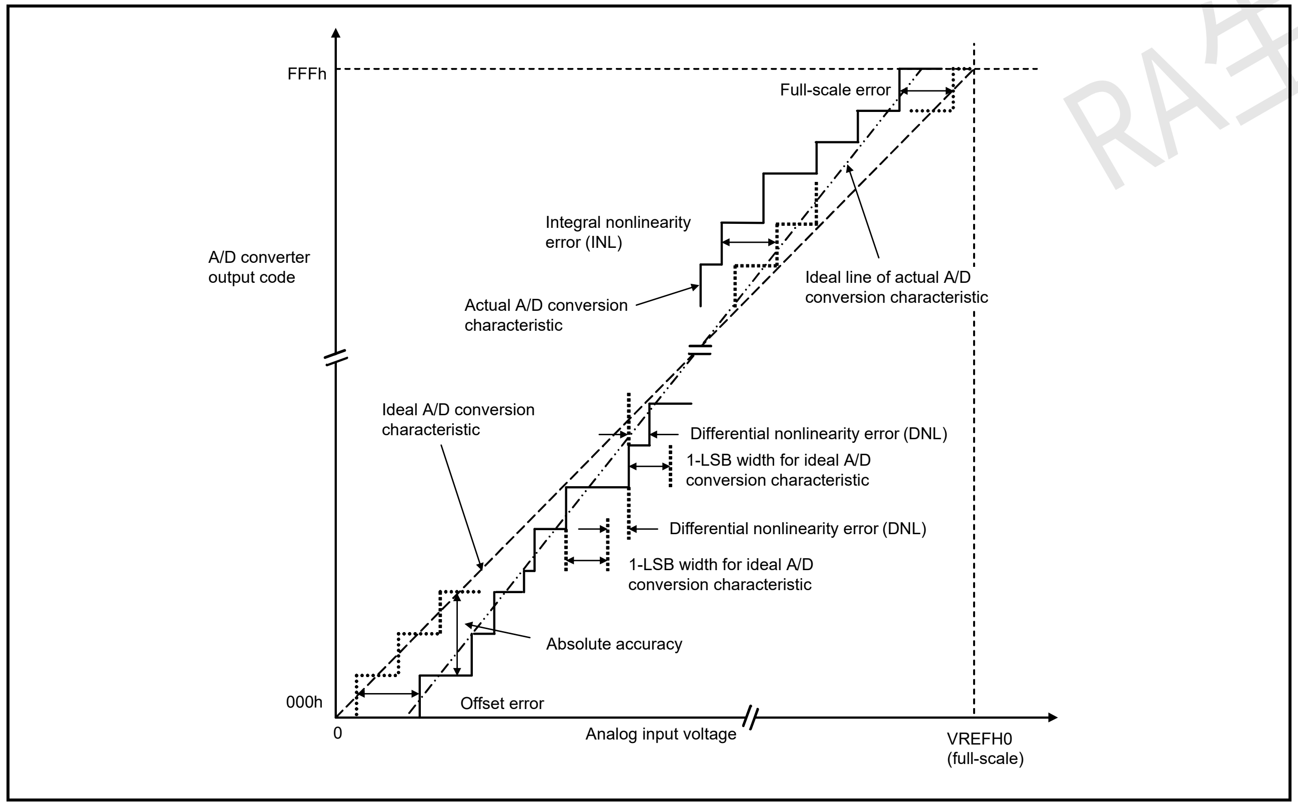


Figure 2.64 Illustration of ADC12 characteristic terms

表2.35在单元0和单元1中同时使用通道专用采样保持电路的AD转换特性条件：PCLKC=3060MHz

Parameter		Min	Typ	Max	测试条件
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±5.0	PCLKC=60MHz 15种状态采样
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±3.5	PCLKC=30MHz 7种状态采样
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	+4.5/-6.5	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	+4.5/-6.5	

Note: 在单元0和单元1中同时使用通道专用采样保持电路时，建议将ADSHMSR.SHMD位设置为1。

Table 2.36 AD内部参考电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部参考电压	1.13	1.18	1.23	V	-
采样时间	4.15	-	-	μs	-

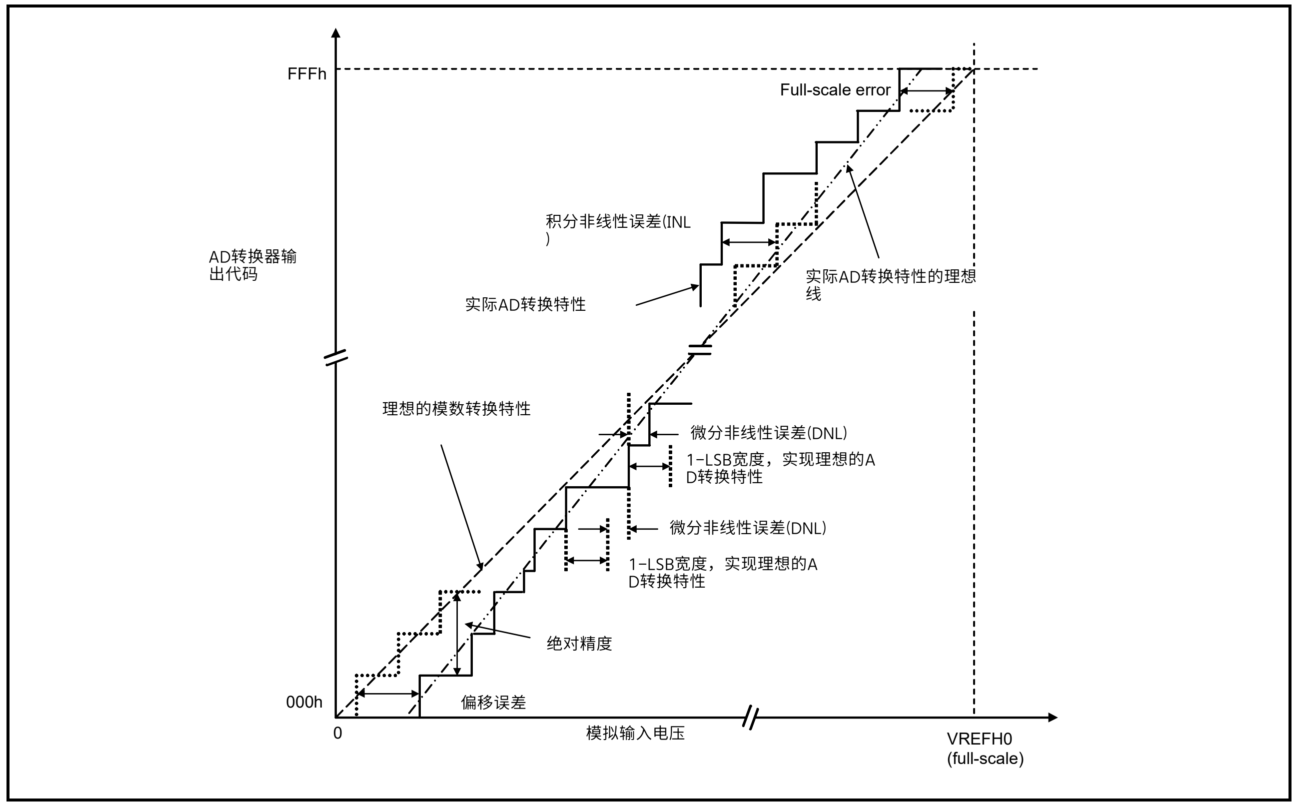


Figure 2.64 ADC12特征项说明

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 is 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.37 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	μs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	μs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH - 0.2	V	-

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压在理论上可以满足输出等码的期望。.例如，如果使用12位分辨率且参考电压VREFH0为3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在003h到00Dh的范围内，尽管从理论上的AD转换特性可以预期输出码为008h。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

2.6 DAC12 Characteristics

Table 2.37 DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	12	Bits	-
无输出放大器					
绝对精度	-	-	±24	LSB	阻性负载2MΩ
INL	-	±2.0	±8.0	LSB	阻性负载2MΩ
DNL	-	±1.0	±2.0	LSB	-
输出阻抗	-	8.5	-	kΩ	-
转换时间	-	-	3.0	μs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	-	VREFH	V	-
带输出放大器					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
转换时间	-	-	4.0	μs	-
阻性负载	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
输出电压范围	0.2	-	VREFH - 0.2	V	-

2.7 TSN Characteristics

Table 2.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.39 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.65

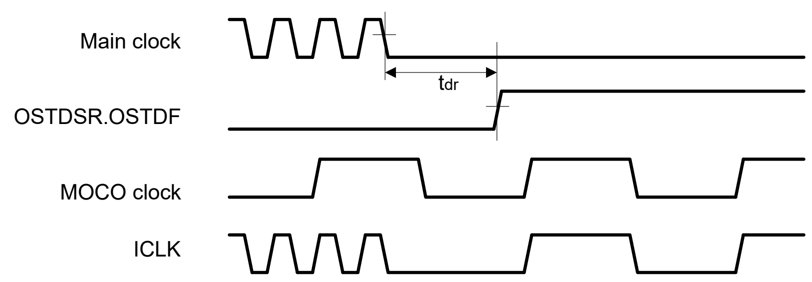


Figure 2.65 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 2.66
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.67
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.68
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.69
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		

2.7 TSN Characteristics

Table 2.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	-	-	±1.0	-	°C	-
温度斜率	-	-	4.0	-	mV/°C	-
输出电压（25°C时）	-	-	1.24	-	V	-
温度传感器启动时间	t_{START}	-	-	30	µs	-
采样时间	-	4.15	-	-	µs	-

2.8 OSC停止检测特性

Table 2.39 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	-	-	1	ms	Figure 2.65

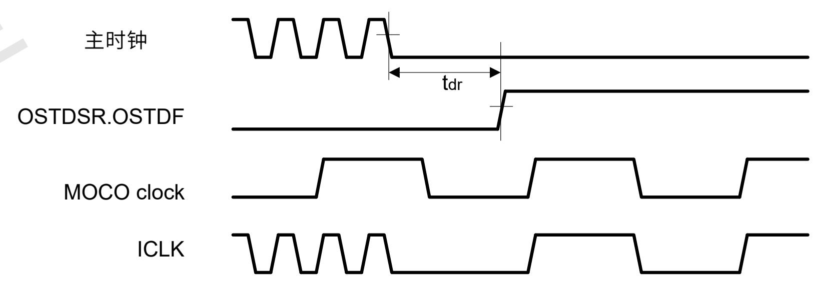


Figure 2.65 振荡停止检测时机

2.9 POR和LVD特性

Table 2.40 上电复位电路和电压检测电路特性（1of2）

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 2.66
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	电压检测电路（LVD0）		V_{det0_1}	2.84	2.94	3.04		Figure 2.67
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路（LVD1）		V_{det1_1}	2.89	2.99	3.09		Figure 2.68
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路（LVD2）		V_{det2_1}	2.89	2.99	3.09		Figure 2.69
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		

Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Internal reset time	Power-on reset time	t_{POR}	-	4.5	-	ms	Figure 2.66
	LVD0 reset time	t_{LVD0}	-	0.51	-		Figure 2.67
	LVD1 reset time	t_{LVD1}	-	0.38	-		Figure 2.68
	LVD2 reset time	t_{LVD2}	-	0.38	-		Figure 2.69
Minimum VCC down time*1		t_{VOFF}	200	-	-	μs	Figure 2.66, Figure 2.67
Response delay		t_{det}	-	-	200	μs	Figure 2.66 to Figure 2.69
LVD operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	-	-	10	μs	Figure 2.68, Figure 2.69
Hysteresis width (LVD1 and LVD2)		V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.

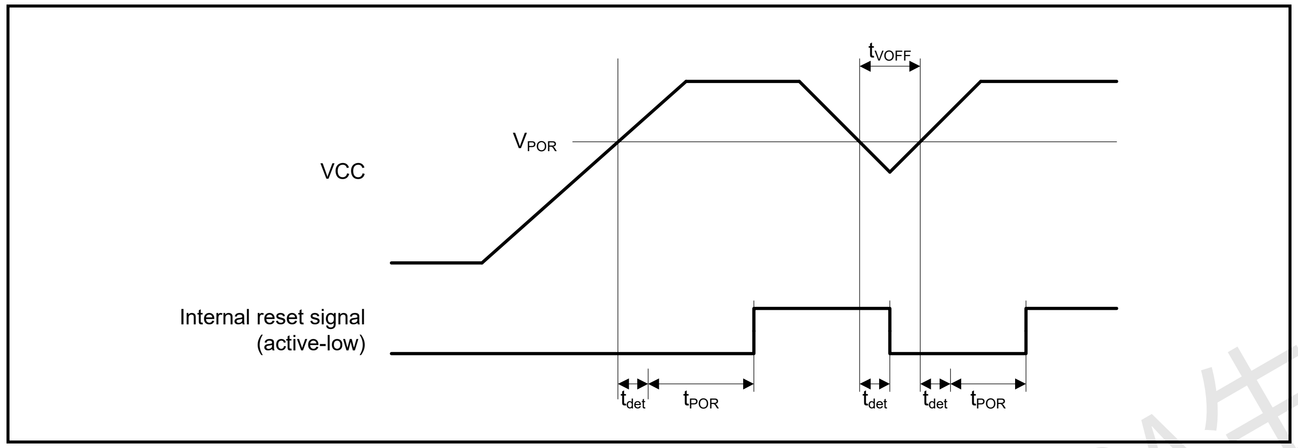


Figure 2.66 Power-on reset timing

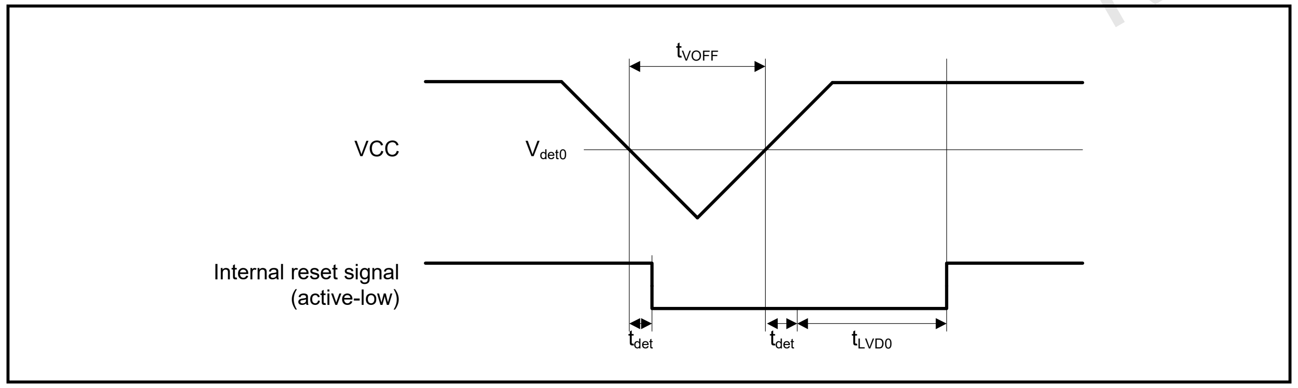


Figure 2.67 Voltage detection circuit timing (V_{det0})

Table 2.40 上电复位电路和电压检测电路特性(2of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
内部复位时间	上电复位时间	t_{POR}	-	4.5	-	ms	Figure 2.66
	LVD0复位时间	t_{LVD0}	-	0.51	-		Figure 2.67
	LVD1复位时间	t_{LVD1}	-	0.38	-		Figure 2.68
	LVD2复位时间	t_{LVD2}	-	0.38	-		Figure 2.69
最短VCC停机时间*1		t_{VOFF}	200	-	-	μs	Figure 2.66, Figure 2.67
响应延迟		t_{det}	-	-	200	μs	图2.66至 Figure 2.69
LVD操作稳定时间（启用LVD后）		$t_{d(E-A)}$	-	-	10	μs	Figure 2.68, Figure 2.69
迟滞宽度（LVD1和LVD2）		V_{LVH}	-	70	-	mV	

Note 1. 最小VCC停机时间表示VCC低于电压检测电平VPOR的最小值的时间，Vdet1和Vdet2用于POR和LVD。

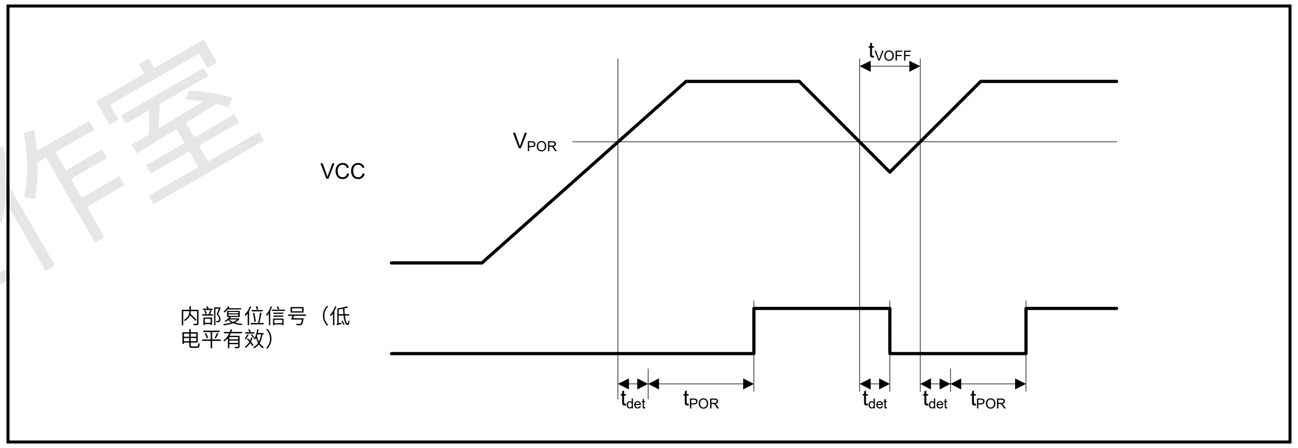


Figure 2.66 上电复位时序

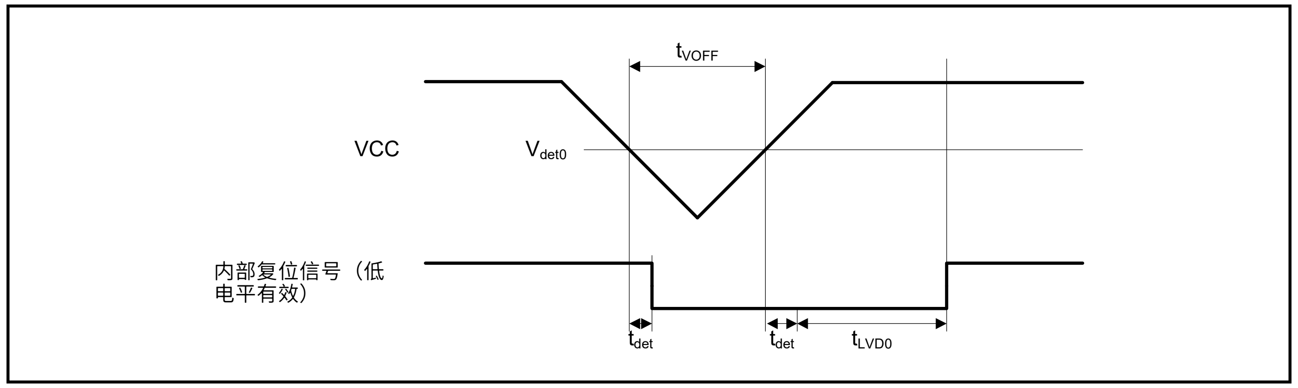


Figure 2.67 电压检测电路时序（Vdet0）

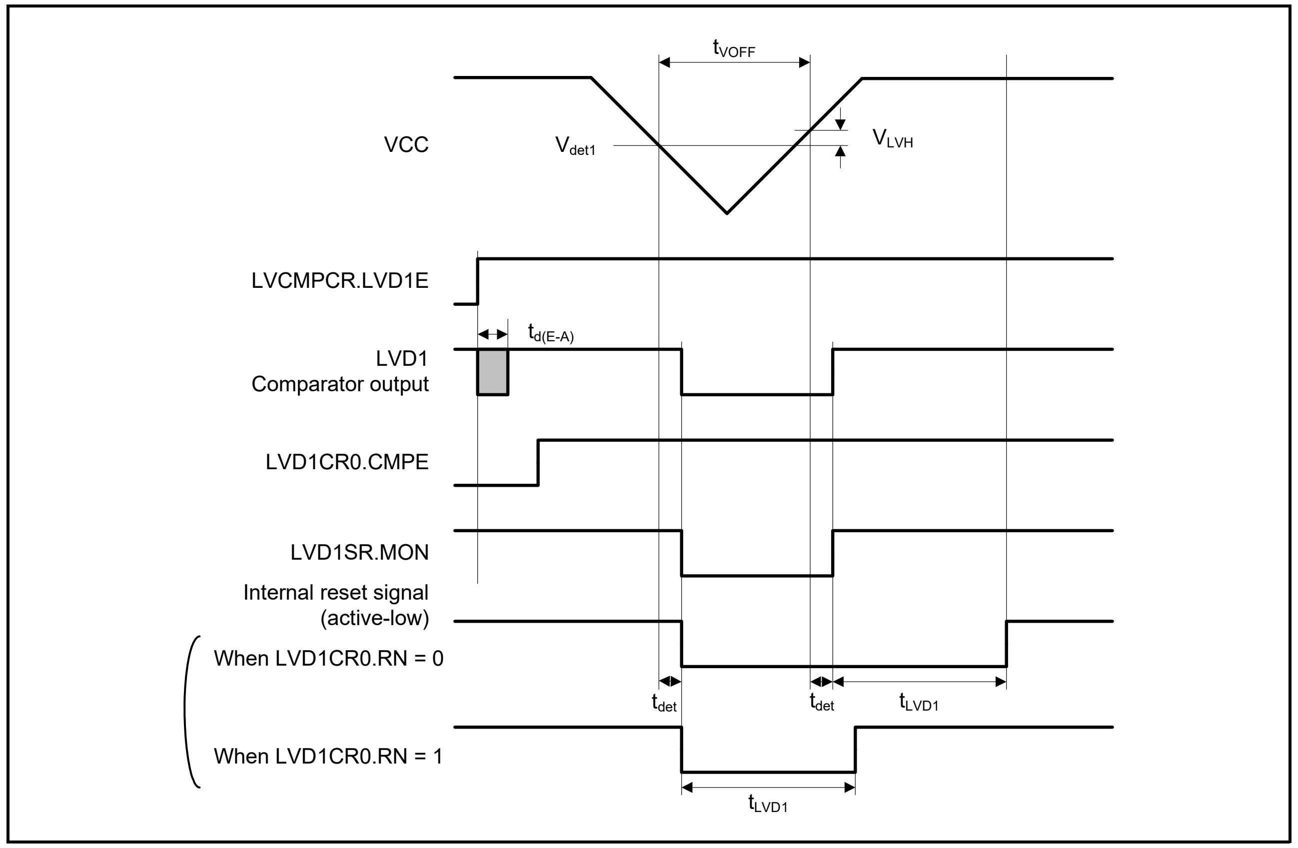


Figure 2.68 Voltage detection circuit timing (V_{det1})

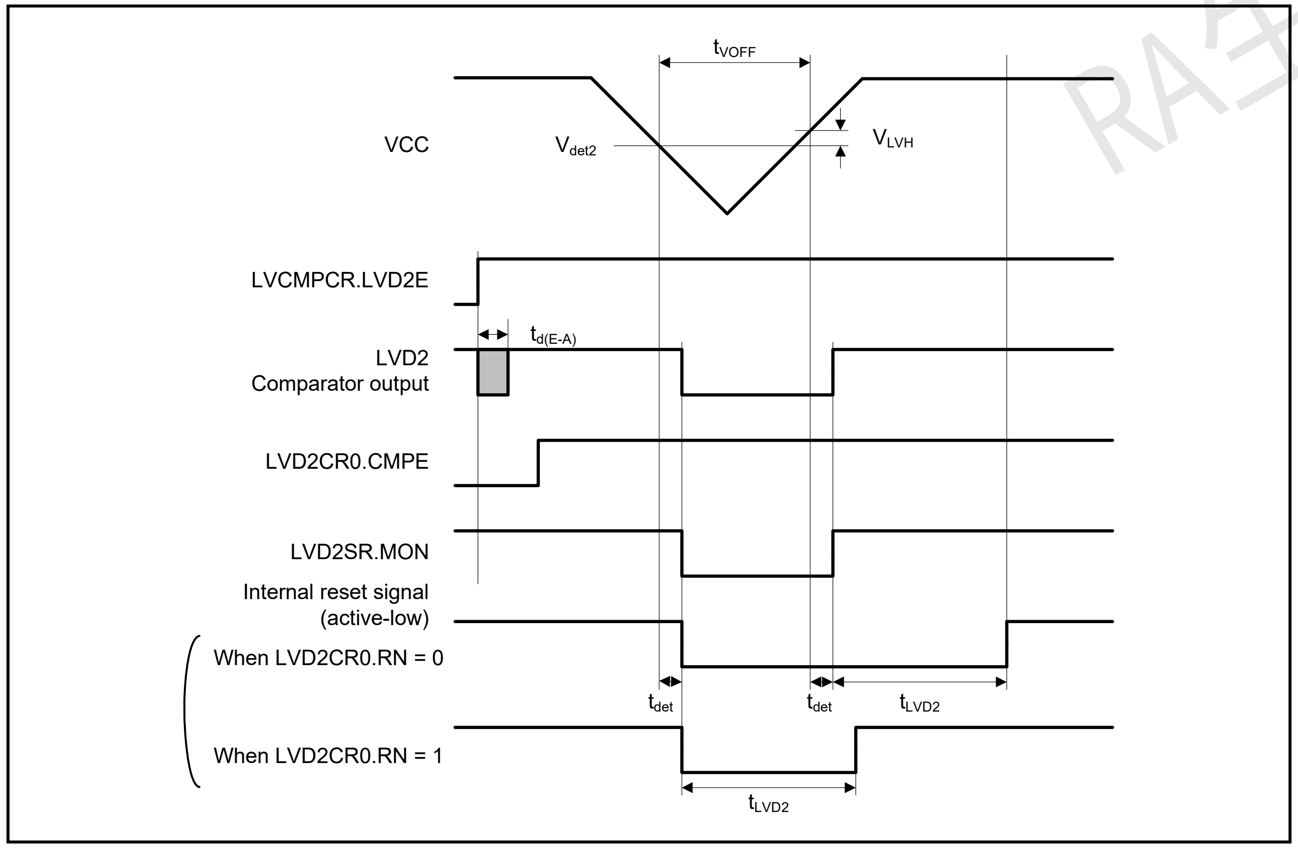


Figure 2.69 Voltage detection circuit timing (V_{det2})

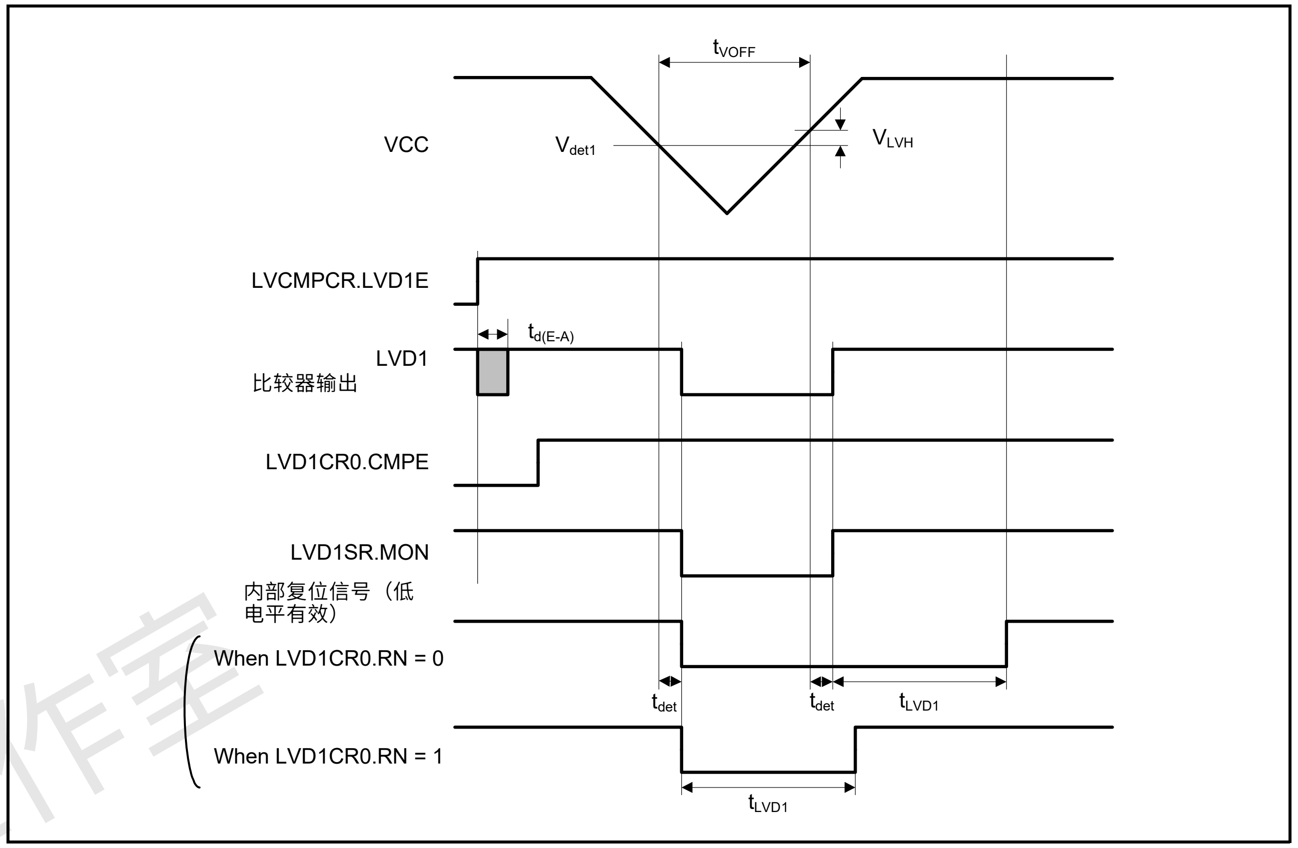


Figure 2.68 电压检测电路时序（Vdet1）

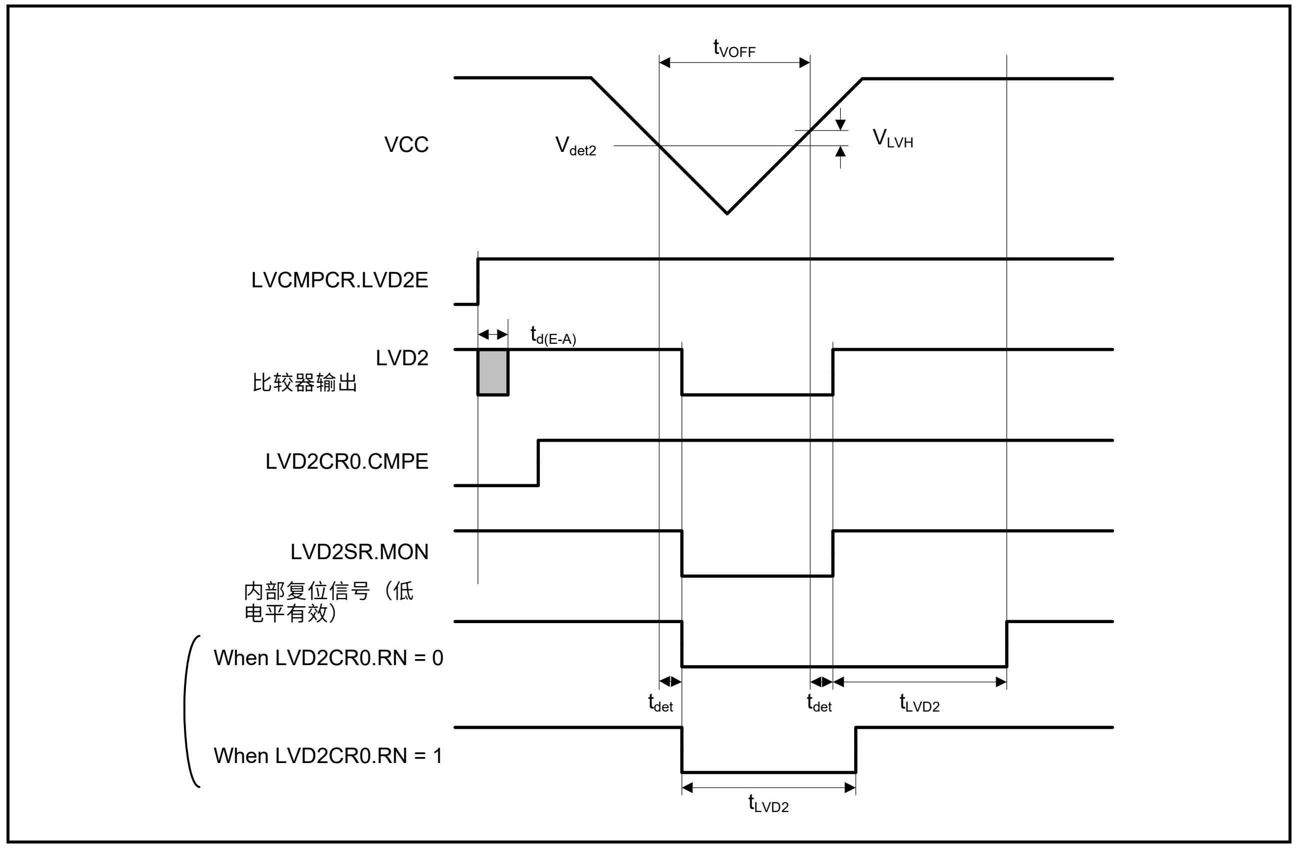


Figure 2.69 电压检测电路时序（Vdet2）

2.10 VBATT Characteristics

Table 2.41 Battery backup function characteristics
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.70
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	-	-	μs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

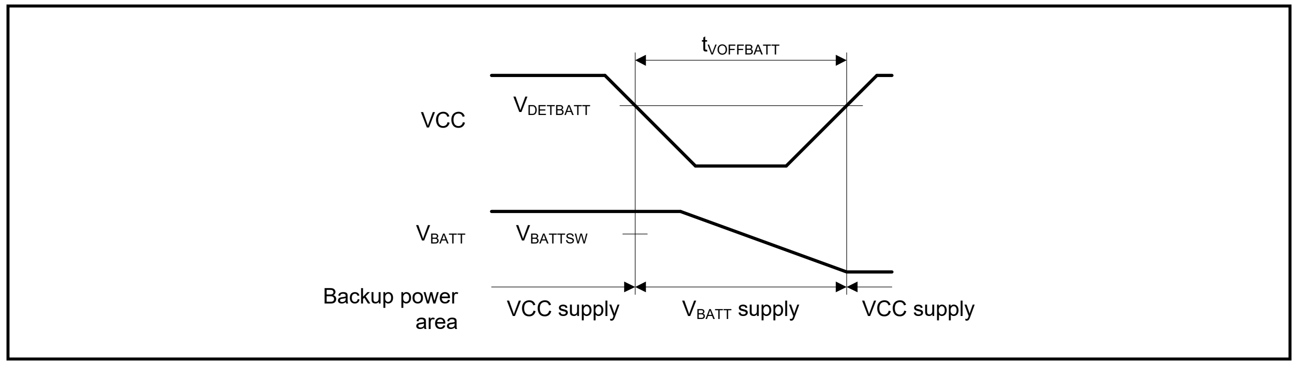


Figure 2.70 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.42 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{oH}	-	-	-40	mA	When the mutual capacitance method is applied

2.12 ACMPHS Characteristics

Table 2.43 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
Internal reference voltage	Vref	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

2.10 VBATT Characteristics

Table 2.41 电池备份功能特点
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
切换到备用电池的电压电平	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.70
VCC压降引起的电源切换下限VBATT电压	V_{BATTSW}	2.70	-	-	V	
启动电源切换的VCC-off周期	$t_{VOFFBATT}$	200	-	-	μs	

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值(VDETBATT)的周期。

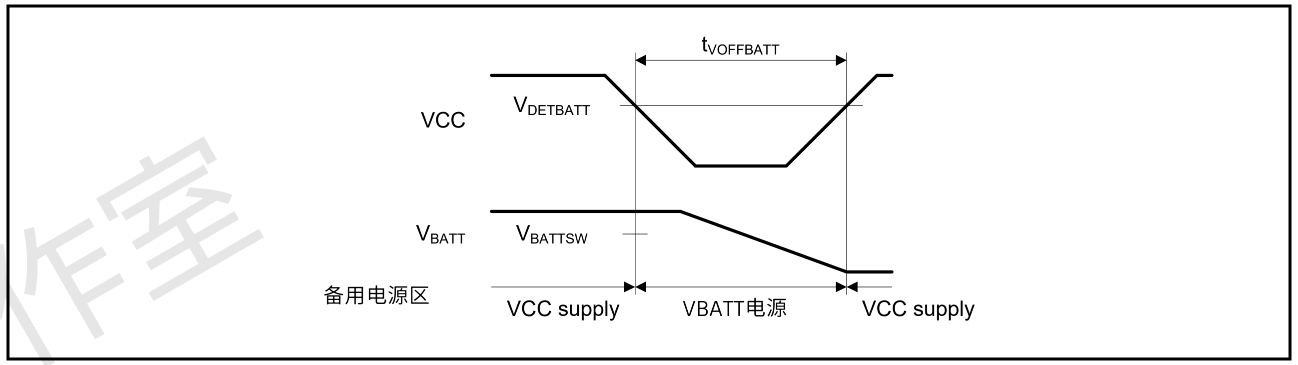


Figure 2.70 电池备份功能特点

2.11 CTSU Characteristics

Table 2.42 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	-
TS引脚容性负载	C_{base}	-	-	50	pF	-
允许输出大电流	ΣI_{oH}	-	-	-40	mA	应用互电容法时

2.12 ACMPHS Characteristics

Table 2.43 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
参考电压范围	VREF	0	-	AVCC0	V	-
输入电压范围	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
内部参考电压	Vref	1.13	1.18	1.23	V	-

Note 1. 该值是内部传播延迟。

2.13 PGA Characteristics

Table 2.44 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
Gain error	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
Offset error	Voff	-8	-	8	mV

Table 2.45 PGA characteristics in differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	-	0.3	V
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

2.13 PGA特性

Table 2.44 单模PGA特性

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
增益误差	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
偏移误差	Voff	-8	-	8	mV

Table 2.45 差模下的PGA特性(1of2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围		PGAVSS	-0.5	-	0.3	V
差分输入电压范围	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

Table 2.45 PGA characteristics in differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.46 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

			FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz				Test
Parameter		Symbol	Min	Typ	Max	Min	Typ	Max	Unit	conditions
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	μs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	μs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	μs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Table 2.45 差模下的PGA特性(2of2)

Parameter		Symbol	Min	Typ	Max	Unit
增益误差	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

2.14 闪存特性

2.14.1 代码闪存特性

Table 2.46 代码闪存特性
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

			FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz				测试条件
Parameter		Symbol	Min	Typ	Max	Min	Typ	Max	Unit	
编程时间NPEC 100次	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
编程时间NPEC>100次	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
擦除时间 NPEC 100次	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
编程期间暂停延迟		t_{SPD}	-	-	264	-	-	120	μs	
挂起优先模式下擦除期间的第一个挂起延迟		t_{SESD1}	-	-	216	-	-	120	μs	
挂起优先模式下擦除期间的第二挂起延迟		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
擦除优先模式下擦除期间的挂起延迟		t_{SEED}	-	-	1.7	-	-	1.7	ms	
强制停止命令		t_{FD}	-	-	32	-	-	20	μs	
数据保持时间*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note 1. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
Note 2. 这表示在指定范围内执行重新编程时特性的最小值。
Note 3. 这个结果是从可靠性测试中获得的。
Note 4. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=10000）时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

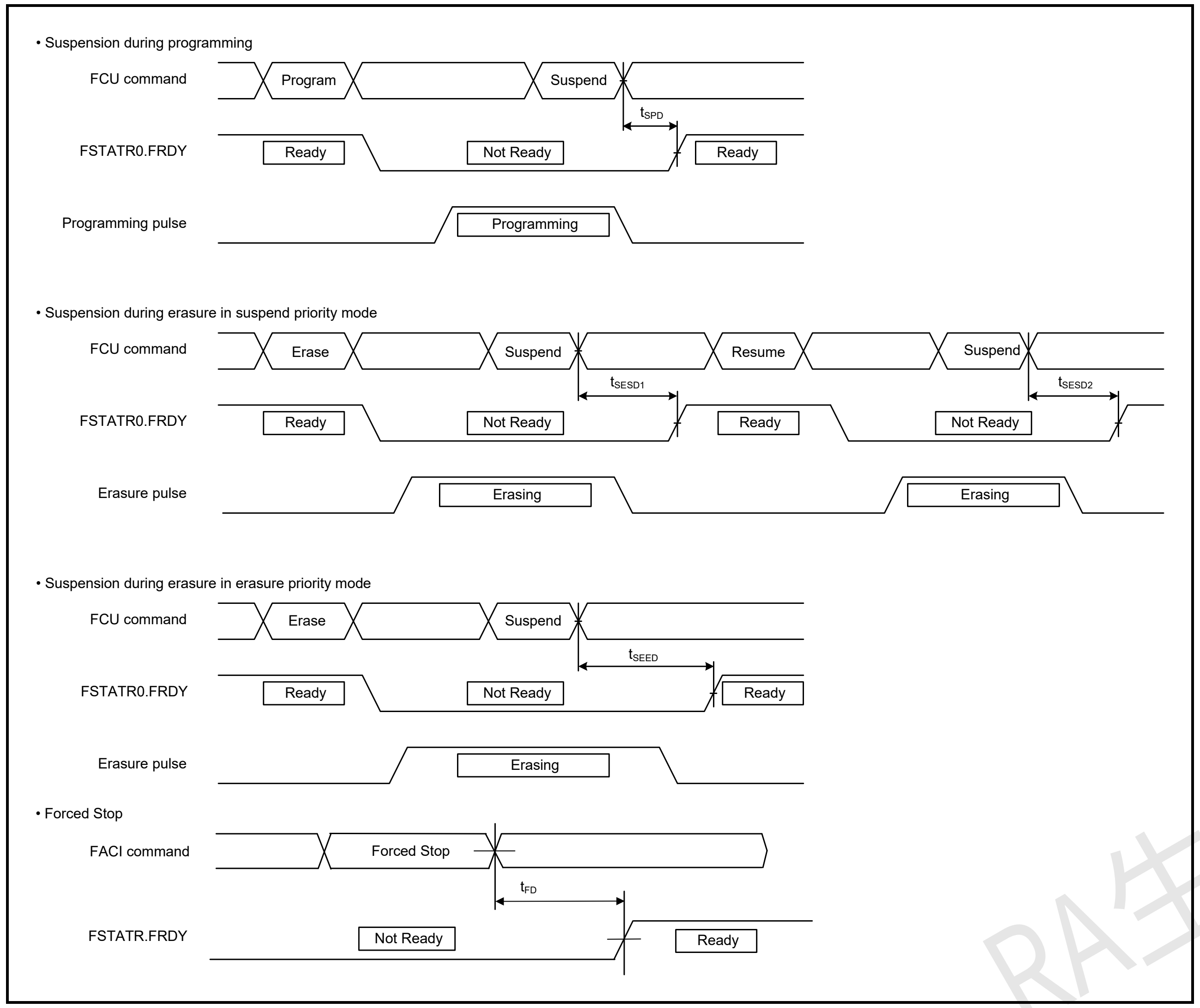


Figure 2.71 Suspension and forced stop timing for flash memory programming and erasure

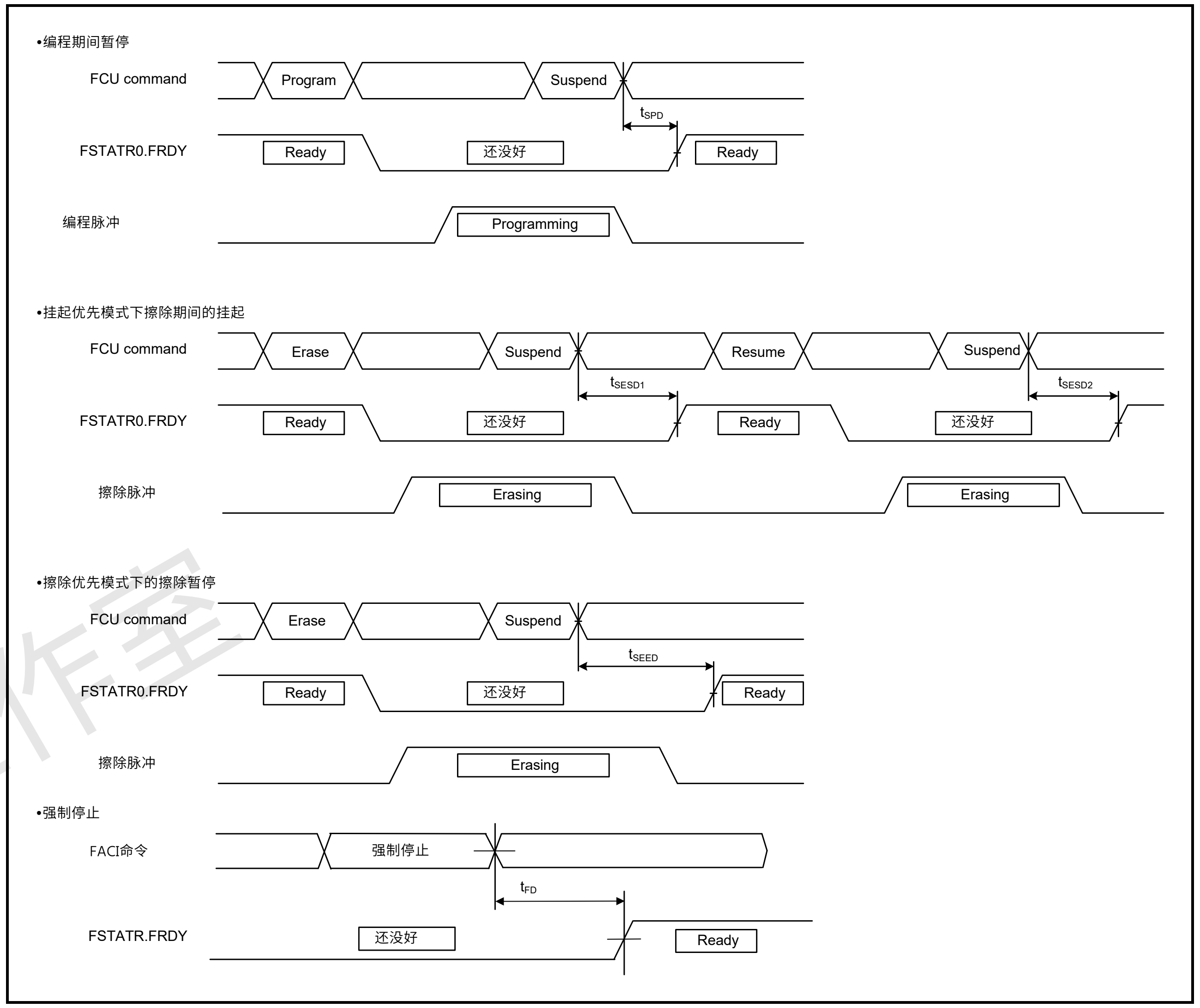


Figure 2.71 闪存编程和擦除的暂停和强制停止时序

2.14.2 Data Flash Memory Characteristics

Table 2.47 Data flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
Erasure time	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	μs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	-	-	125000*2	-	-	-	
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	μs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	μs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	μs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

2.15 Boundary Scan

Table 2.48 Boundary scan characteristics (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.72
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	

2.14.2 数据闪存特性

Table 2.47 数据闪存特性
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程时间	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
擦除时间	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
空白检查时间	4-byte	t_{DBC4}	-	-	84	-	-	30	μs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	-	-	125000*2	-	-	-	
编程期间暂停延迟	4-byte	t_{DSPD}	-	-	264	-	-	120	μs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
挂起优先模式下擦除期间的第一个挂起延迟	64-byte	t_{DSESD1}	-	-	216	-	-	120	μs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
挂起优先模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
强制停止命令		t_{FD}	-	-	32	-	-	20	μs	
数据保持时间*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125000）时，每个块可以执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

Note 2. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

Note 3. 这表示在指定范围内执行重新编程时特性的最小值。
Note 4. 这个结果是从可靠性测试中获得的。

2.15 边界扫描

Table 2.48 边界扫描特征(1of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	100	-	-	ns	Figure 2.72
TCK时钟高脉冲宽度	t_{TCKH}	45	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	45	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	

Table 2.48 Boundary scan characteristics (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.73
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.74

Note 1. Boundary scan does not function until the power-on reset becomes negative.

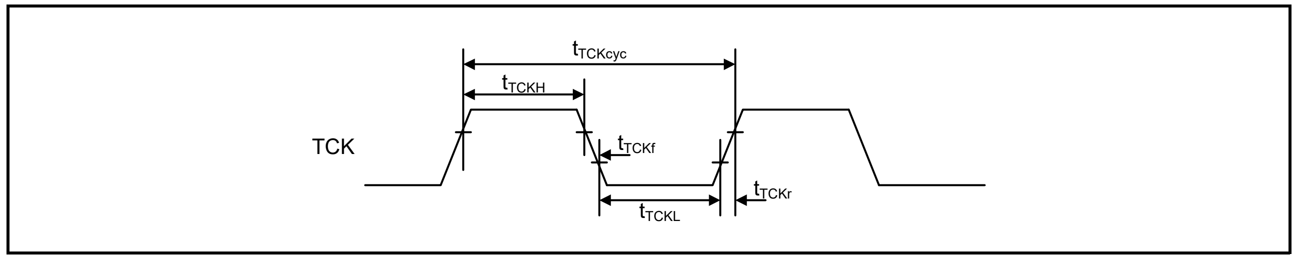


Figure 2.72 Boundary scan TCK timing

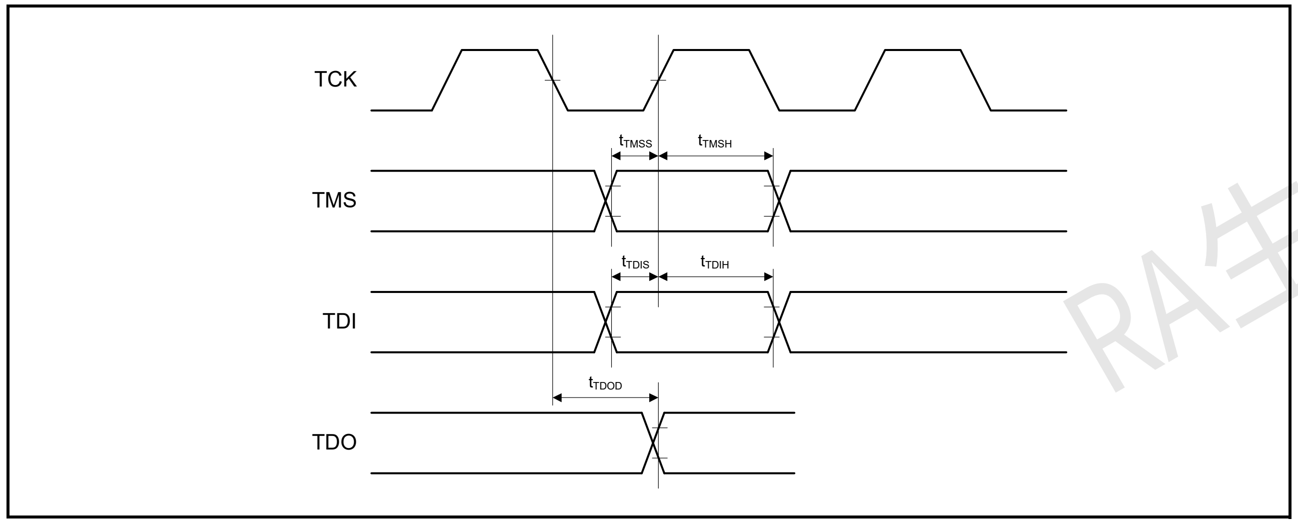


Figure 2.73 Boundary scan input/output timing

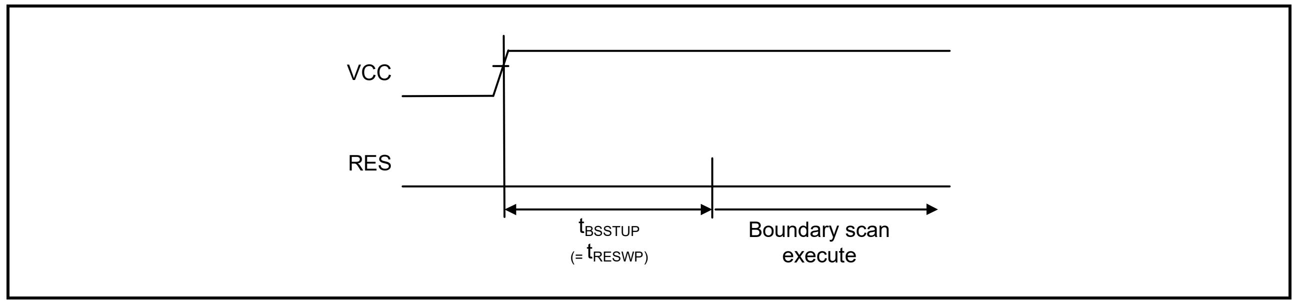


Figure 2.74 Boundary scan circuit startup timing

Table 2.48 边界扫描特征(2of2)

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TMS设置时间	t_{TMSS}	20	-	-	ns	Figure 2.73
TMS保持时间	t_{TMSH}	20	-	-	ns	
TDI建立时间	t_{TDIS}	20	-	-	ns	
TDI保持时间	t_{TDIH}	20	-	-	ns	
TDO数据延迟	t_{TDOD}	-	-	40	ns	
边界扫描电路启动时间*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.74

Note 1. 在上电复位变为负值之前，边界扫描不起作用。

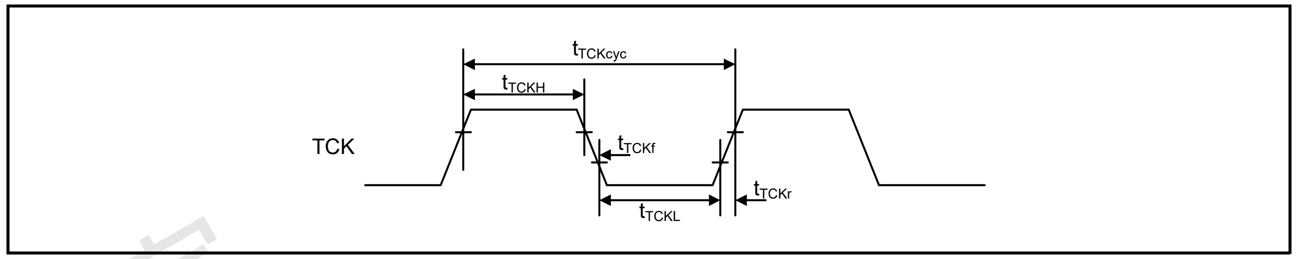


Figure 2.72 边界扫描TCK时序

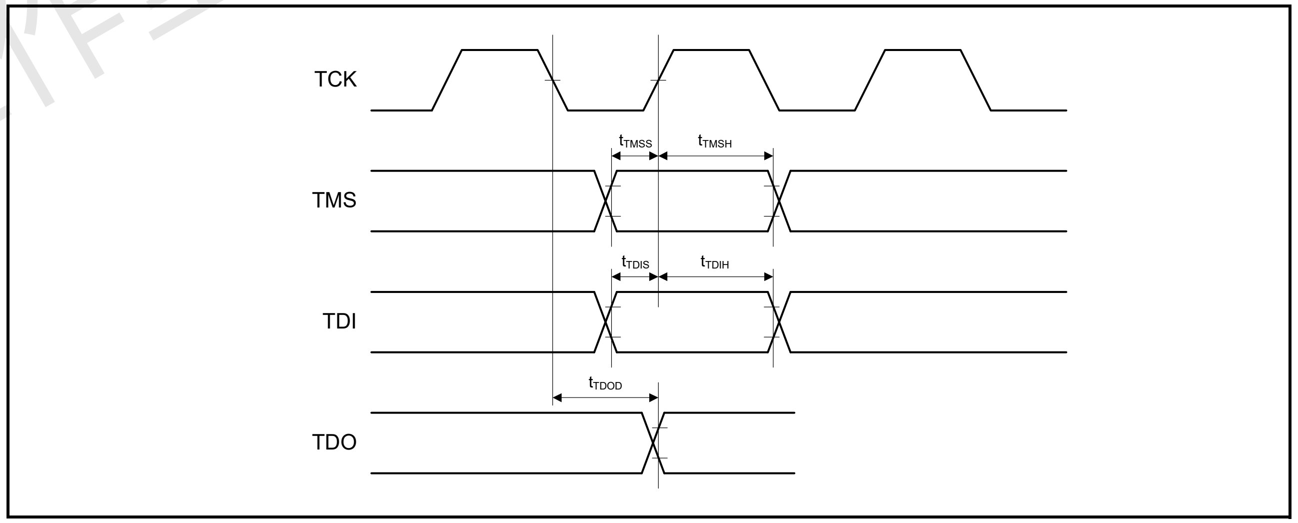


Figure 2.73 边界扫描输入输出时序

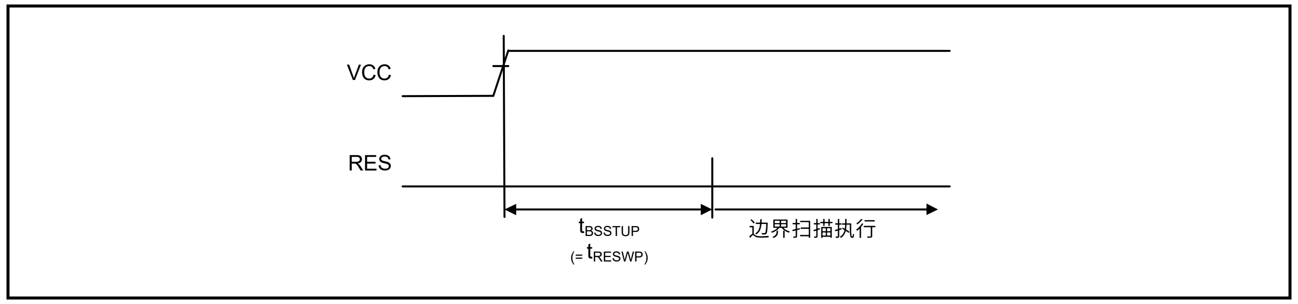


Figure 2.74 边界扫描电路启动时序

2.16 Joint Test Action Group (JTAG)

Table 2.49 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 2.72
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 2.73
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

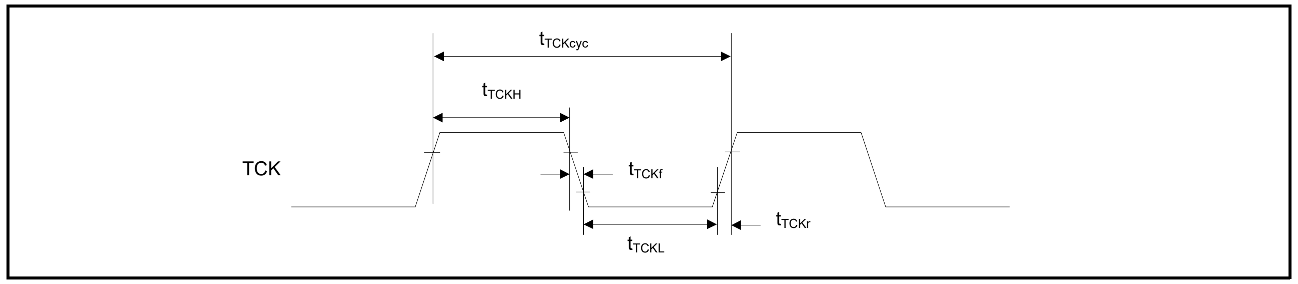


Figure 2.75 JTAG TCK timing

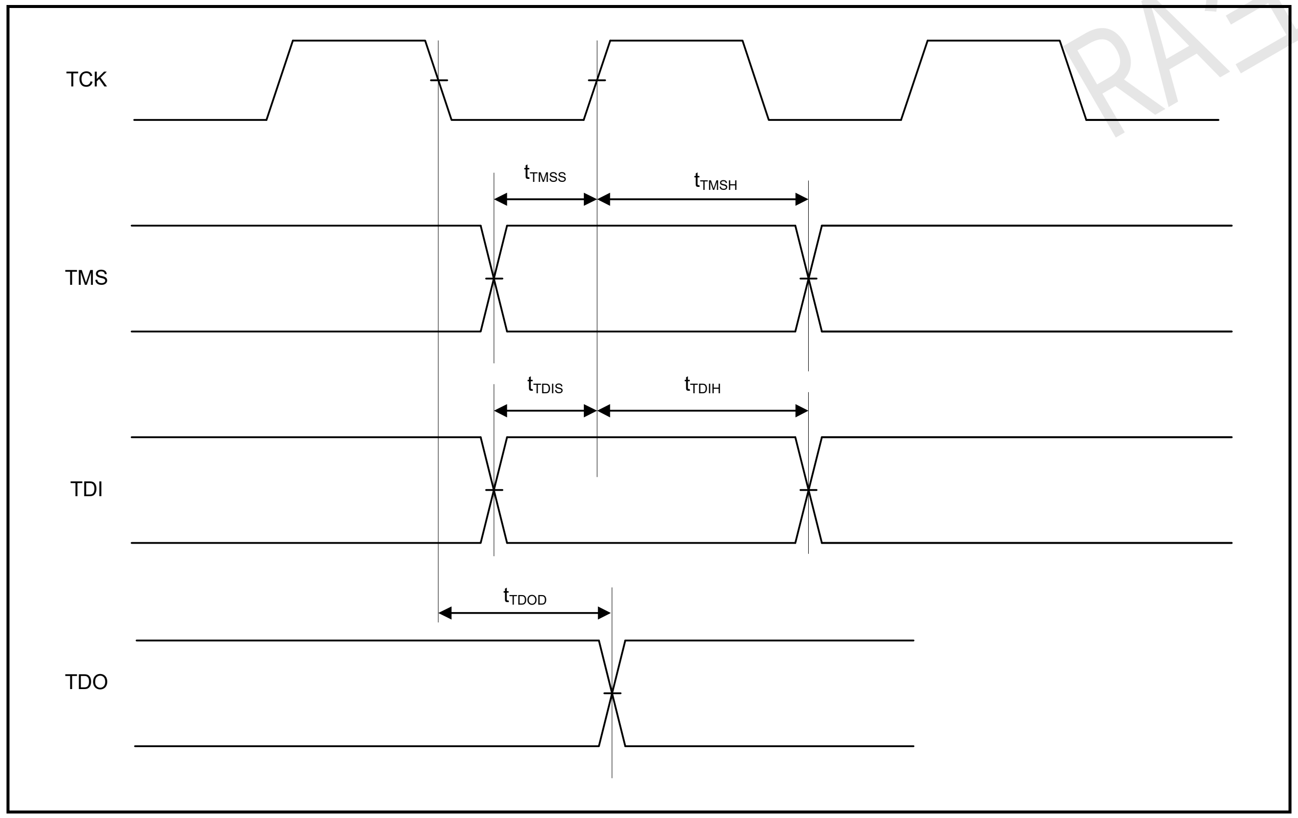


Figure 2.76 JTAG input/output timing

2.16 联合测试行动组(JTAG)

Table 2.49 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	40	-	-	ns	Figure 2.72
TCK时钟高脉冲宽度	t_{TCKH}	15	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	15	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	
TMS设置时间	t_{TMSS}	8	-	-	ns	Figure 2.73
TMS保持时间	t_{TMSH}	8	-	-	ns	
TDI建立时间	t_{TDIS}	8	-	-	ns	
TDI保持时间	t_{TDIH}	8	-	-	ns	
TDO数据延迟时间	t_{TDOD}	-	-	20	ns	

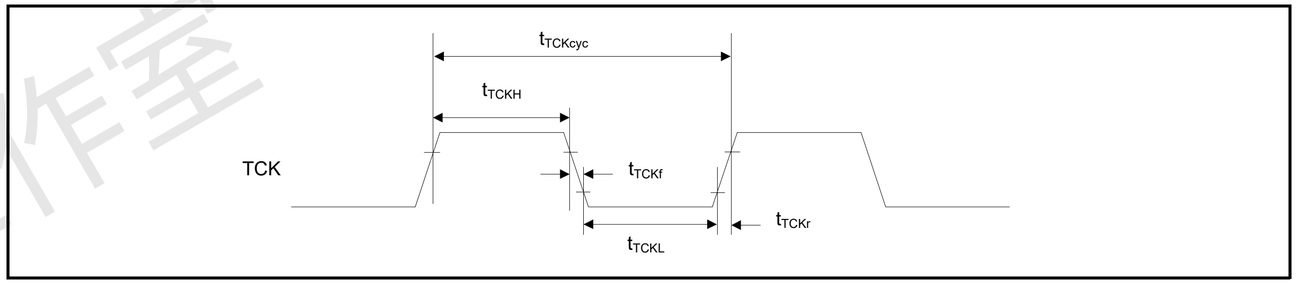


Figure 2.75 JTAG TCK timing

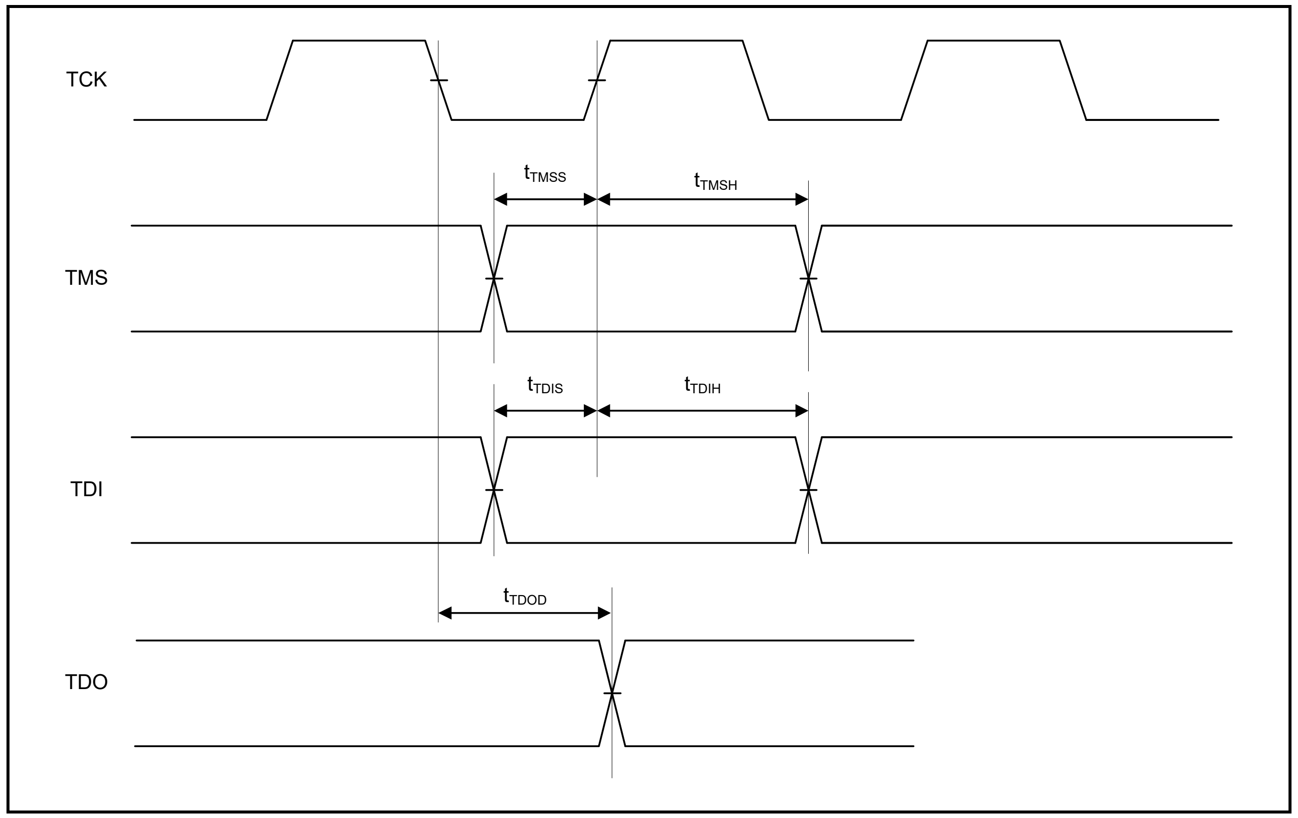


Figure 2.76 JTAG input/output timing

2.17 Serial Wire Debug (SWD)

Table 2.50 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.77
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.78
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

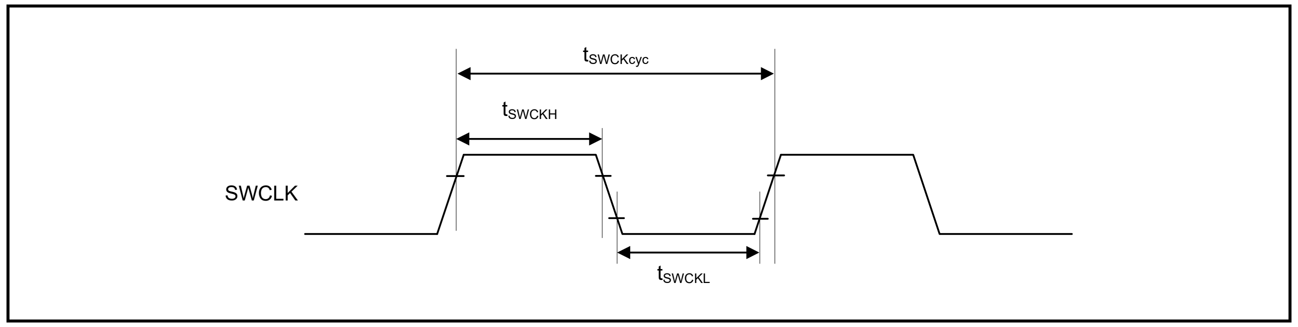


Figure 2.77 SWD SWCLK timing

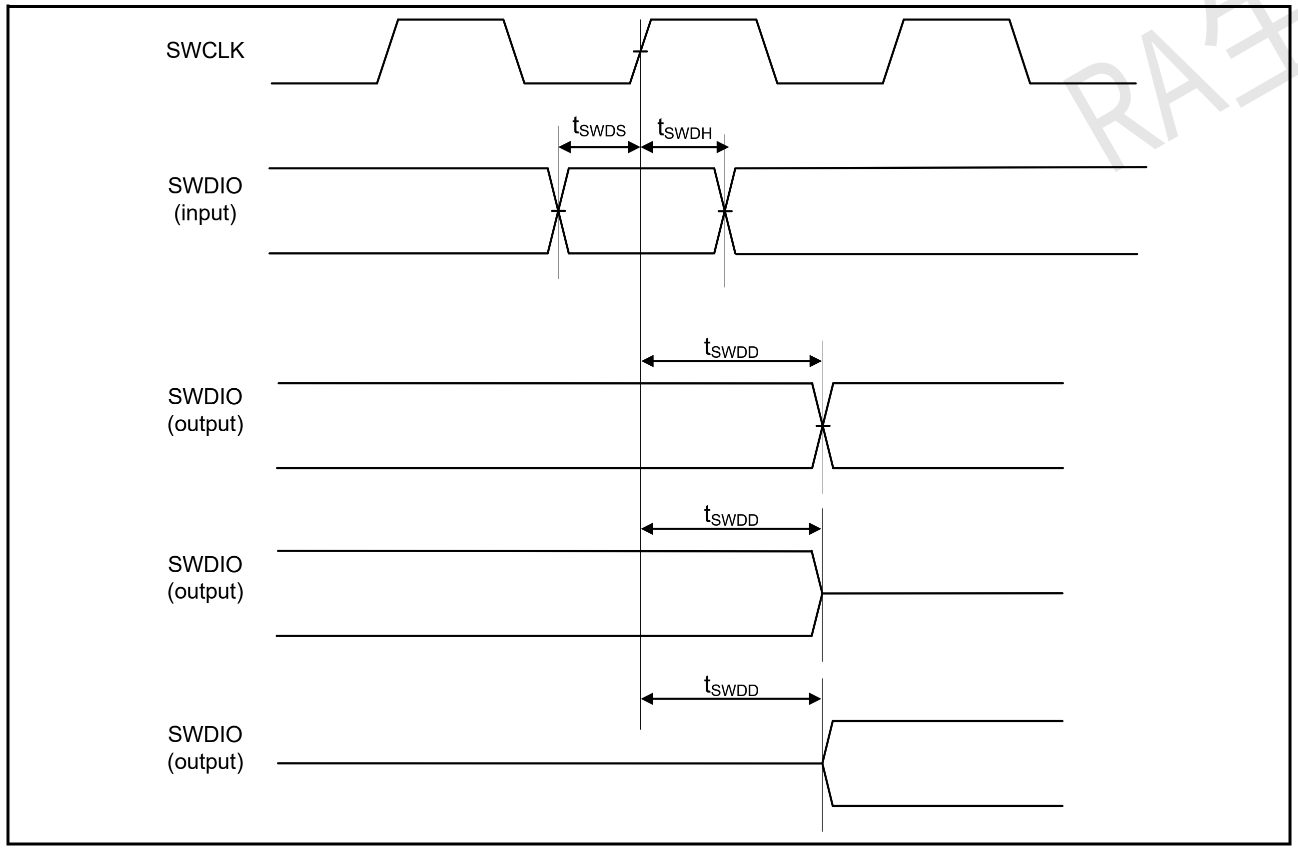


Figure 2.78 SWD input/output timing

2.17 串行线调试(SWD)

Table 2.50 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.77
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	-	-	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	-	-	ns	
SWCLK时钟上升时间	t_{SWCKr}	-	-	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	-	-	5	ns	
SWDIO设置时间	t_{SWDS}	8	-	-	ns	Figure 2.78
SWDIO保持时间	t_{SWDH}	8	-	-	ns	
SWDIO数据延迟时间	t_{SWDD}	2	-	28	ns	

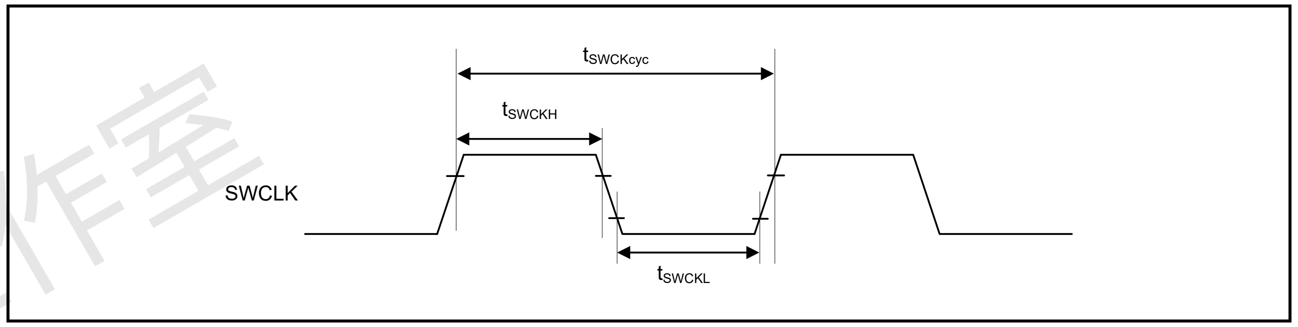


Figure 2.77 SWD SWCLK timing

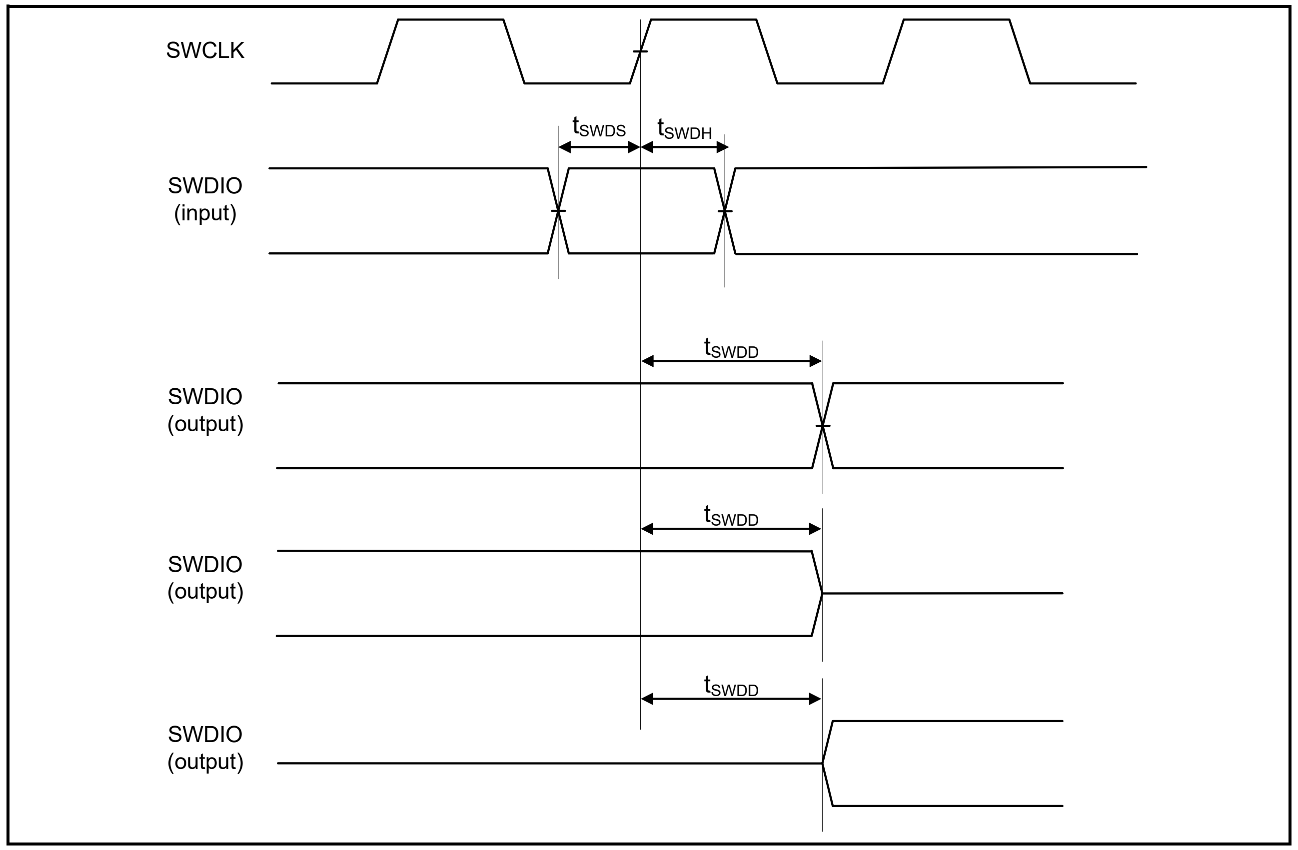


Figure 2.78 SWD input/output timing

2.18 Embedded Trace Macro Interface (ETM)

Table 2.51 ETM
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 2.79
TCLK clock high pulse width	t_{TCLKH}	13.6	-	-	ns	
TCLK clock low pulse width	t_{TCLKL}	13.6	-	-	ns	
TCLK clock rise time	t_{TCLKr}	-	-	3	ns	
TCLK clock fall time	t_{TCLKf}	-	-	3	ns	
TDATA[3:0] output setup time	t_{TRDS}	3.5	-	-	ns	Figure 2.80
TDATA[3:0] output hold time	t_{TRDH}	2.5	-	-	ns	

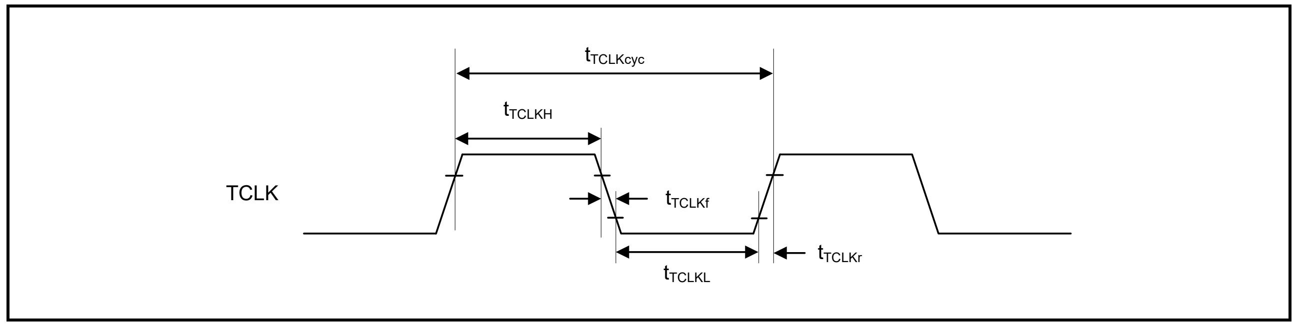


Figure 2.79 ETM TCLK timing

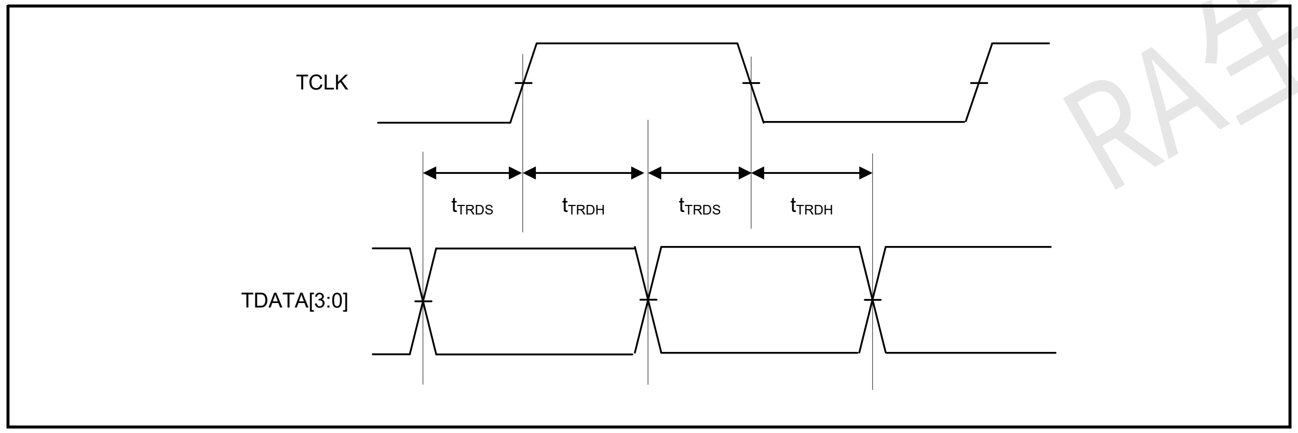


Figure 2.80 ETM output timing

2.18 嵌入式跟踪宏接口(ETM)

Table 2.51 ETM
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCLK时钟周期时间	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 2.79
TCLK时钟高脉冲宽度	t_{TCLKH}	13.6	-	-	ns	
TCLK时钟低脉冲宽度	t_{TCLKL}	13.6	-	-	ns	
TCLK时钟上升时间	t_{TCLKr}	-	-	3	ns	
TCLK时钟下降时间	t_{TCLKf}	-	-	3	ns	
TDATA[3:0]输出建立时间	t_{TRDS}	3.5	-	-	ns	Figure 2.80
TDATA[3:0]输出保持时间	t_{TRDH}	2.5	-	-	ns	

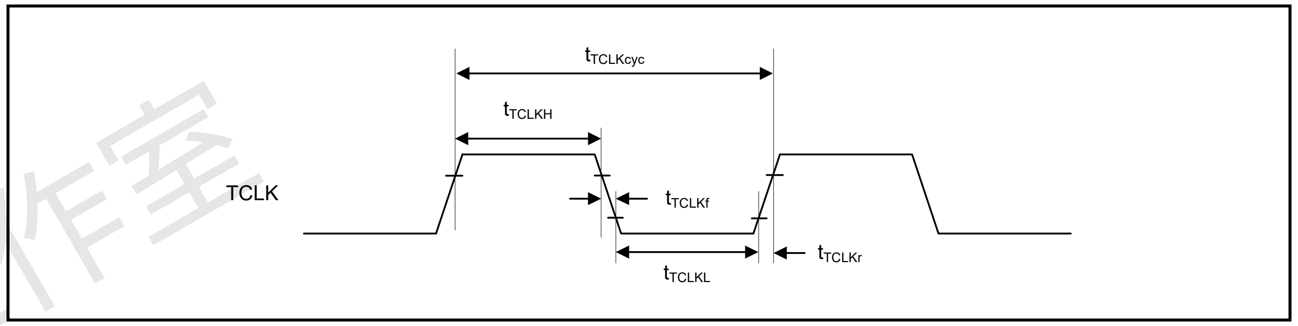


Figure 2.79 ETM TCLK timing

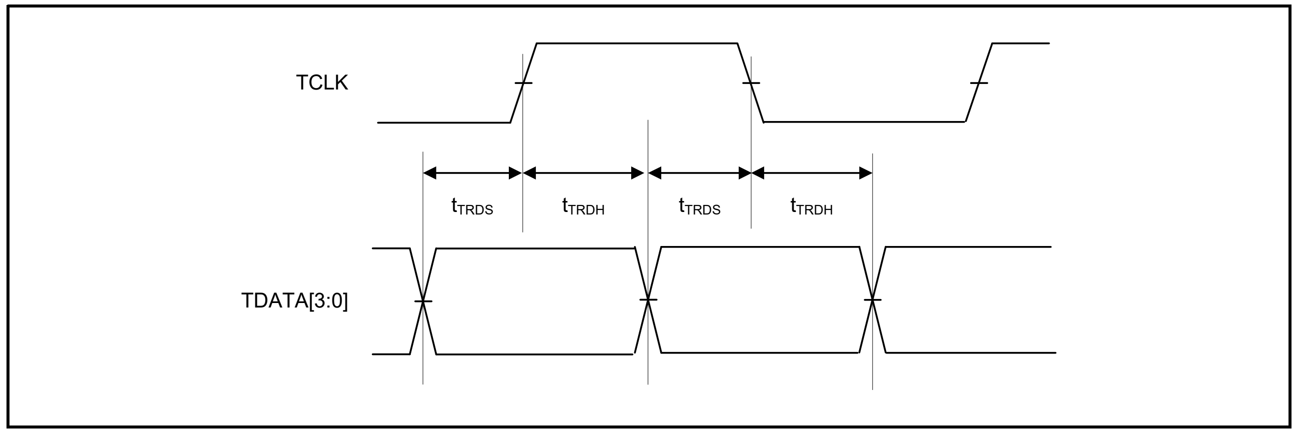
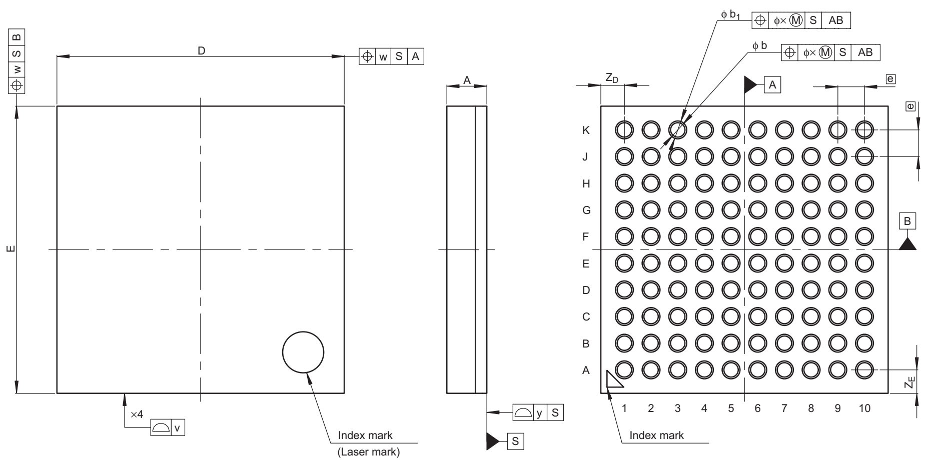


Figure 2.80 ETM输出时序

Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings is shown in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



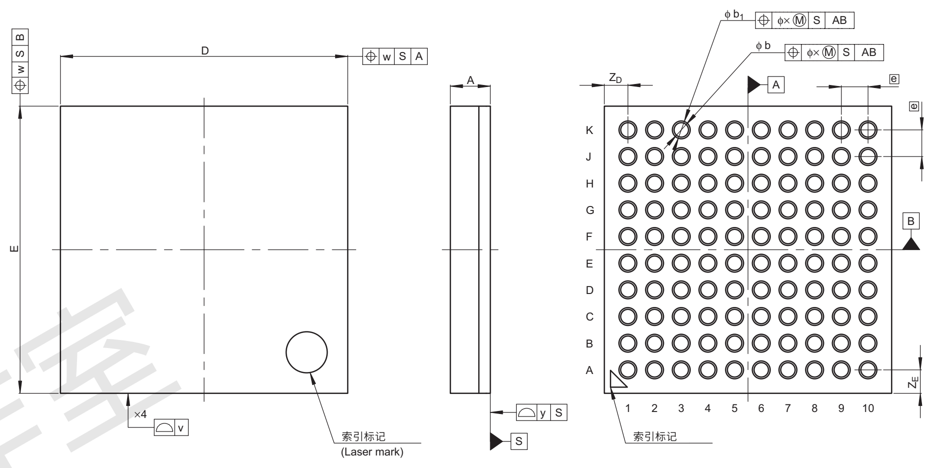
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure 1.1 100-pin LGA

附录1.包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨电子的“封装”中
电子公司网站。

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g

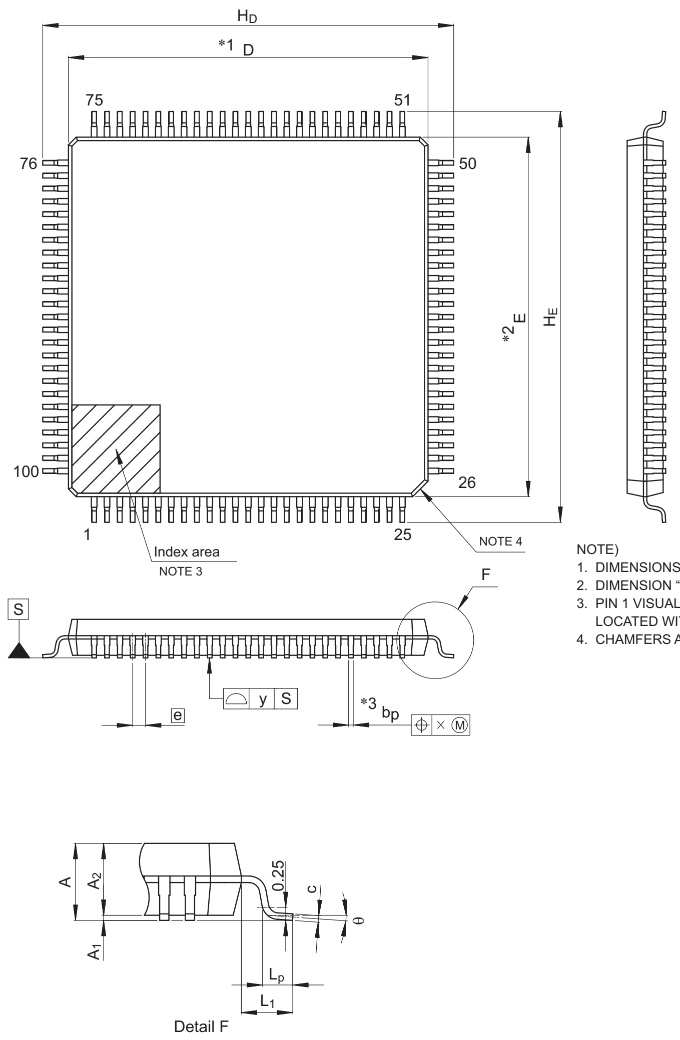


符号参考	以毫米为单位的尺寸		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure 1.1 100-pin LGA

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

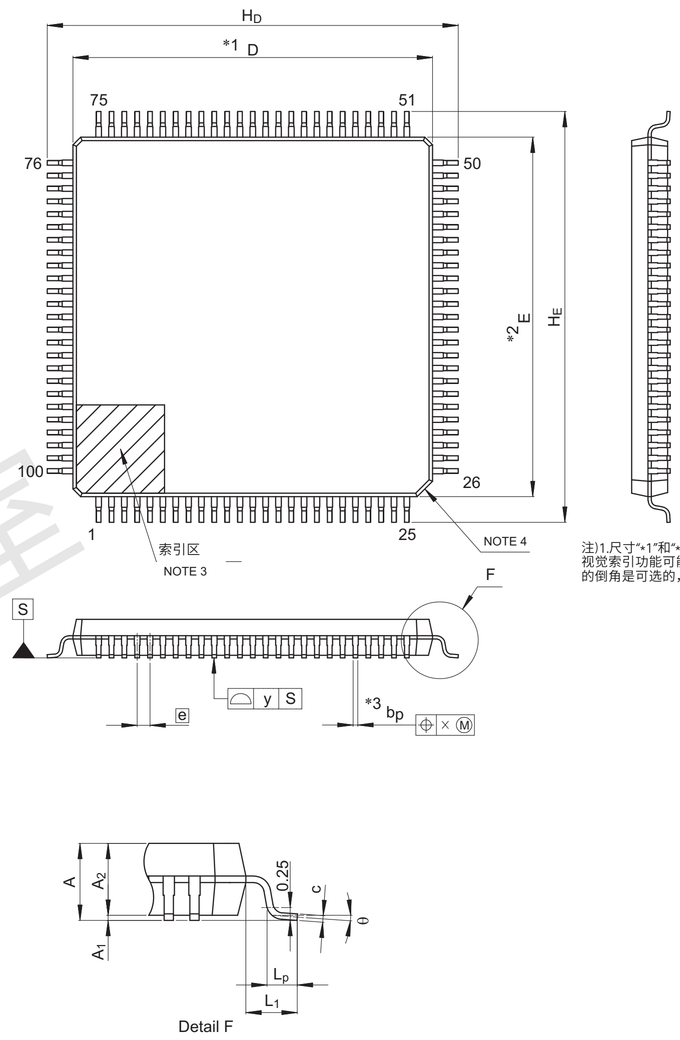
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.2 100-pin LQFP

RA6M1 Group 附录1.封装尺寸

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



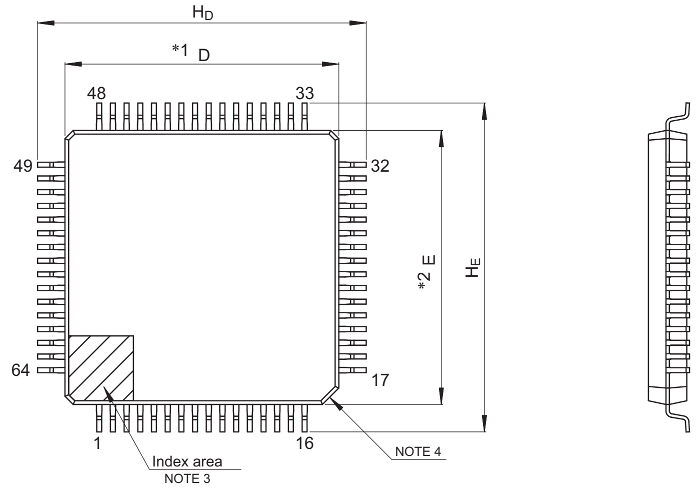
注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

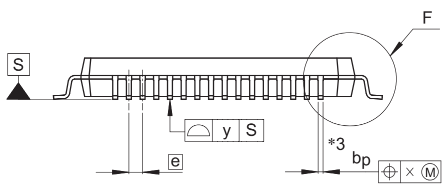
参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.2 100-pin LQFP

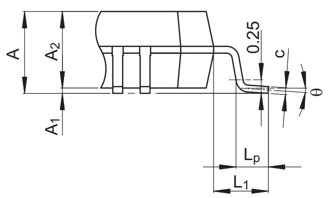
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



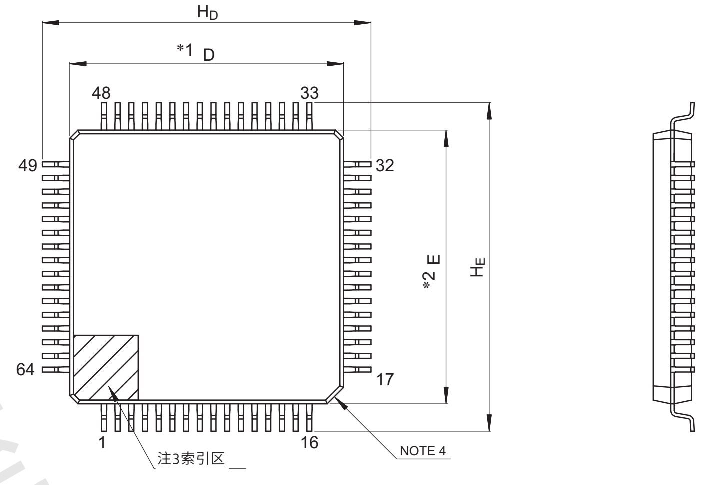
Detail F

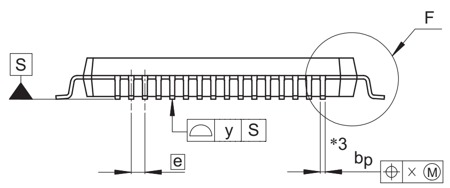
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.3 64-pin LQFP

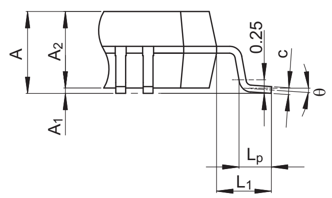
JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm





注1.尺寸“*1”和“*2”不包括毛边。2.尺寸“*3”不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

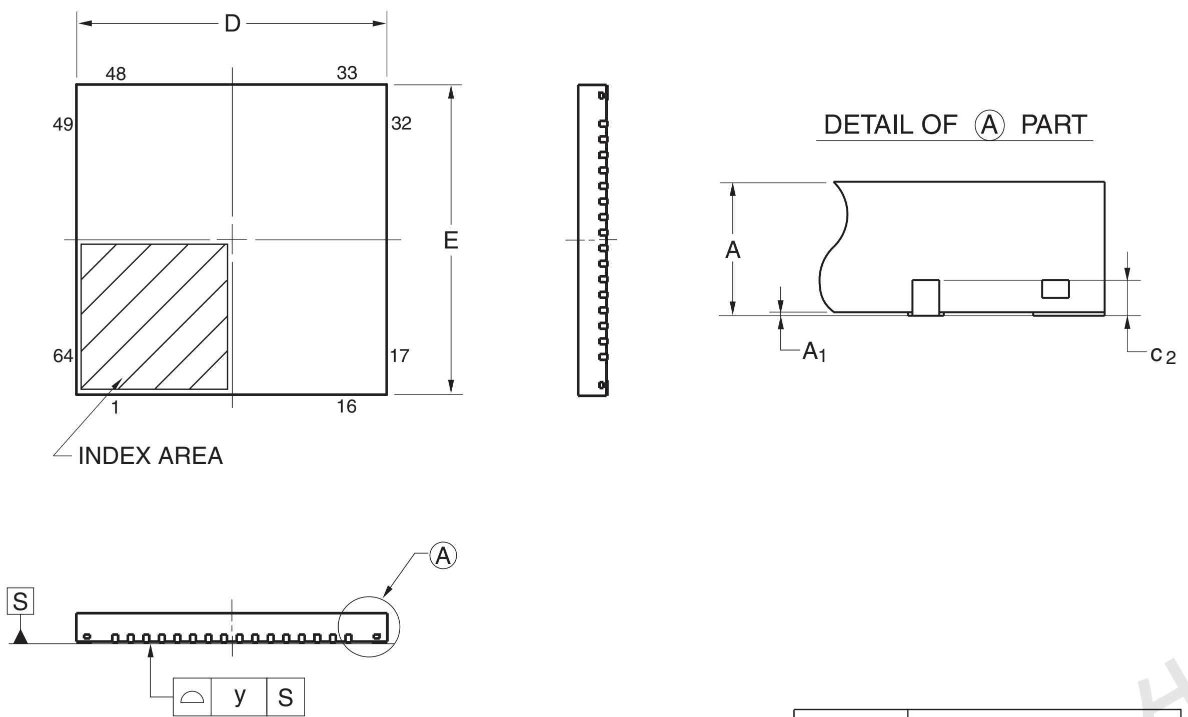


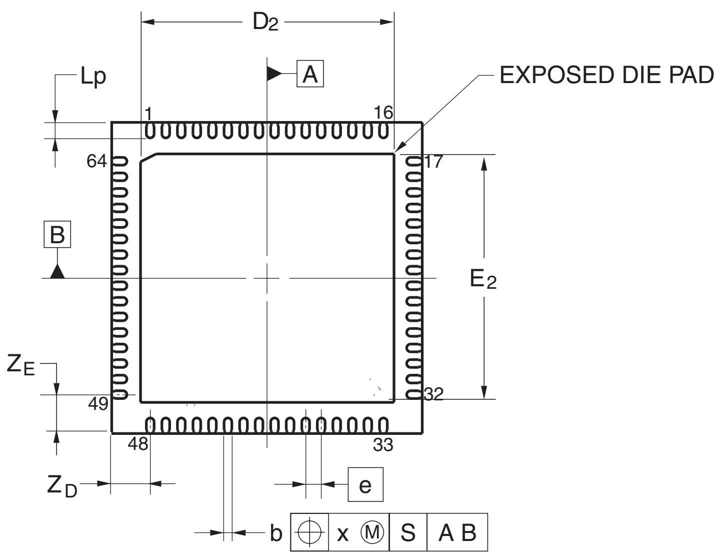
Detail F

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.3 64-pin LQFP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16

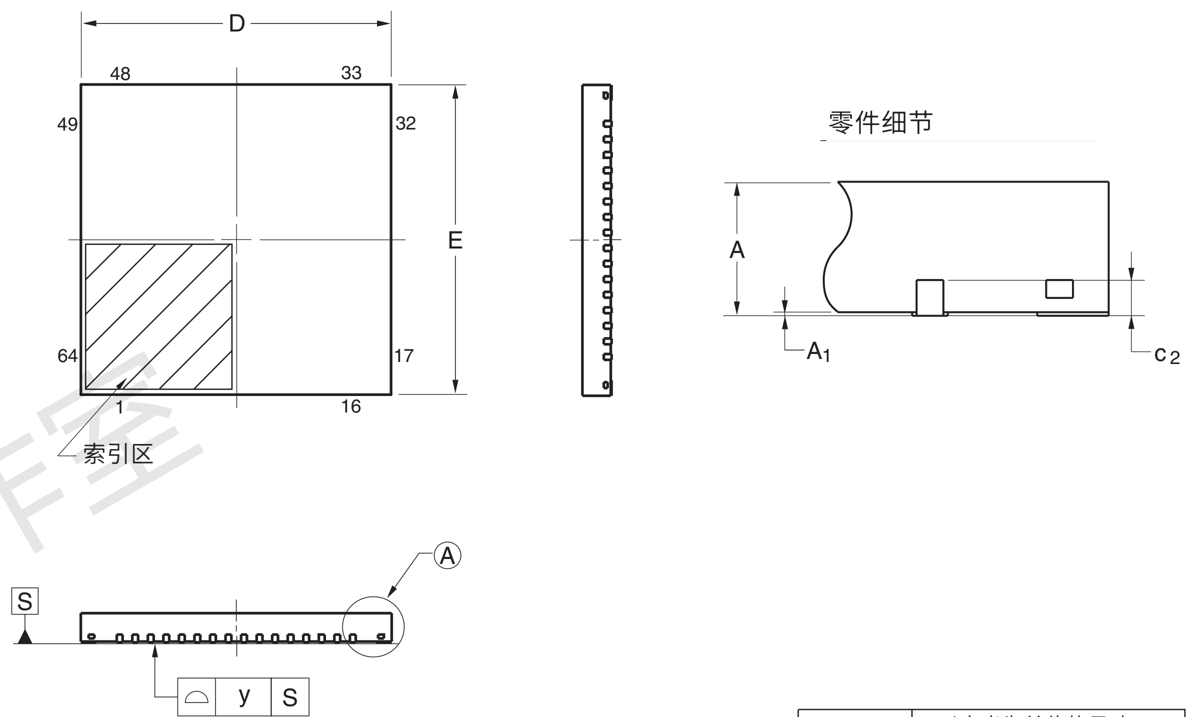


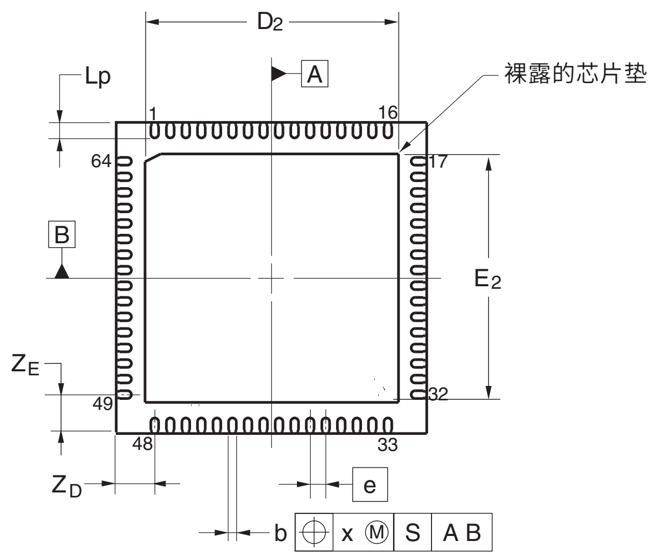


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

Figure 1.4 64-pin QFN

JEITA包装代码	RENESAS code	以前的代码	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16





Referance Symbol	以毫米为单位的尺寸		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

Figure 1.4 64-pin QFN

Revision History	RA6M1 Group Datasheet

Rev.	Date	Summary
1.00	Oct 8, 2019	First release

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修订记录	RA6M1 Group Datasheet

Rev.	Date	Summary
1.00	Oct 8, 2019	首次发布

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RA6M1 Group Datasheet

Publication Date: Rev.1.00 Oct 8, 2019

Published by: Renesas Electronics Corporation

RA6M1 Group Datasheet

Publication Date: Rev.1.00 Oct 8, 2019

Published by: 瑞萨电子公司

General Precautions

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

一般注意事项

1.防止静电放电(ESD)强电场暴露于CMOS器件时，会导致栅极氧化物的破坏，并最终导致

降级设备操作。必须采取措施，尽可能地阻止静电的产生，并在产生时迅速消散。环境控制必须充分。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具，包括工作台和地板都必须接地。操作员还必须使用腕带接地。不得赤手触摸半导体器件。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。

2.通电时的处理通电时产品的状态是不确定的。LSI内部电路的状态为

indeterminate并且在供电时寄存器设置和引脚的状态未定义。在将复位信号施加到外部复位管脚的成品中，从通电到复位过程完成，管脚的状态不能得到保证。同样，通过片内上电复位功能复位的产品，从通电到电源达到指定的复位电平，其引脚的状态也无法保证。

3.关机状态下的信号输入不要在设备关机状态下输入信号或IO上拉电源。输入此类信号或IO上拉电源导致的电流注入可能会导致故障，此时通过设备的异常电流可能会导致内部元件退化。遵循产品文档中所述的断电状态下输入信号指南。

4.未使用引脚的处理按照手册中未使用引脚处理中的说明处理未使用引脚。CMOS产品的输入引脚一般处于高阻状态。在未使用的引脚处于开路状态的情况下，在LSI附近会感应出额外的电磁噪声，相关的直通电流会在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。

5.时钟信号应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序执行过程中切换时钟信号时，请等待目标时钟信号稳定。在复位期间使用外部谐振器或外部振荡器生成时钟信号时，请确保仅在时钟信号完全稳定后才释放复位线。此外，在程序执行过程中切换到由外部谐振器或外部振荡器产生的时钟信号时，请等待目标时钟信号稳定。

6.输入引脚的电压施加波形由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS设备的输入

由于噪声等原因，会停留在VIL(Max.)和VIH(Min.)之间的区域内，例如，设备可能会发生故障。当输入电平固定时，以及输入电平通过VIL(Max.)和VIH(Min.)之间的区域时，请注意防止颤振噪声进入器件。

7.禁止访问保留地址
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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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瑞萨电子株式会社TOYOSUFORESIA 3-2-24Toyosu Koto-ku Tokyo135
-0061 Japan
瑞萨电子美国公司1001MurphyRanchRoad Milpitas CA
95035 U.S.A.电话：+1-408-432-8888，传真：+1-40
8-434-5351
瑞萨电子加拿大有限公司9251YongeStreet Suite8309RichmondHill Ont
arioCanadaL4C9T3电话：+1-905-237-2004

瑞萨电子欧洲有限公司
Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327
瑞萨电子（中国）有限公司
中国北京市海淀区上地8街7号院7号楼1层101-T01室100085

瑞萨电子（上海）有限公司
中国上海市普陀区岚皋路555号中央大厦A座301单元200333

瑞萨电子香港有限公司香港九龙旺角太子道西193号世纪广场2座16楼1601-1611室

RenesasElectronicsTaiwanCo. Ltd.13F No.363 FuShingNort
hRoad Taipei10543 Taiwan电话：+886-2-8175-9600，
传真：+8862-8175-9670
瑞萨电子新加坡私人有限公司Ltd.80BendemeerRoad Unit#06-02HyfluxInnovat
ionCentre Singapore339949电话：+65-6213-0200，传真：+65-6213-0300
RenesasElectronicsMalaysiaSdn.Bhd.

UnitNo3A-1Level3ATower8UOABusinessPark No1JalanPengaturcaraU151A SeksyenU1 40150ShahAlam Selangor Malaysia

瑞萨电子印度列兵。有限公司
No.777C 100FeetRoad HAL2ndStage Indiranagar Bangalore560038 India

RenesasElectronicsKoreaCo. Ltd.17F KAMCOYangjaeTower 262 Gangnam-daero Gangn
am-gu Seoul 06265KoreaTel:+82-2-558-3737 Fax:+82-2-558-5338

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