

High-performance 240 MHz Arm Cortex-M33 core, up to 512 KB code flash memory with background operation, 16 KB Data flash memory, and 64 KB SRAM with ECC. Integrated 12-bit A/D Converter with sample-and-hold circuit for simultaneous sampling and single-end/pseudo-differential input supportive amplifier. Integrated General PWM Timer with 200 MHz operation and high resolution. Integrated Secure Cryptographic Engine with cryptography accelerators and key management support in concert with Arm TrustZone for integrated secure element functionality.

## Features

- **Arm® Cortex®-M33 Core**
  - Armv8-M architecture with the main extension
  - Maximum operating frequency: 240 MHz
  - Arm Memory Protection Unit (Arm MPU)
    - Protected Memory System Architecture (PMSAv8)
    - Secure MPU (MPU\_S): 8 regions
    - Non-secure MPU (MPU\_NS): 8 regions
  - SysTick timer
    - Embeds two SysTick timers: Secure and Non-secure instance
    - Driven by LOCO or system clock
  - CoreSight™ ETM-M33
- **Memory**
  - Up to 512-KB code flash memory
  - 16-KB data flash memory (125,000 program/erase (P/E) cycles)
  - 64-KB SRAM
- **Connectivity**
  - Serial Communications Interface (SCI) × 6
    - Asynchronous interfaces
    - 8-bit clock synchronous interface
    - Smart card interface
    - Simple IIC
    - Simple SPI
    - Simple LIN
    - Manchester coding
  - I<sup>2</sup>C bus interface (IIC) × 2
    - Transfer at up to 3.2 Mbps (high speed mode)
  - Serial Peripheral Interface (SPI) × 2
  - CAN with Flexible Data-rate (CANFD)
- **Analog**
  - 12-bit A/D Converter (ADC) × 2
    - Sample-and-hold circuits × 6
    - Programmable Gain Amplifier × 4
  - High-Speed Analog Comparator (ACMPHS) × 4
  - 12-bit D/A Converter (DAC12) × 4
  - Temperature Sensor (TSN)
- **Timers**
  - General PWM Timer 32-bit (GPT32) with High Resolution × 4
    - 156 ps resolution in 200 MHz
  - General PWM Timer 32-bit (GPT32) × 6
  - Low Power Asynchronous General Purpose Timer (AGT) × 2
- **Security and Encryption**
  - Secure Cryptographic Engine (SCE5)
    - Symmetric algorithms: AES
    - Hash-value generation: GHASH
    - 128-bit unique ID
  - Arm® TrustZone®
    - Up to three regions for the code flash
    - Up to two regions for the data flash
    - Up to three regions for the SRAM
    - Individual secure or non-secure security attribution for each peripheral
  - Device lifecycle management
- **System and Power Management**
  - Low power modes
  - Event Link Controller (ELC)
  - Data Transfer Controller (DTC)
  - DMA Controller (DMAC) × 8
  - Power-on reset
  - Low Voltage Detection (LVD) with voltage settings
  - Watchdog Timer (WDT)
  - Independent Watchdog Timer (IWDT)
  - Key Interrupt Function (KINT)
- **Data Processing Accelerator**
  - Trigonometric Function Unit (TFU)
  - IIR Filter Accelerator (IIRFA)
- **Multiple Clock Sources**
  - Main clock oscillator (MOSC) (8 to 24 MHz)
  - High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
  - Middle-speed on-chip oscillator (MOCO) (8 MHz)
  - Low-speed on-chip oscillator (LOCO) (32.768 kHz)
  - IWDG-dedicated on-chip oscillator (15 kHz)
  - Clock trim function for HOCO/MOCO/LOCO
  - PLL/PLL2
  - Clock out support
- **General-Purpose I/O Ports**
  - 5-V tolerance, open drain, input pull-up, switchable driving ability
- **Operating Voltage**
  - VCC: 2.7 to 3.6 V
- **Operating Temperature and Packages**
  - Ta = -40°C to +105°C
    - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
    - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
    - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
    - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
    - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

高性能240MHzArmCortex-M33内核、高达512KB的后台运行代码闪存、16KB数据闪存和带ECC的64KBSRAM。集成12位AD转换器，带有用于同步采样的采样保持电路和单端伪差分输入支持放大器。具有200MHz操作和高分辨率的集成通用PWM定时器。具有加密加速器和密钥管理支持的集成安全加密引擎与ArmTrustZone相结合，可实现集成安全元件功能。

## Features

- **Arm®Cortex®-M33内核**
  - 带有主扩展的Armv8-M架构 ● 最大工作频率: 240MHz ● Arm内存保护单元 (ArmMPU)
- 受保护的内存系统架构(PMSAv8) 安全MPU(MPU\_S): 8个区域 非安全MPU(MPU\_NS): 8个区域 ● SysTick计时器
- 嵌入两个SysTick计时器: 安全和非安全实例 由LOCO或系统时钟驱动 ● CoreSight ETM-M33
- **Memory**
  - 高达512-KB代码闪存 ● 16-KB数据闪存 (125 000次程序擦除(PE)周期) ● 64-KBSRAM
- **Connectivity**
  - 串行通信接口(SCI)×6 异步接口 8位时钟同步接口 智能卡接口 SimpleIIC SimpleSPI SimpleLIN Manchester编码 ● I2C总线接口(IIC)×2
- 传输速率高达3.2Mbps (高速模式) ● 串行外设接口(SPI)×2 ● 具有灵活数据速率的CAN(CANFD)
- **Analog**
  - 12位模数转换器(ADC)×2 采样保持电路×6 可编程增益放大器×4 ● 高速模拟比较器(ACMPHS)×4 ● 12位数模转换器(DAC12)×4 ● 温度传感器(TSN)
- **Timers**
  - 通用PWM定时器32位(GPT32), 高分辨率×4 156ps分辨率, 200MHz ● 通用PWM定时器32位(GPT32)×6 ● 低功耗异步通用定时器(AGT)×2
- **安全和加密**
  - 安全加密引擎(SCE5) 对称算法: AES 哈希值生成: GHASH 128位唯一ID ● Arm®TrustZone®
- 代码闪存最多三个区域 数据闪存最多两个区域 SRAM最多三个区域 每个外围设备的单独安全或非安全安全属性 ● 设备生命周期管理
- **系统和电源管理** ● 低功耗模式 ● 事件链接控制器(ELC) ● 数据传输控制器(DTC) ● DMA控制器(DMAC) ×8 ● 上电复位 ● 具有电压设置的低电压检测(LVD) ● 看门狗定时器(WDT) ● 独立看门狗定时器(IWDT) ● 按键中断功能(KINT)
- **数据处理加速器**
  - 三角函数单元(TFU) ● IIR滤波器加速器(IIRFA)
- **多个时钟源**
  - 主时钟振荡器 (MOSC) (8至24MHz) ● 高速片上振荡器 (HOCO) (16/18/20MHz) ● 中速片上振荡器 (MOCO) (8MHz) ● 低速片上振荡器 (LOCO) (32.768kHz) ● IWDG专用片上振荡器 (15kHz) ● HOCO/MOCO/LOCO的时钟微调功能 ● PLL/PLL2 ● 时钟输出支持
- **General-Purpose I/O Ports**
  - 5V容差、开漏、输入上拉、可切换驱动能力
- **工作电压** ● VCC: 2.7至3.6V
- **工作温度和封装** ● Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

## 1. Overview

The MCU integrates multiple series of software-compatible Arm<sup>®</sup>-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex<sup>®</sup>-M33 core running up to 240 MHz with the following features:

- Up to 512 KB code flash memory
- 64 KB SRAM
- General PWM Timer (GPT) - Enhanced High Resolution
- Analog peripherals
- Security and safety features

### 1.1 Function Outline

Table 1.1 Arm core

| Feature             | Functional description   |
|---------------------|--|
| Arm Cortex-M33 core | <ul style="list-style-type: none"> <li>● Maximum operating frequency: up to 240 MHz</li> <li>● Arm Cortex-M33 core: <ul style="list-style-type: none"> <li>– Armv8-M architecture with security extension</li> <li>– Revision: r0p4-00rel0</li> </ul> </li> <li>● Arm Memory Protection Unit (Arm MPU) <ul style="list-style-type: none"> <li>– Protected Memory System Architecture (PMSAv8)</li> <li>– Secure MPU (MPU_S): 8 regions</li> <li>– Non-secure MPU (MPU_NS): 8 regions</li> </ul> </li> <li>● SysTick timer <ul style="list-style-type: none"> <li>– Embeds two SysTick timers: Secure and Non-secure instance</li> <li>– Driven by SysTick timer clock (SYSTICCLK) or system clock (ICKLK)</li> </ul> </li> <li>● CoreSight™ ETM-M33</li> </ul> |

Table 1.2 Memory

| Feature               | Functional description   |
|-----------------------|--|
| Code flash memory     | Maximum 512 KB of code flash memory.                                     |
| Data flash memory     | 16 KB of data flash memory.  |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. |
| SRAM                  | On-chip high-speed SRAM with Error Correction Code (ECC).                |

Table 1.3 System (1 of 2)

| Feature                     | Functional description   |
|-----------------------------|--|
| Operating modes             | Two operating modes: <ul style="list-style-type: none"> <li>● Single-chip mode</li> <li>● SCI boot mode</li> </ul>   |
| Resets                      | The MCU provides 14 resets.  |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. |
| Clocks                      | <ul style="list-style-type: none"> <li>● Main clock oscillator (MOSC)</li> <li>● High-speed on-chip oscillator (HOCO)</li> <li>● Middle-speed on-chip oscillator (MOCO)</li> <li>● Low-speed on-chip oscillator (LOCO)</li> <li>● IWDG-dedicated on-chip oscillator</li> <li>● PLL/PLL2</li> <li>● Clock out support</li> </ul>  |

## 1. Overview

该MCU集成了多个基于Arm<sup>®</sup>软件兼容的32位内核，这些内核共享一组通用的瑞萨外设，以促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达240MHz的高性能ArmCortex<sup>®</sup>-M33内核，具有以下特性：

- 高达512KB的代码闪存
- 64 KB SRAM
- 通用PWM定时器(GPT)增强型高分辨率
- 模拟外设
- 安全和安全功能

### 1.1 功能概要

Table 1.1 臂芯

| Feature         | 功能说明   |
|-----------------|--|
| ArmCortex-M33内核 | <ul style="list-style-type: none"> <li>● 最大工作频率：高达240MHz</li> <li>● Arm Cortex-M33 core: <ul style="list-style-type: none"> <li>– 带有安全扩展的Armv8-M架构</li> <li>– Revision: r0p4-00rel0</li> </ul> </li> <li>● Arm内存保护单元 (ArmMPU) <ul style="list-style-type: none"> <li>– 受保护的内存系统架构(PMSAv8)</li> <li>– 安全MPU(MPU_S): 8个区域</li> <li>– Non-secure MPU (MPU_NS): 8 regions</li> </ul> </li> <li>● SysTick timer <ul style="list-style-type: none"> <li>– 嵌入两个SysTick计时器：安全和非安全实例</li> <li>– 由SysTick定时器时钟(SYSTICCLK)或系统时钟(ICKLK)驱动</li> </ul> </li> <li>● CoreSight™ ETM-M33</li> </ul> |

Table 1.2 Memory

| Feature               | 功能说明                 |
|-----------------------|----------------------|
| 代码闪存                  | 最大512KB的代码闪存。        |
| 数据闪存                  | 16KB数据闪存。            |
| Option-setting memory | 选项设置存储器确定复位后MCU的状态。  |
| SRAM                  | 具有纠错码(ECC)的片上高速SRAM。 |

Table 1.3 系统(1of2)

| Feature    | 功能说明   |
|------------|--|
| 操作模式       | 两种操作模式：● <ul style="list-style-type: none"> <li>● SCI开机模式</li> </ul>   |
| Resets     | MCU提供14次复位。  |
| 低电压检测(LVD) | 低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器 (LVD0、LVD1、LVD2) 组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。   |
| Clocks     | <ul style="list-style-type: none"> <li>● 主时钟振荡器(MOSC)</li> <li>● High-speed on-chip oscillator (HOCO)</li> <li>● Middle-speed on-chip oscillator (MOCO)</li> <li>● Low-speed on-chip oscillator (LOCO)</li> <li>● IWDG-dedicated on-chip oscillator</li> <li>● PLL/PLL2</li> <li>● 打卡支持</li> </ul> |

Table 1.3 System (2 of 2)

| Feature  | Functional description   |
|--|--|
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. |
| Interrupt Controller Unit (ICU)                    | The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.  |
| Key Interrupt Function (KINT)                      | The key interrupt function (KINT) generates the key interrupt by detecting rising or falling edge on the key interrupt input pins.   |
| Low power modes                                    | Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.   |
| Register write protection                          | The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).   |
| Memory Protection Unit (MPU)                       | The MCU has one Memory Protection Unit (MPU).  |

Table 1.4 Event link

| Feature                     | Functional description   |
|-----------------------------|--|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. |

Table 1.5 Direct memory access

| Feature                        | Functional description  |
|--------------------------------|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.   |
| DMA Controller (DMAC)          | The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. |

Table 1.6 Timers (1 of 2)

| Feature  | Functional description  |
|--|---|
| General PWM Timer (GPT)                            | The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 10 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.  |
| PWM Delay Generation Circuit (PDG)                 | The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323.  |
| Port Output Enable for GPT (POEG)                  | The POEG issues requests to stop output from output pins of the general PWM timer (GPT). Select the method of detection for stopping the output from the list below.  |
| Low power Asynchronous General Purpose Timer (AGT) | The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. |
| Watchdog Timer (WDT)                               | The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.  |

Table 1.3 系统(2之2)

| Feature         | 功能说明  |
|-----------------|---|
| 时钟频率精度测量电路(CAC) | 时钟频率精度测量电路(CAC)在被选为测量基准的时钟(测量基准时钟)产生的时间内对要测量的时钟(测量目标时钟)的脉冲进行计数,并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时,将产生中断请求。 |
| 中断控制器单元(ICU)    | 中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。                                   |
| 按键中断功能(KINT)    | 按键中断功能(KINT)通过检测按键中断输入引脚的上升沿或下降沿来产生按键中断。  |
| 低功耗模式           | 可以通过多种方式降低功耗,包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。   |
| 寄存器写保护          | 寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。   |
| 内存保护单元(MPU)     | MCU有一个内存保护单元(MPU)。  |

Table 1.4 活动链接

| Feature      | 功能说明   |
|--------------|--|
| 事件链接控制器(ELC) | EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号,将它们连接到不同的模块,允许模块之间直接链接,无需CPU干预。 |

Table 1.5 直接内存访问

| Feature               | 功能说明   |
|-----------------------|--|
| 数据传输控制器(DTC)          | 数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。   |
| DMA Controller (DMAC) | MCU包括一个8通道直接内存访问控制器(DMAC),无需CPU干预即可传输数据。当产生DMA传输请求时,DMAC将存储在传输源地址的数据传输到传输目标地址。 |

Table 1.6 计时器(1of2)

| Feature           | 功能说明  |
|-------------------|---|
| 通用PWM定时器(GPT)     | 通用PWM定时器(GPT)是一个具有GPT32×10通道的32位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外,可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。        |
| PWM延迟产生电路(PDG)    | PWM延迟生成电路(PDG)有4个通道的延迟电路,可以连接到GPT。PDG可以控制PWM输出的上升沿和下降沿时序GPT320通过GPT323。                                       |
| GPT(POEG)的端口输出使能  | POEG发出请求以停止通用PWM定时器(GPT)的输出引脚的输出。从下表中选择停止输出的检测方法。   |
| 低功耗异步通用目的定时器(AGT) | 低功耗异步通用定时器(AGT)是一个32位定时器,可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址,可以通过AGT寄存器访问。 |
| 看门狗定时器(WDT)       | 看门狗定时器(WDT)是一个14位递减计数器,可用于在计数器下溢时复位MCU,因为系统已失控且无法刷新WDT。此外,WDT可用于产生不可屏蔽中断或下溢中断。                                |

Table 1.6 Timers (2 of 2)

| Feature                           | Functional description   |
|-----------------------------------|--|
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. |

Table 1.7 Communication interfaces

| Feature                               | Functional description  |
|---------------------------------------|---|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> <li>Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))</li> <li>8-bit clock synchronous interface</li> <li>Simple IIC (master-only)</li> <li>Simple SPI</li> <li>Simple LIN</li> <li>Smart card interface</li> <li>Manchester interface</li> </ul> The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0 to 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. |
| I <sup>2</sup> C bus interface (IIC)  | The I <sup>2</sup> C bus interface (IIC) has 2 channels. The IIC module conform with and provide a subset of the NXP I <sup>2</sup> C (Inter-Integrated Circuit) bus interface functions.   |
| Serial Peripheral Interface (SPI)     | The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.  |
| CAN with Flexible Data-rate (CANFD)   | The CAN with Flexible Data-rate (CANFD) module can handle classical CAN frames and CAN-FD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffer.  |

Table 1.8 Analog

| Feature                               | Functional description   |
|---------------------------------------|--|
| 12-bit A/D Converter (ADC)            | The 12-bit A/D Converter (ADC) has two units of 12-bit successive approximation A/D Converters with sample-and-hold circuits and programmable gain amplifiers (PGA) provided. The A/D converter unit 0 (ADC0) can select up to 21 channels of analog inputs. The A/D converter unit 1 (ADC1) can select up to 17 channels of analog inputs. The temperature sensor, internal reference voltage, and D/A converters can be A/D-converted by ADC0 or ADC1.   |
| 12-bit D/A Converter (DAC12)          | A 12-bit D/A converter (DAC12) is provided.  |
| High-Speed Analog Comparator (ACMPHS) | The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. |
| Temperature Sensor (TSN)              | The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC for conversion and can be further used by the end application.   |

Table 1.6 计时器 (2个中的2个)

| Feature        | 功能说明   |
|----------------|--|
| 独立看门狗定时器(IWDT) | 独立看门狗定时器(IWDT)包含一个14位递减计数器, 必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行, 因此当系统失控时, 它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。 |

Table 1.7 通讯接口

| Feature             | 功能说明   |
|---------------------|--|
| 串行通信接口(SCI)         | 串行通信接口(SCI)×6通道具有异步和同步串行接口: ● <ul style="list-style-type: none"> <li>异步接口 (UART和异步通信接口适配器(ACIA))</li> <li>8位时钟同步接口</li> <li>Simple IIC (master-only)</li> <li>简单的SPI</li> <li>简单的LIN</li> <li>智能卡接口</li> <li>曼彻斯特界面</li> </ul> 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0到4 9)具有FIFO缓冲区以实现连续和全双工通信, 并且可以使用片上波特率发生器独立配置数据传输速度。 |
| I2C总线接口(IIC)        | I2C总线接口(IIC)有2个通道。IIC模块符合并提供NXP I2C (内部集成电路) 总线接口功能的子集。  |
| 串行外设接口(SPI)         | 串行外设接口(SPI)有2个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。   |
| 具有灵活数据速率的CAN(CANFD) | 具有灵活数据速率(CANFD)模块的CAN可以处理经典CAN帧和CAN-FD帧符合ISO11898-1标准。该模块支持4个发送缓冲区和32个接收缓冲区。   |

Table 1.8 Analog

| Feature                      | 功能说明  |
|------------------------------|---|
| 12-bit A/D Converter (ADC)   | 12位AD转换器(ADC)有两个单元12位逐次逼近AD提供带有采样保持电路和可编程增益放大器(PGA)的转换器。AD转换器单元0(ADC0)最多可以选择21个模拟输入通道。AD转换器单元1(ADC1)最多可以选择17个模拟输入通道。温度传感器、内部参考电压和DA转换器可通过ADC0或ADC1进行AD转换。 |
| 12-bit D/A Converter (DAC12) | 提供了一个12位DA转换器(DAC12)。   |
| 高速模拟比较器(ACMPHS)              | 高速模拟比较器(ACMPHS)将测试电压与参考电压进行比较, 并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源 (例如DAC12输出和内部参考电压) 以及带有或不带有内部PGA的外部源提供给比较器。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。    |
| 温度传感器(TSN)                   | 片上温度传感器(TSN)确定并监控芯片温度, 以确保器件可靠运行。传感器输出与管芯温度成正比的电压, 管芯温度与输出电压之间的关系相当线性。输出电压提供给ADC进行转换, 并可进一步供最终应用使用。   |

Table 1.9 Data processing

| Feature                       | Functional description   |
|-------------------------------|--|
| Cyclic Redundancy Check (CRC) | The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. |
| Data Operation Circuit (DOC)  | The data operation circuit (DOC) is used to compare, add, and subtract 16 or 32-bit data. An interrupt can be generated when the following conditions apply. <ul style="list-style-type: none"> <li>• When the 16 or 32-bit compared values match the detection condition</li> <li>• When the result of 16 or 32-bit data addition overflows</li> <li>• When the result of 16 or 32-bit data subtraction underflows</li> </ul>   |

Table 1.10 Data processing accelerator

| Feature                           | Functional description   |
|-----------------------------------|--|
| Trigonometric function unit (TFU) | Calculation of sine, cosine, arctangent, and $\sqrt{x^2 + y^2}$ <ul style="list-style-type: none"> <li>• A sine and cosine can be simultaneously calculated.</li> <li>• An arctangent and <math>\sqrt{x^2 + y^2}</math> can be simultaneously calculated.</li> </ul> |
| IIR Filter Accelerator (IIRFA)    | <ul style="list-style-type: none"> <li>• 16 channels of biquad IIR filter</li> <li>• cascaded biquad filter (max.32 stages)</li> <li>• Operations using single-precision floating-point numbers</li> </ul>   |

Table 1.9 数据处理

| Feature     | 功能说明   |
|-------------|--|
| 循环冗余校验(CRC) | 循环冗余校验(CRC)生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外,还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的访问。此功能在需要在某些事件中自动生成CRC代码的应用中很有用,例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。                     |
| 数据运算电路(DOC) | 数据运算电路(DOC)用于对16位或32位数据进行比较、加法和减法。当以下条件适用时,可以产生中断。● <ul style="list-style-type: none"> <li>• 当16位或32位比较值与检测条件匹配时</li> <li>• 当16位或32位数据相加结果溢出时</li> <li>• 当16位或32位数据减法的结果下溢时</li> </ul> |

Table 1.10 数据处理加速器

| Feature          | 功能说明   |
|------------------|--|
| 三角函数单元(TFU)      | 计算正弦、余弦、反正切和 $x^2+y^2$<br>可以同时计算正弦和余弦。<br>可以同时计算反正切和 $x^2+y^2$ 。 |
| IIR滤波器加速器(IIRFA) | 16通道双二阶IIR滤波器<br>级联双二阶滤波器(最多32级)<br>使用单精度浮点数的运算                  |

### 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

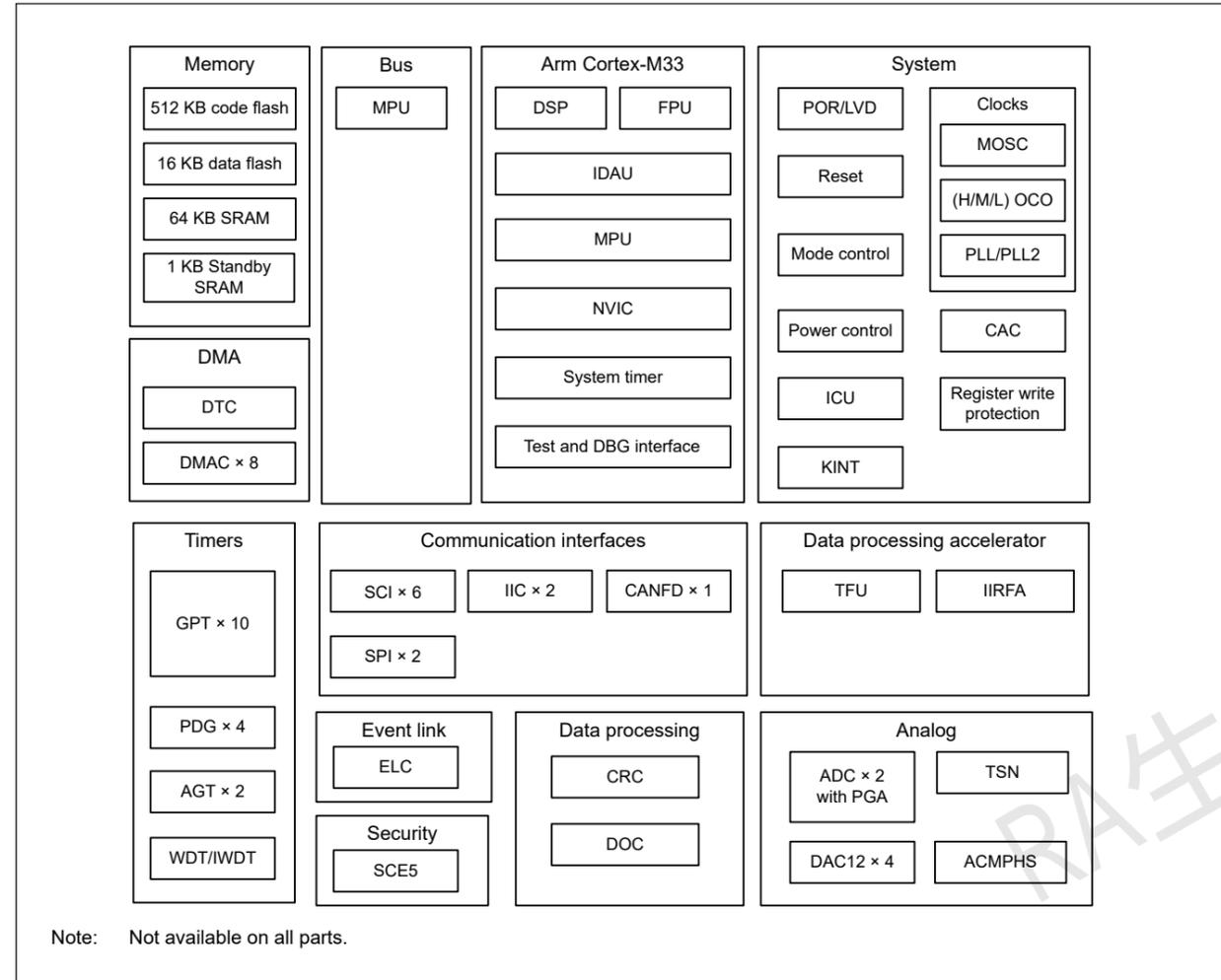


Figure 1.1 Block diagram

### 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.

### 1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。

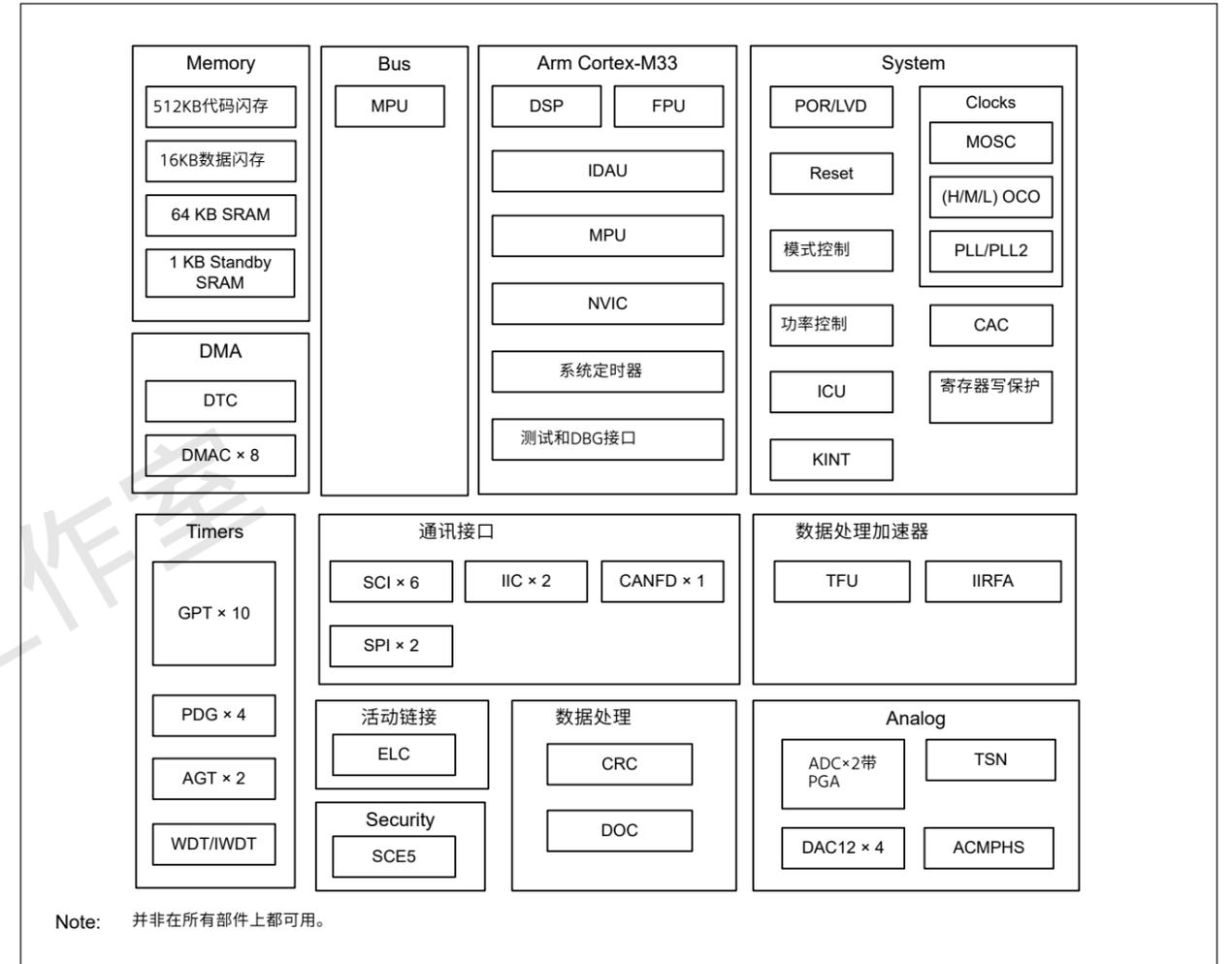


Figure 1.1 框图

### 1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.11显示了产品列表。

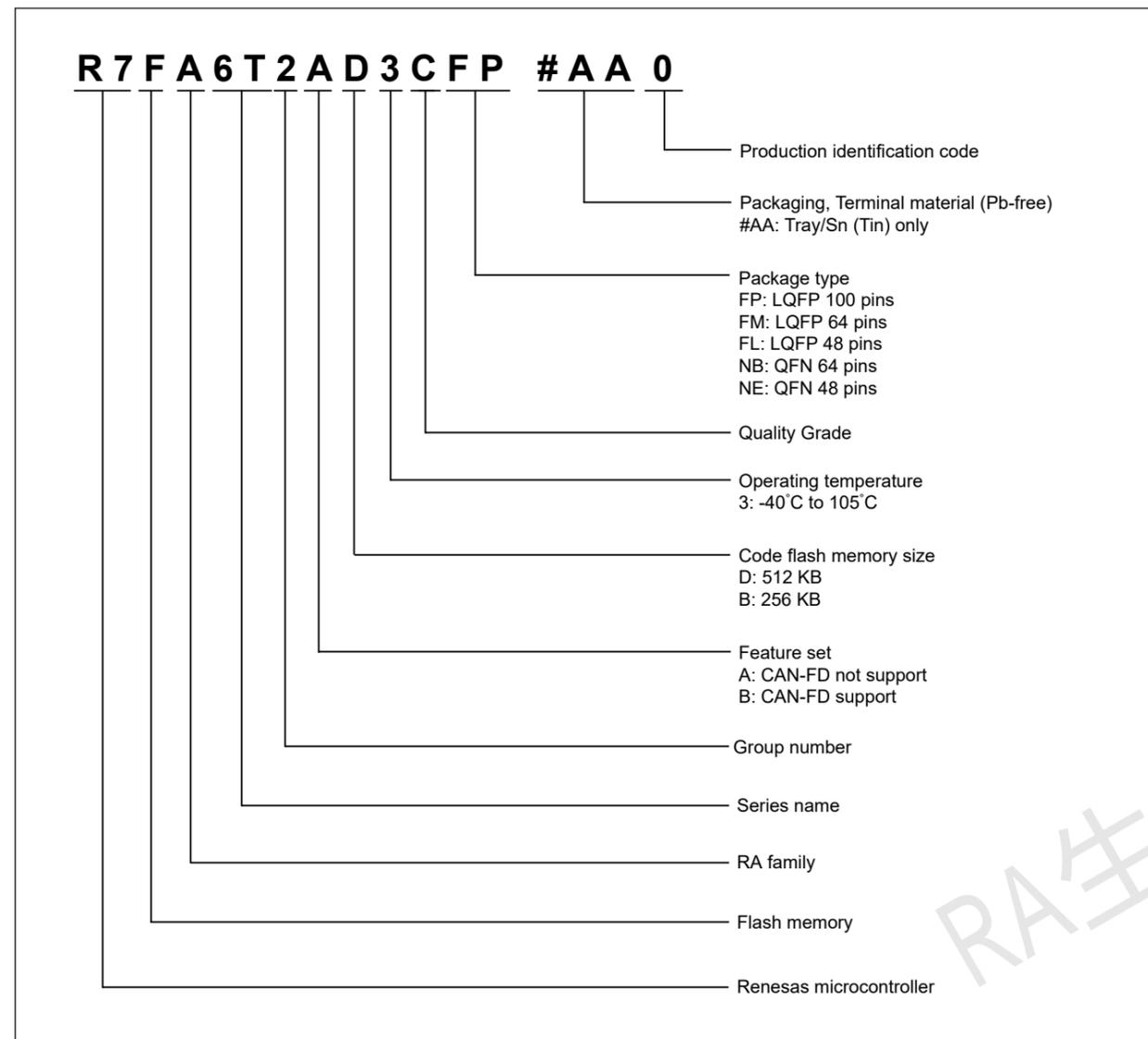


Figure 1.2 Part numbering scheme

Table 1.11 Product list (1 of 2)

| Product part number | Package code | Code flash | Data flash | SRAM  | CAN-FD      | Operating temperature |
|---------------------|--------------|------------|------------|-------|-------------|-----------------------|
| R7FA6T2AD3CFP       | PLQP0100KB-B | 512 KB     | 16 KB      | 64 KB | Not support | -40 to +105°C         |
| R7FA6T2AD3CFM       | PLQP0064KB-C |            |            |       |             |                       |
| R7FA6T2AD3CFL       | PLQP0048KB-B |            |            |       |             |                       |
| R7FA6T2AD3CNP       | PWQN0064LA-A |            |            |       |             |                       |
| R7FA6T2AD3CNE       | PWQN0048KB-A |            |            |       |             |                       |
| R7FA6T2AB3CFP       | PLQP0100KB-B |            |            |       |             |                       |
| R7FA6T2AB3CFM       | PLQP0064KB-C |            |            |       |             |                       |
| R7FA6T2AB3CFL       | PLQP0048KB-B |            |            |       |             |                       |
| R7FA6T2AB3CNP       | PWQN0064LA-A |            |            |       |             |                       |
| R7FA6T2AB3CNE       | PWQN0048KB-A |            |            |       |             |                       |
|                     |              |            |            |       |             |                       |

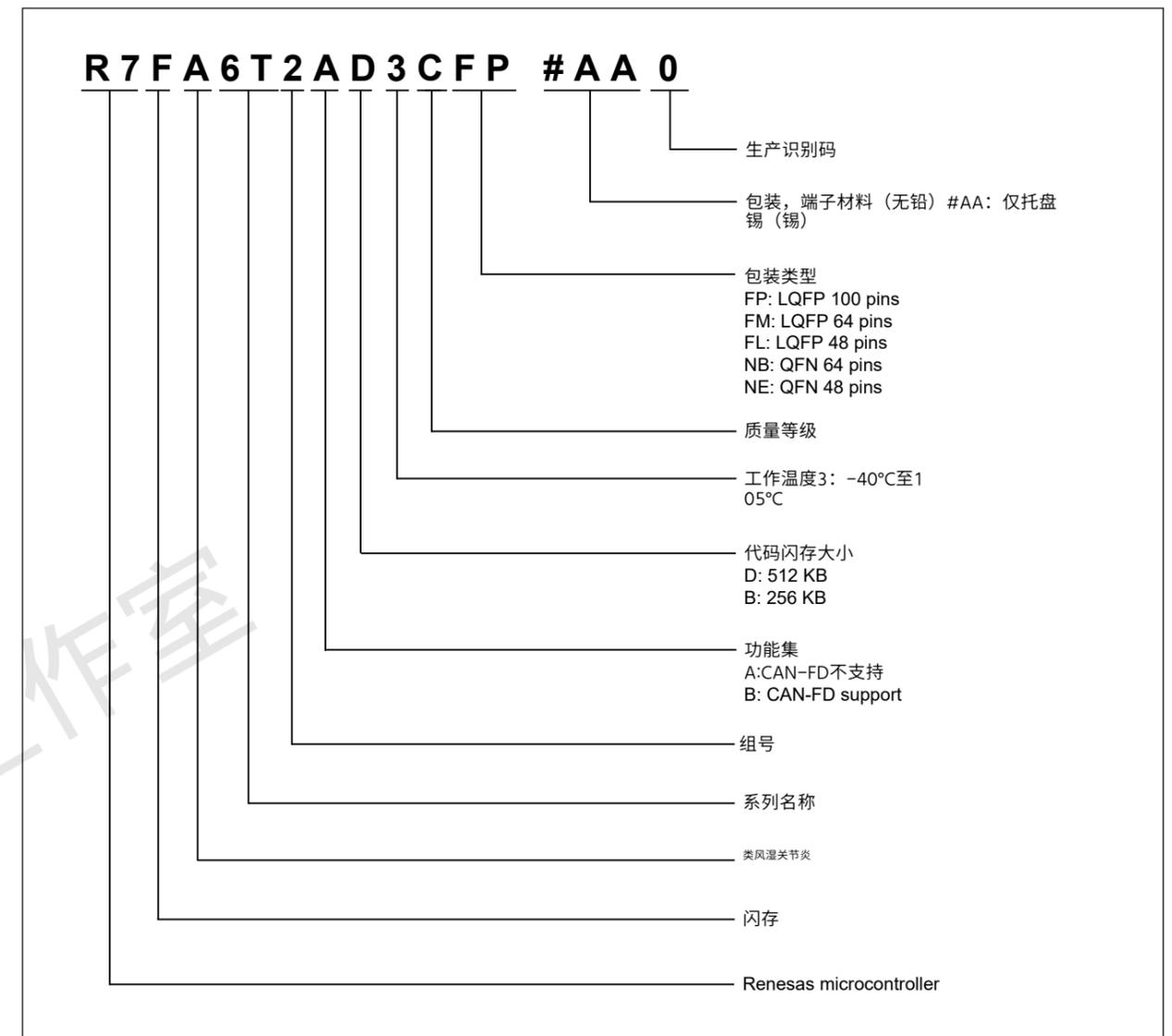


Figure 1.2 零件编号方案

Table 1.11 产品列表(1of2)

| 产品部件号         | 包装代码         | 代码闪存   | 数据闪存  | SRAM  | CAN-FD | 工作温度          |
|---------------|--------------|--------|-------|-------|--------|---------------|
| R7FA6T2AD3CFP | PLQP0100KB-B | 512 KB | 16 KB | 64 KB | 不支持    | -40 to +105°C |
| R7FA6T2AD3CFM | PLQP0064KB-C |        |       |       |        |               |
| R7FA6T2AD3CFL | PLQP0048KB-B |        |       |       |        |               |
| R7FA6T2AD3CNP | PWQN0064LA-A |        |       |       |        |               |
| R7FA6T2AD3CNE | PWQN0048KB-A |        |       |       |        |               |
| R7FA6T2AB3CFP | PLQP0100KB-B |        |       |       |        |               |
| R7FA6T2AB3CFM | PLQP0064KB-C |        |       |       |        |               |
| R7FA6T2AB3CFL | PLQP0048KB-B |        |       |       |        |               |
| R7FA6T2AB3CNP | PWQN0064LA-A |        |       |       |        |               |
| R7FA6T2AB3CNE | PWQN0048KB-A |        |       |       |        |               |
|               |              |        |       |       |        |               |

Table 1.11 Product list (2 of 2)

| Product part number | Package code | Code flash | Data flash | SRAM  | CAN-FD  | Operating temperature |
|---------------------|--------------|------------|------------|-------|---------|-----------------------|
| R7FA6T2BD3CFP       | PLQP0100KB-B | 512 KB     | 16 KB      | 64 KB | Support | -40 to +105°C         |
| R7FA6T2BD3CFM       | PLQP0064KB-C |            |            |       |         |                       |
| R7FA6T2BD3CFL       | PLQP0048KB-B |            |            |       |         |                       |
| R7FA6T2BD3CNB       | PWQN0064LA-A |            |            |       |         |                       |
| R7FA6T2BD3CNE       | PWQN0048KB-A |            |            |       |         |                       |
| R7FA6T2BB3CFP       | PLQP0100KB-B | 256 KB     |            |       |         |                       |
| R7FA6T2BB3CFM       | PLQP0064KB-C |            |            |       |         |                       |
| R7FA6T2BB3CFL       | PLQP0048KB-B |            |            |       |         |                       |
| R7FA6T2BB3CNB       | PWQN0064LA-A |            |            |       |         |                       |
| R7FA6T2BB3CNE       | PWQN0048KB-A |            |            |       |         |                       |

Table 1.11 产品列表 (2个中的2个)

| 产品部件号         | 包装代码         | 代码闪存   | 数据闪存  | SRAM  | CAN-FD  | 工作温度          |
|---------------|--------------|--------|-------|-------|---------|---------------|
| R7FA6T2BD3CFP | PLQP0100KB-B | 512 KB | 16 KB | 64 KB | Support | -40 to +105°C |
| R7FA6T2BD3CFM | PLQP0064KB-C |        |       |       |         |               |
| R7FA6T2BD3CFL | PLQP0048KB-B |        |       |       |         |               |
| R7FA6T2BD3CNB | PWQN0064LA-A |        |       |       |         |               |
| R7FA6T2BD3CNE | PWQN0048KB-A |        |       |       |         |               |
| R7FA6T2BB3CFP | PLQP0100KB-B | 256 KB |       |       |         |               |
| R7FA6T2BB3CFM | PLQP0064KB-C |        |       |       |         |               |
| R7FA6T2BB3CFL | PLQP0048KB-B |        |       |       |         |               |
| R7FA6T2BB3CNB | PWQN0064LA-A |        |       |       |         |               |
| R7FA6T2BB3CNE | PWQN0048KB-A |        |       |       |         |               |

RA生态工作室

## 1.4 Function Comparison

Table 1.12 Function Comparison

| Parts number      | R7FA6T2XX3CFP                            | R7FA6T2XX3CFM   | R7FA6T2XX3CFL            | R7FA6T2XX3CNB           | R7FA6T2XX3CNE            |                         |
|-------------------|--|---|--------------------------|-------------------------|--------------------------|-------------------------|
| Pin count         | 100                                      | 64  | 48                       | 64                      | 48                       |                         |
| Package           | LQFP                                     |   |                          | QFN                     |                          |                         |
| Code flash memory | 512 KB, 256KB                            |   |                          |                         |                          |                         |
| Data flash memory | 16 KB                                    |   |                          |                         |                          |                         |
| SRAM              | ECC                                      | 64 KB   |                          |                         |                          |                         |
| Standby SRAM      | Parity                                   | 1 KB  |                          |                         |                          |                         |
| DMA               | DTC                                      | Yes   |                          |                         |                          |                         |
|                   | DMAC                                     | 8   |                          |                         |                          |                         |
| System            | CPU clock                                | 240 MHz (max.)  |                          |                         |                          |                         |
|                   | CPU clock sources                        | MOSC, HOCO, MOCO, LOCO, PLL                                 |                          |                         |                          |                         |
|                   | CAC                                      | Yes   |                          |                         |                          |                         |
|                   | WDT/IWDT                                 | Yes   |                          |                         |                          |                         |
|                   | KINT                                     | Yes   |                          |                         |                          |                         |
| Communication     | SCI                                      | 6   |                          |                         |                          |                         |
|                   | IIC                                      | 2 <sup>2</sup>  |                          |                         |                          |                         |
|                   | SPI                                      | 2   |                          |                         |                          |                         |
|                   | CANFD                                    | 1   |                          |                         |                          |                         |
| Timers            | GPT <sup>*1</sup>                        | 10  |                          |                         |                          |                         |
|                   | AGT <sup>*1</sup>                        | 2   |                          |                         |                          |                         |
| Analog            | ADC                                      | Unit 0: 12 + 9 <sup>3</sup> ,<br>Unit 1: 8 + 9 <sup>3</sup> | Unit 0: 10,<br>Unit 1: 8 | Unit 0: 6,<br>Unit 1: 4 | Unit 0: 10,<br>Unit 1: 8 | Unit 0: 6,<br>Unit 1: 4 |
|                   | DAC12                                    | 4   | 2                        | 4                       | 4                        | 2                       |
|                   | ACMPHS                                   | 4   | 2                        | 4                       | 4                        | 2                       |
|                   | PGA                                      | 4   | 3                        | 4                       | 4                        | 3                       |
|                   | TSN                                      | Yes   |                          |                         |                          |                         |
| Data processing   | CRC                                      | Yes   |                          |                         |                          |                         |
|                   | DOC                                      | Yes   |                          |                         |                          |                         |
| Event control     | ELC                                      | Yes   |                          |                         |                          |                         |
| Accelerator       | TFU                                      | Yes   |                          |                         |                          |                         |
|                   | IIRFA                                    | Yes   |                          |                         |                          |                         |
| Security          | SCE5, TrustZone and Lifecycle management |   |                          |                         |                          |                         |

Note: The product name differs depend on the memory size and CAN-FD support. see [section 1.3. Part Numbering](#).

Note 1. Available pins depend on the Pin count, about details see [section 1.7. Pin Lists](#).

Note 2. Fm+ and Hs-mode is only available for IIC channel IIC0.

Note 3. Shared terminal for UNIT0 and UNIT1.

## 1.4 功能比较

Table 1.12 功能比较

| 零件编号          | R7FA6T2XX3CFP         | R7FA6T2XX3CFM   | R7FA6T2XX3CFL            | R7FA6T2XX3CNB           | R7FA6T2XX3CNE            |                         |
|---------------|-----------------------|---|--------------------------|-------------------------|--------------------------|-------------------------|
| 针数            | 100                   | 64  | 48                       | 64                      | 48                       |                         |
| Package       | LQFP                  |   |                          | QFN                     |                          |                         |
| 代码闪存          | 512 KB, 256KB         |   |                          |                         |                          |                         |
| 数据闪存          | 16 KB                 |   |                          |                         |                          |                         |
| SRAM          | ECC                   | 64 KB   |                          |                         |                          |                         |
| Standby SRAM  | Parity                | 1 KB  |                          |                         |                          |                         |
| DMA           | DTC                   | Yes   |                          |                         |                          |                         |
|               | DMAC                  | 8   |                          |                         |                          |                         |
| System        | 中央处理器时钟               | 240 MHz (max.)  |                          |                         |                          |                         |
|               | CPU时钟源                | MOSC, HOCO, MOCO, LOCO, PLL                                 |                          |                         |                          |                         |
|               | CAC                   | Yes   |                          |                         |                          |                         |
|               | WDT/IWDT              | Yes   |                          |                         |                          |                         |
|               | KINT                  | Yes   |                          |                         |                          |                         |
| Communication | SCI                   | 6   |                          |                         |                          |                         |
|               | IIC                   | 2 <sup>2</sup>  |                          |                         |                          |                         |
|               | SPI                   | 2   |                          |                         |                          |                         |
|               | CANFD                 | 1   |                          |                         |                          |                         |
| Timers        | GPT <sup>*1</sup>     | 10  |                          |                         |                          |                         |
|               | AGT <sup>*1</sup>     | 2   |                          |                         |                          |                         |
| Analog        | ADC                   | Unit 0: 12 + 9 <sup>3</sup> ,<br>Unit 1: 8 + 9 <sup>3</sup> | Unit 0: 10,<br>Unit 1: 8 | Unit 0: 6,<br>Unit 1: 4 | Unit 0: 10,<br>Unit 1: 8 | Unit 0: 6,<br>Unit 1: 4 |
|               | DAC12                 | 4   | 2                        | 4                       | 4                        | 2                       |
|               | ACMPHS                | 4   | 2                        | 4                       | 4                        | 2                       |
|               | PGA                   | 4   | 3                        | 4                       | 4                        | 3                       |
|               | TSN                   | Yes   |                          |                         |                          |                         |
| 数据处理          | CRC                   | Yes   |                          |                         |                          |                         |
|               | DOC                   | Yes   |                          |                         |                          |                         |
| 事件控制          | ELC                   | Yes   |                          |                         |                          |                         |
| Accelerator   | TFU                   | Yes   |                          |                         |                          |                         |
|               | IIRFA                 | Yes   |                          |                         |                          |                         |
| Security      | SCE5、TrustZone和生命周期管理 |   |                          |                         |                          |                         |

Note: 产品名称因内存大小和CAN-FD支持而异。见第1.3节。零件编号。

注1.可用管脚取决于管脚数，详情见1.7节。引脚列表。

注2.Fm+和Hs模式仅适用于IIC通道IIC0。

注3.UNIT0和UNIT1共用端子。

## 1.5 Pin Functions

Table 1.13 Pin functions (1 of 3)

| Function               | Signal           | I/O    | Description  |
|------------------------|------------------|--------|--|
| Power supply           | VCC              | Input  | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- $\mu$ F capacitor. The capacitor should be placed close to the pin. |
|                        | VCL              | I/O    | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.                  |
|                        | VSS              | Input  | Ground pin. Connect it to the system power supply (0 V).   |
| Clock                  | EXTAL            | Input  | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.   |
|                        | XTAL             | Output |  |
|                        | CLKOUT           | Output | Clock output pin   |
| Operating mode control | MD               | Input  | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.         |
| System control         | RES              | Input  | Reset signal input pin. The MCU enters the reset state when this signal goes low.  |
| CAC                    | CACREF           | Input  | Measurement reference clock input pin  |
| On-chip emulator       | TMS              | Input  | On-chip emulator or boundary scan pins   |
|                        | TDI              | Input  |  |
|                        | TCK              | Input  |  |
|                        | TDO              | Output |  |
|                        | TCLK             | Output | Output clock for synchronization with the trace data   |
|                        | TDATA0 to TDATA3 | Output | Trace data output  |
|                        | SWO              | Output | Serial wire trace output pin   |
|                        | SWDIO            | I/O    | Serial wire debug data input/output pin  |
|                        | SWCLK            | Input  | Serial wire clock pin  |
| Interrupt              | NMI              | Input  | Non-maskable interrupt request pin   |
|                        | IRQn             | Input  | Maskable interrupt request pins  |
|                        | IRQn-DS          | Input  | Maskable interrupt request pins that can also be used in Deep Software Standby mode  |
| KINT                   | KR00 to KR07     | Input  | A key interrupt can be generated by inputting a falling edge to the key interrupt input pins   |

## 1.5 引脚功能

Table 1.13 引脚功能(1of3)

| Function         | Signal           | I/O    | Description   |
|------------------|------------------|--------|---|
| 电源               | VCC              | Input  | 电源引脚。将其连接到系统电源。通过一个0.1 $\mu$ F电容将此引脚连接到VSS。电容应靠近引脚放置。 |
|                  | VCL              | I/O    | 通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。              |
|                  | VSS              | Input  | 接地引脚。将其连接到系统电源(0V)。                                   |
| Clock            | EXTAL            | Input  | 晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。                         |
|                  | XTAL             | Output |   |
|                  | CLKOUT           | Output | 时钟输出引脚  |
| 操作模式控制           | MD               | Input  | 用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。          |
| 系统控制             | RES              | Input  | 复位信号输入引脚。当该信号变低时，MCU进入复位状态。                           |
| CAC              | CACREF           | Input  | 测量参考时钟输入引脚  |
| On-chip emulator | TMS              | Input  | 片上仿真器或边界扫描引脚  |
|                  | TDI              | Input  |   |
|                  | TCK              | Input  |   |
|                  | TDO              | Output |   |
|                  | TCLK             | Output | 用于与跟踪数据同步的输出时钟  |
|                  | TDATA0 to TDATA3 | Output | 跟踪数据输出  |
|                  | SWO              | Output | 串行线迹输出引脚  |
|                  | SWDIO            | I/O    | 串行线调试数据输入输出引脚   |
|                  | SWCLK            | Input  | 串行线时钟引脚   |
| Interrupt        | NMI              | Input  | 不可屏蔽中断请求引脚  |
|                  | IRQn             | Input  | 可屏蔽中断请求引脚   |
|                  | IRQn-DS          | Input  | 可屏蔽中断请求引脚，也可用于Deep Software Standby mode              |
| KINT             | KR00 to KR07     | Input  | 通过向按键中断输入引脚输入下降沿可以产生按键中断                              |

Table 1.13 Pin functions (2 of 3)

| Function | Signal                             | I/O    | Description   |
|----------|------------------------------------|--------|---|
| GPT      | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input  | External trigger input pins   |
|          | GTIOCnA, GTIOCnB                   | I/O    | Input capture, output compare, or PWM output pins   |
|          | GTADSM0, GTADSM1                   | Output | A/D conversion start request monitoring output pins   |
|          | GTCPP00 to GTCPP04, GTCPP07        | Output | Toggle output synchronized with PWM period  |
|          | GTIU                               | Input  | Hall sensor input pin U   |
|          | GTIV                               | Input  | Hall sensor input pin V   |
|          | GTIW                               | Input  | Hall sensor input pin W   |
|          | GTOUUP                             | Output | 3-phase PWM output for BLDC motor control (positive U phase)  |
|          | GTOULO                             | Output | 3-phase PWM output for BLDC motor control (negative U phase)  |
|          | GTOVUP                             | Output | 3-phase PWM output for BLDC motor control (positive V phase)  |
|          | GTOVLO                             | Output | 3-phase PWM output for BLDC motor control (negative V phase)  |
|          | GTOVUP                             | Output | 3-phase PWM output for BLDC motor control (positive W phase)  |
|          | GTOVLO                             | Output | 3-phase PWM output for BLDC motor control (negative W phase)  |
|          | AGT                                | AGTEEn | Input   |
| AGTIOn   |                                    | I/O    | External event input and pulse output pins  |
| AGTOAn   |                                    | Output | Pulse output pins   |
| AGTOAn   |                                    | Output | Output compare match A output pins  |
| AGTOBn   |                                    | Output | Output compare match B output pins  |
| SCI      | SCKn                               | I/O    | Input/output pins for the clock (clock synchronous mode)  |
|          | RXDn                               | Input  | Input pins for received data (asynchronous mode/clock synchronous mode)   |
|          | TXDn                               | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode)   |
|          | CTS <sub>n</sub> _RTS <sub>n</sub> | I/O    | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low. |
|          | CTS <sub>n</sub>                   | Input  | Input for the start of transmission.  |
|          | DEn                                | Output | Output pins for Driver Enable signal  |
|          | SCLn                               | I/O    | Input/output pins for the IIC clock (simple IIC mode)   |
|          | SDAn                               | I/O    | Input/output pins for the IIC data (simple IIC mode)  |
|          | SCKn                               | I/O    | Input/output pins for the clock (simple SPI mode)   |
|          | MISO <sub>n</sub>                  | I/O    | Input/output pins for slave transmission of data (simple SPI mode)  |
|          | MOSI <sub>n</sub>                  | I/O    | Input/output pins for master transmission of data (simple SPI mode)   |
|          | SS <sub>n</sub>                    | Input  | Chip-select input pins (simple SPI mode), active-low  |
|          | IIC                                | SCLn   | I/O   |
| SDAn     |                                    | I/O    | Input/output pins for data  |
| SPI      | RSPCKA, RSPCKB                     | I/O    | Clock input/output pin  |
|          | MOSIA, MOSIB                       | I/O    | Input or output pins for data output from the master  |
|          | MISOA, MISOB                       | I/O    | Input or output pins for data output from the slave   |
|          | SSLA0, SSLB0                       | I/O    | Input or output pin for slave selection   |
|          | SSLA1 to SSLA3, SSLB1 to SSLB3     | Output | Output pins for slave selection   |

Table 1.13 引脚功能 (2个, 共3个)

| Function | Signal                             | I/O    | Description                             |
|----------|------------------------------------|--------|---|
| GPT      | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input  | 外部触发输入引脚                                |
|          | GTIOCnA, GTIOCnB                   | I/O    | 输入捕捉、输出比较或PWM输出引脚                       |
|          | GTADSM0, GTADSM1                   | Output | AD转换开始请求监视输出引脚                          |
|          | GTCPP00 to GTCPP04, GTCPP07        | Output | 与PWM周期同步的切换输出                           |
|          | GTIU                               | Input  | 霍尔传感器输入引脚U                              |
|          | GTIV                               | Input  | 霍尔传感器输入引脚V                              |
|          | GTIW                               | Input  | 霍尔传感器输入引脚W                              |
|          | GTOUUP                             | Output | 用于BLDC电机控制的3相PWM输出 (正U相)                |
|          | GTOULO                             | Output | 用于BLDC电机控制的3相PWM输出 (负U相)                |
|          | GTOVUP                             | Output | 用于BLDC电机控制的3相PWM输出 (正V相)                |
|          | GTOVLO                             | Output | 用于BLDC电机控制的3相PWM输出 (负V相)                |
|          | GTOVUP                             | Output | 用于BLDC电机控制的3相PWM输出 (正W相)                |
|          | GTOVLO                             | Output | 用于BLDC电机控制的3相PWM输出 (负W相)                |
|          | AGT                                | AGTEEn | Input                                   |
| AGTIOn   |                                    | I/O    | 外部事件输入和脉冲输出引脚                           |
| AGTOAn   |                                    | Output | 脉冲输出引脚                                  |
| AGTOAn   |                                    | Output | 输出比较匹配A输出引脚                             |
| AGTOBn   |                                    | Output | 输出比较匹配B输出引脚                             |
| SCI      | SCKn                               | I/O    | 时钟输入输出引脚 (时钟同步模式)                       |
|          | RXDn                               | Input  | 接收数据的输入引脚 (异步模式时钟同步模式)                  |
|          | TXDn                               | Output | 传输数据的输出引脚 (异步模式时钟同步模式)                  |
|          | CTS <sub>n</sub> _RTS <sub>n</sub> | I/O    | 输入输出引脚用于控制发送和接收的开始 (异步模式时钟同步模式), 低电平有效。 |
|          | CTS <sub>n</sub>                   | Input  | 开始传输的输入。                                |
|          | DEn                                | Output | 驱动器使能信号的输出引脚                            |
|          | SCLn                               | I/O    | IIC时钟的输入输出引脚 (简单IIC模式)                  |
|          | SDAn                               | I/O    | IIC数据的输入输出引脚 (简单IIC模式)                  |
|          | SCKn                               | I/O    | 时钟输入输出引脚 (简单SPI模式)                      |
|          | MISO <sub>n</sub>                  | I/O    | 用于从机传输数据的输入输出引脚 (简单SPI模式)               |
|          | MOSI <sub>n</sub>                  | I/O    | 输入输出引脚用于主数据传输 (简单SPI模式)                 |
|          | SS <sub>n</sub>                    | Input  | 片选输入引脚 (简单SPI模式), 低电平有效                 |
|          | IIC                                | SCLn   | I/O                                     |
| SDAn     |                                    | I/O    | 数据输入输出引脚                                |
| SPI      | RSPCKA, RSPCKB                     | I/O    | 时钟输入输出引脚                                |
|          | MOSIA, MOSIB                       | I/O    | 用于从主机输出数据的输入或输出引脚                       |
|          | MISOA, MISOB                       | I/O    | 从机数据输出的输入或输出引脚                          |
|          | SSLA0, SSLB0                       | I/O    | 从机选择的输入或输出引脚                            |
|          | SSLA1 to SSLA3, SSLB1 to SSLB3     | Output | 从机选择的输出引脚                               |

Table 1.13 Pin functions (3 of 3)

| Function            | Signal   | I/O    | Description  |
|---------------------|--|--------|--|
| CANFD               | CRX0   | Input  | Receive data   |
|                     | CTX0   | Output | Transmit data  |
| Analog power supply | AVCC0  | Input  | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin. |
|                     | AVSS0  | Input  | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.               |
|                     | VREFH0   | Input  | Analog reference voltage supply pin for the ADC. Connect this pin to AVCC0 when not using the ADC.   |
|                     | VREFL0   | Input  | Analog reference ground pin for the ADC. Connect this pin to AVSS0 when not using the ADC.   |
| ADC                 | AN000 to AN028   | Input  | Input pins for the analog signals to be processed by the A/D converter.  |
|                     | PGAIN0 to PGAIN3   | Input  | Pseudo-differential input pins of programmable gain amplifier (Signal source side)   |
|                     | PGAVSS0 to PGAVSS3   | Input  | Pseudo-differential input pins of programmable gain amplifier (reference ground side)  |
|                     | PGAOUT0 to PGAOUT3   | Output | Monitor output pins of programmable gain amplifier   |
|                     | ADTRGm   | Input  | Input pins for the external trigger signals that start the A/D conversion, active-low.   |
| DAC12               | DAn  | Output | Output pins for the analog signals processed by the D/A converter.   |
| ACMPHS              | VCOUt  | Output | Comparator output pin (OR output of all units)   |
|                     | CMPOUt <sub>m</sub>  | Output | Comparator output pin (m:unit number)  |
|                     | CMPOUt012  | Output | Comparator output pin (OR output of units 0, 1 and 2)  |
|                     | IVREF0, IVREF1   | Input  | Reference voltage input pins for comparator  |
|                     | IVCMP <sub>m</sub> 0, IVCMP <sub>m</sub> 2, IVCMP <sub>m</sub> 3   | Input  | Analog voltage input pins for comparator (m:unit number)   |
| I/O ports           | P201, P212, P213, PA08 to PA15, PB03 to PB10, PB12 to PB15, PC06 to PC12, PC14, PC15, PD00 to PD15, PE00 to PE06, PE08 to PE15 | I/O    | General-purpose input/output pins  |
|                     | P000, P001, P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13   | Input  | General-purpose input pins   |

Table 1.13 引脚功能 (3个中的3个)

| Function  | Signal   | I/O    | Description                              |
|-----------|--|--------|--|
| CANFD     | CRX0   | Input  | 接收数据                                     |
|           | CTX0   | Output | 传输数据                                     |
| 模拟电源      | AVCC0  | Input  | 模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。 |
|           | AVSS0  | Input  | 模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。    |
|           | VREFH0   | Input  | ADC的模拟参考电压电源引脚。将此引脚连接到不使用ADC时的AVCC0。     |
|           | VREFL0   | Input  | ADC的模拟参考接地引脚。将此引脚连接到不使用ADC时为AVSS0。       |
| ADC       | AN000 to AN028   | Input  | AD转换器要处理的模拟信号的输入引脚。                      |
|           | PGAIN0 to PGAIN3   | Input  | 可编程增益放大器的伪差分输入引脚 (信号源侧)                  |
|           | PGAVSS0 to PGAVSS3   | Input  | 可编程增益放大器的伪差分输入引脚 (参考地侧)                  |
|           | PGAOUT0 to PGAOUT3   | Output | 监控可编程增益放大器的输出引脚                          |
|           | ADTRGm   | Input  | 用于启动AD转换的外部触发信号的输入引脚, 低电平有效。             |
| DAC12     | DAn  | Output | 由数模转换器处理的模拟信号输出引脚。                       |
| ACMPHS    | VCOUt  | Output | 比较器输出引脚 (所有单元的OR输出)                      |
|           | CMPOUt <sub>m</sub>  | Output | 比较器输出引脚 (m: 单元号)                         |
|           | CMPOUt012  | Output | 比较器输出引脚 (单元0、1和2的OR输出)                   |
|           | IVREF0, IVREF1   | Input  | 比较器的参考电压输入引脚                             |
|           | IVCMP <sub>m</sub> 0, IVCMP <sub>m</sub> 2, IVCMP <sub>m</sub> 3   | Input  | 比较器的模拟电压输入引脚 (m: 单元数)                    |
| I/O ports | P201, P212, P213, PA08 to PA15, PB03 to PB10, PB12 to PB15, PC06 to PC12, PC14, PC15, PD00 to PD15, PE00 to PE06, PE08 to PE15 | I/O    | General-purpose input/output pins        |
|           | P000, P001, P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13   | Input  | 通用输入引脚                                   |



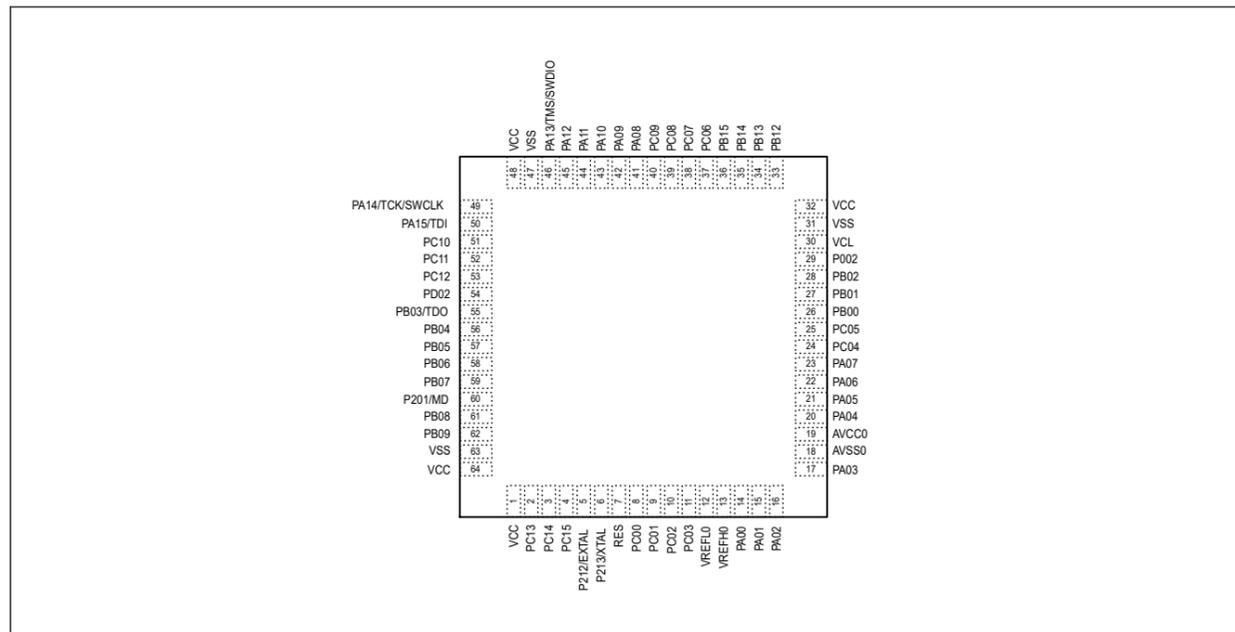


Figure 1.5 Pin assignment for QFN 64-pin

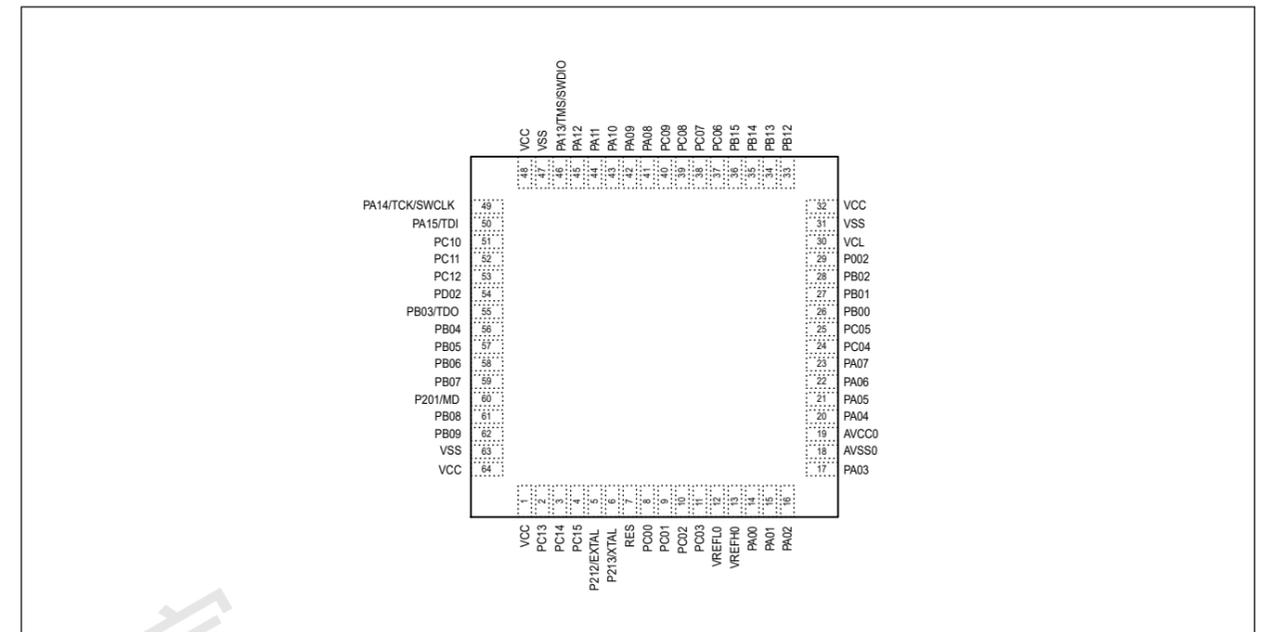


Figure 1.5 QFN64引脚的引脚分配

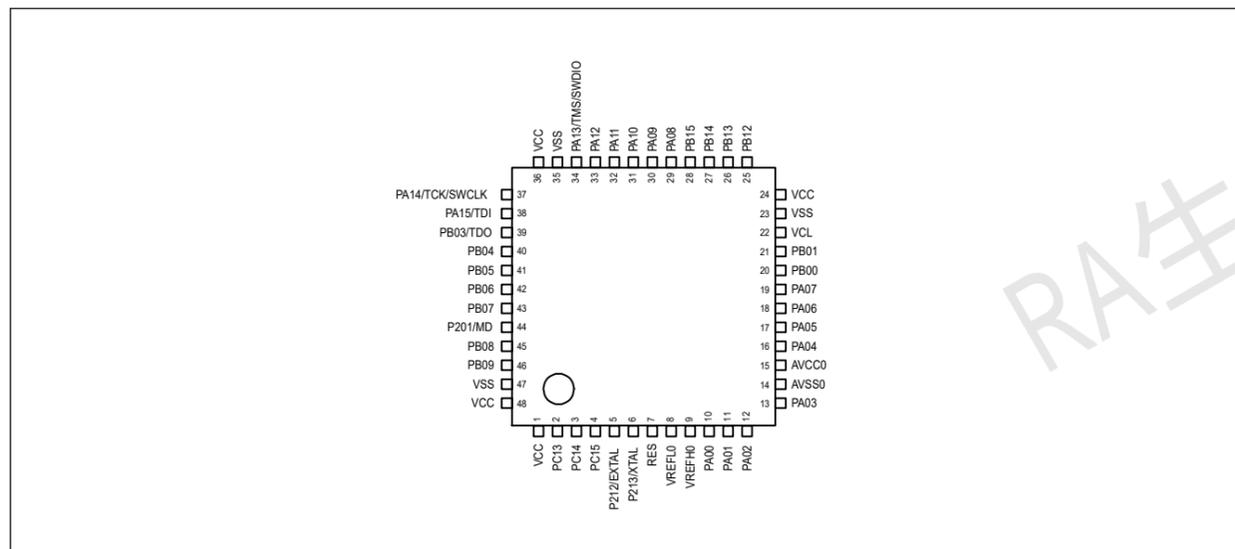


Figure 1.6 Pin assignment for LQFP 48-pin

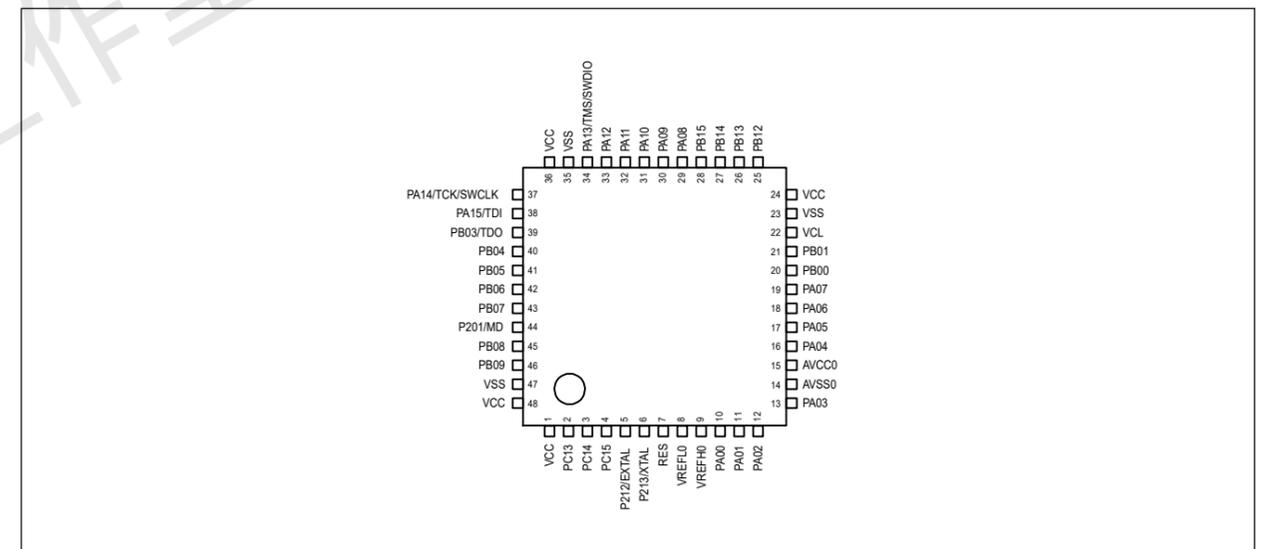


Figure 1.6 LQFP48引脚的引脚分配

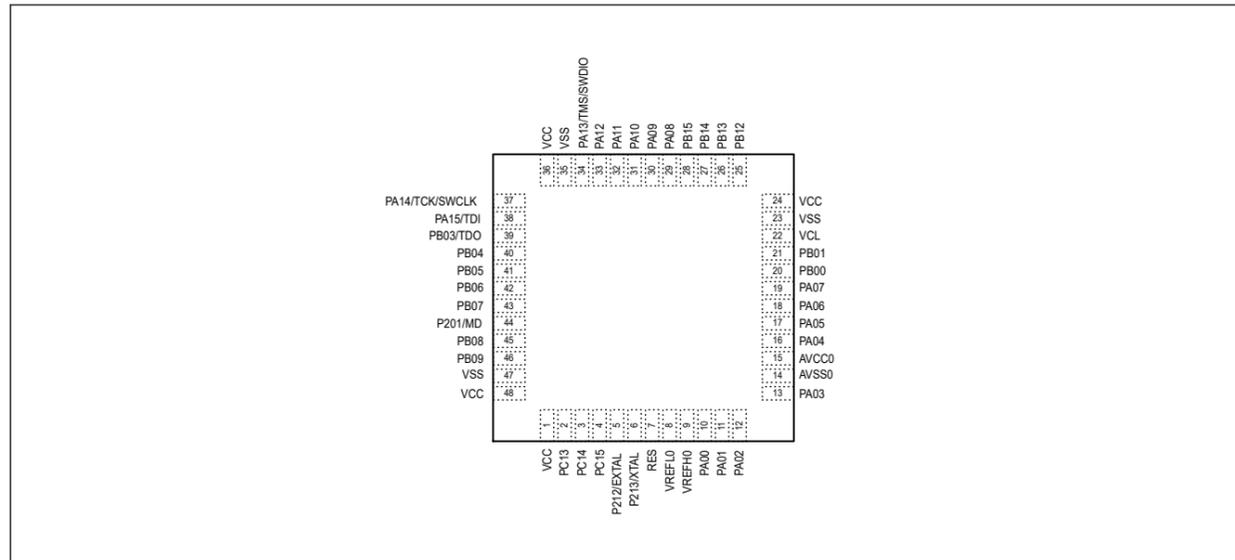


Figure 1.7 Pin assignment for QFN 48-pin

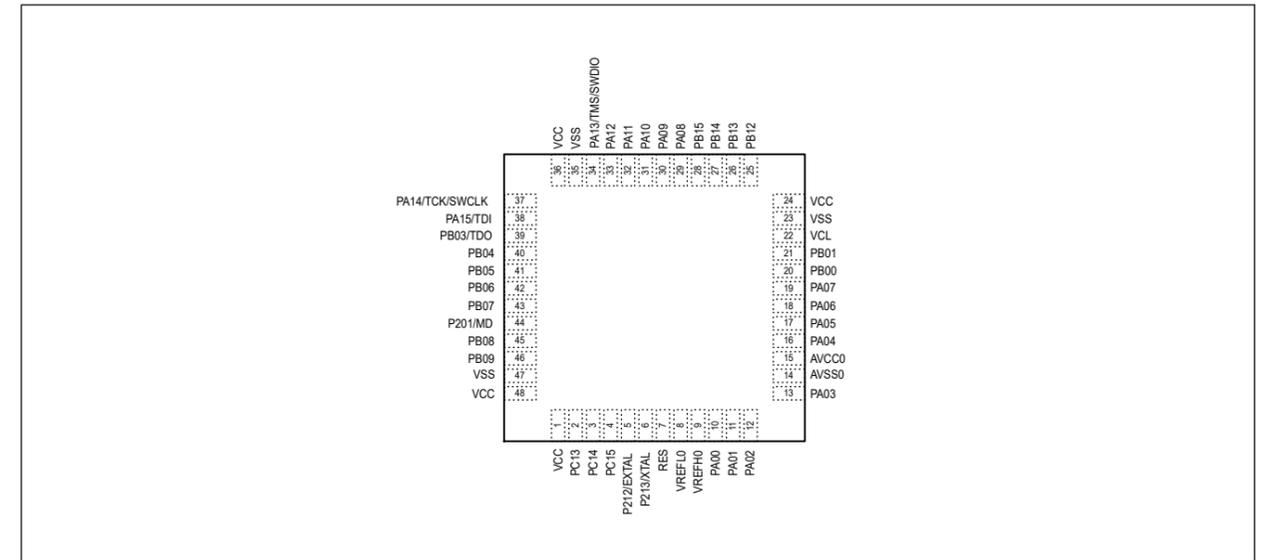


Figure 1.7 QFN48引脚的引脚分配

RA生态工作室

1.7 Pin Lists

Table 1.14 Pin list (1 of 3)

| LQFP100 | LQFP64,<br>QFN64 | LQFP48,<br>QFN48 | Power, System,<br>Clock, Debug,<br>CAC | I/O<br>ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                               | GPT/AGT  | ADC/DAC12/ACMPHS            |
|---------|------------------|------------------|--|--------------|--------------------|---|--|-----------------------------|
| 1       | —                | —                | CLKOUT/TCLK                            | PE02         | —                  | SCK0_B/DE0/SCK3_A/DE3/RSPCKB_C                  | GTOVLO/GTIOC7B/GTIOC8A                         | CMPOUT0                     |
| 2       | —                | —                | TDATA0                                 | PE03         | —                  | RXD0_B/MISO0_B/SCL0/CTS3_A/SSLB0_C              | GTOVLO/GTIOC8A/GTIOC9A                         | CMPOUT1                     |
| 3       | —                | —                | TDATA1                                 | PE04         | —                  | TXD0_B/MOSI0_B/SDA0/CTS3_RTS3/SS3_A/DE3/SSLB1_C | GTOUUP/GTIOC8B/GTIOC7B                         | CMPOUT2                     |
| 4       | —                | —                | TDATA2                                 | PE05         | —                  | CTS0_RTS0/SS0_B/DE0/RXD3_A/MISO3_A/SCL3/MISOB_C | GTOVUP/GTIOC9A/GTIOC8B/GTCCPO2                 | CMPOUT3                     |
| 5       | —                | —                | TDATA3                                 | PE06         | —                  | CTS0_B/TXD3_A/MOSI3_A/SDA3/MOSIB_C              | GTOVUP/GTIOC9B/GTCCPO3                         | —                           |
| 6       | 1                | 1                | VCC                                    | —            | —                  | —   | —  | —                           |
| 7       | 2                | 2                | —                                      | PC13         | NMI                | —   | GTETRGD  | —                           |
| 8       | 3                | 3                | —                                      | PC14         | IRQ14              | —   | GTETRGA/GTIOC3A/GTCCPO0/GTADSM0/GTCCPO4/AGTIO0 | ADTRG0/CMPOUT012            |
| 9       | 4                | 4                | —                                      | PC15         | IRQ15              | —   | GTETRGB/GTIOC3B/GTCCPO1/GTADSM1/GTCCPO7/AGTIO1 | ADTRG1/CMPOUT3              |
| 10      | —                | —                | VSS                                    | —            | —                  | —   | —  | —                           |
| 11      | —                | —                | VCC                                    | —            | —                  | —   | —  | —                           |
| 12      | 5                | 5                | EXTAL                                  | P212         | —                  | —   | —  | —                           |
| 13      | 6                | 6                | XTAL                                   | P213         | IRQ0               | —   | —  | —                           |
| 14      | 7                | 7                | RES                                    | —            | —                  | —   | —  | —                           |
| 15      | 8                | —                | —                                      | PC00         | IRQ11-DS           | —   | —  | AN012/PGAOUT0/IVCMP00       |
| 16      | 9                | —                | —                                      | PC01         | IRQ12-DS           | —   | —  | AN013/PGAOUT1/IVCMP10       |
| 17      | 10               | —                | —                                      | PC02         | IRQ13-DS           | —   | —  | AN014/PGAOUT2/IVCMP20       |
| 18      | 11               | —                | —                                      | PC03         | IRQ14-DS           | —   | —  | AN015/PGAOUT3/IVCMP30       |
| 19      | —                | —                | —                                      | P000         | IRQ0               | —   | —  | AN016/IVREF0                |
| 20      | 12               | 8                | VREFL0                                 | —            | —                  | —   | —  | —                           |
| 21      | 13               | 9                | VREFH0                                 | —            | —                  | —   | —  | —                           |
| 22      | —                | —                | —                                      | P001         | IRQ2               | —   | —  | AN017/IVREF1                |
| 23      | 14               | 10               | —                                      | PA00         | IRQ0-DS            | —   | —  | AN000/PAIN0/IVCMP02/IVCMP03 |
| 24      | 15               | 11               | —                                      | PA01         | IRQ1               | —   | —  | AN001/PAGVSS0               |
| 25      | 16               | 12               | —                                      | PA02         | IRQ2               | —   | —  | AN002/PAIN1/IVCMP12/IVCMP13 |
| 26      | 17               | 13               | —                                      | PA03         | IRQ3               | —   | —  | AN003/PAGVSS1               |
| 27      | 18               | 14               | AVSS0                                  | —            | —                  | —   | —  | —                           |
| 28      | 19               | 15               | AVCC0                                  | —            | —                  | —   | —  | —                           |
| 29      | 20               | 16               | —                                      | PA04         | IRQ4               | —   | —  | AN004/PAIN2/IVCMP22/IVCMP23 |
| 30      | 21               | 17               | —                                      | PA05         | IRQ5               | —   | —  | AN005/PAGVSS2               |
| 31      | 22               | 18               | —                                      | PA06         | IRQ6               | —   | —  | AN006/DA0                   |
| 32      | 23               | 19               | —                                      | PA07         | IRQ7               | —   | —  | AN007/DA1                   |
| 33      | 24               | —                | —                                      | PC04         | IRQ10              | —   | —  | AN010/DA2                   |
| 34      | 25               | —                | —                                      | PC05         | IRQ11              | —   | —  | AN011/DA3                   |
| 35      | 26               | 20               | —                                      | PB00         | IRQ0               | —   | —  | AN008/PGAOUT0/PGAOUT2       |
| 36      | 27               | 21               | —                                      | PB01         | IRQ1               | —   | —  | AN009/PGAOUT1/PGAOUT3       |
| 37      | 28               | —                | —                                      | PB02         | IRQ15-DS           | —   | —  | AN018/PAIN3/IVCMP32/IVCMP33 |
| 38      | 29               | —                | —                                      | P002         | —                  | —   | —  | AN019/PAGVSS3               |
| 39      | —                | —                | —                                      | PE08         | KR00               | SSLA3_C   | GTIV/GTIOC3A/GTETRGC/GTADSM0                   | AN020/ADTRG0/CMPOUT012      |
| 40      | —                | —                | CACREF                                 | PE09         | KR01               | SSLA2_C   | GTIW/GTIOC3B/GTETRGD/GTADSM1                   | AN021/ADTRG1/CMPOUT3        |
| 41      | —                | —                | —                                      | PE10         | KR02               | SSLA1_C   | GTOULO/GTIOC2A/GTIOC4A/GTIOC7A                 | AN022                       |

1.7 引脚列表

Table 1.14 引脚列表 (1个, 共3个)

| LQFP100 | LQFP64,<br>QFN64 | LQFP48,<br>QFN48 | 电源、系统、时<br>钟、调试、<br>CAC | I/O<br>ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                               | GPT/AGT  | ADC/DAC12/ACMPHS            |
|---------|------------------|------------------|-------------------------|--------------|--------------------|---|--|-----------------------------|
| 1       | —                | —                | CLKOUT/TCLK             | PE02         | —                  | SCK0_B/DE0/SCK3_A/DE3/RSPCKB_C                  | GTOVLO/GTIOC7B/GTIOC8A                         | CMPOUT0                     |
| 2       | —                | —                | TDATA0                  | PE03         | —                  | RXD0_B/MISO0_B/SCL0/CTS3_A/SSLB0_C              | GTOVLO/GTIOC8A/GTIOC9A                         | CMPOUT1                     |
| 3       | —                | —                | TDATA1                  | PE04         | —                  | TXD0_B/MOSI0_B/SDA0/CTS3_RTS3/SS3_A/DE3/SSLB1_C | GTOUUP/GTIOC8B/GTIOC7B                         | CMPOUT2                     |
| 4       | —                | —                | TDATA2                  | PE05         | —                  | CTS0_RTS0/SS0_B/DE0/RXD3_A/MISO3_A/SCL3/MISOB_C | GTOVUP/GTIOC9A/GTIOC8B/GTCCPO2                 | CMPOUT3                     |
| 5       | —                | —                | TDATA3                  | PE06         | —                  | CTS0_B/TXD3_A/MOSI3_A/SDA3/MOSIB_C              | GTOVUP/GTIOC9B/GTCCPO3                         | —                           |
| 6       | 1                | 1                | VCC                     | —            | —                  | —   | —  | —                           |
| 7       | 2                | 2                | —                       | PC13         | NMI                | —   | GTETRGD  | —                           |
| 8       | 3                | 3                | —                       | PC14         | IRQ14              | —   | GTETRGA/GTIOC3A/GTCCPO0/GTADSM0/GTCCPO4/AGTIO0 | ADTRG0/CMPOUT012            |
| 9       | 4                | 4                | —                       | PC15         | IRQ15              | —   | GTETRGB/GTIOC3B/GTCCPO1/GTADSM1/GTCCPO7/AGTIO1 | ADTRG1/CMPOUT3              |
| 10      | —                | —                | VSS                     | —            | —                  | —   | —  | —                           |
| 11      | —                | —                | VCC                     | —            | —                  | —   | —  | —                           |
| 12      | 5                | 5                | EXTAL                   | P212         | —                  | —   | —  | —                           |
| 13      | 6                | 6                | XTAL                    | P213         | IRQ0               | —   | —  | —                           |
| 14      | 7                | 7                | RES                     | —            | —                  | —   | —  | —                           |
| 15      | 8                | —                | —                       | PC00         | IRQ11-DS           | —   | —  | AN012/PGAOUT0/IVCMP00       |
| 16      | 9                | —                | —                       | PC01         | IRQ12-DS           | —   | —  | AN013/PGAOUT1/IVCMP10       |
| 17      | 10               | —                | —                       | PC02         | IRQ13-DS           | —   | —  | AN014/PGAOUT2/IVCMP20       |
| 18      | 11               | —                | —                       | PC03         | IRQ14-DS           | —   | —  | AN015/PGAOUT3/IVCMP30       |
| 19      | —                | —                | —                       | P000         | IRQ0               | —   | —  | AN016/IVREF0                |
| 20      | 12               | 8                | VREFL0                  | —            | —                  | —   | —  | —                           |
| 21      | 13               | 9                | VREFH0                  | —            | —                  | —   | —  | —                           |
| 22      | —                | —                | —                       | P001         | IRQ2               | —   | —  | AN017/IVREF1                |
| 23      | 14               | 10               | —                       | PA00         | IRQ0-DS            | —   | —  | AN000/PAIN0/IVCMP02/IVCMP03 |
| 24      | 15               | 11               | —                       | PA01         | IRQ1               | —   | —  | AN001/PAGVSS0               |
| 25      | 16               | 12               | —                       | PA02         | IRQ2               | —   | —  | AN002/PAIN1/IVCMP12/IVCMP13 |
| 26      | 17               | 13               | —                       | PA03         | IRQ3               | —   | —  | AN003/PAGVSS1               |
| 27      | 18               | 14               | AVSS0                   | —            | —                  | —   | —  | —                           |
| 28      | 19               | 15               | AVCC0                   | —            | —                  | —   | —  | —                           |
| 29      | 20               | 16               | —                       | PA04         | IRQ4               | —   | —  | AN004/PAIN2/IVCMP22/IVCMP23 |
| 30      | 21               | 17               | —                       | PA05         | IRQ5               | —   | —  | AN005/PAGVSS2               |
| 31      | 22               | 18               | —                       | PA06         | IRQ6               | —   | —  | AN006/DA0                   |
| 32      | 23               | 19               | —                       | PA07         | IRQ7               | —   | —  | AN007/DA1                   |
| 33      | 24               | —                | —                       | PC04         | IRQ10              | —   | —  | AN010/DA2                   |
| 34      | 25               | —                | —                       | PC05         | IRQ11              | —   | —  | AN011/DA3                   |
| 35      | 26               | 20               | —                       | PB00         | IRQ0               | —   | —  | AN008/PGAOUT0/PGAOUT2       |
| 36      | 27               | 21               | —                       | PB01         | IRQ1               | —   | —  | AN009/PGAOUT1/PGAOUT3       |
| 37      | 28               | —                | —                       | PB02         | IRQ15-DS           | —   | —  | AN018/PAIN3/IVCMP32/IVCMP33 |
| 38      | 29               | —                | —                       | P002         | —                  | —   | —  | AN019/PAGVSS3               |
| 39      | —                | —                | —                       | PE08         | KR00               | SSLA3_C   | GTIV/GTIOC3A/GTETRGC/GTADSM0                   | AN020/ADTRG0/CMPOUT012      |
| 40      | —                | —                | CACREF                  | PE09         | KR01               | SSLA2_C   | GTIW/GTIOC3B/GTETRGD/GTADSM1                   | AN021/ADTRG1/CMPOUT3        |
| 41      | —                | —                | —                       | PE10         | KR02               | SSLA1_C   | GTOULO/GTIOC2A/GTIOC4A/GTIOC7A                 | AN022                       |

Table 1.14 Pin list (2 of 3)

| LOFP100 | LOFP64 | LOFP48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                                      | GPT/AGT                                       | ADC/DAC12/ACMPHS |
|---------|--------|--------|----------------------------------|-----------|--------------------|--|---|------------------|
| 42      | —      | —      | —                                | PE11      | KR03               | SSLA0_C  | GTOUUP/GTIOC2B/GTIOC5A/GTIOC8A                | AN023            |
| 43      | —      | —      | —                                | PE12      | KR04               | RSPCKA_C   | GTOVLO/GTIOC1A/GTIOC6A/GTIOC9A                | AN024            |
| 44      | —      | —      | —                                | PE13      | KR05               | MISOA_C  | GTOVUP/GTIOC1B/GTIOC4B/GTIOC7B                | AN025            |
| 45      | —      | —      | —                                | PE14      | KR06               | MOSIA_C  | GTOWLO/GTIOC0A/GTIOC5B/GTIOC8B                | AN026            |
| 46      | —      | —      | —                                | PE15      | KR07               | RXD4_A/MISO4_A/SCL4                                    | GTOWUP/GTIOC0B/GTIOC6B/GTIOC9B                | AN027            |
| 47      | —      | —      | CACREF/VCOUT                     | PB10      | IRQ10-DS           | TXD4_A/MISO4_A/SDA4/CTS3_B                             | GTIU/GTETRGA/GTETRGB/GTCPPO4/GTCPPO7          | AN028            |
| 48      | 30     | 22     | VCL                              | —         | —                  | —  | —   | —                |
| 49      | 31     | 23     | VSS                              | —         | —                  | —  | —   | —                |
| 50      | 32     | 24     | VCC                              | —         | —                  | —  | —   | —                |
| 51      | 33     | 25     | —                                | PB12      | IRQ2               | SCK4_A/DE4/RXD3_B/MISO3_B/SCL3/SSLB0_A/CRX0            | GTETRGA/GTIOC0A/GTIOC4A                       | ADTRG0           |
| 52      | 34     | 26     | —                                | PB13      | IRQ3               | CTS4_A/TXD3_B/MOSI3_B/SDA3/RSPCKB_A/CTX0               | GTOULO/GTIOC0B/GTIOC7A/GTIOC5A                | —                |
| 53      | 35     | 27     | —                                | PB14      | IRQ4               | CTS4_RTS4/SS4_A/DE4/SCK3_B/DE3/SDA0_C/MISOB_A          | GTOVLO/GTIOC1A/GTIOC8A/GTIOC6A                | —                |
| 54      | 36     | 28     | —                                | PB15      | IRQ5               | RXD4_A/MISO4_A/SCL4/CTS3_RTS3/SS3_B/DE3/SCL0_C/MOSIB_A | GTOWLO/GTIOC1B/GTIOC9A/GTIOC4B                | —                |
| 55      | —      | —      | —                                | PD08      | KR00               | CTS2_B/TXD1_A/MOSI1_A/SDA1/SSLB1_A                     | GTIOC2A                                       | —                |
| 56      | —      | —      | —                                | PD09      | KR01               | CTS2_RTS2/SS2_B/DE2/RXD1_A/MISO1_A/SCL1/SSLB2_A        | GTIOC2B                                       | —                |
| 57      | —      | —      | —                                | PD10      | KR02               | SCK2_C/DE2/SCK1_A/DE1/SSLB3_A                          | GTETRGC/GTIOC3A                               | —                |
| 58      | —      | —      | —                                | PD11      | KR03               | RXD2_C/MOSI2_C/SCL2/CTS1_A                             | GTIOC3B                                       | —                |
| 59      | —      | —      | —                                | PD12      | IRQ12/KR04         | TXD2_C/MOSI2_C/SDA2/CTS1_RTS1/SS1_A/DE1/SCL1_D         | GTIOC4A                                       | —                |
| 60      | —      | —      | —                                | PD13      | IRQ13/KR05         | SCK4_C/DE4/SCK9_C/DE9/SDA1_D                           | GTIOC4B                                       | —                |
| 61      | —      | —      | —                                | PD14      | IRQ14/KR06         | RXD4_C/MISO4_C/SCL4/RXD9_C/MISO9_C/SCL9/SCL0_F         | GTIOC5A                                       | —                |
| 62      | —      | —      | —                                | PD15      | IRQ15/KR07         | TXD4_C/MISO4_C/SDA4/TXD9_C/MOSI9_C/SDA9/DE9/SDA0_F     | GTIOC5B                                       | —                |
| 63      | 37     | —      | —                                | PC06      | IRQ6               | TXD2_B/MOSI2_B/SDA2/CTS9_RTS9/SS9_C/DE9/SCL1_E         | GTETRGD/GTIOC6A/GTIOC5B/AGTO0                 | —                |
| 64      | 38     | —      | —                                | PC07      | IRQ7               | RXD2_B/MOSI2_B/SCL2/CTS9_C/SDA1_E                      | GTETRGA/GTIOC6B/AGTEE0                        | —                |
| 65      | 39     | —      | CACREF                           | PC08      | IRQ8               | SCK2_B/DE2/CTS3_RTS3/SS3_C/DE3/SCL0_E/SSLA3_B          | GTIV/GTIOC7A/AGTOA0                           | —                |
| 66      | 40     | —      | CLKOUT                           | PC09      | IRQ9               | CTS2_RTS2/SS2_B/DE2/CTS3_C/SDA0_D/SDA0_E/SSLA2_B       | GTIW/GTIOC7B/GTIOC8A/AGTOB0                   | —                |
| 67      | 41     | 29     | CLKOUT                           | PA08      | IRQ8/KR00          | SCK0_A/DE0/SCK1_C/DE1/SCL0_D/SSLA1_B                   | GTOUUP/GTIOC8A/GTIOC7B/GTIOC2A/GTIOC9A/AGTIO0 | CMPOUT2          |
| 68      | 42     | 30     | —                                | PA09      | IRQ9/KR01          | TXD0_A/MOSI0_A/SDA0/SCL1_C/SSLA0_B                     | GTOVUP/GTIOC8B/GTIOC8B/GTIOC2B/GTIOC7B        | CMPOUT3          |
| 69      | 43     | 31     | —                                | PA10      | IRQ10/KR02         | RXD0_A/MISO0_A/SCL0/SDA1_C/RSPCKA_B                    | GTOWUP/GTIOC9A/GTIOC9B/GTIOC3A/GTIOC8B        | CMPOUT0          |
| 70      | 44     | 32     | —                                | PA11      | IRQ11/KR03         | CTS0_A/RXD1_C/MISO1_C/SCL1/MOSIA_B/CTX0                | GTETRGD/GTIOC9B/GTETRGC/GTIOC3B               | CMPOUT1          |
| 71      | 45     | 33     | CACREF                           | PA12      | IRQ12/KR04         | CTS0_RTS0/SS0_A/DE0/TXD1_C/MOSI1_C/SDA1/MISOA_B/CRX0   | GTETRGB/GTCPPO0/GTCPPO2/GTADSM0/GTCPPO7       | ADTRG1           |
| 72      | 46     | 34     | TMS/SWDIO                        | PA13      | —                  | SCK0_C/DE0/CTS1_RTS1/SS1_C/DE1                         | AGTO0   | —                |
| 73      | —      | —      | VCL                              | —         | —                  | —  | —   | —                |
| 74      | 47     | 35     | VSS                              | —         | —                  | —  | —   | —                |
| 75      | 48     | 36     | VCC                              | —         | —                  | —  | —   | —                |
| 76      | 49     | 37     | TCK/SWCLK                        | PA14      | —                  | TXD0_C/MOSI0_C/SDA0/SCK9_B/DE9                         | AGTO1   | —                |
| 77      | 50     | 38     | TDI                              | PA15      | IRQ1/KR02          | RXD0_C/MISO0_C/SCL0/RXD9_B/MISO9_B/SCL9/SSLA0_A        | GTETRGB/GTADSM1/GTCPPO4                       | ADTRG0/CMPOUT012 |
| 78      | 51     | —      | —                                | PC10      | IRQ6-DS/KR05       | TXD1_B/MOSI1_B/SDA1/SCL0_B/RSPCKB_B                    | AGTIO1  | CMPOUT0          |

Table 1.14 引脚列表 (2个, 共3个)

| LOFP100 | LOFP64 | LOFP48 | 电源、系统、时钟、调试、CAC | I/O ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                                      | GPT/AGT                                       | ADC/DAC12/ACMPHS |
|---------|--------|--------|-----------------|-----------|--------------------|--|---|------------------|
| 42      | —      | —      | —               | PE11      | KR03               | SSLA0_C  | GTOUUP/GTIOC2B/GTIOC5A/GTIOC8A                | AN023            |
| 43      | —      | —      | —               | PE12      | KR04               | RSPCKA_C   | GTOVLO/GTIOC1A/GTIOC6A/GTIOC9A                | AN024            |
| 44      | —      | —      | —               | PE13      | KR05               | MISOA_C  | GTOVUP/GTIOC1B/GTIOC4B/GTIOC7B                | AN025            |
| 45      | —      | —      | —               | PE14      | KR06               | MOSIA_C  | GTOWLO/GTIOC0A/GTIOC5B/GTIOC8B                | AN026            |
| 46      | —      | —      | —               | PE15      | KR07               | RXD4_A/MISO4_A/SCL4                                    | GTOWUP/GTIOC0B/GTIOC6B/GTIOC9B                | AN027            |
| 47      | —      | —      | CACREF/VCOUT    | PB10      | IRQ10-DS           | TXD4_A/MISO4_A/SDA4/CTS3_B                             | GTIU/GTETRGA/GTETRGB/GTCPPO4/GTCPPO7          | AN028            |
| 48      | 30     | 22     | VCL             | —         | —                  | —  | —   | —                |
| 49      | 31     | 23     | VSS             | —         | —                  | —  | —   | —                |
| 50      | 32     | 24     | VCC             | —         | —                  | —  | —   | —                |
| 51      | 33     | 25     | —               | PB12      | IRQ2               | SCK4_A/DE4/RXD3_B/MISO3_B/SCL3/SSLB0_A/CRX0            | GTETRGA/GTIOC0A/GTIOC4A                       | ADTRG0           |
| 52      | 34     | 26     | —               | PB13      | IRQ3               | CTS4_A/TXD3_B/MOSI3_B/SDA3/RSPCKB_A/CTX0               | GTOULO/GTIOC0B/GTIOC7A/GTIOC5A                | —                |
| 53      | 35     | 27     | —               | PB14      | IRQ4               | CTS4_RTS4/SS4_A/DE4/SCK3_B/DE3/SDA0_C/MISOB_A          | GTOVLO/GTIOC1A/GTIOC8A/GTIOC6A                | —                |
| 54      | 36     | 28     | —               | PB15      | IRQ5               | RXD4_A/MISO4_A/SCL4/CTS3_RTS3/SS3_B/DE3/SCL0_C/MOSIB_A | GTOWLO/GTIOC1B/GTIOC9A/GTIOC4B                | —                |
| 55      | —      | —      | —               | PD08      | KR00               | CTS2_B/TXD1_A/MOSI1_A/SDA1/SSLB1_A                     | GTIOC2A                                       | —                |
| 56      | —      | —      | —               | PD09      | KR01               | CTS2_RTS2/SS2_B/DE2/RXD1_A/MISO1_A/SCL1/SSLB2_A        | GTIOC2B                                       | —                |
| 57      | —      | —      | —               | PD10      | KR02               | SCK2_C/DE2/SCK1_A/DE1/SSLB3_A                          | GTETRGC/GTIOC3A                               | —                |
| 58      | —      | —      | —               | PD11      | KR03               | RXD2_C/MOSI2_C/SCL2/CTS1_A                             | GTIOC3B                                       | —                |
| 59      | —      | —      | —               | PD12      | IRQ12/KR04         | TXD2_C/MOSI2_C/SDA2/CTS1_RTS1/SS1_A/DE1/SCL1_D         | GTIOC4A                                       | —                |
| 60      | —      | —      | —               | PD13      | IRQ13/KR05         | SCK4_C/DE4/SCK9_C/DE9/SDA1_D                           | GTIOC4B                                       | —                |
| 61      | —      | —      | —               | PD14      | IRQ14/KR06         | RXD4_C/MISO4_C/SCL4/RXD9_C/MISO9_C/SCL9/SCL0_F         | GTIOC5A                                       | —                |
| 62      | —      | —      | —               | PD15      | IRQ15/KR07         | TXD4_C/MISO4_C/SDA4/TXD9_C/MOSI9_C/SDA9/DE9/SDA0_F     | GTIOC5B                                       | —                |
| 63      | 37     | —      | —               | PC06      | IRQ6               | TXD2_B/MOSI2_B/SDA2/CTS9_RTS9/SS9_C/DE9/SCL1_E         | GTETRGD/GTIOC6A/GTIOC5B/AGTO0                 | —                |
| 64      | 38     | —      | —               | PC07      | IRQ7               | RXD2_B/MOSI2_B/SCL2/CTS9_C/SDA1_E                      | GTETRGA/GTIOC6B/AGTEE0                        | —                |
| 65      | 39     | —      | CACREF          | PC08      | IRQ8               | SCK2_B/DE2/CTS3_RTS3/SS3_C/DE3/SCL0_E/SSLA3_B          | GTIV/GTIOC7A/AGTOA0                           | —                |
| 66      | 40     | —      | CLKOUT          | PC09      | IRQ9               | CTS2_RTS2/SS2_B/DE2/CTS3_C/SDA0_D/SDA0_E/SSLA2_B       | GTIW/GTIOC7B/GTIOC8A/AGTOB0                   | —                |
| 67      | 41     | 29     | CLKOUT          | PA08      | IRQ8/KR00          | SCK0_A/DE0/SCK1_C/DE1/SCL0_D/SSLA1_B                   | GTOUUP/GTIOC8A/GTIOC7B/GTIOC2A/GTIOC9A/AGTIO0 | CMPOUT2          |
| 68      | 42     | 30     | —               | PA09      | IRQ9/KR01          | TXD0_A/MOSI0_A/SDA0/SCL1_C/SSLA0_B                     | GTOVUP/GTIOC8B/GTIOC8B/GTIOC2B/GTIOC7B        | CMPOUT3          |
| 69      | 43     | 31     | —               | PA10      | IRQ10/KR02         | RXD0_A/MISO0_A/SCL0/SDA1_C/RSPCKA_B                    | GTOWUP/GTIOC9A/GTIOC9B/GTIOC3A/GTIOC8B        | CMPOUT0          |
| 70      | 44     | 32     | —               | PA11      | IRQ11/KR03         | CTS0_A/RXD1_C/MISO1_C/SCL1/MOSIA_B/CTX0                | GTETRGD/GTIOC9B/GTETRGC/GTIOC3B               | CMPOUT1          |
| 71      | 45     | 33     | CACREF          | PA12      | IRQ12/KR04         | CTS0_RTS0/SS0_A/DE0/TXD1_C/MOSI1_C/SDA1/MISOA_B/CRX0   | GTETRGB/GTCPPO0/GTCPPO2/GTADSM0/GTCPPO7       | ADTRG1           |
| 72      | 46     | 34     | TMS/SWDIO       | PA13      | —                  | SCK0_C/DE0/CTS1_RTS1/SS1_C/DE1                         | AGTO0   | —                |
| 73      | —      | —      | VCL             | —         | —                  | —  | —   | —                |
| 74      | 47     | 35     | VSS             | —         | —                  | —  | —   | —                |
| 75      | 48     | 36     | VCC             | —         | —                  | —  | —   | —                |
| 76      | 49     | 37     | TCK/SWCLK       | PA14      | —                  | TXD0_C/MOSI0_C/SDA0/SCK9_B/DE9                         | AGTO1   | —                |
| 77      | 50     | 38     | TDI             | PA15      | IRQ1/KR02          | RXD0_C/MISO0_C/SCL0/RXD9_B/MISO9_B/SCL9/SSLA0_A        | GTETRGB/GTADSM1/GTCPPO4                       | ADTRG0/CMPOUT012 |
| 78      | 51     | —      | —               | PC10      | IRQ6-DS/KR05       | TXD1_B/MOSI1_B/SDA1/SCL0_B/RSPCKB_B                    | AGTIO1  | CMPOUT0          |

Table 1.14 Pin list (3 of 3)

| LOFP100 | LOFP64, QFN64 | LOFP48, QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                                     | GPT/AGT                               | ADC/DAC12/ACMPHS |
|---------|---------------|---------------|----------------------------------|-----------|--------------------|---|---------------------------------------|------------------|
| 79      | 52            | —             | —                                | PC11      | IRQ7-DS/KR06       | RXD1_B/MISO1_B/SCL1/SDA0_B/MISOB_B                    | AGTOA1                                | CMPOUT1          |
| 80      | 53            | —             | —                                | PC12      | IRQ8-DS/KR07       | TXD4_B/MOSI4_B/SDA4/SCK1_B/DE1/MOSIB_B                | AGTOB1                                | CMPOUT2          |
| 81      | —             | —             | —                                | PD00      | KR00               | CTS2_A/RXD3_C/MISO3_C/SCL3/SSLB0_B/CRX0               | GTADSM0/GTCPPO4                       | —                |
| 82      | —             | —             | —                                | PD01      | KR01               | CTS2_RTS2/SS2_A/DE2/TXD3_C/MOSI3_C/SDA3/SSLB1_B/CTX0  | GTADSM1/GTCPPO7                       | —                |
| 83      | 54            | —             | CLKOUT                           | PD02      | IRQ9-DS/KR02       | RXD4_B/MISO4_B/SCL4/SCK3_C/DE3                        | GTCPP00/GTCPPO2/AGTEE1                | CMPOUT3          |
| 84      | —             | —             | —                                | PD03      | KR03               | SCK4_B/DE4/CTS9_A/SSLB2_B                             | GTCPP00                               | CMPOUT0          |
| 85      | —             | —             | —                                | PD04      | KR04               | CTS4_RTS4/SS4_B/DE4/CTS9_RTS9/SS9_A/DE9/SSLB3_B       | GTCPP01                               | CMPOUT1          |
| 86      | —             | —             | —                                | PD05      | KR05               | TXD9_A/MOSI9_A/SDA9/SDA1_B/SSLA3_A                    | GTADSM0/GTCPPO3                       | —                |
| 87      | —             | —             | —                                | PD06      | KR06               | RXD9_A/MOSI9_A/SCL9/SCL1_B/SSLA2_A                    | GTCPP04                               | —                |
| 88      | —             | —             | —                                | PD07      | KR07               | SCK9_A/DE9/SSLA1_A                                    | GTADSM1/GTCPPO7                       | —                |
| 89      | 55            | 39            | TDO/SWO                          | PB03      | IRQ0/KR03          | TXD2_A/MOSI2_A/SDA2/TXD9_B/MOSI9_B/SDA9/RSPCKA_A/CRX0 | GTIOC4A/GTCPPO1/GTCPPO3/AGTO1         | ADTRG1/CMPOUT3   |
| 90      | 56            | 40            | CACREF/VCOUT                     | PB04      | IRQ13/KR04         | RXD2_A/MISO2_A/SCL2/RXD3_D/MISO3_D/SCL3/MISOA_A/CTX0  | GTIOC4A/GTI0C5A/GTI0C0A/AGTOA0        | —                |
| 91      | 57            | 41            | —                                | PB05      | IRQ3-DS/KR05       | SCK2_A/DE2/TXD3_D/MOSI3_D/SDA3/MOSIA_A/CRX0           | GTIU/GTI0C4B/GTI0C6A/GTI0C0B/AGTOB0   | —                |
| 92      | 58            | 42            | —                                | PB06      | IRQ4-DS/KR06       | TXD0_D/MOSI0_D/SDA0/CTS3_RTS3/SS3_D/DE3/SCL0_A/CTX0   | GTIV/GTI0C5A/GTI0C4B/GTI0C1A/AGTOA1   | —                |
| 93      | 59            | 43            | —                                | PB07      | IRQ5-DS/KR07       | RXD0_D/MISO0_D/SCL0/CTS1_RTS1/SS1_D/DE1/SDA0_A        | GTIW/GTI0C5B/GTETRCG/GTI0C1B/AGTOB1   | —                |
| 94      | 60            | 44            | MD                               | P201      | —                  | —   | —                                     | —                |
| 95      | 61            | 45            | —                                | PB08      | IRQ1-DS/KR00       | RXD4/MISO4_C/SCL4/RXD1_D/MISO1_D/SCL1/SCL1_A/CRX0     | GTIOC6A/GTI0C5B/GTI0C2A/AGTIO0        | —                |
| 96      | 62            | 46            | —                                | PB09      | IRQ2-DS/KR01       | TXD4/MOSI4_C/SDA4/TXD1_D/MOSI1_D/SDA1/SDA1_A/CTX0     | GTIOC6B/GTI0C2B/AGTIO1                | —                |
| 97      | —             | —             | CACREF                           | PE00      | —                  | TXD0_E/MOSI0_E/SDA0/TXD9_D/MOSI9_D/SDA9/SSLB3_C       | GTETRGA/GTI0C4A/GTADSM0/AGTEE0        | ADTRG0           |
| 98      | —             | —             | —                                | PE01      | —                  | RXD0_E/MISO0_E/SCL0/RXD9_D/MISO9_D/SCL9/SSLB2_C       | GTOULO/GTI0C7A/GTI0C4B/GTADSM1/AGTEE1 | ADTRG1           |
| 99      | 63            | 47            | VSS                              | —         | —                  | —   | —                                     | —                |
| 100     | 64            | 48            | VCC                              | —         | —                  | —   | —                                     | —                |

Note: Several pin names have the added suffix of \_A, \_B, \_C, \_D, \_E and \_F. The suffix can be ignored when assigning functionality.

Table 1.14 引脚列表 (3个中的3个)

| LOFP100 | LOFP64, QFN64 | LOFP48, QFN48 | 电源、系统、时钟、调试、CAC | I/O ports | Ex. Interrupt/KINT | SCI/IIC/SPI/CANFD                                     | GPT/AGT                               | ADC/DAC12/ACMPHS |
|---------|---------------|---------------|-----------------|-----------|--------------------|---|---------------------------------------|------------------|
| 79      | 52            | —             | —               | PC11      | IRQ7-DS/KR06       | RXD1_B/MISO1_B/SCL1/SDA0_B/MISOB_B                    | AGTOA1                                | CMPOUT1          |
| 80      | 53            | —             | —               | PC12      | IRQ8-DS/KR07       | TXD4_B/MOSI4_B/SDA4/SCK1_B/DE1/MOSIB_B                | AGTOB1                                | CMPOUT2          |
| 81      | —             | —             | —               | PD00      | KR00               | CTS2_A/RXD3_C/MISO3_C/SCL3/SSLB0_B/CRX0               | GTADSM0/GTCPPO4                       | —                |
| 82      | —             | —             | —               | PD01      | KR01               | CTS2_RTS2/SS2_A/DE2/TXD3_C/MOSI3_C/SDA3/SSLB1_B/CTX0  | GTADSM1/GTCPPO7                       | —                |
| 83      | 54            | —             | CLKOUT          | PD02      | IRQ9-DS/KR02       | RXD4_B/MISO4_B/SCL4/SCK3_C/DE3                        | GTCPP00/GTCPPO2/AGTEE1                | CMPOUT3          |
| 84      | —             | —             | —               | PD03      | KR03               | SCK4_B/DE4/CTS9_A/SSLB2_B                             | GTCPP00                               | CMPOUT0          |
| 85      | —             | —             | —               | PD04      | KR04               | CTS4_RTS4/SS4_B/DE4/CTS9_RTS9/SS9_A/DE9/SSLB3_B       | GTCPP01                               | CMPOUT1          |
| 86      | —             | —             | —               | PD05      | KR05               | TXD9_A/MOSI9_A/SDA9/SDA1_B/SSLA3_A                    | GTADSM0/GTCPPO3                       | —                |
| 87      | —             | —             | —               | PD06      | KR06               | RXD9_A/MOSI9_A/SCL9/SCL1_B/SSLA2_A                    | GTCPP04                               | —                |
| 88      | —             | —             | —               | PD07      | KR07               | SCK9_A/DE9/SSLA1_A                                    | GTADSM1/GTCPPO7                       | —                |
| 89      | 55            | 39            | TDO/SWO         | PB03      | IRQ0/KR03          | TXD2_A/MOSI2_A/SDA2/TXD9_B/MOSI9_B/SDA9/RSPCKA_A/CRX0 | GTIOC4A/GTCPPO1/GTCPPO3/AGTO1         | ADTRG1/CMPOUT3   |
| 90      | 56            | 40            | CACREF/VCOUT    | PB04      | IRQ13/KR04         | RXD2_A/MISO2_A/SCL2/RXD3_D/MISO3_D/SCL3/MISOA_A/CTX0  | GTIOC4A/GTI0C5A/GTI0C0A/AGTOA0        | —                |
| 91      | 57            | 41            | —               | PB05      | IRQ3-DS/KR05       | SCK2_A/DE2/TXD3_D/MOSI3_D/SDA3/MOSIA_A/CRX0           | GTIU/GTI0C4B/GTI0C6A/GTI0C0B/AGTOB0   | —                |
| 92      | 58            | 42            | —               | PB06      | IRQ4-DS/KR06       | TXD0_D/MOSI0_D/SDA0/CTS3_RTS3/SS3_D/DE3/SCL0_A/CTX0   | GTIV/GTI0C5A/GTI0C4B/GTI0C1A/AGTOA1   | —                |
| 93      | 59            | 43            | —               | PB07      | IRQ5-DS/KR07       | RXD0_D/MISO0_D/SCL0/CTS1_RTS1/SS1_D/DE1/SDA0_A        | GTIW/GTI0C5B/GTETRCG/GTI0C1B/AGTOB1   | —                |
| 94      | 60            | 44            | MD              | P201      | —                  | —   | —                                     | —                |
| 95      | 61            | 45            | —               | PB08      | IRQ1-DS/KR00       | RXD4/MISO4_C/SCL4/RXD1_D/MISO1_D/SCL1/SCL1_A/CRX0     | GTIOC6A/GTI0C5B/GTI0C2A/AGTIO0        | —                |
| 96      | 62            | 46            | —               | PB09      | IRQ2-DS/KR01       | TXD4/MOSI4_C/SDA4/TXD1_D/MOSI1_D/SDA1/SDA1_A/CTX0     | GTIOC6B/GTI0C2B/AGTIO1                | —                |
| 97      | —             | —             | CACREF          | PE00      | —                  | TXD0_E/MOSI0_E/SDA0/TXD9_D/MOSI9_D/SDA9/SSLB3_C       | GTETRGA/GTI0C4A/GTADSM0/AGTEE0        | ADTRG0           |
| 98      | —             | —             | —               | PE01      | —                  | RXD0_E/MISO0_E/SCL0/RXD9_D/MISO9_D/SCL9/SSLB2_C       | GTOULO/GTI0C7A/GTI0C4B/GTADSM1/AGTEE1 | ADTRG1           |
| 99      | 63            | 47            | VSS             | —         | —                  | —   | —                                     | —                |
| 100     | 64            | 48            | VCC             | —         | —                  | —   | —                                     | —                |

Note: 几个管脚名称添加了\_A、\_B、\_C、\_D、\_E和\_F的后缀。分配功能时可以忽略后缀。

## 2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC = AVCC0 = 2.7$  to  $3.6$  V
- $2.7 \leq VREFH0 \leq AVCC0$
- $VSS = AVSS0 = VREFL0 = 0$  V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

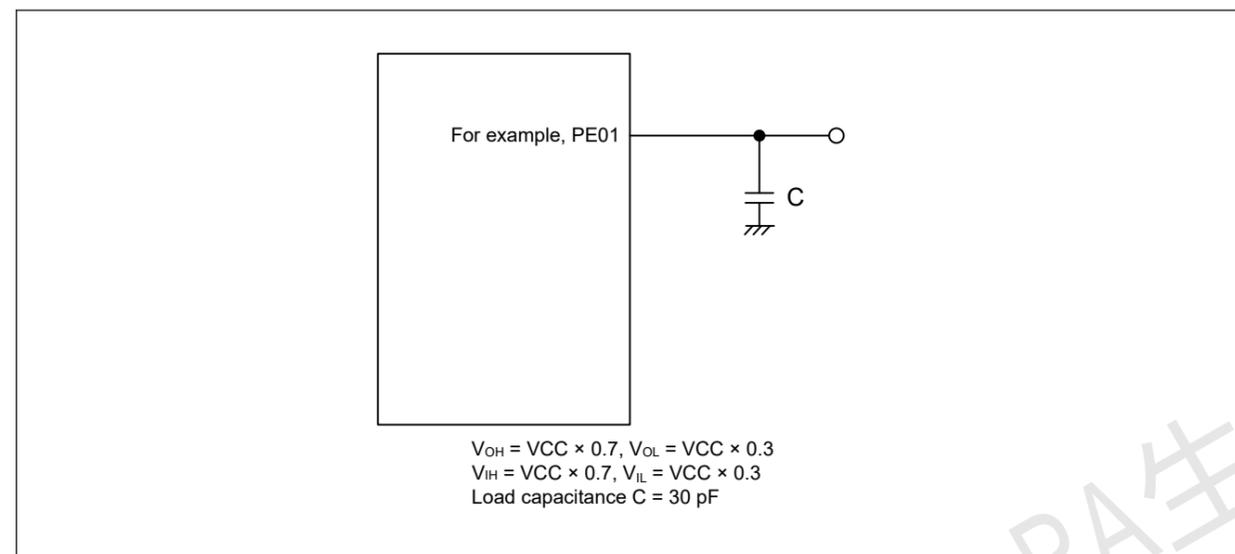


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

### 2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

| Parameter   | Symbol   | Value                          | Unit |
|---|----------|--------------------------------|------|
| Power supply voltage  | VCC      | -0.3 to +4.0                   | V    |
| Input voltage (except for 5 V-tolerant ports*1)   | $V_{in}$ | -0.3 to VCC + 0.3              | V    |
| Input voltage (5 V-tolerant ports*1)  | $V_{in}$ | -0.3 to + VCC + 4.0 (max. 5.8) | V    |
| Reference power supply voltage  | VREFH0   | -0.3 to VCC + 0.3              | V    |
| Analog power supply voltage   | AVCC0*2  | -0.3 to +4.0                   | V    |
| Analog input voltage (except for PA00 to PA05, PB02, P002)                              | $V_{AN}$ | -0.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (PA00 to PA05, PB02, P002) when PGA differential input is disabled | $V_{AN}$ | -0.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (PA00, PA02, PA04, PB02) when PGA differential input is enabled    | $V_{AN}$ | -1.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (PA01, PA03, PA05, P002) when PGA differential input is enabled    | $V_{AN}$ | -0.8 to AVCC0 + 0.3            | V    |

## 2. 电气特性

除非另有说明，否则最小值和最大值由设计模拟、表征结果或生产测试来保证。

支持的外围功能和引脚因产品名称而异。

除非另有规定，MCU的电气特性在以下条件下定义：

- $VCC = AVCC0 = 2.7$  to  $3.6$  V
- $2.7 \leq VREFH0 \leq AVCC0$
- $VSS = AVSS0 = VREFL0 = 0$  V
- $T_a = T_{opr}$

图2.1显示了时序条件。

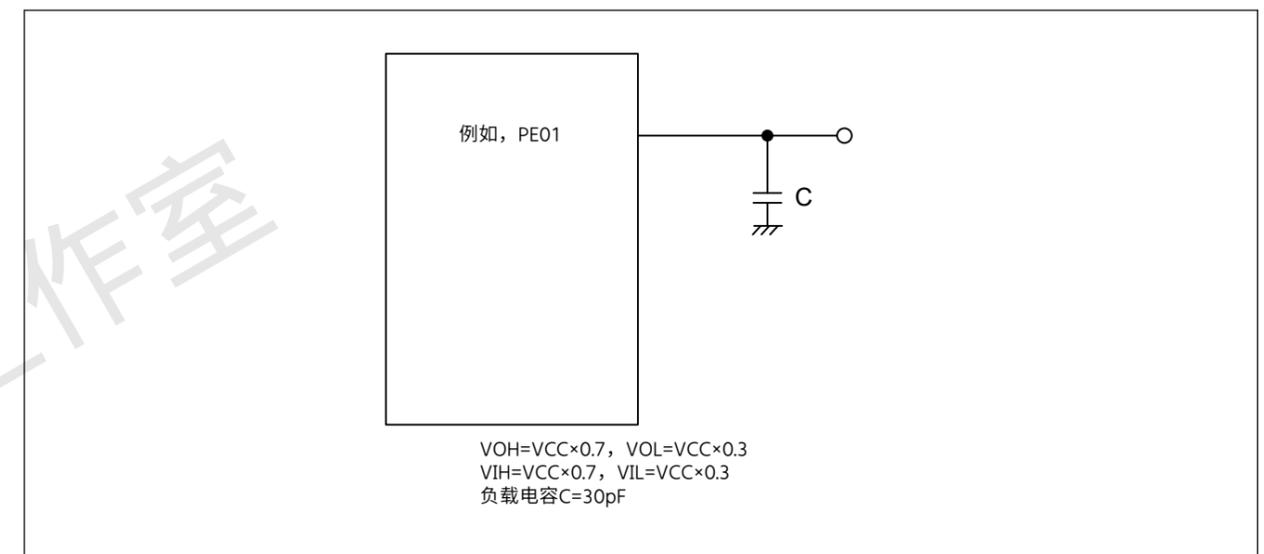


Figure 2.1 输入或输出定时测量条件

所提供的每个外设时序规范的推荐测量条件是为了实现最佳外设操作。确保调整每个引脚的驱动能力以满足您的条件。

### 2.1 绝对最大额定值

Table 2.1 绝对最大额定值(1 of 2)

| Parameter                                 | Symbol   | Value                          | Unit |
|---|----------|--------------------------------|------|
| 电源电压                                      | VCC      | -0.3 to +4.0                   | V    |
| 输入电压 (5V容限端口*1除外)                         | $V_{in}$ | -0.3 to VCC + 0.3              | V    |
| 输入电压 (5V耐压端口*1)                           | $V_{in}$ | -0.3 to + VCC + 4.0 (max. 5.8) | V    |
| 参考电源电压                                    | VREFH0   | -0.3 to VCC + 0.3              | V    |
| 模拟电源电压                                    | AVCC0*2  | -0.3 to +4.0                   | V    |
| 模拟输入电压 (除了PA00到PA05、PB02、P002)            | $V_{AN}$ | -0.3 to AVCC0 + 0.3            | V    |
| 模拟输入电压 (PA00至PA05、PB02、P002) 时 PGA差分输入被禁用 | $V_{AN}$ | -0.3 to AVCC0 + 0.3            | V    |
| PGA差分输入使能时的模拟输入电压 (PA00、PA02、PA04、PB02)   | $V_{AN}$ | -1.3 to AVCC0 + 0.3            | V    |
| PGA差分输入使能时的模拟输入电压 (PA01、PA03、PA05、P002)   | $V_{AN}$ | -0.8 to AVCC0 + 0.3            | V    |

Table 2.1 Absolute maximum ratings (2 of 2)

| Parameter                              | Symbol           | Value       | Unit |
|--|------------------|-------------|------|
| Operating temperature <sup>*3 *4</sup> | T <sub>opr</sub> | -40 to +105 | °C   |
| Storage temperature                    | T <sub>stg</sub> | -55 to +125 | °C   |

Note 1. Ports PA12 to PA15, PB03 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC.

Note 3. See section 2.2.1. Tj/Ta Definition.

Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

**Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.**

Table 2.2 Recommended operating conditions

| Parameter                    | Symbol              | Min | Typ | Max | Unit |
|------------------------------|---------------------|-----|-----|-----|------|
| Power supply voltages        | VCC                 | 2.7 | —   | 3.6 | V    |
|                              | VSS                 | —   | 0   | —   | V    |
| Analog power supply voltages | AVCC0 <sup>*1</sup> | —   | VCC | —   | V    |
|                              | AVSS0               | —   | 0   | —   | V    |

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH0, AVSS0, and VREFL0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

| Parameter                        | Symbol         | Typ | Max | Unit | Test conditions                   |
|----------------------------------|----------------|-----|-----|------|-----------------------------------|
| Permissible junction temperature | T <sub>j</sub> | —   | 125 | °C   | High-speed mode<br>Low-speed mode |

Note: Make sure that  $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$ , where total power consumption =  $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times VCC$ .

Table 2.1 绝对最大额定值(2of2)

| Parameter | Symbol           | Value       | Unit |
|-----------|------------------|-------------|------|
| 工作温度*3*4  | T <sub>opr</sub> | -40 to +105 | °C   |
| 贮存温度      | T <sub>stg</sub> | -55 to +125 | °C   |

注1.端口PA12至PA15、PB03至PB09、PC10至PC12、PC14、PC15、PD00至PD07、PE00和PE01可承受5V。

注2.将AVCC0连接到VCC。

注3: 见第2.2.1节。Tj/Ta定义。

注4.有关在Ta=+85°C至+105°C时降额运行的信息, 请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。

**Caution: 如果超过绝对最大额定值, 可能会对MCU造成永久性损坏。**

Table 2.2 推荐工作条件

| Parameter | Symbol              | Min | Typ | Max | Unit |
|-----------|---------------------|-----|-----|-----|------|
| 电源电压      | VCC                 | 2.7 | —   | 3.6 | V    |
|           | VSS                 | —   | 0   | —   | V    |
| 模拟电源电压    | AVCC0 <sup>*1</sup> | —   | VCC | —   | V    |
|           | AVSS0               | —   | 0   | —   | V    |

注1.将AVCC0连接到VCC。不使用AD转换器和DA转换器时, 请勿将AVCC0、VREFH0、AVSS0和VREFL0引脚悬空。将AVCC0和VREFH0引脚连接到VCC, 将AVSS0和VREFL0引脚分别连接到VSS。

## 2.2 DC Characteristics

### 2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

| Parameter | Symbol         | Typ | Max | Unit | 测试条件                              |
|-----------|----------------|-----|-----|------|-----------------------------------|
| 允许结温      | T <sub>j</sub> | —   | 125 | °C   | High-speed mode<br>Low-speed mode |

Note: 确保 $T_j = T_a + \theta_{ja} \times \text{总功耗(W)}$ , 其中总功耗 =  $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times VCC$ .

2.2.2 I/O  $V_{IH}$ ,  $V_{IL}$ Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$ 

| Parameter   |                         |  | Symbol       | Min               | Typ | Max                      | Unit |
|---|-------------------------|--|--------------|-------------------|-----|--------------------------|------|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL (external clock input), SPI (except RSPCK) | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        | V    |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|   |                         | IIC (SMBus)*1                                    | $V_{IH}$     | 2.1               | —   | —                        |      |
|   |                         |  | $V_{IL}$     | —                 | —   | 0.8                      |      |
|   |                         | IIC (SMBus)*2                                    | $V_{IH}$     | 2.1               | —   | $VCC + 3.6$<br>(max 5.8) |      |
|   |                         |  | $V_{IL}$     | —                 | —   | 0.8                      |      |
| Schmitt trigger input voltage                         | Peripheral function pin | IIC (Except for SMBus)*1                         | $V_{IH}$     | $VCC \times 0.7$  | —   | —                        |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.3$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|   |                         | IIC (Except for SMBus)*2                         | $V_{IH}$     | $VCC \times 0.7$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.3$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|   |                         | 5 V-tolerant ports*3 *7                          | $V_{IH}$     | $VCC \times 0.8$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|   |                         | Other input pins*4                               | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|   | Ports                   | 5 V-tolerant ports*5 *7                          | $V_{IH}$     | $VCC \times 0.8$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|   |                         | Other input pins*6                               | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        |      |
|   |                         |  | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|   |                         |  | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |

Note 1. SCL0\_C, SDA0\_C, SCL0\_D, SDA0\_D, SCL0\_E, SDA0\_E, SCL0\_F, SDA0\_F, SCL1\_C, SDA1\_C, SCL1\_D, SDA1\_D, SCL1\_E, SDA1\_E (total 14 pins). This is the value when IIC function is selected.

Note 2. SCL0\_A, SDA0\_A, SCL0\_B, SDA0\_B, SCL1\_A, SDA1\_A, SCL1\_B, SDA1\_B (total 8 pins). This is the value when IIC function is selected.

Note 3. RES and peripheral function pins associated with PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 26 pins).

Note 4. All input pins except for the peripheral function pins already described in the table.

Note 5. PA12 to PA15, PB03, PB05 to PB09, PC10 to PC12, PC14, PC15, PD00 to PD07, PE00, and PE01 (total 25 pins).

Note 6. All input pins except for the ports already described in the table.

Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

## 2.2.2 I O V I H

Table 2.4 I O V I H

| Parameter           |        |                              | 象征           | Min               | Typ | Max                      | Unit |
|---------------------|--------|------------------------------|--------------|-------------------|-----|--------------------------|------|
| 输入电压 (施密特触发器输入引脚除外) | 外设功能引脚 | EXTAL (外部时钟输入)、SPI (除 RSPCK) | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        | V    |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|                     |        | IIC (SMBus)*1                | $V_{IH}$     | 2.1               | —   | —                        |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | 0.8                      |      |
|                     |        | IIC (SMBus)*2                | $V_{IH}$     | 2.1               | —   | $VCC + 3.6$<br>(max 5.8) |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | 0.8                      |      |
| 施密特触发器输入电压          | 外设功能引脚 | IIC (Except for SMBus)*1     | $V_{IH}$     | $VCC \times 0.7$  | —   | —                        |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.3$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|                     |        | IIC (Except for SMBus)*2     | $V_{IH}$     | $VCC \times 0.7$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.3$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|                     |        | 5 V-tolerant ports*3 *7      | $V_{IH}$     | $VCC \times 0.8$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|                     |        | 其他输入引脚*4                     | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|                     | Ports  | 5 V-tolerant ports*5 *7      | $V_{IH}$     | $VCC \times 0.8$  | —   | $VCC + 3.6$<br>(max 5.8) |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |
|                     |        | 其他输入引脚*6                     | $V_{IH}$     | $VCC \times 0.8$  | —   | —                        |      |
|                     |        |                              | $V_{IL}$     | —                 | —   | $VCC \times 0.2$         |      |
|                     |        |                              | $\Delta V_T$ | $VCC \times 0.05$ | —   | —                        |      |

Note 1. SCL0\_C, SDA0\_C, SCL0\_D, SDA0\_D, SCL0\_E, SDA0\_E, SCL0\_F, SDA0\_F, SCL1\_C, SDA1\_C, SCL1\_D, SDA1\_D, SCL1\_E, SDA1\_E (共14个引脚)。这是选择IIC功能时的值。

注2.SCL0\_A、SDA0\_A、SCL0\_B、SDA0\_B、SCL1\_A、SDA1\_A、SCL1\_B、SDA1\_B (共8个引脚)。这是选择IIC功能时的值。

注3.与PA12至PA15、PB03、PB05至PB09、PC10至PC12、PC14、PC15、PD00至PD07相关的RES和外围功能引脚，PE00, and PE01 (total 26 pins)。

注4.除表中已描述的外围功能引脚外的所有输入引脚。

注5.PA12~PA15、PB03、PB05~PB09、PC10~PC12、PC14、PC15、PD00~PD07、PE00、PE01 (共25个引脚)。

注6.除表中已描述的端口外的所有输入引脚。

注7.当VCC小于2.7V时，5V容限端口的输入电压应小于3.6V，否则可能发生击穿，因为5V容限端口是电控的，不会违反击穿电压。

2.2.3 I/O I<sub>OH</sub>, I<sub>OL</sub>Table 2.5 I/O I<sub>OH</sub>, I<sub>OL</sub>

| Parameter  |   | Symbol   | Min                        | Typ                    | Max             | Unit |     |     |    |
|--|---|--|----------------------------|------------------------|-----------------|------|-----|-----|----|
| Permissible output current (average value per pin) | IIC pins  | Standard mode*1                                | I <sub>OL</sub>            | —                      | —               | 3.0  | mA  |     |    |
|  |   | Fast mode*1                                    | I <sub>OL</sub>            | —                      | —               | 6.0  | mA  |     |    |
|  |   | Fast mode plus*2                               | I <sub>OL</sub>            | —                      | —               | 20   | mA  |     |    |
|  |   | High speed mode*2                              | I <sub>OL</sub>            | —                      | —               | 3.0  | mA  |     |    |
|  | Other output pins*3   | Low drive*4                                    | I <sub>OH</sub>            | —                      | —               | -2.0 | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 2.0  | mA  |     |    |
|  |   | Middle drive*5                                 | I <sub>OH</sub>            | —                      | —               | -4.0 | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 4.0  | mA  |     |    |
|  |   | High drive*6                                   | I <sub>OH</sub>            | —                      | —               | -10  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 10   | mA  |     |    |
|  |   | High speed high drive*7                        | I <sub>OH</sub>            | —                      | —               | -10  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 10   | mA  |     |    |
|  |   | High current drive*8                           | I <sub>OH</sub>            | —                      | —               | -10  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 20   | mA  |     |    |
|  |   | Permissible output current (max value per pin) | IIC pins                   | Standard mode*1        | I <sub>OL</sub> | —    | —   | 3.0 | mA |
|  |   |  |                            | Fast mode*1            | I <sub>OL</sub> | —    | —   | 6.0 | mA |
| Fast mode plus*2                                   | I <sub>OL</sub>   |  |                            | —                      | —               | 20   | mA  |     |    |
| High speed mode*2                                  | I <sub>OL</sub>   |  |                            | —                      | —               | 3.0  | mA  |     |    |
| Other output pins*3                                | Low drive*4   |  | I <sub>OH</sub>            | —                      | —               | -2.0 | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 2.0  | mA  |     |    |
|  | Middle drive*5  |  | I <sub>OH</sub>            | —                      | —               | -4.0 | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 4.0  | mA  |     |    |
|  | High drive*6  |  | I <sub>OH</sub>            | —                      | —               | -16  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 16   | mA  |     |    |
|  | High speed high drive*7                                     |  | I <sub>OH</sub>            | —                      | —               | -16  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 16   | mA  |     |    |
|  | High current drive*8  |  | I <sub>OH</sub>            | —                      | —               | -16  | mA  |     |    |
|  |   |  | I <sub>OL</sub>            | —                      | —               | 20   | mA  |     |    |
|  | Permissible output current (max value of total of all pins) |  | Maximum of all output pins | ΣI <sub>OH</sub> (max) | —               | —    | -80 | mA  |    |
|  |   |  |                            | ΣI <sub>OL</sub> (max) | —               | —    | 80  | mA  |    |

Note 1. SCL0\_A, SDA0\_A, SCL1\_A, SDA1\_A (total 4 pins). This is the value when IIC function is selected.

Note 2. SCL0\_A, SDA0\_A (total 2 pins). This is the value when IIC function is selected.

Note 3. Except for P000 to P002, PA00 to PA07, PB00 to PB02, PC00 to PC05, PC13, which are input ports.

Note 4. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 5. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 6. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

## 2.2.3 我爱我哦

Table 2.5 我爱我哦

| Parameter         |                     | Symbol            | Min             | Typ                    | Max             | Unit |     |     |    |
|-------------------|---------------------|-------------------|-----------------|------------------------|-----------------|------|-----|-----|----|
| 允许输出电流 (每个引脚的平均值) | IIC pins            | 标准模式*1            | I <sub>OL</sub> | —                      | —               | 3.0  | mA  |     |    |
|                   |                     | 快速模式*1            | I <sub>OL</sub> | —                      | —               | 6.0  | mA  |     |    |
|                   |                     | 快速模式加*2           | I <sub>OL</sub> | —                      | —               | 20   | mA  |     |    |
|                   |                     | 高速模式*2            | I <sub>OL</sub> | —                      | —               | 3.0  | mA  |     |    |
|                   | 其他输出引脚*3            | 低驱动*4             | I <sub>OH</sub> | —                      | —               | -2.0 | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 2.0  | mA  |     |    |
|                   |                     | 中间驱动器*5           | I <sub>OH</sub> | —                      | —               | -4.0 | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 4.0  | mA  |     |    |
|                   |                     | 高速驱动*6            | I <sub>OH</sub> | —                      | —               | -10  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 10   | mA  |     |    |
|                   |                     | 高速高速*7            | I <sub>OH</sub> | —                      | —               | -10  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 10   | mA  |     |    |
|                   |                     | 大电流驱动*8           | I <sub>OH</sub> | —                      | —               | -10  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 20   | mA  |     |    |
|                   |                     | 允许输出电流 (每个引脚的最大值) | IIC pins        | 标准模式*1                 | I <sub>OL</sub> | —    | —   | 3.0 | mA |
|                   |                     |                   |                 | 快速模式*1                 | I <sub>OL</sub> | —    | —   | 6.0 | mA |
| 快速模式加*2           | I <sub>OL</sub>     |                   |                 | —                      | —               | 20   | mA  |     |    |
| 高速模式*2            | I <sub>OL</sub>     |                   |                 | —                      | —               | 3.0  | mA  |     |    |
| 其他输出引脚*3          | 低驱动*4               |                   | I <sub>OH</sub> | —                      | —               | -2.0 | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 2.0  | mA  |     |    |
|                   | 中间驱动器*5             |                   | I <sub>OH</sub> | —                      | —               | -4.0 | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 4.0  | mA  |     |    |
|                   | 高速驱动*6              |                   | I <sub>OH</sub> | —                      | —               | -16  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 16   | mA  |     |    |
|                   | 高速高速*7              |                   | I <sub>OH</sub> | —                      | —               | -16  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 16   | mA  |     |    |
|                   | 大电流驱动*8             |                   | I <sub>OH</sub> | —                      | —               | -16  | mA  |     |    |
|                   |                     |                   | I <sub>OL</sub> | —                      | —               | 20   | mA  |     |    |
|                   | 允许输出电流 (所有引脚总和的最大值) |                   | 所有输出引脚的最大值      | ΣI <sub>OH</sub> (max) | —               | —    | -80 | mA  |    |
|                   |                     |                   |                 | ΣI <sub>OL</sub> (max) | —               | —    | 80  | mA  |    |

注1.SCL0\_A、SDA0\_A、SCL1\_A、SDA1\_A (共4个引脚)。这是选择IIC功能时的值。

注2.SCL0\_A、SDA0\_A (共2个引脚)。这是选择IIC功能时的值。

注3.P000~P002、PA00~PA07、PB00~PB02、PC00~PC05、PC13为输入端口除外。

注4.这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

注5.这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

注6.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

Note 7. This is the value when high speed high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 8. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

**Caution:** To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100  $\mu$ s.

## 2.2.4 I/O $V_{OH}$ , $V_{OL}$ , and Other Characteristics

Table 2.6 I/O  $V_{OH}$ ,  $V_{OL}$ , and other characteristics

| Parameter  | Symbol   | Min         | Typ        | Max | Unit | Test conditions |  |
|--|--|-------------|------------|-----|------|-----------------|--|
| Output voltage   | IIC <sup>*1</sup>  | $V_{OL}$    | —          | —   | 0.4  | V               | $I_{OL} = 3.0 \text{ mA}$  |
|  |  | $V_{OL}$    | —          | —   | 0.6  |                 | $I_{OL} = 6.0 \text{ mA}$  |
|  | IIC <sup>*2</sup>  | $V_{OL}$    | —          | —   | 0.4  |                 | $I_{OL} = 15.0 \text{ mA}$<br>(BFCTL.FMPE = 1)   |
|  |  | $V_{OL}$    | —          | 0.4 | —    |                 | $I_{OL} = 20.0 \text{ mA}$<br>(BFCTL.FMPE = 1)   |
|  |  | $V_{OL}$    | —          | —   | 0.4  |                 | $I_{OL} = 3.0 \text{ mA}$<br>(BFCTL.HSME = 1)  |
|  | Ports PA08 to PA11, PB12 to PB15,<br>PC06 to PC09, PD08 to PD15, PE10 to<br>PE15 <sup>*3</sup> | $V_{OH}$    | VCC – 0.5  | —   | —    |                 | $I_{OH} = -1.0 \text{ mA}$   |
|  |  | $V_{OL}$    | —          | —   | 0.6  |                 | $I_{OL} = 20 \text{ mA}$   |
|  | Other output pins  | $V_{OH}$    | VCC – 0.5  | —   | —    |                 | $I_{OH} = -1.0 \text{ mA}$   |
|  |  | $V_{OL}$    | —          | —   | 0.5  |                 | $I_{OL} = 1.0 \text{ mA}$  |
|  | Input leakage current  | RES         | $ I_{in} $ | —   | —    | 5.0             | $\mu\text{A}$  |
| Port P000, P001, PA06, PA07, PB00,<br>PB01, PC00 to PC05, PC13 |  |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| Port PA00, PA02, PA04, PB02 (PGA<br>input pins)                |  |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| Port PA01, PA03, PA05, P002 (PGA/VSS<br>pins) <sup>*4</sup>    |  |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| Three-state leakage<br>current (off state)                     | 5 V-tolerant ports   | $ I_{TSL} $ | —          | —   | 5.0  | $\mu\text{A}$   | $V_{in} = 0 \text{ V}$<br>$V_{in} = 5.5 \text{ V}$   |
|  | Other ports (except for input ports)   |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| Input pull-up MOS<br>current                                   | Ports P0, P2, PA to PE (except for ports<br>P002, PA00 to PA05, PB02)                          | $I_p$       | -300       | —   | -10  | $\mu\text{A}$   | VCC = 2.7 to 3.6 V<br>$V_{in} = 0 \text{ V}$   |
| Pull-up current<br>serving as the SCL<br>current source        | IIC <sup>*5</sup>  | $I_{CS}$    | 3          | —   | 12   | mA              | VCC = 3.0 to 3.6 V<br>$V_{in} = 0.3 \times \text{VCC}$ to $0.7 \times \text{VCC}$                        |
| Input capacitance  | All input pins   | $C_{in}$    | —          | —   | 8    | pF              | $V_{bias} = 0 \text{ V}$<br>$V_{amp} = 20 \text{ mV}$<br>$f = 1 \text{ MHz}$<br>$T_a = 25^\circ\text{C}$ |

Note 1. SCL0\_A, SDA0\_A, SCL1\_A, SDA1\_A (total 4 pins). This is the value when IIC function is selected.

Note 2. SCL0\_A, SDA0\_A (total 2 pins). This is the value when IIC function is selected.

Note 3. This is the value when high current driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. This is the value when the pseudo-differential input on the PGAn pin is disabled (single-ended input).

Note 5. SCL0\_A (1 pin). This is the value when IIC high speed mode is selected.

注7.这是在PmnPFS寄存器的端口驱动能力位中选择高速驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

注8.这是在PmnPFS寄存器的端口驱动能力位中选择高电流驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

**Caution:** 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流表示在100 $\mu$ s期间测量的电流平均值。

## 2.2.4 IOVOH VOL和其他特性

Table 2.6 IOVOH、VOL和其他特性

| Parameter  | Symbol  | Min         | Typ        | Max | Unit | Test conditions |  |
|--|---|-------------|------------|-----|------|-----------------|--|
| 输出电压   | IIC <sup>*1</sup>   | $V_{OL}$    | —          | —   | 0.4  | V               | $I_{OL}=3.0\text{毫安}$  |
|  |   | $V_{OL}$    | —          | —   | 0.6  |                 | $I_{OL}=6.0\text{毫安}$  |
|  | IIC <sup>*2</sup>   | $V_{OL}$    | —          | —   | 0.4  |                 | $I_{OL}=15.0\text{mA}$ (BFCTL.FMPE=1)  |
|  |   | $V_{OL}$    | —          | 0.4 | —    |                 | $I_{OL}=20.0\text{mA}$ (BFCTL.FMPE=1)  |
|  |   | $V_{OL}$    | —          | —   | 0.4  |                 | $I_{OL}=3.0\text{mA}$ (BFCTL.HSME=1)   |
|  | 端口PA08至PA11、PB12至PB15、<br>PC06 to PC09, PD08 to PD15, PE10 to<br>PE15 <sup>*3</sup> | $V_{OH}$    | VCC – 0.5  | —   | —    |                 | $I_{OH}= 1.0\text{毫安}$   |
|  |   | $V_{OL}$    | —          | —   | 0.6  |                 | $I_{OL}=20\text{毫安}$   |
|  | 其他输出引脚  | $V_{OH}$    | VCC – 0.5  | —   | —    |                 | $I_{OH}= 1.0\text{毫安}$   |
|  |   | $V_{OL}$    | —          | —   | 0.5  |                 | $I_{OL}=1.0\text{毫安}$  |
|  | 输入漏电流   | RES         | $ I_{in} $ | —   | —    | 5.0             | $\mu\text{A}$  |
| Port P000, P001, PA06, PA07, PB00,<br>PB01, PC00 to PC05, PC13 |   |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| 端口PA00、PA02、PA04、PB02 (P<br>GA输入引脚)                            |   |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| Port PA01, PA03, PA05, P002 (PGA/VSS<br>pins) <sup>*4</sup>    |   |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| 三态漏电流 (关闭<br>状态)   | 5 V-tolerant ports  | $ I_{TSL} $ | —          | —   | 5.0  | $\mu\text{A}$   | $V_{in} = 0 \text{ V}$<br>$V_{in} = 5.5 \text{ V}$   |
|  | 其他端口 (输入端口除外)   |             | —          | —   | 1.0  |                 | $V_{in} = 0 \text{ V}$<br>$V_{in} = \text{VCC}$  |
| 输入上拉MOS电<br>流  | 端口P0、P2、PA到PE (端口除外<br>P002, PA00 to PA05, PB02)                                    | $I_p$       | -300       | —   | -10  | $\mu\text{A}$   | VCC = 2.7 to 3.6 V<br>$V_{in} = 0 \text{ V}$   |
| 上拉电流作为SCL<br>电流源   | IIC <sup>*5</sup>   | $I_{CS}$    | 3          | —   | 12   | mA              | VCC = 3.0 to 3.6 V<br>$V_{in}=0.3\times\text{VCC}$ 至 $0.7\times\text{VCC}$                     |
| 输入电容   | 所有输入引脚  | $C_{in}$    | —          | —   | 8    | pF              | $V_{bias} = 0 \text{ V}$<br>$V_{amp}=20\text{mV}$<br>$f=1\text{MHz}$<br>$T_a=25^\circ\text{C}$ |

注1.SCL0\_A、SDA0\_A、SCL1\_A、SDA1\_A (共4个引脚)。这是选择IIC功能时的值。

注2.SCL0\_A、SDA0\_A (共2个引脚)。这是选择IIC功能时的值。

注3.这是在PmnPFS寄存器的端口驱动能力位中选择高电流驱动能力时的值。在深度软件待机模式下会保留所选的驱动能力。

注4.这是禁用PGAn引脚上的伪差分输入 (单端输入) 时的值。

注5.SCL0\_A (1个引脚)。这是选择IIC高速模式时的值。

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current

| Parameter   |   | Symbol                         | Min  | Typ  | Max          | Unit              | Test conditions   |   |
|---|---|--------------------------------|--|--|--------------|-------------------|---|---|
| Supply current*1  | High-speed mode                               | Maximum*2                      | I <sub>CC</sub> *3                                 | —  | —            | 150               | mA<br>ICLK = 240 MHz<br>PCLKA = 120 MHz<br>PCLKB = 60 MHz<br>PCLKC = 60 MHz<br>PCLKD = 120 MHz<br>FCLK = 60 MHz |   |
|   |   | CoreMark®*5 *6                 |  | —  | 34           | —                 |   |   |
|   |   | Normal mode                    |  | All peripheral clocks enabled, while (1) code executing from flash*4     | —            | 44                |   | — |
|   |   |                                |  | All peripheral clocks disabled, while (1) code executing from flash*5 *6 | —            | 28                |   | — |
|   |   | Sleep mode*5 *6                |  | —  | 13           | 78                |   |   |
|   |   | Increase during BGO operation  |  | Data flash P/E   | —            | 6                 |   | — |
|   | Code flash P/E                                |                                | —  | 8  | —            |                   |   |   |
|   | Low-speed mode*5 *10                          | —                              | 5  | —  | ICLK = 1 MHz |                   |   |   |
|   | Software Standby mode                         | SNZCR.RXDREQEN = 1             | —  | —  | 63           | ICLK = 32.768 kHz |   |   |
|   |   | SNZCR.RXDREQEN = 0             | —  | 5.1  | —            | —                 |   |   |
|   | Deep Software Standby mode                    | Power supplied to Standby SRAM | —  | 22.7   | 60           | μA                | —   |   |
|   |   | Power not supplied to SRAM     | Power-on reset circuit low power function disabled | —  | 11.3         | 30                | —   |   |
| Power-on reset circuit low power function enabled           |   |                                | —  | 4.4  | 20           | —                 |   |   |
| Inrush current on returning from deep software standby mode | Inrush current*7                              | I <sub>RUSH</sub>              | —  | 160  | —            | mA                |   |   |
|   | Energy of inrush current*7                    | E <sub>RUSH</sub>              | —  | 1.0  | —            | μC                |   |   |
| Analog power supply current                                 | During ADC conversion (1unit)                 | Without SH                     | A <sub>I<sub>CC</sub></sub>                        | —  | 4.8          | 6.0               | mA  |   |
|   |   | With SH                        |  | —  | 7.3          | 11.5              | mA  |   |
|   | PGA (1channel)                                | —                              | 1  | 3  | mA           |                   |   |   |
|   | ACMPHS (1unit)                                | —                              | 0.1  | 0.2  | mA           |                   |   |   |
|   | Temperature sensor                            | —                              | 0.1  | 0.2  | mA           |                   |   |   |
|   | During D/A conversion (1channel)*8            | Without AMP output             | —  | 0.2  | 0.3          | mA                |   |   |
|   |   | With AMP output                | —  | 0.8  | 1.3          | mA                |   |   |
|   | Waiting for ADC, DAC12 conversion (all units) | —                              | 3.8  | 4.5  | mA           |                   |   |   |
|   | ADC, DAC12 in standby modes (all units)*9     | —                              | 0.7  | 10   | μA           |                   |   |   |
| Reference power supply current (VREFH0)                     | During ADC conversion (1unit)                 | A <sub>I<sub>REFH0</sub></sub> | —  | 21   | 50           | μA                |   |   |
|   | Waiting for ADC, DAC12 conversion (all units) |                                | —  | 18   | 50           | μA                |   |   |
|   | ADC, DAC12 in standby modes (all units)*9     |                                | —  | 0.03   | 1            | μA                |   |   |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.  
 Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.  
 Note 3. I<sub>CC</sub> depends on f (ICLK) as follows.  
 I<sub>CC</sub> Max. = 0.34 × f + 67 (max. operation in high-speed mode)  
 I<sub>CC</sub> Typ. = 0.095 × f + 4.7 (normal operation in high-speed mode, all peripheral clocks disabled)  
 I<sub>CC</sub> Typ. = 0.9 × f + 4.1 (low-speed mode)  
 I<sub>CC</sub> Max. = 0.045 × f + 67 (sleep mode)  
 Note 4. This does not include the BGO operation.  
 Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.  
 Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).  
 Note 7. Reference value  
 Note 8. The DAC12 includes the Reference current in the analog power supply current.

2.2.5 工作和待机电流

Table 2.7 工作和待机电流

| Parameter         |                            | 符号                             |                             | 最小值                       | 典型值          | 最大单元测试条件          |   |   |
|-------------------|----------------------------|--------------------------------|-----------------------------|---------------------------|--------------|-------------------|---|---|
| 供电电流*1            | High-speed mode            | Maximum*2                      | I <sub>CC</sub> *3          | —                         | —            | 150               | mA<br>ICLK = 240 MHz<br>PCLKA = 120 MHz<br>PCLKB = 60 MHz<br>PCLKC = 60 MHz<br>PCLKD = 120 MHz<br>FCLK = 60 MHz |   |
|                   |                            | CoreMark®*5 *6                 |                             | —                         | 34           | —                 |   |   |
|                   |                            | 正常模式                           |                             | 启用所有外设时钟，同时(1)代码从闪存执行*4   | —            | 44                |   | — |
|                   |                            |                                |                             | 禁用所有外设时钟，同时(1)代码从闪存执行*5*6 | —            | 28                |   | — |
|                   |                            | 睡眠模式*5*6                       |                             | —                         | 13           | 78                |   |   |
|                   |                            | BGO运行期间增加                      |                             | 数据闪存PE                    | —            | 6                 |   | — |
|                   | 代码闪存PE                     |                                | —                           | 8                         | —            |                   |   |   |
|                   | Low-speed mode*5 *10       | —                              | 5                           | —                         | ICLK = 1 MHz |                   |   |   |
|                   | 软件待机模式                     | SNZCR.RXDREQEN = 1             | —                           | —                         | 63           | ICLK = 32.768 kHz |   |   |
|                   |                            | SNZCR.RXDREQEN = 0             | —                           | 5.1                       | —            | —                 |   |   |
|                   | Deep Software Standby mode | 为备用SRAM供电                      | —                           | 22.7                      | 60           | μA                | —   |   |
|                   |                            | 未向SRAM供电                       | 上电复位电路低功耗功能禁用               | —                         | 11.3         | 30                | —   |   |
| 上电复位电路低功耗功能启用     |                            |                                | —                           | 4.4                       | 20           | —                 |   |   |
| 从深度软件待机模式返回时的浪涌电流 | Inrush current*7           | I <sub>RUSH</sub>              | —                           | 160                       | —            | mA                |   |   |
|                   | 浪涌电流能量*7                   | E <sub>RUSH</sub>              | —                           | 1.0                       | —            | μC                |   |   |
| 模拟电源电流            | ADC转换期间 (1个单位)             | Without SH                     | A <sub>I<sub>CC</sub></sub> | —                         | 4.8          | 6.0               | mA  |   |
|                   |                            | With SH                        |                             | —                         | 7.3          | 11.5              | mA  |   |
|                   | PGA (1channel)             | —                              | 1                           | 3                         | mA           |                   |   |   |
|                   | ACMPHS (1unit)             | —                              | 0.1                         | 0.2                       | mA           |                   |   |   |
|                   | 温度感应器                      | —                              | 0.1                         | 0.2                       | mA           |                   |   |   |
|                   | DA转换期间 (1通道) *8            | 无AMP输出                         | —                           | 0.2                       | 0.3          | mA                |   |   |
|                   |                            | 带AMP输出                         | —                           | 0.8                       | 1.3          | mA                |   |   |
|                   | 等待ADC、DAC12转换 (所有单元)       | —                              | 3.8                         | 4.5                       | mA           |                   |   |   |
|                   | 待机模式下的ADC、DAC12 (所有单元) *9  | —                              | 0.7                         | 10                        | μA           |                   |   |   |
| 参考电源电流(VREFH0)    | ADC转换期间 (1个单位)             | A <sub>I<sub>REFH0</sub></sub> | —                           | 21                        | 50           | μA                |   |   |
|                   | 等待ADC、DAC12转换 (所有单元)       |                                | —                           | 18                        | 50           | μA                |   |   |
|                   | 待机模式下的ADC、DAC12 (所有单元) *9  |                                | —                           | 0.03                      | 1            | μA                |   |   |

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。  
 注2.使用提供外设功能的时钟测量。这包括BGO操作。  
 注3.I<sub>CC</sub>取决于f(ICLK)，如下所示。  
 I<sub>CC</sub>最大。=0.34×f+67 (高速模式下的最大操作)  
 I<sub>CC</sub>典型。=0.095×f+4.7 (高速模式下正常运行，所有外设时钟禁用)  
 I<sub>CC</sub>典型。=0.9×f+4.1 (low-speed mode)  
 I<sub>CC</sub>最大。=0.045×f+67 (sleep mode)  
 注4.这包括BGO操作。  
 注5.在此状态下停止向外围设备提供时钟信号。这包括BGO操作。  
 注6.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频 (3.75MHz)。  
 注7.参考值  
 注8.DAC12在模拟电源电流中包含参考电流。

Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter Module Stop bit) is in the module-stop state.

Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).

**Table 2.8 Coremark and normal mode current**

| Parameter        | Symbol   | Typ             | Unit | Test conditions |  |   |     |
|------------------|--|-----------------|------|-----------------|--|---|-----|
| Supply Current*1 | Coremark   | I <sub>CC</sub> | 139  | μA/MHz          | ICLK = 240 MHz<br>PCLKA =<br>PCLKB =<br>PCLKC =<br>PCLKD =<br>FCLK =<br>3.75 MHz |   |     |
|                  |  |                 |      |                 |  | Normal mode   | 139 |
|                  |  |                 |      |                 |  | All peripheral clocks disabled, cache on, while (1) code executing from flash*2 | 115 |
|                  | All peripheral clocks disabled, cache off, while (1) code executing from flash*2 |                 |      |                 |  |   |     |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

## 2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.9 Rise and fall gradient characteristics**

| Parameter            | Symbol                                      | Min    | Typ | Max | Unit | Test conditions |
|----------------------|---|--------|-----|-----|------|-----------------|
| VCC rising gradient  | Voltage monitor 0 reset disabled at startup | 0.0084 | —   | 20  | ms/V | —               |
|                      | Voltage monitor 0 reset enabled at startup  | 0.0084 | —   | —   | —    | —               |
|                      | SCI boot mode*1                             | 0.0084 | —   | 20  | —    | —               |
| VCC falling gradient | SfVCC                                       | 0.0084 | —   | —   | ms/V | —               |

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

**Table 2.10 Rising and falling gradient and ripple frequency characteristics**

The ripple voltage must meet the allowable ripple frequency  $f_{r(VCC)}$  within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds  $VCC \pm 10\%$ , the allowable voltage change rising and falling gradient  $dt/dVCC$  must be met.

| Parameter  | Symbol       | Min | Typ | Max | Unit | Test conditions                               |
|--|--------------|-----|-----|-----|------|---|
| Allowable ripple frequency                           | $f_{r(VCC)}$ | —   | —   | 10  | kHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.2$  |
|  |              | —   | —   | 1   | MHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.08$ |
|  |              | —   | —   | 10  | MHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | dt/dVCC      | 1.0 | —   | —   | ms/V | When VCC change exceeds $VCC \pm 10\%$        |

注9.当MCU处于软件待机模式或MSTPCRD.MSTPD16（12位AD转换器模块停止位）处于模块停止状态时。

注10.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频（15.6kHz）。

**Table 2.8 Coremark和正常模式电流**

| Parameter | Symbol                       | Typ             | Unit | 测试条件   |  |                              |     |
|-----------|------------------------------|-----------------|------|--------|--|------------------------------|-----|
| 电源电流*1    | Coremark                     | I <sub>CC</sub> | 139  | μA/MHz | ICLK = 240 MHz<br>PCLKA =<br>PCLKB =<br>PCLKC =<br>PCLKD =<br>FCLK =<br>3.75 MHz |                              |     |
|           |                              |                 |      |        |  | 正常模式                         | 139 |
|           |                              |                 |      |        |  | 禁用所有外设时钟，开启缓存，同时(1)从闪存执行代码*2 | 115 |
|           | 所有外设时钟禁用，缓存关闭，同时(1)代码从闪存执行*2 |                 |      |        |  |                              |     |

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。

注2.在此状态下停止向外围设备提供时钟信号。这包括BGO操作。

## 2.2.6 VCC上升和下降梯度和纹波频率

**Table 2.9 上升和下降梯度特性**

| Parameter | Symbol | Min    | Typ | Max | Unit | 测试条件          |
|-----------|--------|--------|-----|-----|------|---------------|
| VCC上升梯度   | SrVCC  | 0.0084 | —   | 20  | ms/V | 启动时禁用电压监视器0复位 |
|           |        |        |     |     |      | 启动时启用电压监视器0复位 |
|           |        |        |     |     |      | SCI开机模式*1     |
| VCC下降梯度   | SfVCC  | 0.0084 | —   | —   | ms/V | —             |

注1.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

**Table 2.10 上升下降梯度和纹波频率特性**

纹波电压必须在VCC上限(3.6V)和下限(2.7V)之间。当VCC变化超过 $VCC \pm 10\%$ 时，必须满足允许的电压变化上升和下降梯度 $dt/dVCC$ 。

| Parameter    | Symbol       | Min | Typ | Max | Unit | 测试条件  |
|--------------|--------------|-----|-----|-----|------|---|
| 允许纹波频率       | $f_{r(VCC)}$ | —   | —   | 10  | kHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.2$  |
|              |              | —   | —   | 1   | MHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.08$ |
|              |              | —   | —   | 10  | MHz  | Figure 2.2<br>$V_r(VCC) \leq VCC \times 0.06$ |
| 允许电压变化上升下降梯度 | dt/dVCC      | 1.0 | —   | —   | ms/V | 当VCC变化超过 $VCC \pm 10\%$                       |

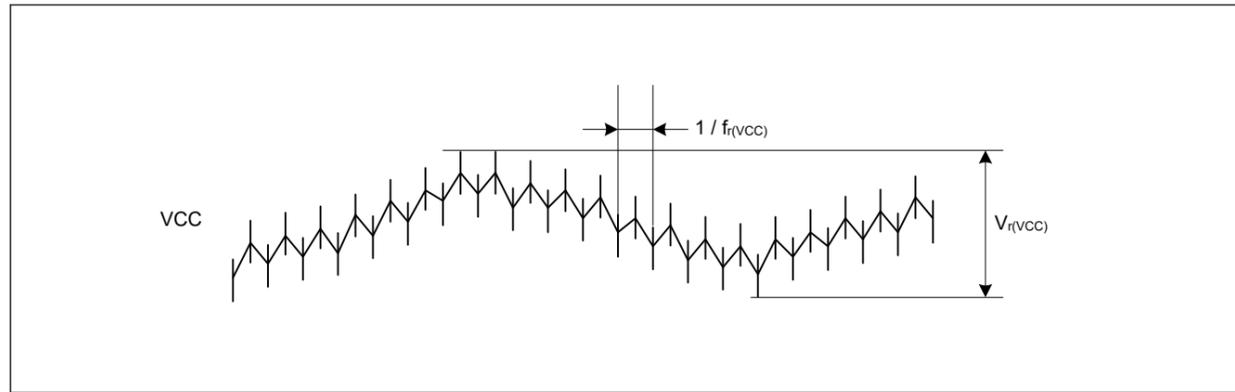


Figure 2.2 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- $T_j = T_a + \theta_{ja} \times \text{Total power consumption}$
- $T_j = T_t + \Psi_{jt} \times \text{Total power consumption}$ 
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - $\theta_{ja}$  : Thermal Resistance of “Junction”-to-“Ambient” (°C/W)
  - $\Psi_{jt}$  : Thermal Resistance of “Junction”-to-“Top Center Case” (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO =  $\Sigma (I_{OL} \times V_{OL}) / \text{Voltage} + \Sigma (I_{OH} \times |V_{CC} - V_{OH}|) / \text{Voltage}$
- Dynamic current of IO =  $\Sigma IO (C_{in} + C_{load}) \times IO \text{ switching frequency} \times \text{Voltage}$ 
  - Cin: Input capacitance
  - Cload: Output capacitance

Regarding  $\theta_{ja}$  and  $\Psi_{jt}$ , refer to Table 2.11.

Table 2.11 Thermal Resistance

| Parameter          | Package                     | Symbol        | Value*1 | Unit | Test conditions              |
|--------------------|-----------------------------|---------------|---------|------|------------------------------|
| Thermal Resistance | 100-pin LQFP (PLQP0100KB-B) | $\theta_{ja}$ | 36      | °C/W | JESD 51-2 and 51-7 compliant |
|                    | 64-pin LQFP (PLQP0064KB-C)  |               | 39      |      |                              |
|                    | 64-pin QFN (PWQN0064LA-A)   |               | 26      |      |                              |
|                    | 48-pin LQFP (PLQP0048KB-B)  |               | 60      |      |                              |
|                    | 48-pin QFN (PWQN0048KB-A)   |               | 28      |      |                              |
|                    | 100-pin LQFP (PLQP0100KB-B) | $\Psi_{jt}$   | 0.65    | °C/W |                              |
|                    | 64-pin LQFP (PLQP0064KB-C)  |               | 0.69    |      |                              |
|                    | 64-pin QFN (PWQN0064LA-A)   |               | 0.15    |      |                              |
|                    | 48-pin LQFP (PLQP0048KB-B)  |               | 2.01    |      |                              |
|                    | 48-pin QFN (PWQN0048KB-A)   |               | 0.17    |      |                              |

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

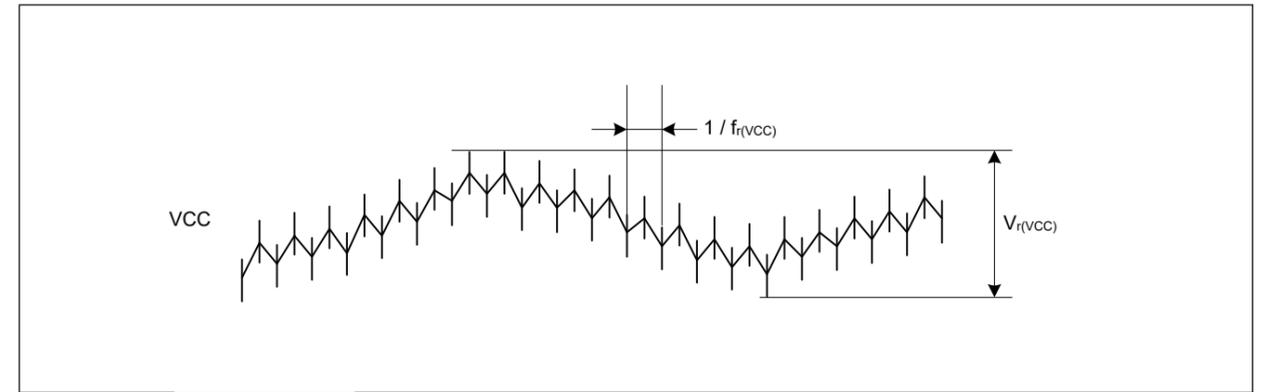


Figure 2.2 纹波波形

2.2.7 热特性

结温最大值(Tj)不得超过第2.2.1节。TjTa定义。

Tj通过以下任一公式计算。

- $T_j = T_a + \theta_{ja} \times \text{总功耗}$
- $T_j = T_t + \Psi_{jt} \times \text{总功耗}$ 
  - Tj: 结温(°C)
  - Ta: 环境温度 (°C)
  - Tt: 顶部中心外壳温度(°C)
  - $\theta_{ja}$ : “结”到“环境”的热阻(°C/W)
  - $\Psi_{jt}$ : “结”到“顶部中心外壳”的热阻(°C/W)
- 总功耗=电压× (漏电流+动态电流)
- IO漏电流= $\Sigma (I_{OL} \times V_{OL})$ 电压+ $\Sigma (I_{OH} \times V_{CC} - V_{OH})$ 电压
- IO的动态电流= $\Sigma IO (C_{in} + C_{load}) \times IO \text{开关频率} \times \text{电压}$ 
  - Cin:输入电容
  - C负载: 输出电容

关于 $\theta_{ja}$ 和 $\Psi_{jt}$ , 请参阅表2.11。

Table 2.11 热阻

| Parameter | Package                     | Symbol        | Value*1 | Unit | 测试条件            |
|-----------|-----------------------------|---------------|---------|------|-----------------|
| 热阻        | 100-pin LQFP (PLQP0100KB-B) | $\theta_{ja}$ | 36      | °C/W | 符合JESD51-2和51-7 |
|           | 64-pin LQFP (PLQP0064KB-C)  |               | 39      |      |                 |
|           | 64-pin QFN (PWQN0064LA-A)   |               | 26      |      |                 |
|           | 48-pin LQFP (PLQP0048KB-B)  |               | 60      |      |                 |
|           | 48-pin QFN (PWQN0048KB-A)   |               | 28      |      |                 |
|           | 100-pin LQFP (PLQP0100KB-B) | $\Psi_{jt}$   | 0.65    | °C/W |                 |
|           | 64-pin LQFP (PLQP0064KB-C)  |               | 0.69    |      |                 |
|           | 64-pin QFN (PWQN0064LA-A)   |               | 0.15    |      |                 |
|           | 48-pin LQFP (PLQP0048KB-B)  |               | 2.01    |      |                 |
|           | 48-pin QFN (PWQN0048KB-A)   |               | 0.17    |      |                 |

注1.数值为使用4层板时的参考值。热阻取决于板的层数或尺寸。有关详细信息, 请参阅JEDEC标准。

## 2.2.7.1 Calculation guide of ICCmax

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

| Dynamic current/Leakage current | MCU Domain      | Category                      | Item              | Frequency [MHz] | Current [uA/MHz] | Current*1 [mA] |
|---------------------------------|-----------------|-------------------------------|-------------------|-----------------|------------------|----------------|
| Leakage current                 | Analog          | LDO and Leak*2                | Ta = 75 °C*3      | —               | —                | 37.8           |
|                                 |                 |                               | Ta = 85 °C*3      | —               | —                | 46.4           |
|                                 |                 |                               | Ta = 95 °C*3      | —               | —                | 56.1           |
|                                 |                 |                               | Ta = 105 °C*3     | —               | —                | 68.0           |
| Dynamic current                 | CPU             | Operation with Flash and SRAM | Coremark          | 240             | 105.324          | 25.28          |
|                                 | Peripheral Unit | Timer                         | GPT32 (10ch)*4    | 120             | 29.697           | 3.56           |
|                                 |                 |                               | POEG (4 Groups)*4 | 60              | 1.483            | 0.09           |
|                                 |                 |                               | AGT (2ch)*4       | 60              | 3.09             | 0.19           |
|                                 |                 |                               | WDT               | 60              | 0.641            | 0.04           |
|                                 |                 |                               | IWDT              | 60              | 0.225            | 0.01           |
|                                 |                 | Communication interfaces      | SCI (6ch)*4       | 120             | 27.683           | 3.32           |
|                                 |                 |                               | IIC (2ch)*4       | 120             | 5.304            | 0.64           |
|                                 |                 |                               | CANFD             | 60              | 5.763            | 0.35           |
|                                 |                 |                               | SPI (2ch)*4       | 120             | 5.738            | 0.69           |
|                                 |                 | Data processing accelerator   | TFU               | 240             | 1.188            | 0.03           |
|                                 |                 |                               | IIRFA             | 240             | 34.252           | 8.22           |
|                                 |                 | Data processing               | DOC               | 120             | 0.221            | 0.03           |
|                                 |                 |                               | CRC               | 120             | 0.508            | 0.06           |
|                                 |                 | Analog                        | ADC (2 Units)*4   | 60              | 172.958          | 10.38          |
|                                 |                 |                               | DAC12 (4ch)*4     | 120             | 1.097            | 0.13           |
|                                 |                 |                               | ACMPHS (4ch)*4    | 60              | 0.641            | 0.04           |
|                                 |                 |                               | TSN               | 60              | 0.111            | 0.01           |
|                                 |                 | Event link                    | ELC               | 60              | 1.852            | 0.11           |
|                                 |                 | Security                      | SCE5              | 120             | 68.404           | 8.21           |
|                                 |                 | System                        | CAC               | 60              | 0.63             | 0.04           |
|                                 | KINT            |                               | 60                | 0.072           | 0.004            |                |
|                                 | DMA             | DMAC                          | 240               | 5.073           | 1.22             |                |
|                                 |                 | DTC                           | 240               | 4.18            | 1                |                |

Note 1. The values are guaranteed by design.

Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.

It is selected according to the temperature of Ta.

Note 3.  $\Delta(Tj-Ta) = 20\text{ }^{\circ}\text{C}$  is considered to measure the current.

Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 Outline of operation for each unit (1 of 2)

| Peripheral | Outline of operation   |
|------------|--|
| GPT        | Operating modes is set to saw-wave PWM mode.<br>GPT is operating with PCLKD. |

## 2.2.7.1 ICCmax的计算指南

表2.12显示了每个单元的功耗。

Table 2.12 各单元耗电量

| 动态电流/漏电流 | MCU Domain | Category   | Item              | Frequency [MHz] | Current [uA/MHz] | Current*1 [mA] |
|----------|------------|------------|-------------------|-----------------|------------------|----------------|
| 漏电流      | Analog     | LDO和泄漏*2   | Ta = 75 °C*3      | —               | —                | 37.8           |
|          |            |            | Ta = 85 °C*3      | —               | —                | 46.4           |
|          |            |            | Ta = 95 °C*3      | —               | —                | 56.1           |
|          |            |            | Ta = 105 °C*3     | —               | —                | 68.0           |
| 动态电流     | CPU        | 操作与闪存和SRAM | Coremark          | 240             | 105.324          | 25.28          |
|          | 外围单元       | Timer      | GPT32 (10ch)*4    | 120             | 29.697           | 3.56           |
|          |            |            | POEG (4 Groups)*4 | 60              | 1.483            | 0.09           |
|          |            |            | AGT (2ch)*4       | 60              | 3.09             | 0.19           |
|          |            |            | WDT               | 60              | 0.641            | 0.04           |
|          |            |            | IWDT              | 60              | 0.225            | 0.01           |
|          |            | 通讯接口       | SCI (6ch)*4       | 120             | 27.683           | 3.32           |
|          |            |            | IIC (2ch)*4       | 120             | 5.304            | 0.64           |
|          |            |            | CANFD             | 60              | 5.763            | 0.35           |
|          |            |            | SPI (2ch)*4       | 120             | 5.738            | 0.69           |
|          |            | 数据处理加速器    | TFU               | 240             | 1.188            | 0.03           |
|          |            |            | IIRFA             | 240             | 34.252           | 8.22           |
|          |            | 数据处理       | DOC               | 120             | 0.221            | 0.03           |
|          |            |            | CRC               | 120             | 0.508            | 0.06           |
|          |            | Analog     | ADC (2 Units)*4   | 60              | 172.958          | 10.38          |
|          |            |            | DAC12 (4ch)*4     | 120             | 1.097            | 0.13           |
|          |            |            | ACMPHS (4ch)*4    | 60              | 0.641            | 0.04           |
|          |            |            | TSN               | 60              | 0.111            | 0.01           |
|          |            | 活动链接       | ELC               | 60              | 1.852            | 0.11           |
|          |            | Security   | SCE5              | 120             | 68.404           | 8.21           |
|          |            | System     | CAC               | 60              | 0.63             | 0.04           |
|          | KINT       |            | 60                | 0.072           | 0.004            |                |
|          | DMA        | DMAC       | 240               | 5.073           | 1.22             |                |
|          |            | DTC        | 240               | 4.18            | 1                |                |

注1.数值由设计保证。

注2.LDO和Leak是内部稳压器的电流和MCU的漏电流。

根据Ta的温度选择。

注3.测量电流时考虑 $\Delta(Tj-Ta)=20\text{ }^{\circ}\text{C}$ 。

注4.要确定每个通道或单元的电流消耗，请将电流[mA]除以通道、组或单元的数量。

Table 2.13 每个单元的操作概要 (2个中的1个)

| Peripheral | 操作概要                              |
|------------|-----------------------------------|
| GPT        | 操作模式设置为锯齿波PWM模式。<br>GPT使用PCLKD运行。 |

Table 2.13 Outline of operation for each unit (2 of 2)

| Peripheral | Outline of operation  |
|------------|---|
| POEG       | Only clear module stop bit.   |
| AGT        | AGT is operating with PCLKB.  |
| WDT        | WDT is operating with PCLKB.  |
| IWDT       | IWDT is operating with IWDTCLK.   |
| SCI        | SCI is transmitting data in clock synchronous mode.   |
| IIC        | Communication format is set to I2C-bus format.<br>IIC is transmitting data in master mode.  |
| CANFD      | CANFD is transmitting and receiving data in self-test mode 1.   |
| SPI        | SPI mode is set to SPI operation (4-wire method).<br>SPI master/slave mode is set to master mode.<br>SPI is transmitting 8-bit width data.  |
| TFU        | Performs sincos operations.   |
| IIRFA      | Channel 0 performs 32 stages of channel processing.   |
| DOC        | DOC is operating in data addition mode.   |
| CRC        | CRC is generating CRC code using 32-bit CRC32-C polynomial.   |
| ADC        | Resolution is set to 12-bit accuracy.<br>Conversion Data Operation Control B Register is set to 16 times average mode.<br>ADC is converting the analog input in continuous scan mode.<br>ADC is operating with PCLKC. |
| DAC12      | DAC12 is outputting the conversion result while updating the value of data register.  |
| ACMPHS     | Compare between IVCMP2 and IVREF0 and enable compare output.  |
| TSN        | TSN is operating.   |
| ELC        | Only clear module stop bit.   |
| SCE5       | SCE5 is executing built-in self test.   |
| DMAC       | Bit length of transfer data is set to 32 bits.<br>Transfer mode is set to block transfer mode.<br>DMAC is transferring data from SRAM0 to SRAM0.  |
| DTC        | Bit length of transfer data is set to 32 bits.<br>Transfer mode is set to block transfer mode.<br>DTC is transferring data from SRAM0 to SRAM0.   |
| CAC        | Measurement target clocks is set to PCLKB.<br>Measurement reference clocks is set to PCLKB.<br>CAC is measuring the clock frequency accuracy.   |
| KINT       | Only clear module stop bit.   |

### 2.2.7.2 Example of Tj calculation

Assumption:

- Package 100-pin LQFP:  $\theta_{ja} = 36.0 \text{ }^\circ\text{C/W}$
- $T_a = 100 \text{ }^\circ\text{C}$
- $I_{CCmax} = 80 \text{ mA}$
- $V_{CC} = 3.5 \text{ V}$  ( $V_{CC} = AVCC0$ )
- $I_{OH} = 1 \text{ mA}$ ,  $V_{OH} = V_{CC} - 0.5 \text{ V}$ , 12 Outputs
- $I_{OL} = 20 \text{ mA}$ ,  $V_{OL} = 1.0 \text{ V}$ , 8 Outputs
- $I_{OL} = 1 \text{ mA}$ ,  $V_{OL} = 0.5 \text{ V}$ , 12 Outputs
- $C_{in} = 8 \text{ pF}$ , 16 pins, Input frequency = 10 MHz

Table 2.13 每个单元的操作概要 (2个中的2个)

| Peripheral | 操作概要   |
|------------|--|
| POEG       | 只清除模块停止位。  |
| AGT        | AGT使用PCLKB运行。  |
| WDT        | WDT使用PCLKB运行。  |
| IWDT       | IWDT使用IWDTCLK运行。   |
| SCI        | SCI在时钟同步模式下传输数据。   |
| IIC        | 通信格式设置为I2C总线格式。<br>IIC在主机模式下传输数据。  |
| CANFD      | CANFD在自检模式1下发送和接收数据。   |
| SPI        | SPI模式设置为SPI操作 (4线方法)。<br>SPI主从模式设置为主模式。<br>SPI正在传输8位宽度的数据。                     |
| TFU        | 执行sincos操作。  |
| IIRFA      | 通道0执行32个通道处理阶段。  |
| DOC        | DOC在数据添加模式下运行。   |
| CRC        | CRC使用32位CRC32-C多项式生成CRC码。  |
| ADC        | 分辨率设置为12位精度。<br>转换数据操作控制B寄存器设置为16次平均模式。<br>ADC在连续扫描模式下转换模拟输入。<br>ADC使用PCLKC运行。 |
| DAC12      | DAC12在更新数据寄存器值的同时输出转换结果。   |
| ACMPHS     | 比较IVCMP2和IVREF0并启用比较输出。  |
| TSN        | TSN正在运行。   |
| ELC        | 只清除模块停止位。  |
| SCE5       | SCE5正在执行内置自检。  |
| DMAC       | 传输数据的位长设置为32位。<br>传输模式设置为块传输模式。<br>DMAC正在将数据从SRAM0传输到SRAM0。                    |
| DTC        | 传输数据的位长设置为32位。<br>传输模式设置为块传输模式。<br>DTC正在将数据从SRAM0传输到SRAM0。                     |
| CAC        | 测量目标时钟设置为PCLKB。<br>测量参考时钟设置为PCLKB。CAC正在测量时钟频率精度。                               |
| KINT       | 只清除模块停止位。  |

### 2.2.7.2 Tj计算示例

Assumption:

- Package 100-pin LQFP:  $\theta_{ja} = 36.0 \text{ }^\circ\text{C/W}$
- $T_a = 100 \text{ }^\circ\text{C}$
- $I_{CC}$ 最大值=80mA
- $V_{CC} = 3.5 \text{ V}$  ( $V_{CC} = AVCC0$ )
- $I_{OH}=1\text{mA}$ ,  $V_{OH}=V_{CC} - 0.5\text{V}$ , 12个输出
- $I_{OL}=20\text{mA}$ ,  $V_{OL}=1.0\text{V}$ , 8个输出
- $I_{OL}=1\text{mA}$ ,  $V_{OL}=0.5\text{V}$ , 12路输出
- $C_{in}=8\text{pF}$ , 16个引脚, 输入频率=10MHz

- $C_{load} = 30 \text{ pF}$ , 16 pins, Output frequency = 10 MHz

$$\begin{aligned} \text{Leakage current of IO} &= \Sigma (V_{OL} \times I_{OL}) / \text{Voltage} + \Sigma ((V_{CC} - V_{OH}) \times I_{OH}) / \text{Voltage} \\ &= (20 \text{ mA} \times 1 \text{ V}) \times 8 / 3.5 \text{ V} + (1 \text{ mA} \times 0.5 \text{ V}) \times 12 / 3.5 \text{ V} + ((V_{CC} - (V_{CC} - 0.5 \text{ V})) \times 1 \text{ mA}) \times 12 / 3.5 \text{ V} \\ &= 45.7 \text{ mA} + 1.71 \text{ mA} + 1.71 \text{ mA} \\ &= 49.1 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{Dynamic current of IO} &= \Sigma IO (C_{in} + C_{load}) \times \text{IO switching frequency} \times \text{Voltage} \\ &= ((8 \text{ pF} \times 16) \times 10 \text{ MHz} + (30 \text{ pF} \times 16) \times 10 \text{ MHz}) \times 3.5 \text{ V} \\ &= 21.3 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{Total power consumption} &= \text{Voltage} \times (\text{Leakage current} + \text{Dynamic current}) \\ &= (80 \text{ mA} \times 3.5 \text{ V}) + (49.1 \text{ mA} + 21.3 \text{ mA}) \times 3.5 \text{ V} \\ &= 526 \text{ mW} (0.526 \text{ W}) \end{aligned}$$

$$\begin{aligned} T_j &= T_a + \theta_{ja} \times \text{Total power consumption} \\ &= 100 \text{ }^\circ\text{C} + 36.0 \text{ }^\circ\text{C/W} \times 0.526 \text{ W} \\ &= 118.9 \text{ }^\circ\text{C} \end{aligned}$$

## 2.3 AC Characteristics

### 2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

| Parameter           | Symbol                          | Min | Typ | Max | Unit |
|---------------------|---------------------------------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK)             | f   | —   | 240 | MHz  |
|                     | Peripheral module clock (PCLKA) | —   | —   | 120 |      |
|                     | Peripheral module clock (PCLKB) | —   | —   | 60  |      |
|                     | Peripheral module clock (PCLKC) | —*2 | —   | 60  |      |
|                     | Peripheral module clock (PCLKD) | —   | —   | 120 |      |
|                     | Flash interface clock (FCLK)    | —*1 | —   | 60  |      |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.  
 Note 2. When the ADC is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

| Parameter           | Symbol                             | Min | Typ | Max | Unit |
|---------------------|------------------------------------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK)                | f   | —   | 1   | MHz  |
|                     | Peripheral module clock (PCLKA)    | —   | —   | 1   |      |
|                     | Peripheral module clock (PCLKB)    | —   | —   | 1   |      |
|                     | Peripheral module clock (PCLKC) *2 | —*2 | —   | 1   |      |
|                     | Peripheral module clock (PCLKD)    | —   | —   | 1   |      |
|                     | Flash interface clock (FCLK)*1     | —   | —   | 1   |      |

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.  
 Note 2. When the ADC is used, the PCLKC frequency must be set to at least 1 MHz.

- C负载=30pF, 16引脚, 输出频率=10MHz

$$\begin{aligned} \text{IO漏电流} &= \Sigma (V_{OL} \times I_{OL}) \text{电压} + \Sigma ((V_{CC} - V_{OH}) \times I_{OH}) \text{电压} \\ &= (20 \text{ mA} \times 1 \text{ V}) \times 8 / 3.5 \text{ V} + (1 \text{ mA} \times 0.5 \text{ V}) \times 12 / 3.5 \text{ V} + ((V_{CC} - (V_{CC} - 0.5 \text{ V})) \times 1 \text{ mA}) \times 12 / 3.5 \text{ V} \\ &= 45.7 \text{ mA} + 1.71 \text{ mA} + 1.71 \text{ mA} \\ &= 49.1 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{IO的动态电流} &= \Sigma IO (C_{in} + C_{load}) \times \text{IO开关频率} \times \text{电压} \\ &= ((8 \text{ pF} \times 16) \times 10 \text{ MHz} + (30 \text{ pF} \times 16) \times 10 \text{ MHz}) \times 3.5 \text{ V} \\ &= 21.3 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{总功耗} &= \text{电压} \times (\text{漏电流} + \text{动态电流}) \\ &= (80 \text{ mA} \times 3.5 \text{ V}) + (49.1 \text{ mA} + 21.3 \text{ mA}) \times 3.5 \text{ V} \\ &= 526 \text{ mW} (0.526 \text{ W}) \end{aligned}$$

$$\begin{aligned} T_j &= T_a + \theta_{ja} \times \text{总功耗} \\ &= 100 \text{ }^\circ\text{C} + 36.0 \text{ }^\circ\text{C/W} \times 0.526 \text{ W} \\ &= 118.9 \text{ }^\circ\text{C} \end{aligned}$$

## 2.3 交流特性

### 2.3.1 Frequency

Table 2.14 高速模式下的运行频率值

| Parameter | Symbol        | Min | Typ | Max | Unit |
|-----------|---------------|-----|-----|-----|------|
| 运行频率      | 系统时钟(ICLK)    | f   | —   | 240 | MHz  |
|           | 外设模块时钟(PCLKA) | —   | —   | 120 |      |
|           | 外设模块时钟(PCLKB) | —   | —   | 60  |      |
|           | 外设模块时钟(PCLKC) | —*2 | —   | 60  |      |
|           | 外设模块时钟(PCLKD) | —   | —   | 120 |      |
|           | 闪存接口时钟(FCLK)  | —*1 | —   | 60  |      |

注1.在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。  
 注2.使用ADC时，PCLKC频率必须至少为1MHz。

Table 2.15 低速模式下的运行频率值

| Parameter | Symbol          | Min | Typ | Max | Unit |
|-----------|-----------------|-----|-----|-----|------|
| 运行频率      | 系统时钟(ICLK)      | f   | —   | 1   | MHz  |
|           | 外设模块时钟(PCLKA)   | —   | —   | 1   |      |
|           | 外设模块时钟(PCLKB)   | —   | —   | 1   |      |
|           | 外围模块时钟(PCLKC)*2 | —*2 | —   | 1   |      |
|           | 外设模块时钟(PCLKD)   | —   | —   | 1   |      |
|           | 闪存接口时钟(FCLK)*1  | —   | —   | 1   |      |

注1.在低速模式下禁止对闪存进行编程或擦除。  
 注2.使用ADC时，PCLKC频率必须设置为至少1MHz。

## 2.3.2 Clock Timing

Table 2.16 Clock timing

| Parameter  | Symbol                 | Min     | Typ    | Max     | Unit | Test conditions  |
|--|------------------------|---------|--------|---------|------|------------------|
| EXTAL external clock input cycle time                      | t <sub>EXcyc</sub>     | 41.66   | —      | —       | ns   | Figure 2.3       |
| EXTAL external clock input high pulse width                | t <sub>EXH</sub>       | 15.83   | —      | —       | ns   |                  |
| EXTAL external clock input low pulse width                 | t <sub>EXL</sub>       | 15.83   | —      | —       | ns   |                  |
| EXTAL external clock rise time                             | t <sub>EXr</sub>       | —       | —      | 5.0     | ns   |                  |
| EXTAL external clock fall time                             | t <sub>EXf</sub>       | —       | —      | 5.0     | ns   |                  |
| Main clock oscillator frequency                            | f <sub>MAIN</sub>      | 8       | —      | 24      | MHz  | —                |
| Main clock oscillation stabilization wait time (crystal)*1 | t <sub>MAINOSCWT</sub> | —       | —      | —*1     | ms   | Figure 2.4       |
| LOCO clock oscillation frequency                           | f <sub>LOCO</sub>      | 29.4912 | 32.768 | 36.0448 | kHz  | —                |
| LOCO clock oscillation stabilization wait time             | t <sub>LOCOWT</sub>    | —       | —      | 60.4    | μs   | Figure 2.5       |
| ILOCO clock oscillation frequency                          | f <sub>ILOCO</sub>     | 13.5    | 15     | 16.5    | kHz  | —                |
| MOCO clock oscillation frequency                           | F <sub>MOCO</sub>      | 6.8     | 8      | 9.2     | MHz  | —                |
| MOCO clock oscillation stabilization wait time             | t <sub>MOCOWT</sub>    | —       | —      | 15.0    | μs   | —                |
| HOCO clock oscillator oscillation frequency                | f <sub>HOCO16</sub>    | 15.78   | 16     | 16.22   | MHz  | -20 ≤ Ta ≤ 105°C |
|  | f <sub>HOCO18</sub>    | 17.75   | 18     | 18.25   |      |                  |
|  | f <sub>HOCO20</sub>    | 19.72   | 20     | 20.28   |      |                  |
|  | f <sub>HOCO16</sub>    | 15.71   | 16     | 16.29   | MHz  | -40 ≤ Ta ≤ -20°C |
|  | f <sub>HOCO18</sub>    | 17.68   | 18     | 18.32   |      |                  |
|  | f <sub>HOCO20</sub>    | 19.64   | 20     | 20.36   |      |                  |
| HOCO clock oscillation stabilization wait time*2           | t <sub>HOCOWT</sub>    | —       | —      | 64.7    | μs   | —                |
| HOCO period jitter   | —                      | —       | ±85    | —       | ps   | —                |
| PLL clock frequency  | f <sub>PLL</sub>       | 120     | —      | 240     | MHz  | —                |
| PLL2 clock frequency                                       | f <sub>PLL2</sub>      | 120     | —      | 240     | MHz  | —                |
| PLL/PLL2 clock oscillation stabilization wait time         | t <sub>PLLWT</sub>     | —       | —      | 174.9   | μs   | Figure 2.6       |
| PLL/PLL2 period jitter                                     | —                      | —       | ±100   | —       | ps   | —                |
| PLL/PLL2 long term jitter                                  | —                      | —       | ±300   | —       | ps   | Term: 1μs, 10μs  |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.

After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f<sub>HOCO</sub>) reaches the range for guaranteed operation.

## 2.3.2 时钟时序

Table 2.16 时钟计时

| Parameter           | Symbol                | Min     | Typ    | Max     | Unit | 测试条件             |
|---------------------|-----------------------|---------|--------|---------|------|------------------|
| EXTAL外部时钟输入周期时间     | t <sub>EXcyc</sub>    | 41.66   | —      | —       | ns   | Figure 2.3       |
| EXTAL外部时钟输入高脉冲宽度    | t <sub>EXH</sub>      | 15.83   | —      | —       | ns   |                  |
| EXTAL外部时钟输入低脉冲宽度    | t <sub>EXL</sub>      | 15.83   | —      | —       | ns   |                  |
| EXTAL外部时钟上升时间       | t <sub>EXr</sub>      | —       | —      | 5.0     | ns   |                  |
| EXTAL外部时钟下降时间       | t <sub>EXf</sub>      | —       | —      | 5.0     | ns   |                  |
| 主时钟振荡器频率            | f <sub>MAIN</sub>     | 8       | —      | 24      | MHz  | —                |
| 主时钟振荡器稳定等待时间(晶体)*1  | t <sub>MANOSCWT</sub> | —       | —      | —*1     | ms   | Figure 2.4       |
| LOCO时钟振荡频率          | f <sub>LOCO</sub>     | 29.4912 | 32.768 | 36.0448 | kHz  | —                |
| LOCO时钟振荡器稳定等待时间     | t <sub>LOCOWT</sub>   | —       | —      | 60.4    | μs   | Figure 2.5       |
| ILOCO时钟振荡频率         | f <sub>ILOCO</sub>    | 13.5    | 15     | 16.5    | kHz  | —                |
| MOCO时钟振荡频率          | F <sub>MOCO</sub>     | 6.8     | 8      | 9.2     | MHz  | —                |
| MOCO时钟振荡器稳定等待时间     | t <sub>MOCOWT</sub>   | —       | —      | 15.0    | μs   | —                |
| HOCO时钟振荡器振荡频率       | f <sub>HOCO16</sub>   | 15.78   | 16     | 16.22   | MHz  | -20 ≤ Ta ≤ 105°C |
|                     | f <sub>HOCO18</sub>   | 17.75   | 18     | 18.25   |      |                  |
|                     | f <sub>HOCO20</sub>   | 19.72   | 20     | 20.28   |      |                  |
|                     | f <sub>HOCO16</sub>   | 15.71   | 16     | 16.29   | MHz  | -40 ≤ Ta ≤ -20°C |
|                     | f <sub>HOCO18</sub>   | 17.68   | 18     | 18.32   |      |                  |
|                     | f <sub>HOCO20</sub>   | 19.64   | 20     | 20.36   |      |                  |
| HOCO时钟振荡器稳定等待时间*2   | t <sub>HOCOWT</sub>   | —       | —      | 64.7    | μs   | —                |
| HOCO周期抖动            | —                     | —       | ±85    | —       | ps   | —                |
| 锁相环时钟频率             | f <sub>PLL</sub>      | 120     | —      | 240     | MHz  | —                |
| PLL2时钟频率            | f <sub>PLL2</sub>     | 120     | —      | 240     | MHz  | —                |
| PLL/PLL2时钟振荡器稳定等待时间 | t <sub>PLLWT</sub>    | —       | —      | 174.9   | μs   | Figure 2.6       |
| PLL/PLL2周期抖动        | —                     | —       | ±100   | —       | ps   | —                |
| PLL/PLL2长期抖动        | —                     | —       | ±300   | —       | ps   | Term: 1μs, 10μs  |

注1.设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

注2.这是从复位状态释放到HOCO振荡频率(f<sub>HOCO</sub>)达到保证工作范围的时间。

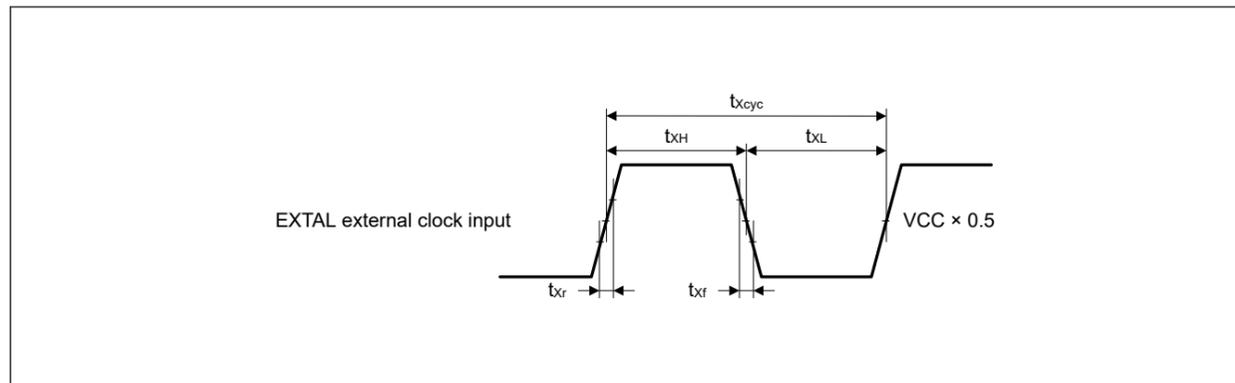


Figure 2.3 EXTAL external clock input timing

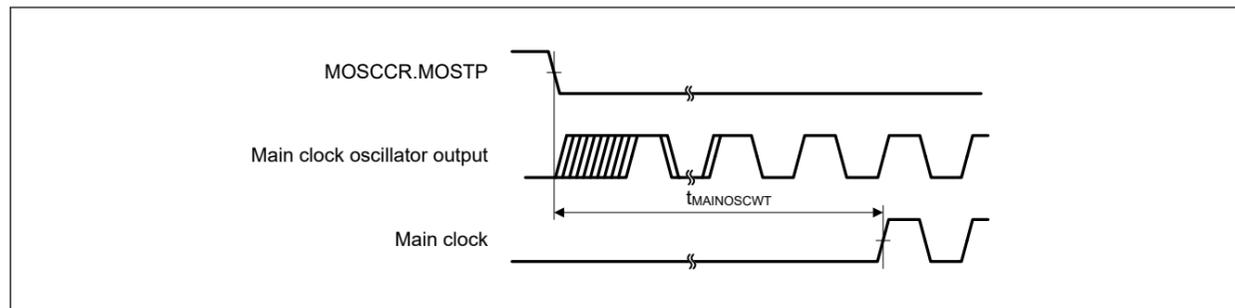


Figure 2.4 Main clock oscillation start timing

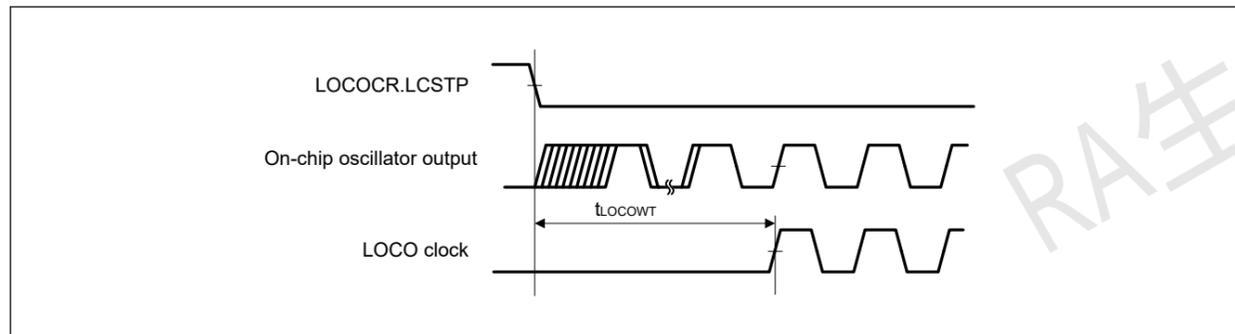


Figure 2.5 LOCO clock oscillation start timing

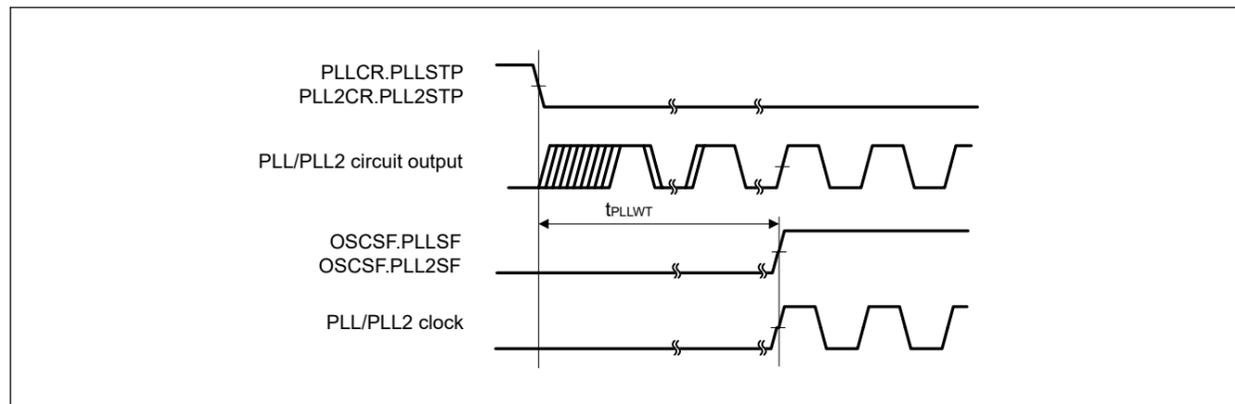


Figure 2.6 PLL/PLL2 clock oscillation start timing

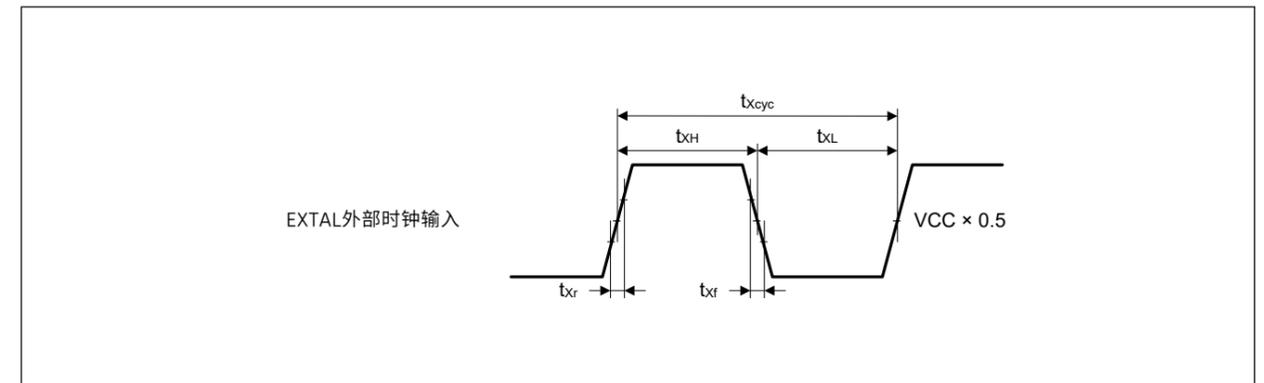


Figure 2.3 EXTAL外部时钟输入时序

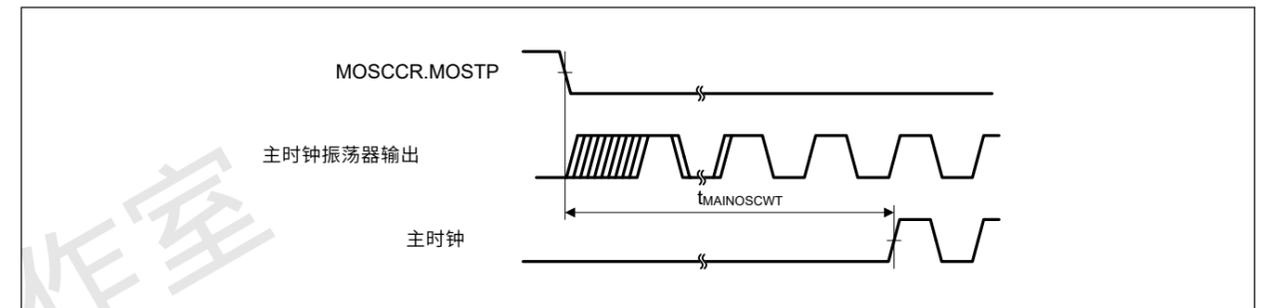


Figure 2.4 主时钟振荡开始时序

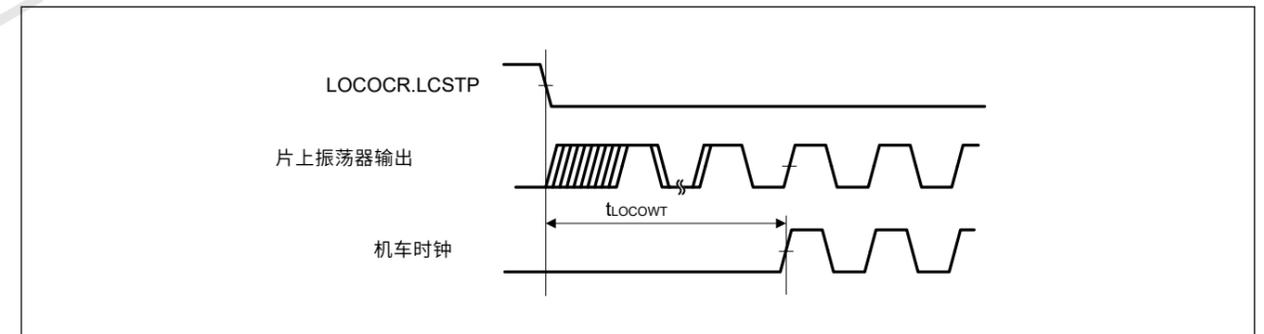


Figure 2.5 LOCO时钟振荡开始时序

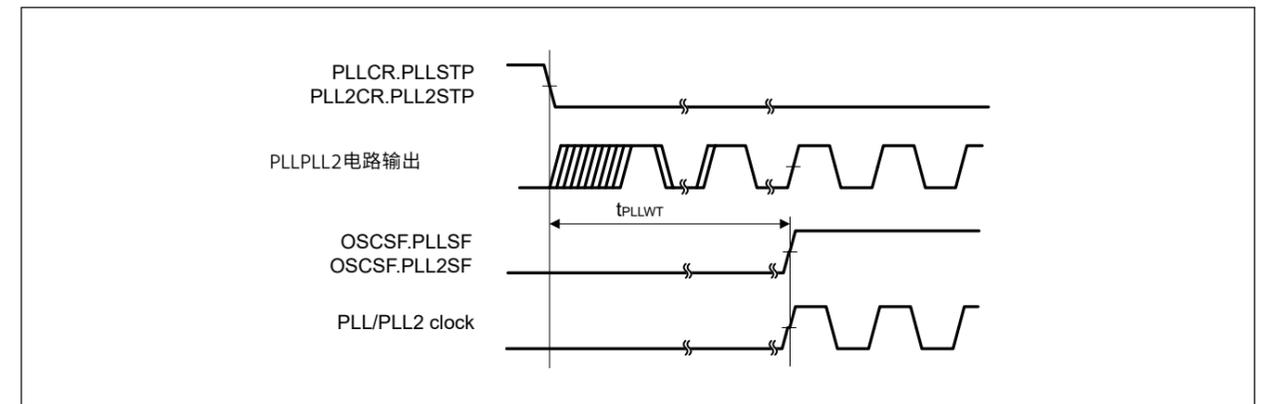


Figure 2.6 PLL/PLL2时钟振荡开始时序

2.3.3 Reset Timing

Table 2.17 Reset timing

| Parameter  | Symbol                     | Min         | Typ  | Max   | Unit    | Test conditions  |
|--|----------------------------|-------------|------|-------|---------|------------------|
| RES pulse width  | Power-on                   | $t_{RESWP}$ | 0.7  | —     | —       | ms<br>Figure 2.7 |
|  | Deep Software Standby mode | $t_{RESWD}$ | 0.6  | —     | —       | ms<br>Figure 2.8 |
|  | Software Standby mode      | $t_{RESWS}$ | 0.3  | —     | —       | ms               |
|  | All other                  | $t_{RESW}$  | 200  | —     | —       | $\mu$ s          |
| Wait time after RES cancellation   | $t_{RESWT}$                | —           | 37.3 | 41.2  | $\mu$ s | Figure 2.7       |
| Wait time after internal reset cancellation<br>(IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset) | $t_{RESW2}$                | —           | 324  | 397.7 | $\mu$ s | —                |

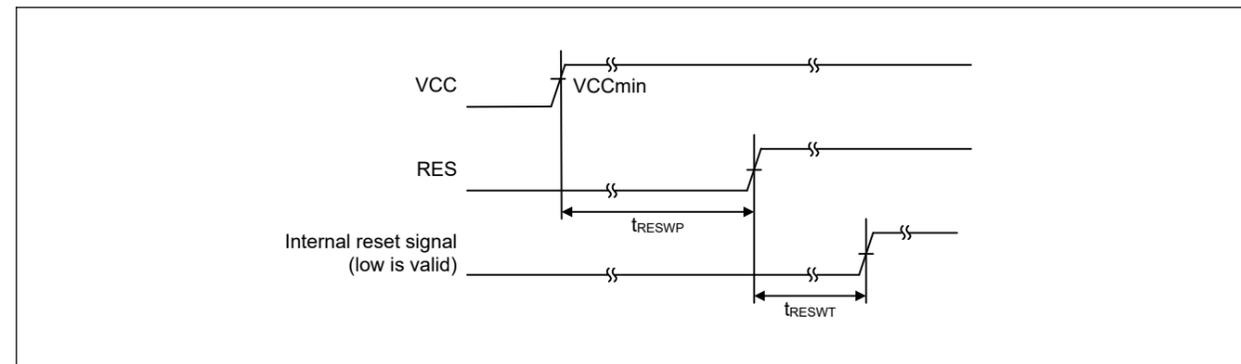


Figure 2.7 RES pin input timing under the condition that VCC exceeds  $V_{POR}$  voltage threshold

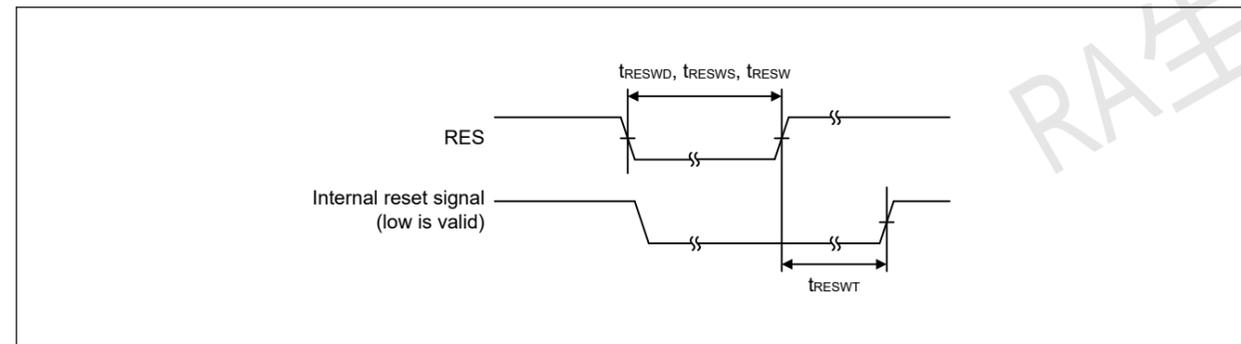


Figure 2.8 Reset input timing

2.3.3 重置时间

Table 2.17 重置时间

| Parameter  | 符号          | 最小值         | 典型值  | Max   | 单元      | 测试条件             |
|--|-------------|-------------|------|-------|---------|------------------|
| RES脉冲宽度  | Power-on    | $t_{RESWP}$ | 0.7  | —     | —       | ms<br>Figure 2.7 |
|  | 深度软件待机模式    | $t_{RESWD}$ | 0.6  | —     | —       | ms<br>Figure 2.8 |
|  | 软件待机模式      | $t_{RESWS}$ | 0.3  | —     | —       | ms               |
|  | 所有其他        | $t_{RESW}$  | 200  | —     | —       | $\mu$ s          |
| RES取消后的等待时间  | $t_{RESWT}$ | —           | 37.3 | 41.2  | $\mu$ s | Figure 2.7       |
| 内部复位取消后的等待时间 (IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、总线主控MPU错误复位、TrustZone错误复位、缓存奇偶校验错误复位) | $t_{RESW2}$ | —           | 324  | 397.7 | $\mu$ s | —                |

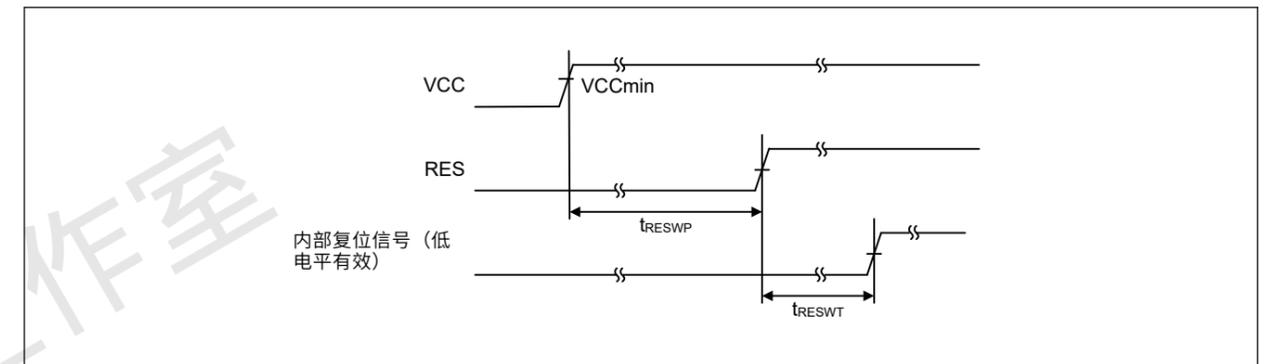


Figure 2.7 VCC超过 $V_{POR}$ 电压阈值条件下的RES引脚输入时序

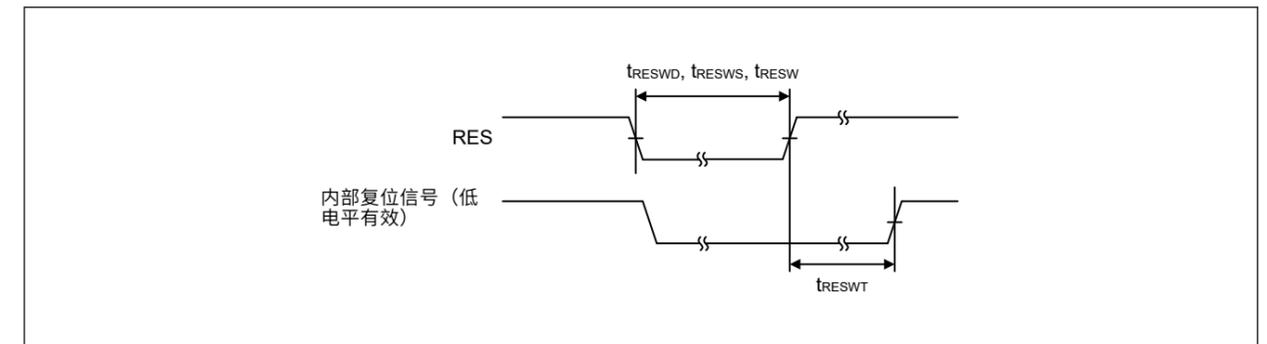


Figure 2.8 复位输入时序

2.3.4 Wakeup Timing

Table 2.18 Timing of recovery from low power modes

| Parameter  | Symbol  | Min   | Typ                    | Max   | Unit             | Test conditions |    |
|--|---|---|------------------------|-------|------------------|-----------------|----|
| Recovery time from Software Standby mode*1                 | Crystal resonator connected to main clock oscillator      | System clock source is main clock oscillator*2          | t <sub>SBYMC</sub> *11 | —     | 2.1              | 2.4             | ms |
|  |   | System clock source is PLL with main clock oscillator*3 | t <sub>SBYPC</sub> *11 | —     | 2.2              | 2.6             | ms |
|  | External clock input to main clock oscillator             | System clock source is main clock oscillator*4          | t <sub>SBYEX</sub> *11 | —     | 45               | 125             | μs |
|  |   | System clock source is PLL with main clock oscillator*5 | t <sub>SBYPE</sub> *11 | —     | 170              | 255             | μs |
|  | System clock source is LOCO*6                             | t <sub>SBYLO</sub> *11                                  | —                      | 0.7   | 0.9              | ms              |    |
|  | System clock source is HOCO clock oscillator*7            | t <sub>SBYHO</sub> *11                                  | —                      | 55    | 130              | μs              |    |
|  | System clock source is PLL with HOCO*8                    | t <sub>SBYPH</sub> *11                                  | —                      | 175   | 265              | μs              |    |
|  | System clock source is MOCO clock oscillator*9            | t <sub>SBYMO</sub> *11                                  | —                      | 35    | 65               | μs              |    |
| Recovery time from Deep Software Standby mode              | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E       | t <sub>DSBY</sub>                                       | —                      | 0.38  | 0.54             | ms              |    |
|  | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19       | t <sub>DSBY</sub>                                       | —                      | 0.55  | 0.73             | ms              |    |
| Wait time after cancellation of Deep Software Standby mode | t <sub>DSBYWT</sub>                                       | 56  | —                      | 57    | t <sub>cyc</sub> |                 |    |
| Recovery time from Software Standby mode to Snooze mode    | High-speed mode when system clock source is HOCO (20 MHz) | t <sub>SNZ</sub>  | —                      | 35*10 | 70*10            | μs              |    |
|  | High-speed mode when system clock source is MOCO (8 MHz)  | t <sub>SNZ</sub>  | —                      | 11*10 | 14*10            | μs              |    |

- Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:  
Total recovery time = recovery time for an oscillator as the system clock source + the longest t<sub>SBYOSCWT</sub> in the active oscillators - t<sub>SBYOSCWT</sub> for the system clock + 2 LOCO cycles (when LOCO is operating)
- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
- Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
- Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
- Note 6. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
- Note 7. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
- Note 8. The PLL frequency is 240 MHz and the greatest value of the internal clock division setting is 4.
- Note 9. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
- Note 10. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 μs (typical), 48 μs (maximum).
- Note 11. The recovery time can be calculated with the equation of t<sub>SBYOSCWT</sub> + t<sub>SBYSEQ</sub>. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

| Wakeup time        | TYP                         |   | MAX                         |   | Unit |
|--------------------|-----------------------------|---|-----------------------------|---|------|
|                    | t <sub>SBYOSCWT</sub>       | t <sub>SBYSEQ</sub>                                 | t <sub>SBYOSCWT</sub>       | t <sub>SBYSEQ</sub>                                 |      |
| t <sub>SBYMC</sub> | (MSTS[7:0]*32 + 3) / 0.262  | 35 + 18 / f <sub>CLK</sub> + 4n / f <sub>MAIN</sub> | (MSTS[7:0]*32 + 14) / 0.236 | 62 + 18 / f <sub>CLK</sub> + 4n / f <sub>MAIN</sub> | μs   |
| t <sub>SBYPC</sub> | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / f <sub>CLK</sub> + 4n / f <sub>PLL</sub>  | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / f <sub>CLK</sub> + 4n / f <sub>PLL</sub>  | μs   |

2.3.4 唤醒时间

Table 2.18 从低功耗模式恢复的时间

| Parameter        | Symbol  | Min                    | Typ                    | Max   | Unit             | 单元测试条件 |    |
|------------------|---|------------------------|------------------------|-------|------------------|--------|----|
| 恢复时间从软件待机模式*1    | 连接到主时钟振荡器的晶体振荡器                                     | 系统时钟源为主时钟振荡器*2         | t <sub>SBYMC</sub> *11 | —     | 2.1              | 2.4    | ms |
|                  |   | 系统时钟源为带主时钟振荡器的PLL*3    | t <sub>SBYPC</sub> *11 | —     | 2.2              | 2.6    | ms |
|                  | 主时钟振荡器的外部时钟输入                                       | 系统时钟源为主时钟振荡器*4         | t <sub>SBYEX</sub> *11 | —     | 45               | 125    | μs |
|                  |   | 系统时钟源为带主时钟振荡器的PLL*5    | t <sub>SBYPE</sub> *11 | —     | 170              | 255    | μs |
|                  | 系统时钟源为LOCO*6  | t <sub>SBYLO</sub> *11 | —                      | 0.7   | 0.9              | ms     |    |
|                  | 系统时钟源为HOCO时钟振荡器*7                                   | t <sub>SBYHO</sub> *11 | —                      | 55    | 130              | μs     |    |
|                  | 系统时钟源是带有HOCO*8的PLL                                  | t <sub>SBYPH</sub> *11 | —                      | 175   | 265              | μs     |    |
|                  | 系统时钟源为MOCO时钟振荡器*9                                   | t <sub>SBYMO</sub> *11 | —                      | 35    | 65               | μs     |    |
| 恢复时间从深度软件待机模式    | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E | t <sub>DSBY</sub>      | —                      | 0.38  | 0.54             | ms     |    |
|                  | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19 | t <sub>DSBY</sub>      | —                      | 0.55  | 0.73             | ms     |    |
| 取消深度软件待机模式后的等待时间 | t <sub>DSBYWT</sub>                                 | 56                     | —                      | 57    | t <sub>cyc</sub> |        |    |
| 恢复时间从软件待机模式到贪睡模式 | 系统时钟源为高速模式HOCO (20 MHz)                             | t <sub>SNZ</sub>       | —                      | 35*10 | 70*10            | μs     |    |
|                  | 系统时钟源为高速模式MOCO (8 MHz)                              | t <sub>SNZ</sub>       | —                      | 11*10 | 14*10            | μs     |    |

- 注1.恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=一个振荡器作为系统时钟源的恢复时间+系统时钟有效振荡器中的最长t<sub>SBYOSCWT</sub>+2个LOCO周期（当LOCO正在运行）
- 注2.当晶振频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为1时。
- 注3.当PLL的频率为240MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为4时。
- 注4.当外部时钟频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为1时。
- 注5.当PLL的频率为240MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为4时。
- 注6.LOCO频率为32.768kHz，内部时钟分频设置的最大值为1。
- 注7.HOCO频率为20MHz，内部时钟分频设置最大值为1。注8.PLL频率为240MHz，内部时钟分频设置最大值为4。注9.MOCO频率为8MHz，内部时钟分频设置的最大值为1。
- 注10.当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：16μs（典型值）、48μs（最大值）。
- 注11.恢复时间可以用t<sub>SBYOSCWT</sub>+t<sub>SBYSEQ</sub>等式计算。并且它们可以通过以下值和等式确定。对于n，从内部时钟分频设置中选择最大值。

| 唤醒时间典型值            | TYP                         |   | MAX                         |   | Unit |
|--------------------|-----------------------------|---|-----------------------------|---|------|
|                    | t <sub>SBYOSCWT</sub>       | t <sub>SBYSEQ</sub>                                 | t <sub>SBYOSCWT</sub>       | t <sub>SBYSEQ</sub>                                 |      |
| t <sub>SBYMC</sub> | (MSTS[7:0]*32 + 3) / 0.262  | 35 + 18 / f <sub>CLK</sub> + 4n / f <sub>MAIN</sub> | (MSTS[7:0]*32 + 14) / 0.236 | 62 + 18 / f <sub>CLK</sub> + 4n / f <sub>MAIN</sub> | μs   |
| t <sub>SBYPC</sub> | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / f <sub>CLK</sub> + 4n / f <sub>PLL</sub>  | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / f <sub>CLK</sub> + 4n / f <sub>PLL</sub>  | μs   |

| Wakeup time | TYP       |  | MAX       |  | Unit |
|-------------|-----------|--|-----------|--|------|
|             | tSBYOSCWT | tSBYSEQ                                | tSBYOSCWT | tSBYSEQ                                |      |
| tSBYEX      | 10        | $35 + 18 / f_{ICLK} + 4n / f_{EXMAIN}$ | 62        | $62 + 18 / f_{ICLK} + 4n / f_{EXMAIN}$ | μs   |
| tSBYPE      | 135       | $35 + 18 / f_{ICLK} + 4n / f_{PLL}$    | 192       | $62 + 18 / f_{ICLK} + 4n / f_{PLL}$    | μs   |
| tSBYLO      | 0         | $35 + 18 / f_{ICLK} + 4n / f_{LOCO}$   | 0         | $62 + 18 / f_{ICLK} + 4n / f_{LOCO}$   | μs   |
| tSBYHO      | 20        | $35 + 18 / f_{ICLK} + 4n / f_{HOCO}$   | 67        | $62 + 18 / f_{ICLK} + 4n / f_{HOCO}$   | μs   |
| tSBYPH      | 140       | $35 + 18 / f_{ICLK} + 4n / f_{PLL}$    | 202       | $62 + 18 / f_{ICLK} + 4n / f_{PLL}$    | μs   |
| tSBYMO      | 0         | $35 + 18 / f_{ICLK} + 4n / f_{MOCO}$   | 0         | $62 + 18 / f_{ICLK} + 4n / f_{MOCO}$   | μs   |

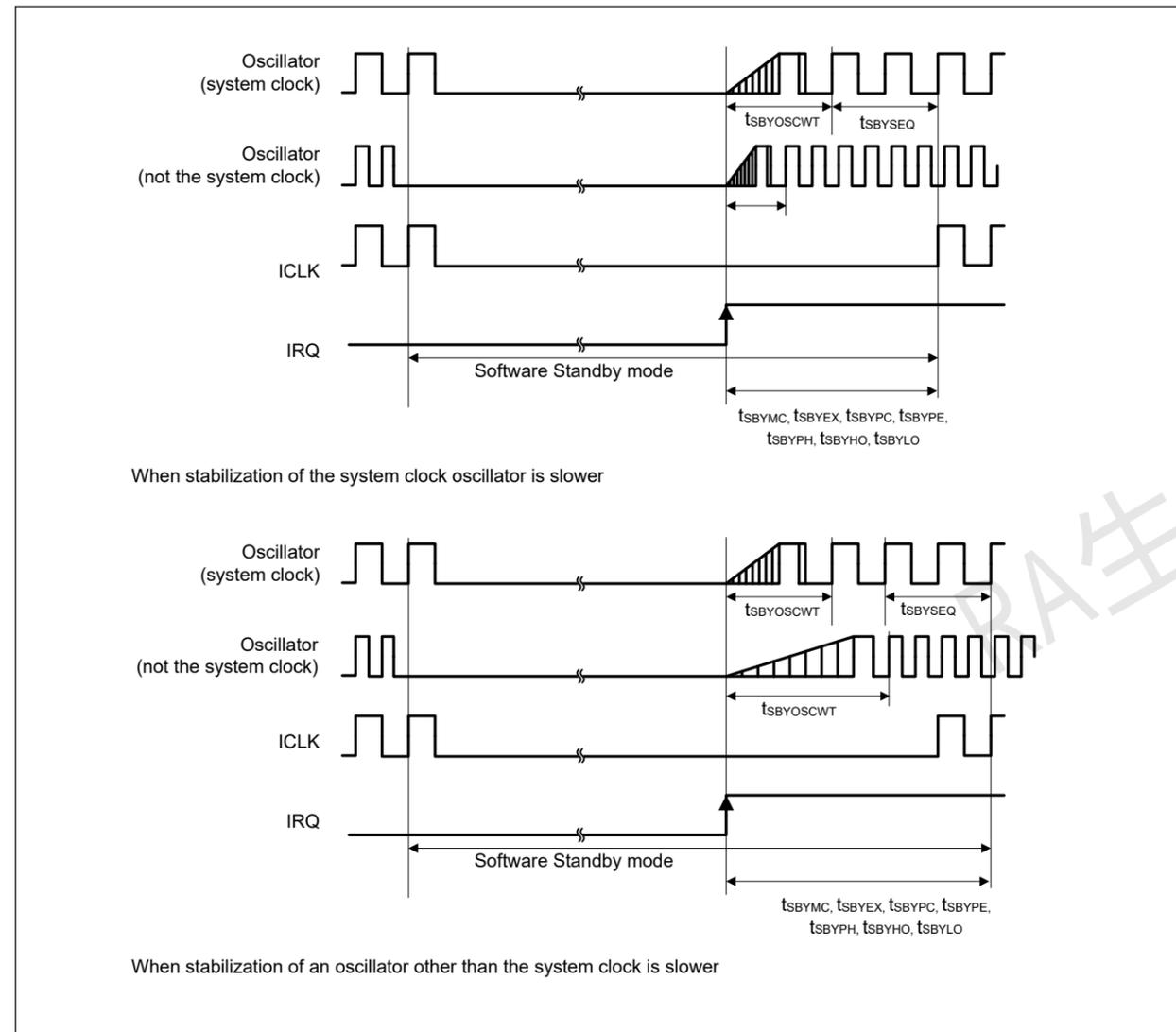


Figure 2.9 Software Standby mode cancellation timing

| 唤醒时间典型值 | TYP       |  | MAX       |  | Unit |
|---------|-----------|--|-----------|--|------|
|         | tSBYOSCWT | tSBYSEQ                                | tSBYOSCWT | tSBYSEQ                                |      |
| tSBYEX  | 10        | $35 + 18 / f_{ICLK} + 4n / f_{EXMAIN}$ | 62        | $62 + 18 / f_{ICLK} + 4n / f_{EXMAIN}$ | μs   |
| tSBYPE  | 135       | $35 + 18 / f_{ICLK} + 4n / f_{PLL}$    | 192       | $62 + 18 / f_{ICLK} + 4n / f_{PLL}$    | μs   |
| tSBYLO  | 0         | $35 + 18 / f_{ICLK} + 4n / f_{LOCO}$   | 0         | $62 + 18 / f_{ICLK} + 4n / f_{LOCO}$   | μs   |
| tSBYHO  | 20        | $35 + 18 / f_{ICLK} + 4n / f_{HOCO}$   | 67        | $62 + 18 / f_{ICLK} + 4n / f_{HOCO}$   | μs   |
| tSBYPH  | 140       | $35 + 18 / f_{ICLK} + 4n / f_{PLL}$    | 202       | $62 + 18 / f_{ICLK} + 4n / f_{PLL}$    | μs   |
| tSBYMO  | 0         | $35 + 18 / f_{ICLK} + 4n / f_{MOCO}$   | 0         | $62 + 18 / f_{ICLK} + 4n / f_{MOCO}$   | μs   |

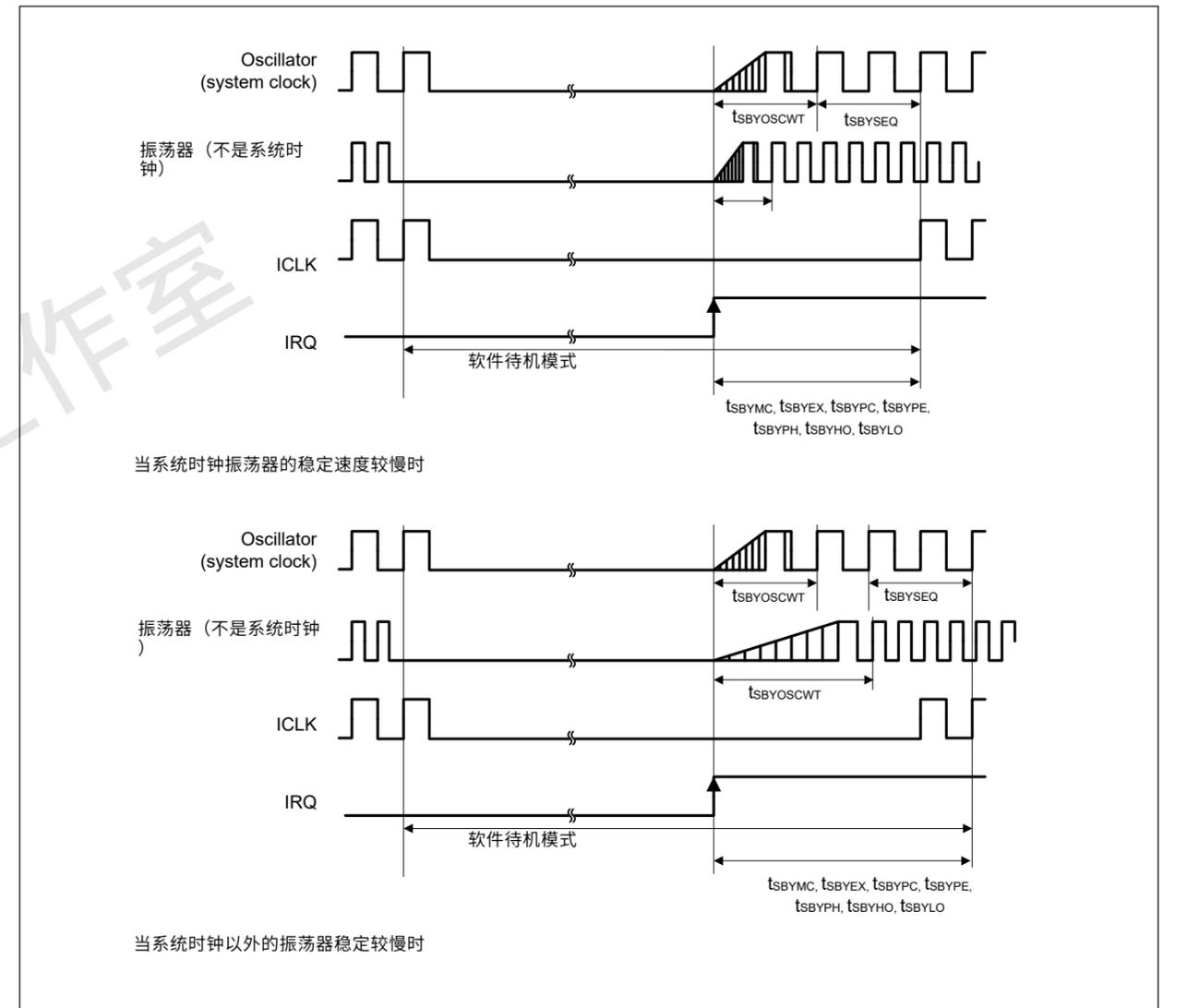


Figure 2.9 软件待机模式取消时序

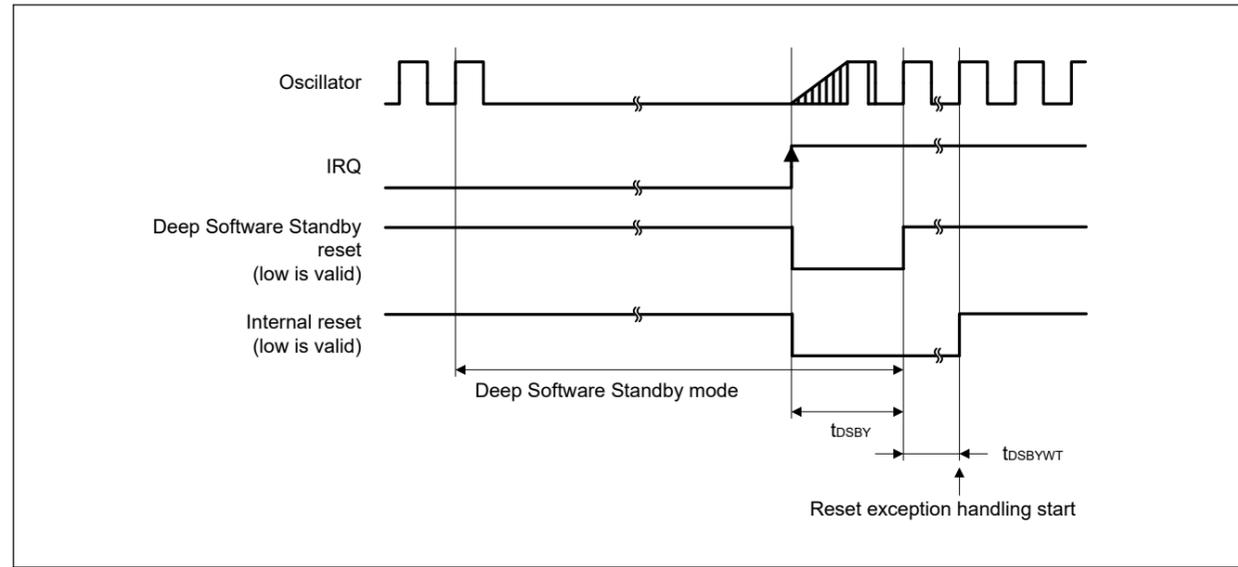


Figure 2.10 Deep Software Standby mode cancellation timing

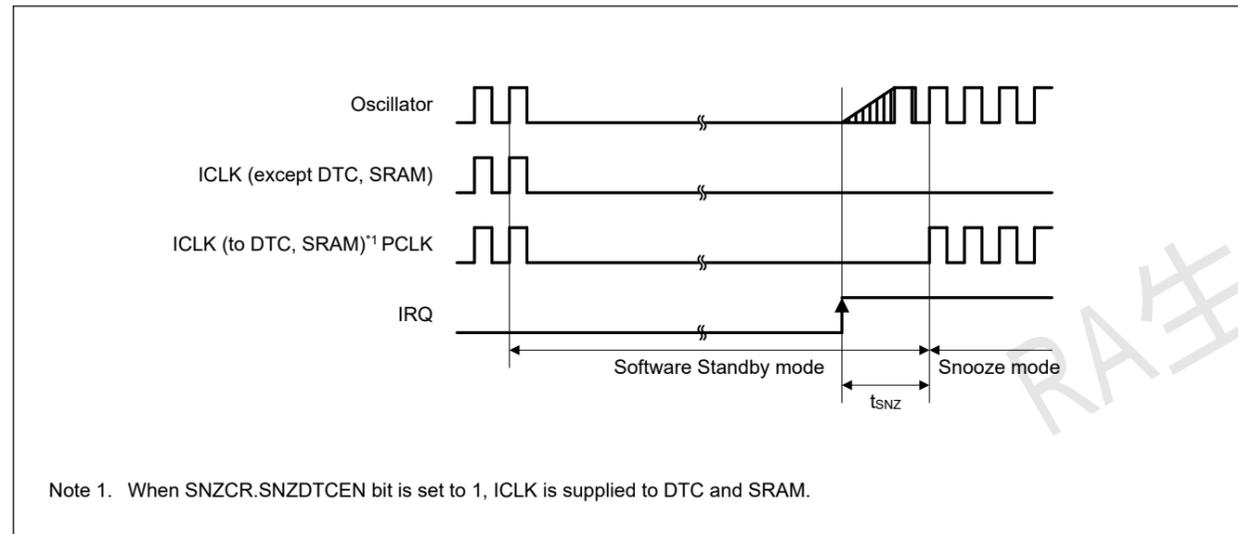


Figure 2.11 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.19 NMI and IRQ noise filter

| Parameter       | Symbol            | Min                                   | Typ | Max | Unit | Test conditions             |                                 |
|-----------------|-------------------|---------------------------------------|-----|-----|------|-----------------------------|---------------------------------|
| NMI pulse width | t <sub>NMIW</sub> | 200                                   | —   | —   | ns   | NMI digital filter disabled |                                 |
|                 |                   | t <sub>Pcyc</sub> × 2 <sup>1</sup>    | —   | —   |      |                             | t <sub>Pcyc</sub> × 2 ≤ 200 ns  |
|                 |                   | 200                                   | —   | —   |      | NMI digital filter enabled  | t <sub>NMICK</sub> × 3 ≤ 200 ns |
|                 |                   | t <sub>NMICK</sub> × 3.5 <sup>2</sup> | —   | —   |      |                             | t <sub>NMICK</sub> × 3 > 200 ns |
| IRQ pulse width | t <sub>IRQW</sub> | 200                                   | —   | —   | ns   | IRQ digital filter disabled |                                 |
|                 |                   | t <sub>Pcyc</sub> × 2 <sup>1</sup>    | —   | —   |      |                             | t <sub>Pcyc</sub> × 2 ≤ 200 ns  |
|                 |                   | 200                                   | —   | —   |      | IRQ digital filter enabled  | t <sub>IRQCK</sub> × 3 ≤ 200 ns |
|                 |                   | t <sub>IRQCK</sub> × 3.5 <sup>3</sup> | —   | —   |      |                             | t <sub>IRQCK</sub> × 3 > 200 ns |

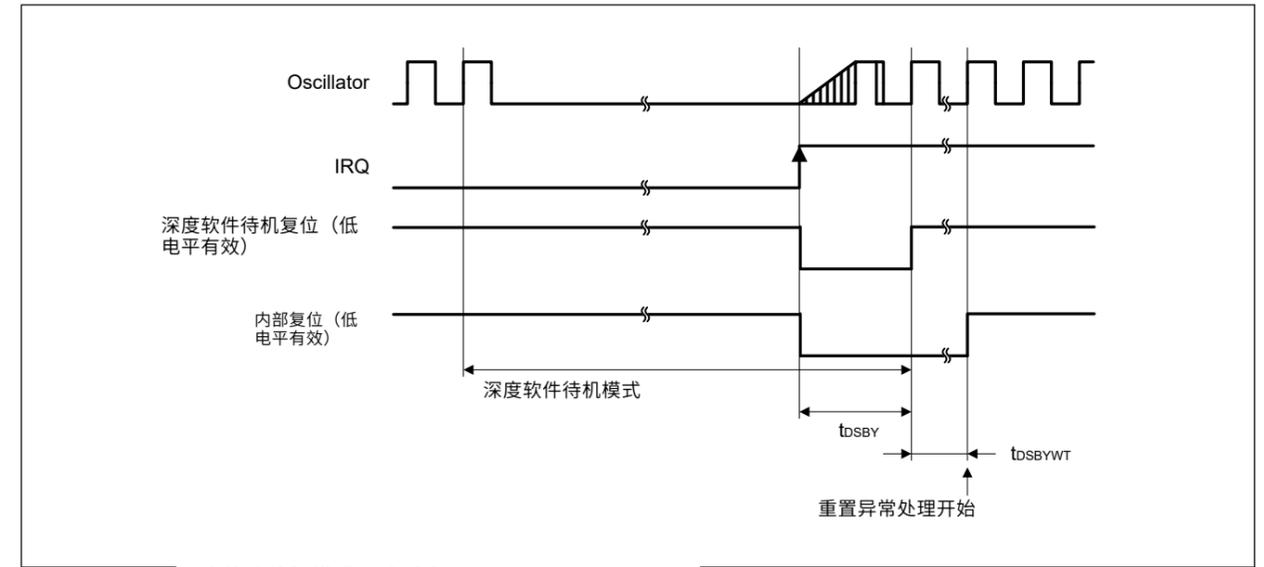


Figure 2.10 深度软件待机模式取消时序

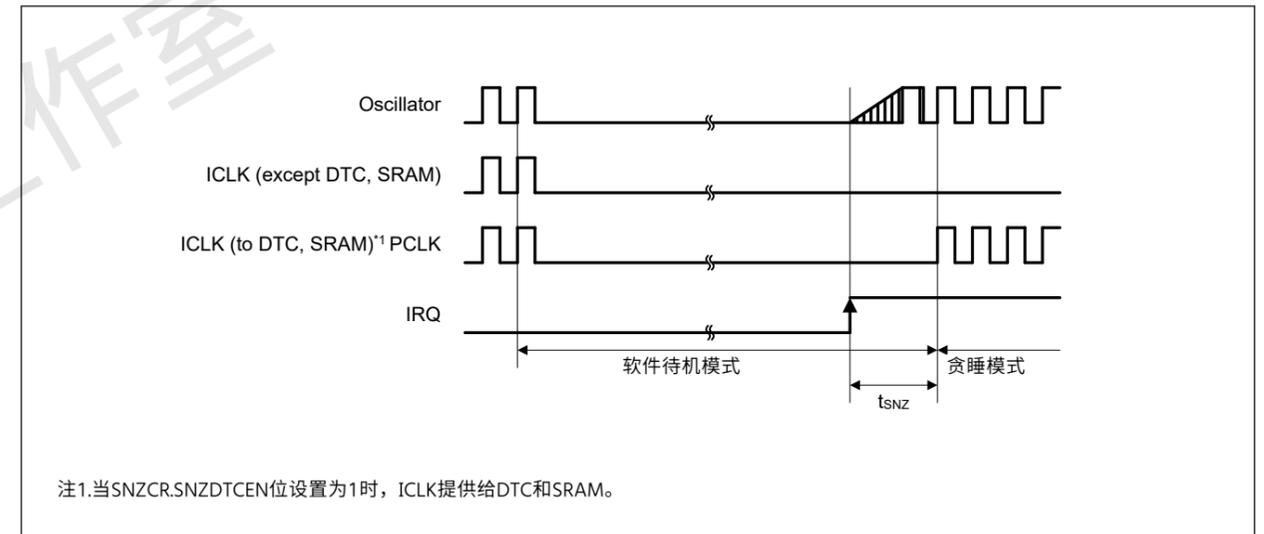


Figure 2.11 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI和IRQ噪声滤波器

Table 2.19 NMI和IRQ噪声滤波器

| Parameter | Symbol            | Min                                   | Typ | Max | Unit | 测试条件       |                                 |
|-----------|-------------------|---------------------------------------|-----|-----|------|------------|---------------------------------|
| NMI脉冲宽度   | t <sub>NMIW</sub> | 200                                   | —   | —   | ns   | NMI数字滤波器禁用 |                                 |
|           |                   | t <sub>Pcyc</sub> × 2 <sup>1</sup>    | —   | —   |      |            | t <sub>Pcyc</sub> × 2 ≤ 200 ns  |
|           |                   | 200                                   | —   | —   |      | 启用NMI数字滤波器 | t <sub>NMICK</sub> × 3 ≤ 200 ns |
|           |                   | t <sub>NMICK</sub> × 3.5 <sup>2</sup> | —   | —   |      |            | t <sub>NMICK</sub> × 3 > 200 ns |
| IRQ脉冲宽度   | t <sub>IRQW</sub> | 200                                   | —   | —   | ns   | IRQ数字滤波器禁用 |                                 |
|           |                   | t <sub>Pcyc</sub> × 2 <sup>1</sup>    | —   | —   |      |            | t <sub>Pcyc</sub> × 2 ≤ 200 ns  |
|           |                   | 200                                   | —   | —   |      | 启用IRQ数字滤波器 | t <sub>IRQCK</sub> × 3 ≤ 200 ns |
|           |                   | t <sub>IRQCK</sub> × 3.5 <sup>3</sup> | —   | —   |      |            | t <sub>IRQCK</sub> × 3 > 200 ns |

- Note: 200 ns minimum in Software Standby mode.  
 Note: If the clock source is switched, add 4 clock cycles of the switched source.  
 Note 1.  $t_{Pcyc}$  indicates the PCLKB cycle.  
 Note 2.  $t_{NMICK}$  indicates the cycle of the NMI digital filter sampling clock.  
 Note 3.  $t_{IRQCK}$  indicates the cycle of the IRQi digital filter sampling clock.

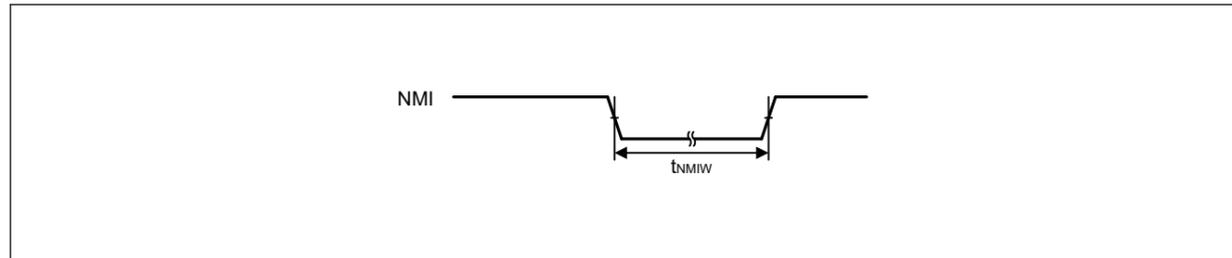


Figure 2.12 NMI interrupt input timing

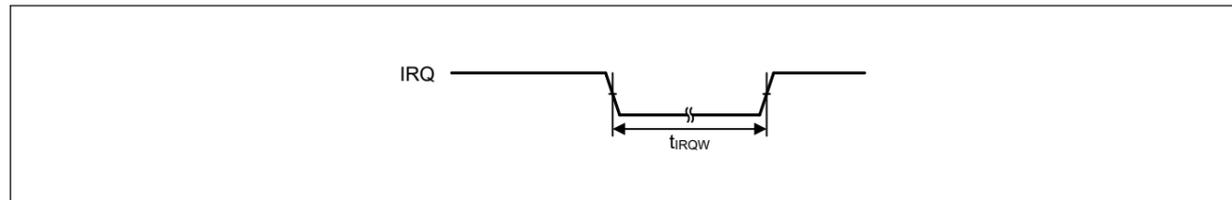


Figure 2.13 IRQ interrupt input timing

### 2.3.6 I/O Ports, POEG, GPT, AGT, KINT and ADC Trigger Timing

**Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (1 of 4)**

GPT Conditions:  
 High drive output is selected in the Port Drive Capability bit in the PmnPFS register.  
 AGT Conditions:  
 Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol                 | Min       | Typ | Max | Unit | Test conditions       |
|-----------|------------------------|-----------|-----|-----|------|-----------------------|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5 | —   | —    | $t_{Cyc}$ Figure 2.14 |

- Note: 软件待机模式下最少200ns。  
 Note: 如果时钟源切换, 则增加切换源的4个时钟周期。  
 注1.  $t_{Pcyc}$ 表示PCLKB周期。  
 注2.  $t_{NMICK}$ 表示NMI数字滤波器采样时钟的周期。注3.  $t_{IRQCK}$ 表示IRQi数字滤波器采样时钟的周期。

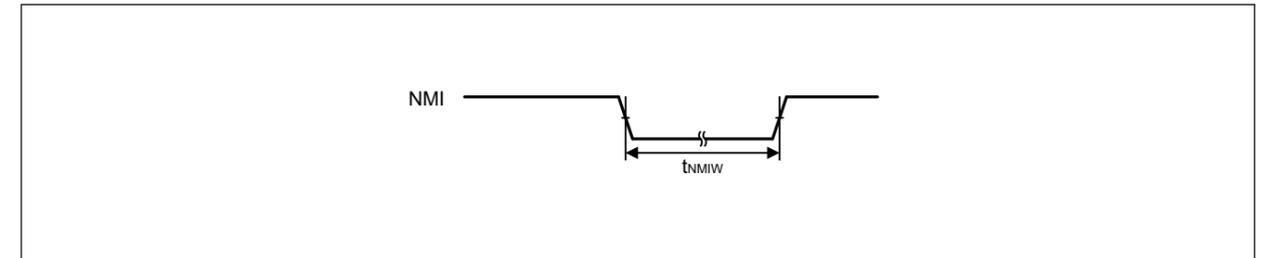


Figure 2.12 NMI中断输入时序

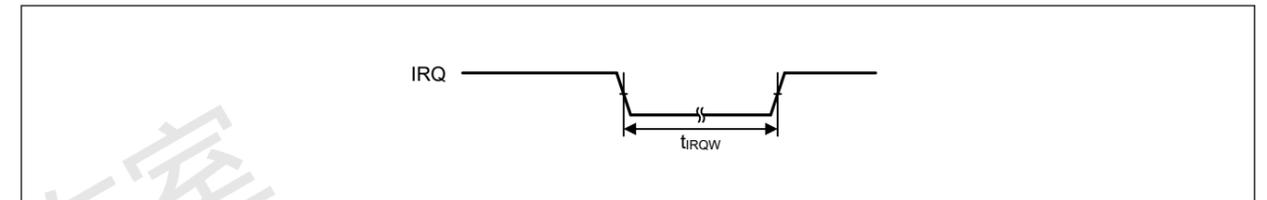


Figure 2.13 IRQ中断输入时序

### 2.3.6 IO端口、POEG、GPT、AGT、KINT和ADC触发时序

**Table 2.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序 (4个中的1个)**

GPT条件: 在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:  
 在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter | Symbol   | Min       | Typ | Max | Unit | 测试条件                  |
|-----------|----------|-----------|-----|-----|------|-----------------------|
| I/O ports | 输入数据脉冲宽度 | $t_{PRW}$ | 1.5 | —   | —    | $t_{Cyc}$ Figure 2.14 |

**Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (2 of 4)**

GPT Conditions:

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:

Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter           | Symbol  | Min                  | Typ | Max | Unit                     | Test conditions  |
|---------------------|---|----------------------|-----|-----|--------------------------|--|
| POEG                | GTETRn input pulse width  | t <sub>POEW</sub>    | 1.5 | —   | —                        | t <sub>Pcyc</sub> <a href="#">Figure 2.15</a>  |
| Output disable time | Input level detection of the GTETRn pin (via flag)  | t <sub>POEGDI</sub>  | —   | —   | 3 PCLKB + 0.34           | μs <a href="#">Figure 2.16</a><br>When the digital noise filter is not in use (POEGn.NFE N = 0 (n = A to D))   |
|                     | Detection of the output stopping signal from GPT (deadtime error, simultaneous high output, or simultaneous low output) | t <sub>POEGDE</sub>  | —   | —   | 0.5                      | μs <a href="#">Figure 2.17</a>   |
|                     | Edge detection signal from a comparator   | t <sub>POEGDC</sub>  | —   | —   | 4 PCLKB + 0.5            | μs <a href="#">Figure 2.18</a><br>The time is that when the noise filter for ACPHNS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACPHNS. |
|                     | Register setting  | t <sub>POEGDS</sub>  | —   | —   | 1 PCLKB + 0.3            | μs <a href="#">Figure 2.19</a><br>Time for access to the register is not included.   |
|                     | Oscillation stop detection <sup>*3</sup>  | t <sub>POEGDOS</sub> | —   | ≤ 1 | —                        | μs <a href="#">Figure 2.20</a>   |
|                     | Input level detection of the GTETRn pin (direct path)   | t <sub>POEGDDI</sub> | —   | —   | 2 PCLKB + 1 PCLKD + 0.34 | μs <a href="#">Figure 2.21</a>   |
|                     | Level detection signal from a comparator  | t <sub>POEGDDC</sub> | —   | —   | 3 PCLKD + 0.3            | μs <a href="#">Figure 2.22</a><br>The time is that when the noise filter for ACPHNS is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by ACPHNS. |

**Table 2.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（4个中的2个）**

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:

在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter | Symbol                            | Min                  | Typ | Max | Unit                     | 测试条件  |
|-----------|-----------------------------------|----------------------|-----|-----|--------------------------|---|
| POEG      | GTETRn输入脉冲宽度                      | t <sub>POEW</sub>    | 1.5 | —   | —                        | t <sub>Pcyc</sub> <a href="#">Figure 2.15</a>   |
| 输出禁用时间    | 的输入电平检测 GTETRn pin (via flag)     | t <sub>POEGDI</sub>  | —   | —   | 3 PCLKB + 0.34           | μs <a href="#">Figure 2.16</a><br>当不使用数字噪声滤波器时 (POEGn.NFEN=0 (n=A到D))                       |
|           | 检测来自GPT的输出停止信号 (死区错误、同时高输出或同时低输出) | t <sub>POEGDE</sub>  | —   | —   | 0.5                      | μs <a href="#">Figure 2.17</a>  |
|           | 来自比较器的边缘检测信号                      | t <sub>POEGDC</sub>  | —   | —   | 4 PCLKB + 0.5            | μs <a href="#">Figure 2.18</a><br>时间是不使用ACMPHS的噪声滤波器时 (CMPCTL.CDFS[1:0]=00)，不包括ACMPHS检测的时间。 |
|           | 注册设置                              | t <sub>POEGDS</sub>  | —   | —   | 1 PCLKB + 0.3            | μs <a href="#">Figure 2.19</a><br>不包括访问寄存器的时间。  |
|           | 振荡停止检测*3                          | t <sub>POEGDOS</sub> | —   | ≤ 1 | —                        | μs <a href="#">Figure 2.20</a>  |
|           | GTETRn引脚的输入电平检测 (直接路径)            | t <sub>POEGDDI</sub> | —   | —   | 2 PCLKB + 1 PCLKD + 0.34 | μs <a href="#">Figure 2.21</a>  |
|           | 来自比较器的电平检测信号                      | t <sub>POEGDDC</sub> | —   | —   | 3 PCLKD + 0.3            | μs <a href="#">Figure 2.22</a><br>时间是不使用ACMPHS的噪声滤波器时 (CMPCTL.CDFS[1:0]=00)，不包括ACMPHS检测的时间。 |

**Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (3 of 4)**

GPT Conditions:  
 High drive output is selected in the Port Drive Capability bit in the PmnPFS register.  
 AGT Conditions:  
 Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter  |   | Symbol                                  | Min                                       | Typ | Max | Unit | Test conditions                |
|--|---|---|---|-----|-----|------|--------------------------------|
| GPT  | Input capture pulse width                           | Single edge                             | t <sub>GTICW</sub>                        | 1.5 | —   | —    | t <sub>PDcyc</sub> Figure 2.23 |
|  |   | Dual edge                               |   | 2.5 | —   | —    |                                |
| GPT  | GTIOCxY output skew (x = 0 to 3, Y = A or B)        | Middle drive buffer                     | t <sub>GTISK</sub> <sup>*1</sup>          | —   | —   | 4    | ns Figure 2.24                 |
|  |   | High drive buffer                       |   | —   | —   | 4    |                                |
|  |   | High current output buffer              |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY output skew (x = 4 to 6, Y = A or B)        | Middle drive buffer                     |   | —   | —   | 4    |                                |
|  |   | High drive buffer                       |   | —   | —   | 4    |                                |
|  |   | High current output buffer              |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY output skew (x = 7 to 9, Y = A or B)        | Middle drive buffer                     |   | —   | —   | 4    |                                |
|  |   | High drive buffer                       |   | —   | —   | 4    |                                |
|  |   | High current output buffer              |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY output skew (x = 0 to 9, Y = A or B)        | Middle drive buffer                     |   | —   | —   | 6    |                                |
|  |   | High drive buffer                       |   | —   | —   | 6    |                                |
|  |   | High current output buffer              |   | —   | —   | 6    |                                |
| OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO |   | t <sub>GTOSK</sub>                      | —   | —   | 5   | ns   | Figure 2.25                    |
| External trigger input pulse width                             | Synchronous clock                                   | Single-edge setting                     | t <sub>GTEW</sub>                         | 1.5 | —   | —    | t <sub>PCyc</sub> Figure 2.26  |
|  |   | Both-edge setting                       |   | 2.5 | —   | —    |                                |
|  | Asynchronous clock                                  | Single-edge setting                     |   | 2.5 | —   | —    |                                |
|  |   | Both-edge setting                       |   | 3.5 | —   | —    |                                |
| Timer clock pulse width  | Synchronous clock                                   | Single-edge setting                     | t <sub>GTCKWH</sub> , t <sub>GTCKWL</sub> | 1.5 | —   | —    | t <sub>PCyc</sub> Figure 2.27  |
|  |   | Both-edge setting                       |   | 2.5 | —   | —    |                                |
|  | Asynchronous clock                                  | Single-edge setting                     |   | 2.5 | —   | —    |                                |
|  |   | Both-edge setting                       |   | 3.5 | —   | —    |                                |
| GPT (PWM Delay Generation Circuit)                             | GTIOCxY_Z skew (x = 0 to 3, Y = A or B, Z = A to D) | t <sub>HRSK</sub> <sup>*2</sup>         | —   | —   | 4.0 | ns   | Figure 2.28                    |
| AGT  | AGTIO, AGTEE input cycle                            | t <sub>ACYC</sub> <sup>*2</sup>         | 50  | —   | —   | ns   | Figure 2.29                    |
|  | AGTIO, AGTEE input high width, low width            | t <sub>ACKWH</sub> , t <sub>ACKWL</sub> | 20  | —   | —   | ns   |                                |
|  | AGTIO, AGTO, AGTOA, AGTOB output cycle              | t <sub>ACYC2</sub>                      | 33.3                                      | —   | —   | ns   |                                |
| KINT   | KRn (n = 00 to 07) pulse width                      | t <sub>KR</sub>                         | 250                                       | —   | —   | ns   | Figure 2.30                    |

**Table 2.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序 (3of4)**

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。  
 AGT Conditions:  
 在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter  |                                   | Symbol                                  | Min                                       | Typ | Max | Unit | 测试条件                           |
|--|-----------------------------------|---|---|-----|-----|------|--------------------------------|
| GPT  | 输入捕捉脉冲宽度                          | 单边                                      | t <sub>GTICW</sub>                        | 1.5 | —   | —    | t <sub>PDcyc</sub> Figure 2.23 |
|  |                                   | 双刃                                      |   | 2.5 | —   | —    |                                |
| GPT  | GTIOCxY输出偏差 (x=0到3, Y=A或B)        | 中间驱动缓冲器                                 | t <sub>GTISK</sub> <sup>*1</sup>          | —   | —   | 4    | ns Figure 2.24                 |
|  |                                   | 高驱动缓冲器                                  |   | —   | —   | 4    |                                |
|  |                                   | 大电流输出缓冲器                                |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY输出偏移 (x=4到6, Y=A或B)        | 中间驱动缓冲器                                 |   | —   | —   | 4    |                                |
|  |                                   | 高驱动缓冲器                                  |   | —   | —   | 4    |                                |
|  |                                   | 大电流输出缓冲器                                |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY输出偏移 (x=7到9, Y=A或B)        | 中间驱动缓冲器                                 |   | —   | —   | 4    |                                |
|  |                                   | 高驱动缓冲器                                  |   | —   | —   | 4    |                                |
|  |                                   | 大电流输出缓冲器                                |   | —   | —   | 4    |                                |
| GPT  | GTIOCxY输出偏移 (x=0到9, Y=A或B)        | 中间驱动缓冲器                                 |   | —   | —   | 6    |                                |
|  |                                   | 高驱动缓冲器                                  |   | —   | —   | 6    |                                |
|  |                                   | 大电流输出缓冲器                                |   | —   | —   | 6    |                                |
| OPS输出偏差GTOUUP、GTOULO、GTOVUP、GTOVLO、GTOWUP、GTOWLO |                                   | t <sub>GTOSK</sub>                      | —   | —   | 5   | ns   | Figure 2.25                    |
| 外部触发输入脉冲宽度                                       | Synchronous clock                 | Single-edge setting                     | t <sub>GTEW</sub>                         | 1.5 | —   | —    | t <sub>PCyc</sub> Figure 2.26  |
|  |                                   | Both-edge setting                       |   | 2.5 | —   | —    |                                |
|  | Asynchronous clock                | Single-edge setting                     |   | 2.5 | —   | —    |                                |
|  |                                   | Both-edge setting                       |   | 3.5 | —   | —    |                                |
| 定时器时钟脉冲宽度  | Synchronous clock                 | Single-edge setting                     | t <sub>GTCKWH</sub> , t <sub>GTCKWL</sub> | 1.5 | —   | —    | t <sub>PCyc</sub> Figure 2.27  |
|  |                                   | Both-edge setting                       |   | 2.5 | —   | —    |                                |
|  | Asynchronous clock                | Single-edge setting                     |   | 2.5 | —   | —    |                                |
|  |                                   | Both-edge setting                       |   | 3.5 | —   | —    |                                |
| GPT (PWM Delay Generation Circuit)               | GTIOCxY_Z偏斜 (x=0到3, Y=A或B, Z=A到D) | t <sub>HRSK</sub> <sup>*2</sup>         | —   | —   | 4.0 | ns   | Figure 2.28                    |
| AGT  | AGTIO、AGTEE输入周期                   | t <sub>ACYC</sub> <sup>*2</sup>         | 50  | —   | —   | ns   | Figure 2.29                    |
|  | AGTIO、AGTEE输入高宽、低宽                | t <sub>ACKWH</sub> , t <sub>ACKWL</sub> | 20  | —   | —   | ns   |                                |
|  | AGTIO、AGTO、AGTOA、AGTOB输出周期        | t <sub>ACYC2</sub>                      | 33.3                                      | —   | —   | ns   |                                |
| KINT   | KRn(n=00to07)脉冲宽度                 | t <sub>KR</sub>                         | 250                                       | —   | —   | ns   | Figure 2.30                    |

**Table 2.20 I/O ports, POEG, GPT, AGT, KINT and ADC trigger timing (4 of 4)**

GPT Conditions:  
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.  
AGT Conditions:  
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol                        | Min               | Typ | Max | Unit | Test conditions                |
|-----------|-------------------------------|-------------------|-----|-----|------|--------------------------------|
| ADC       | ADC trigger input pulse width | t <sub>TRGW</sub> | 1.5 | —   | —    | t <sub>ADcyc</sub> Figure 2.31 |

Note: t<sub>ICLK</sub>: ICLK cycle, t<sub>PCLKB</sub>: PCLKB cycle, t<sub>PDcyc</sub>: GTCLK cycle, t<sub>ADcyc</sub>: ADCLK cycle.  
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.  
Note 2. Constraints on input cycle:  
When not switching the source clock: t<sub>Pcyc</sub> × 2 < t<sub>ACYC</sub> should be satisfied.  
When switching the source clock: t<sub>Pcyc</sub> × 6 < t<sub>ACYC</sub> should be satisfied.  
Note 3. Reference value.

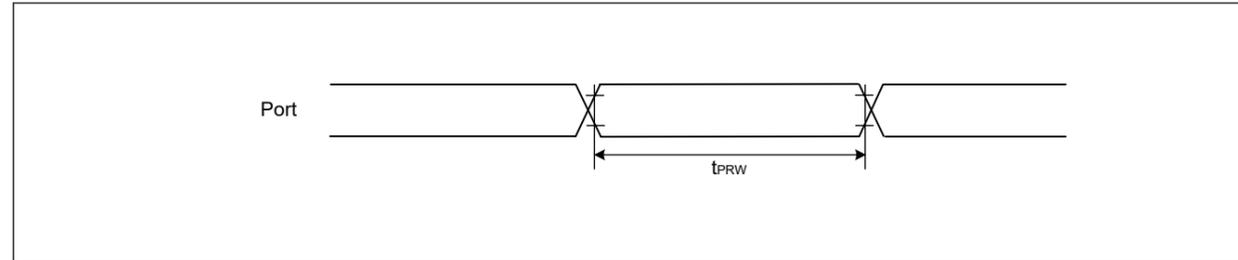


Figure 2.14 I/O ports input timing

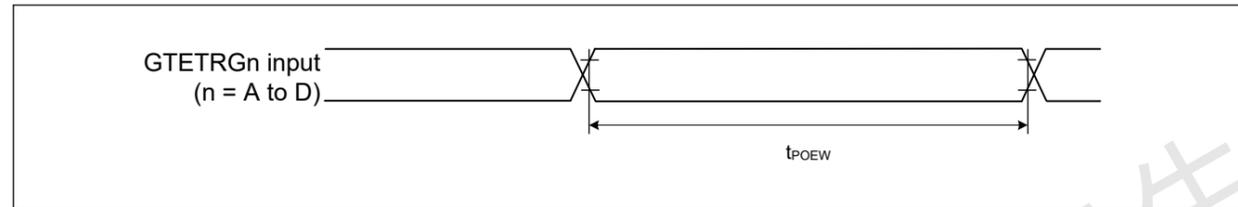


Figure 2.15 POEG input trigger timing

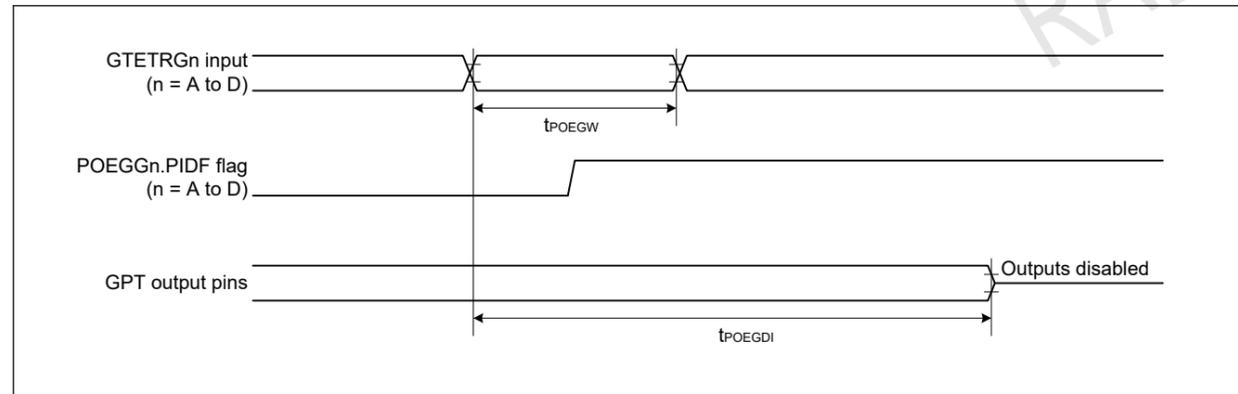


Figure 2.16 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRn pin

**Table 2.20 IO端口、POEG、GPT、AGT、KINT和ADC触发时序（4个中的4个）**

GPT条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。  
AGT条件：  
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter | Symbol      | Min               | Typ | Max | Unit | 测试条件                           |
|-----------|-------------|-------------------|-----|-----|------|--------------------------------|
| ADC       | ADC触发输入脉冲宽度 | t <sub>TRGW</sub> | 1.5 | —   | —    | t <sub>ADcyc</sub> Figure 2.31 |

Note: t<sub>ICLK</sub>: ICLK cycle, t<sub>PCLKB</sub>: PCLKB cycle, t<sub>PDcyc</sub>: GTCLK cycle, t<sub>ADcyc</sub>: ADCLK cycle.  
注1.当使用相同的驱动器IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。  
注2.输入周期的限制：  
不切换源时钟时：t<sub>Pcyc</sub>×2<t<sub>ACYC</sub>应满足。  
切换源时钟时：t<sub>Pcyc</sub>×6<t<sub>ACYC</sub>应满足。  
注3.参考值。

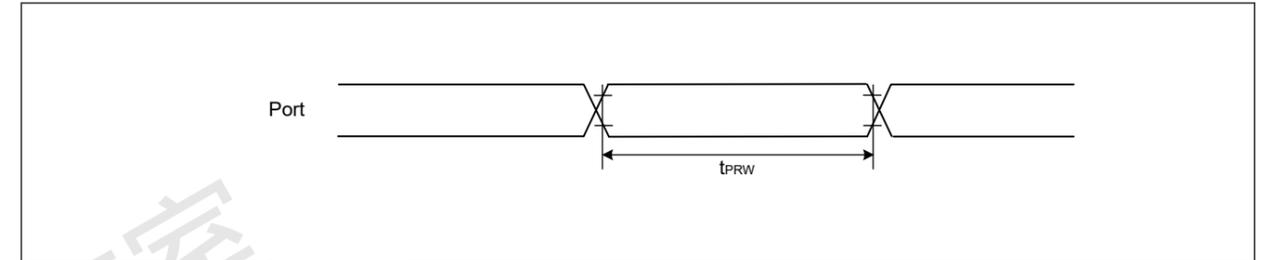


Figure 2.14 IO端口输入时序

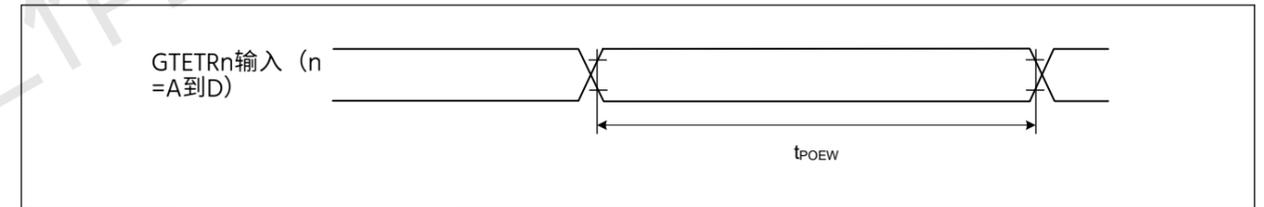


Figure 2.15 POEG输入触发时序

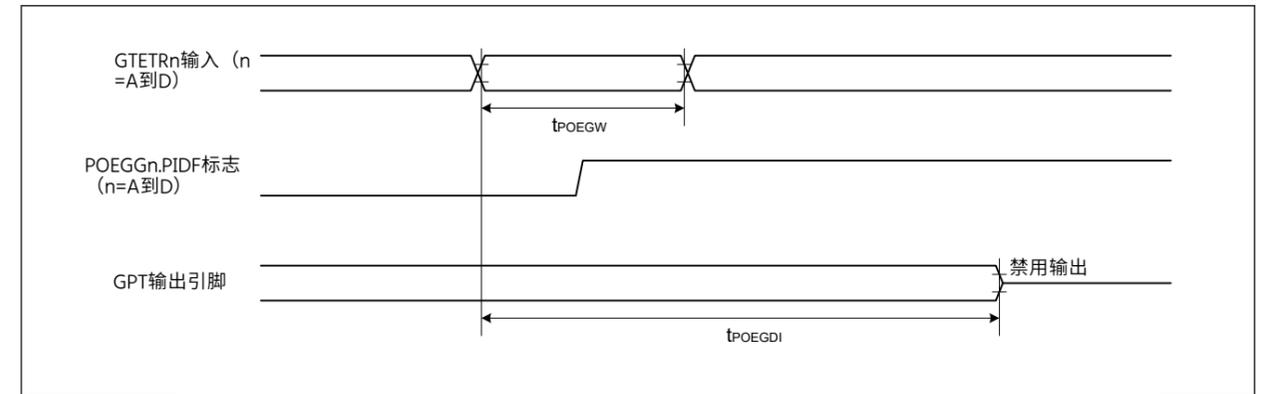


Figure 2.16 响应GTETRn引脚的输入电平检测，通过检测标志的POEG输出禁用时间

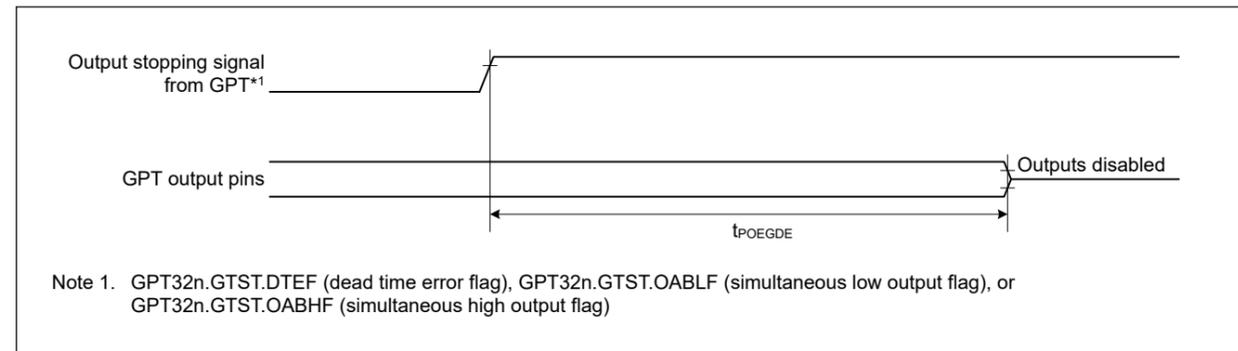


Figure 2.17 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPT

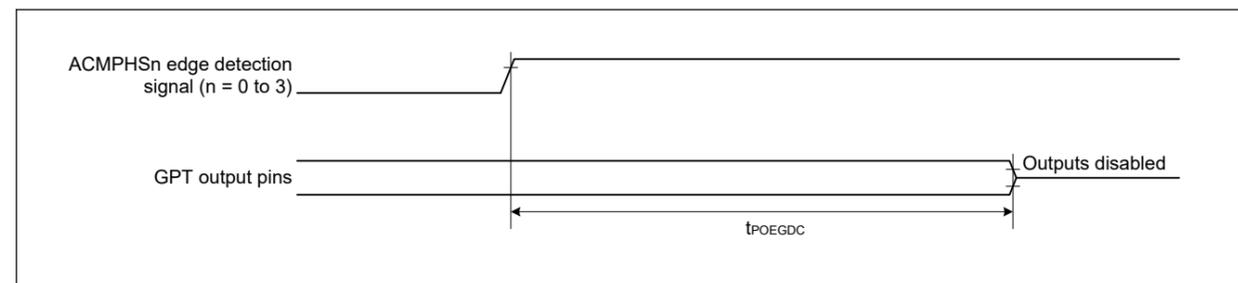


Figure 2.18 Output Disable Time for POEG in Response to Edge Detection Signal from ACMPHS

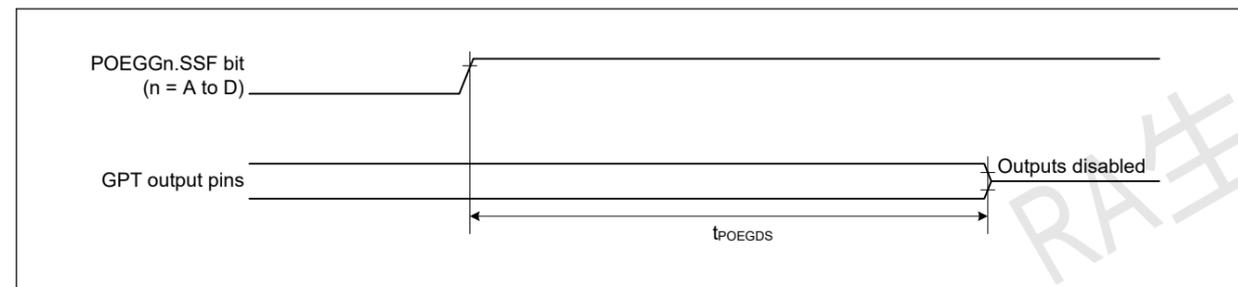


Figure 2.19 Output Disable Time for POEG in Response to the Register Setting

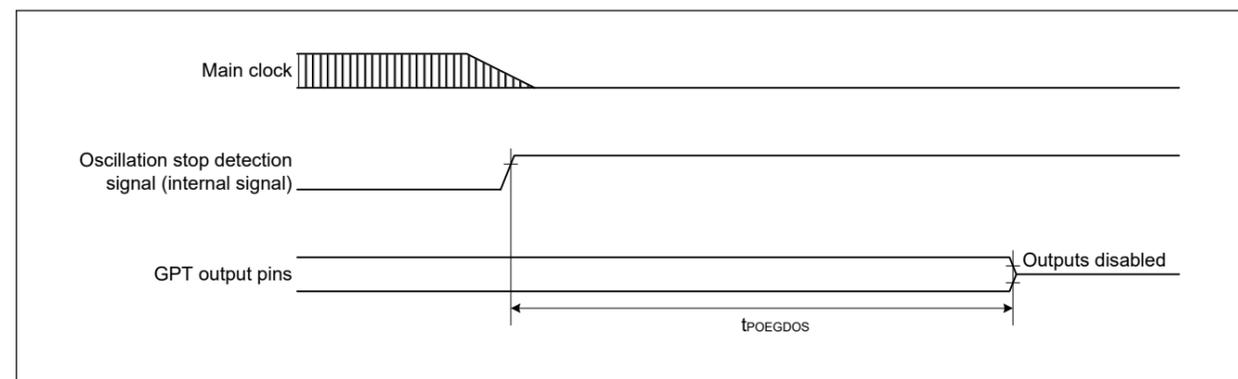


Figure 2.20 Output Disable Time of POEG in Response to the Oscillation Stop Detection

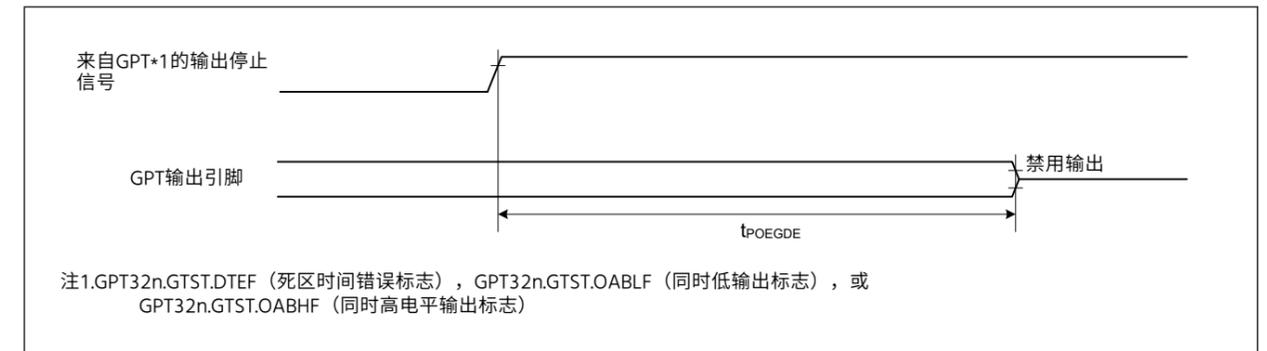


Figure 2.17 POEG响应检测到输出停止信号的输出禁用时间

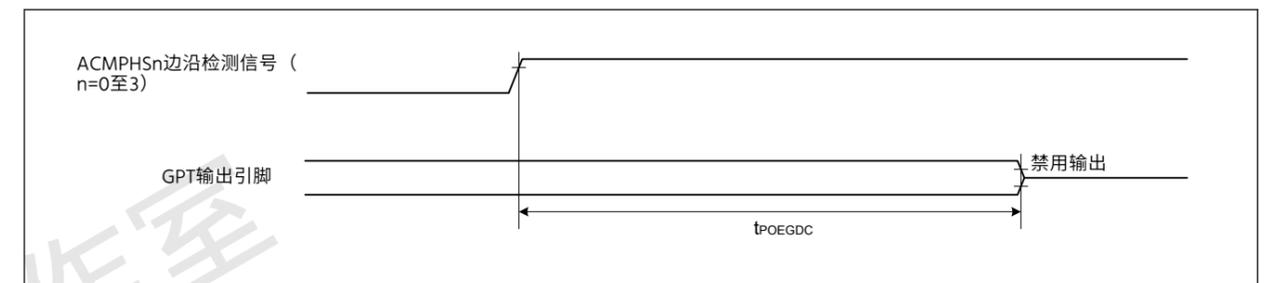


Figure 2.18 POEG响应来自ACMPHS的边缘检测信号的输出禁用时间

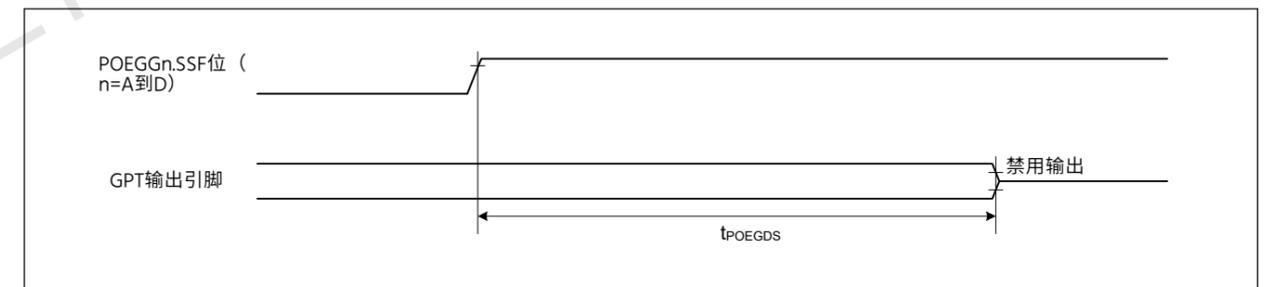


Figure 2.19 POEG响应寄存器设置的输出禁用时间

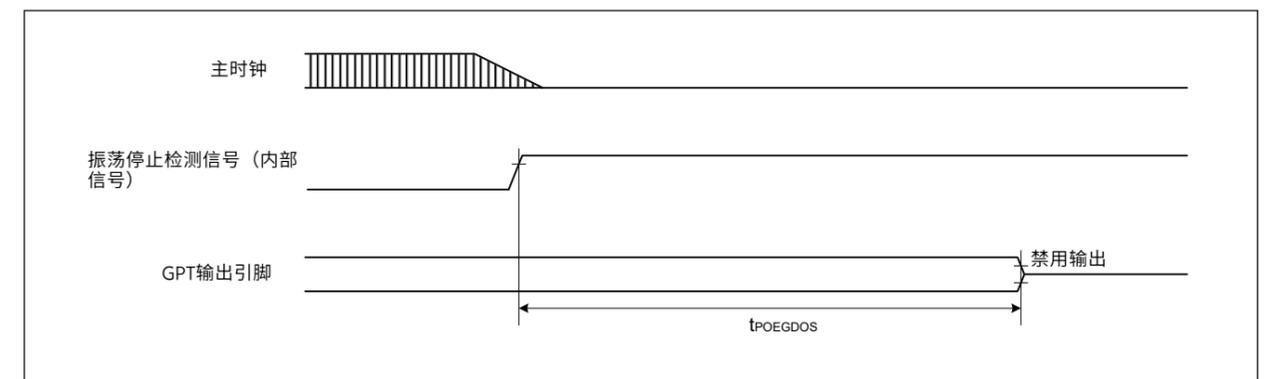


Figure 2.20 POEG响应振荡停止检测的输出禁用时间

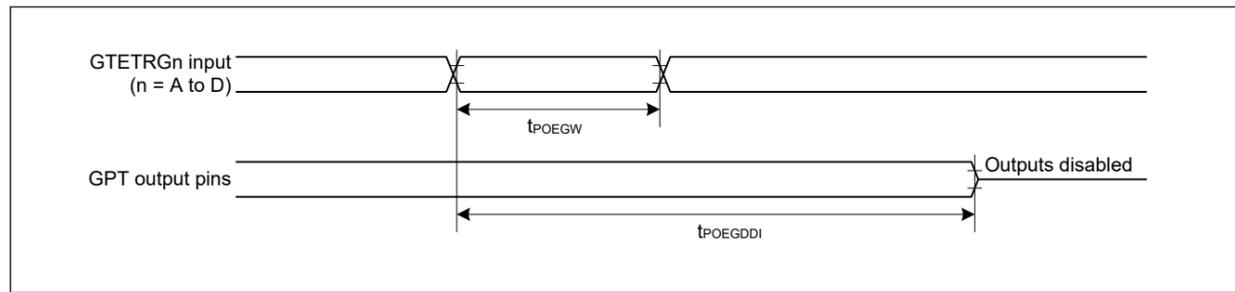


Figure 2.21 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRn pin

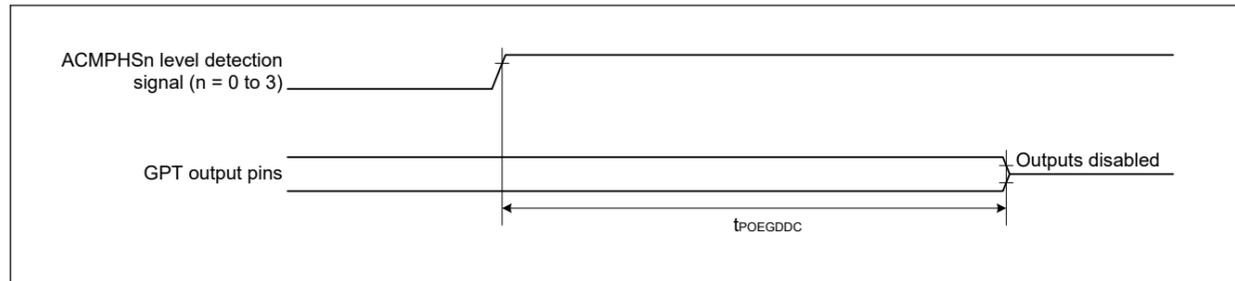


Figure 2.22 Output Disable Time for POEG in Response to Level Detection Signal from ACMPHS

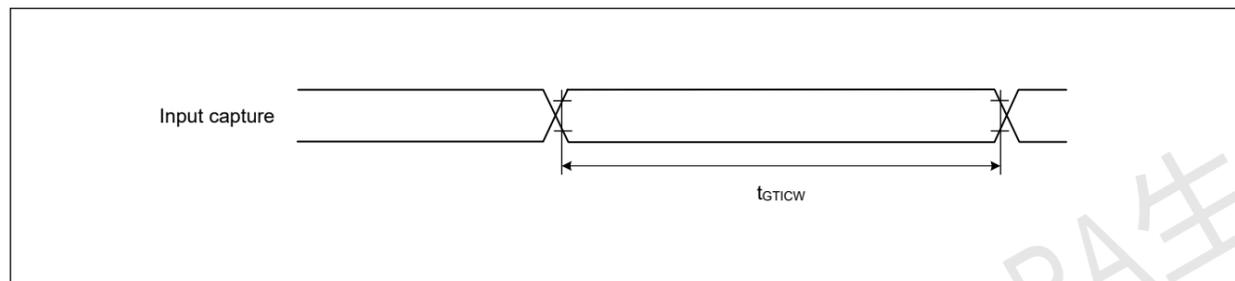


Figure 2.23 GPT input capture timing

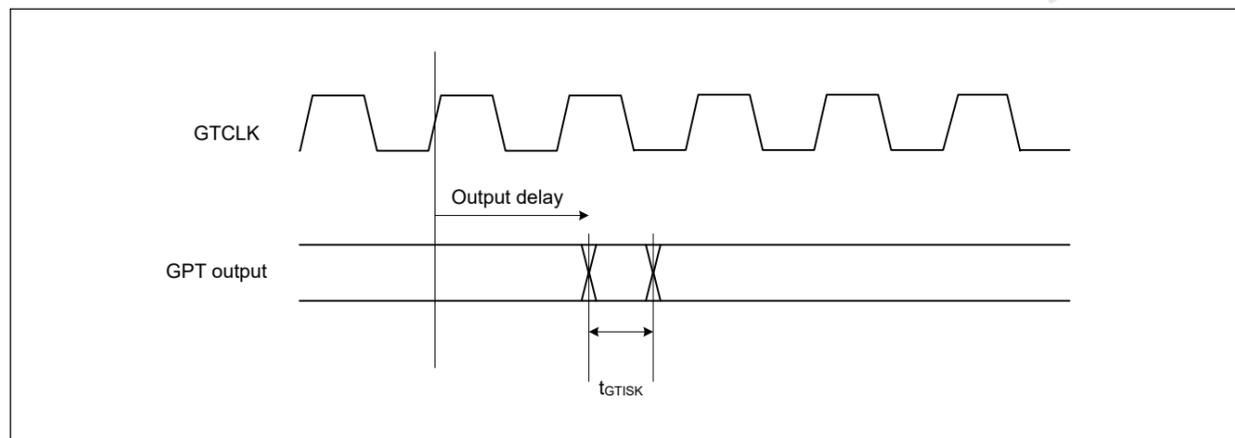


Figure 2.24 GPT output delay skew

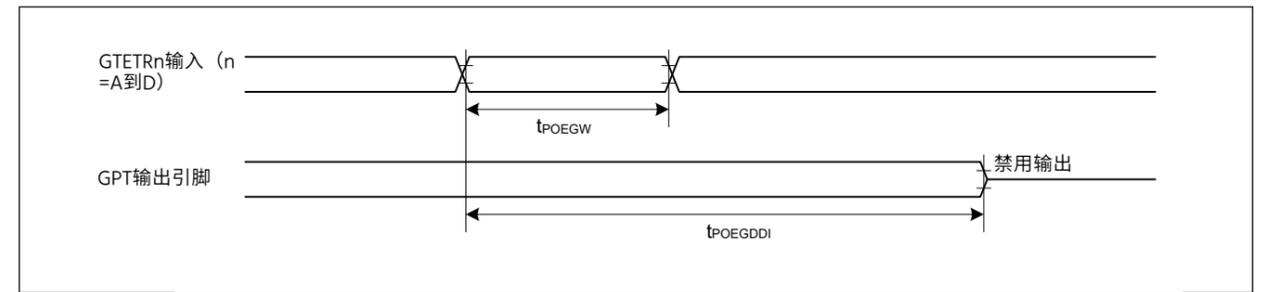


Figure 2.21 POEG的输出禁用时间直接响应GTETRn引脚的输入电平检测

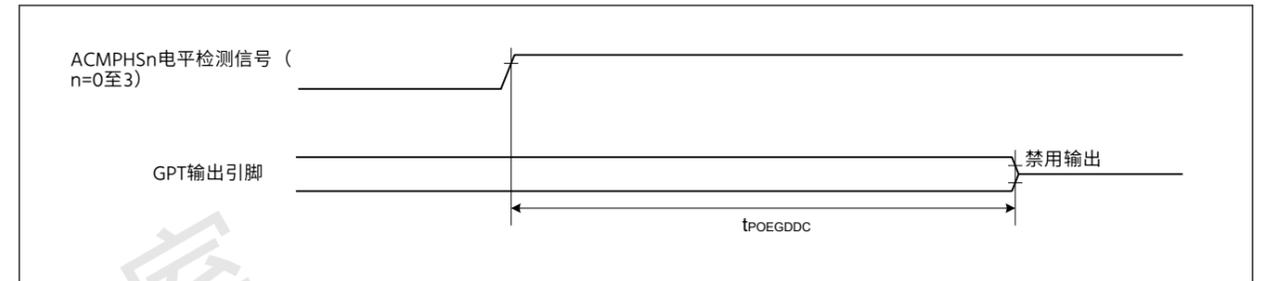


Figure 2.22 POEG响应来自ACMPHS的电平检测信号的输出禁用时间

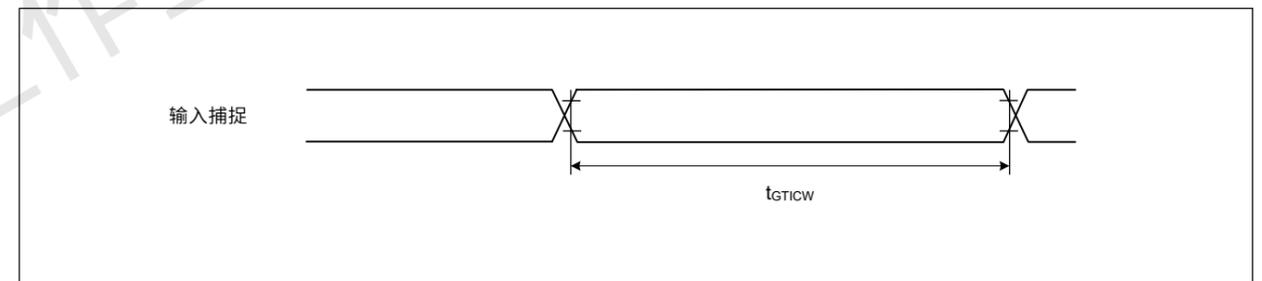


Figure 2.23 GPT输入捕捉时序

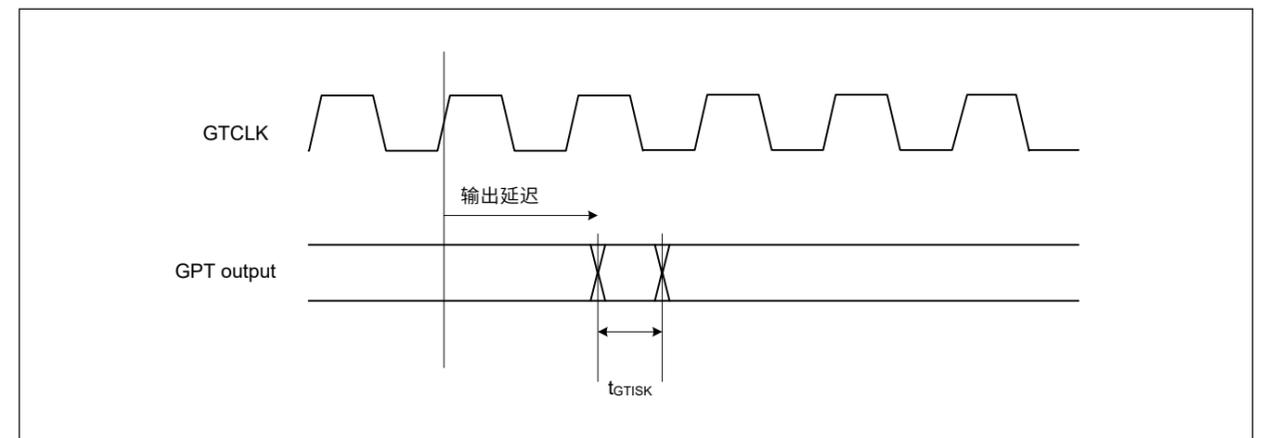


Figure 2.24 GPT输出延迟偏差

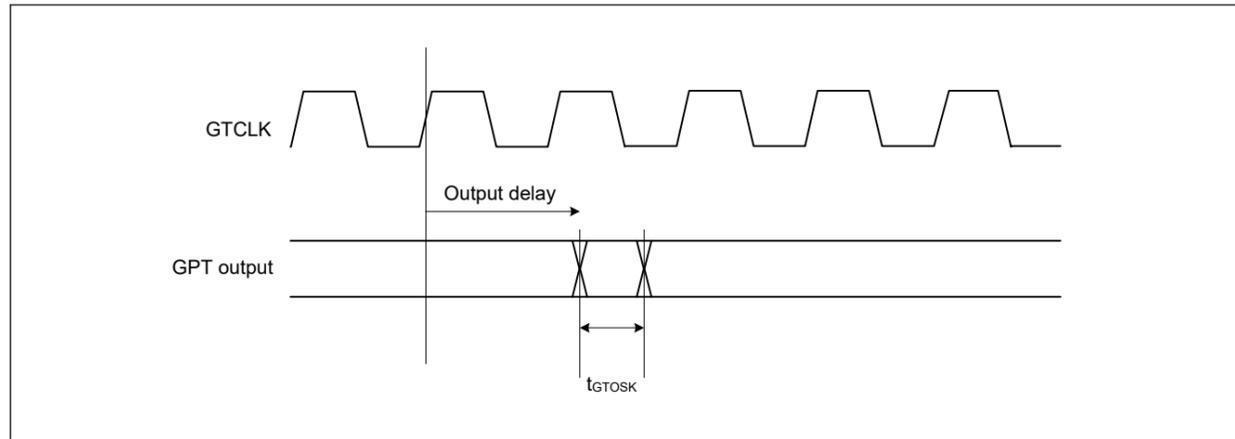


Figure 2.25 GPT output delay skew for OPS

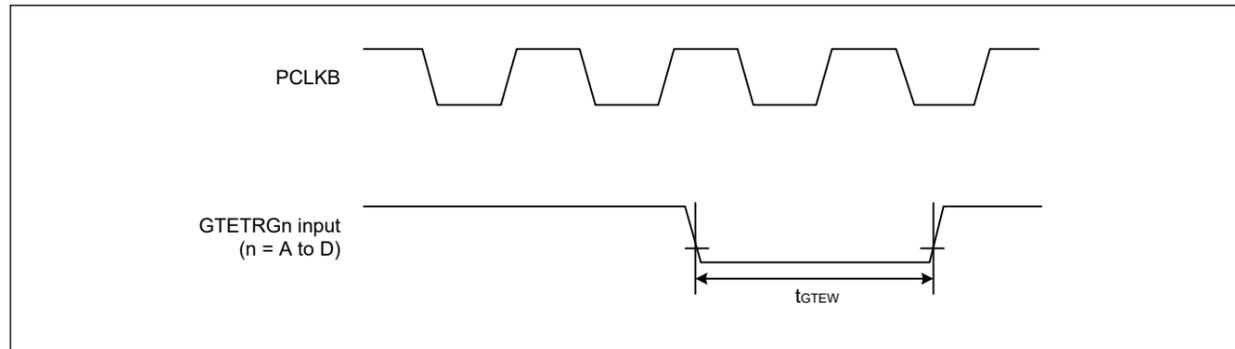


Figure 2.26 GPT External Trigger Input Timing

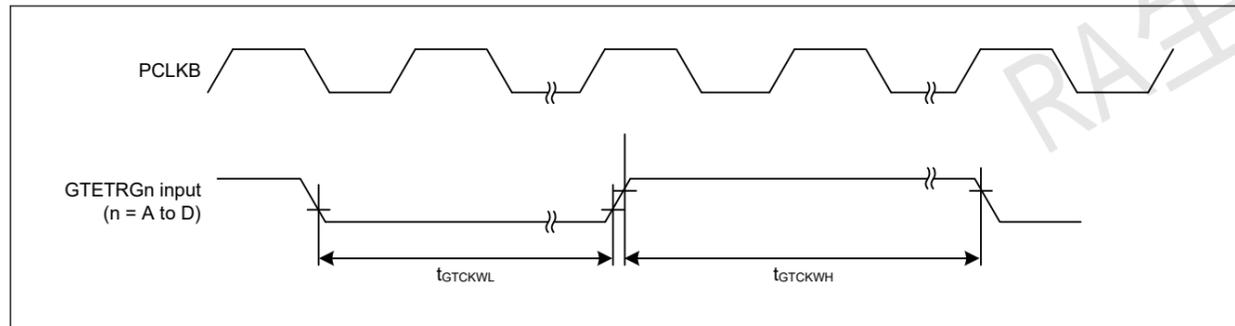


Figure 2.27 GPT Clock Input Timing

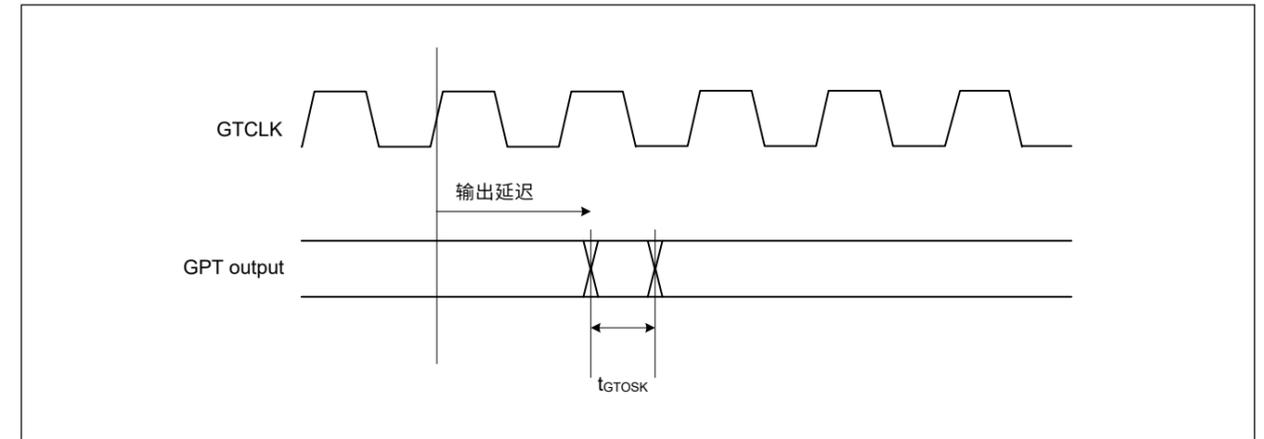


Figure 2.25 OPS的GPT输出延迟偏差

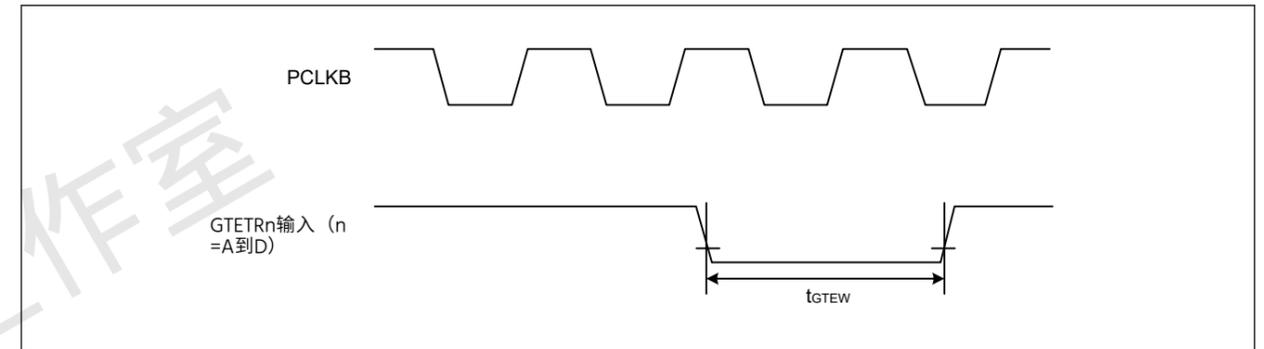


Figure 2.26 GPT外部触发输入时序

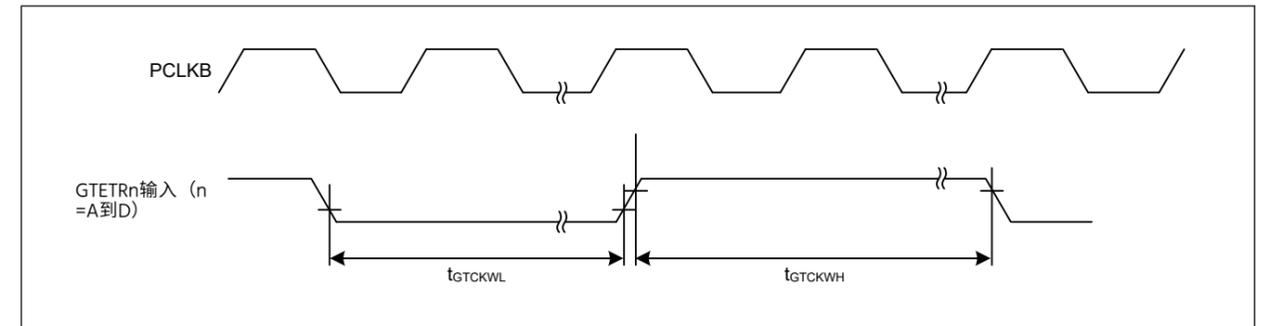


Figure 2.27 GPT时钟输入时序

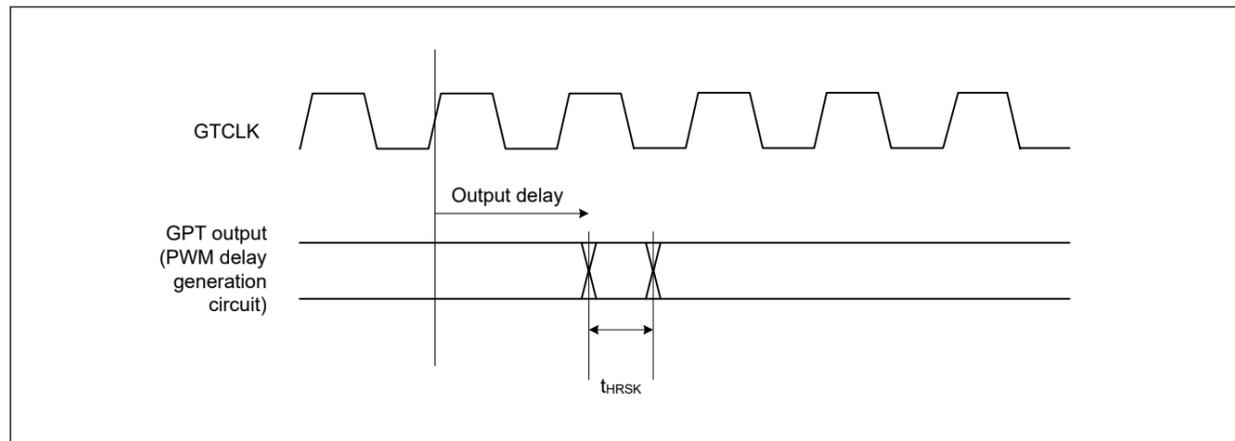


Figure 2.28 GPT (PDG) output delay skew

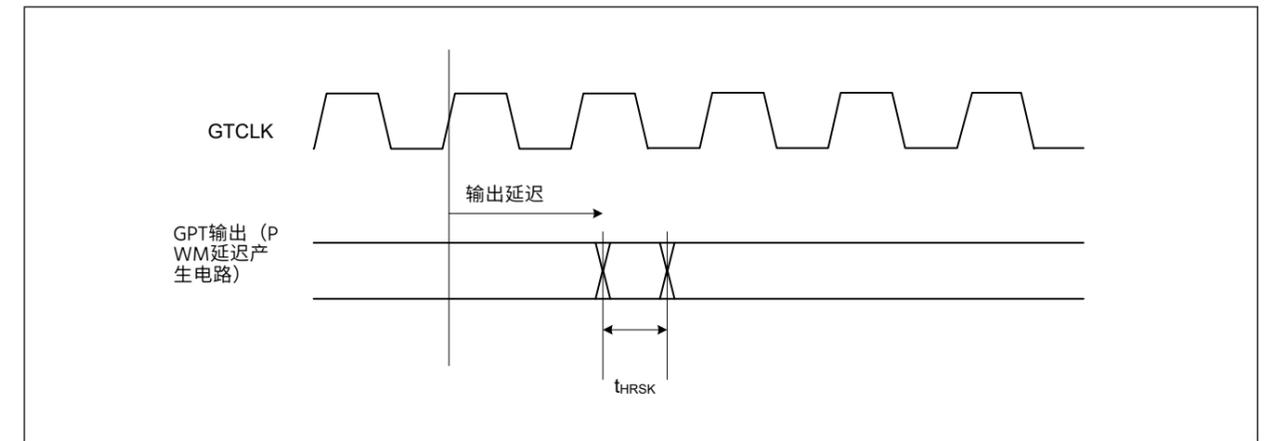


Figure 2.28 GPT(PDG)输出延迟偏差

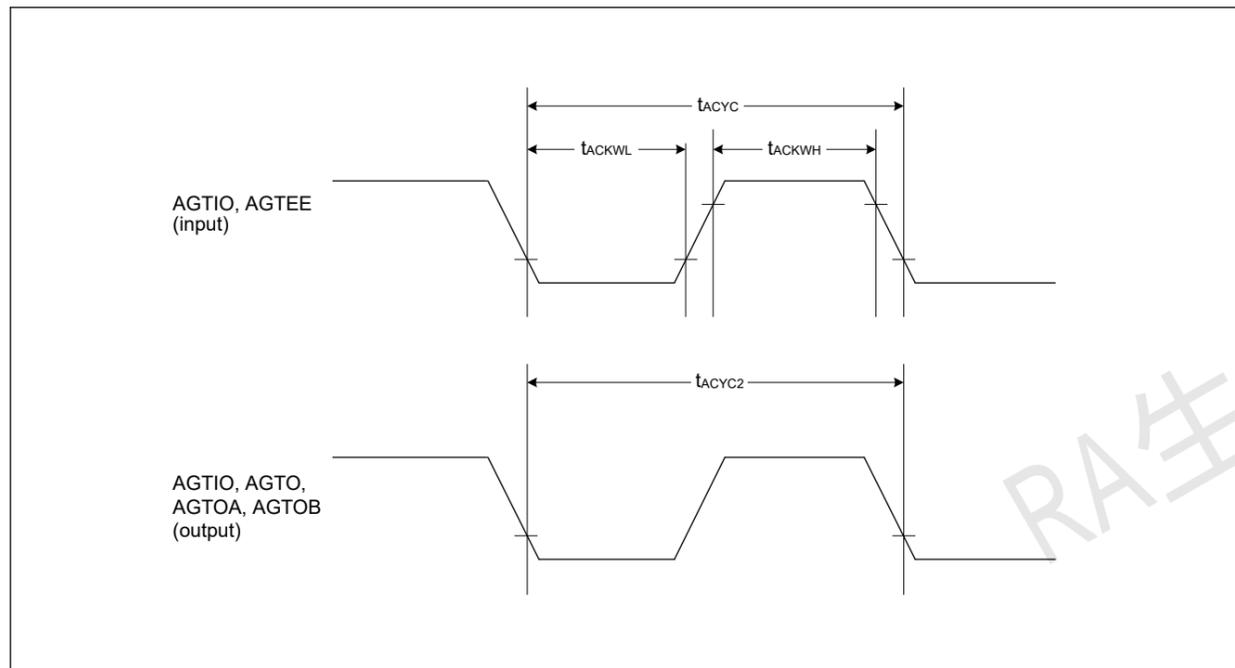


Figure 2.29 AGT input/output timing

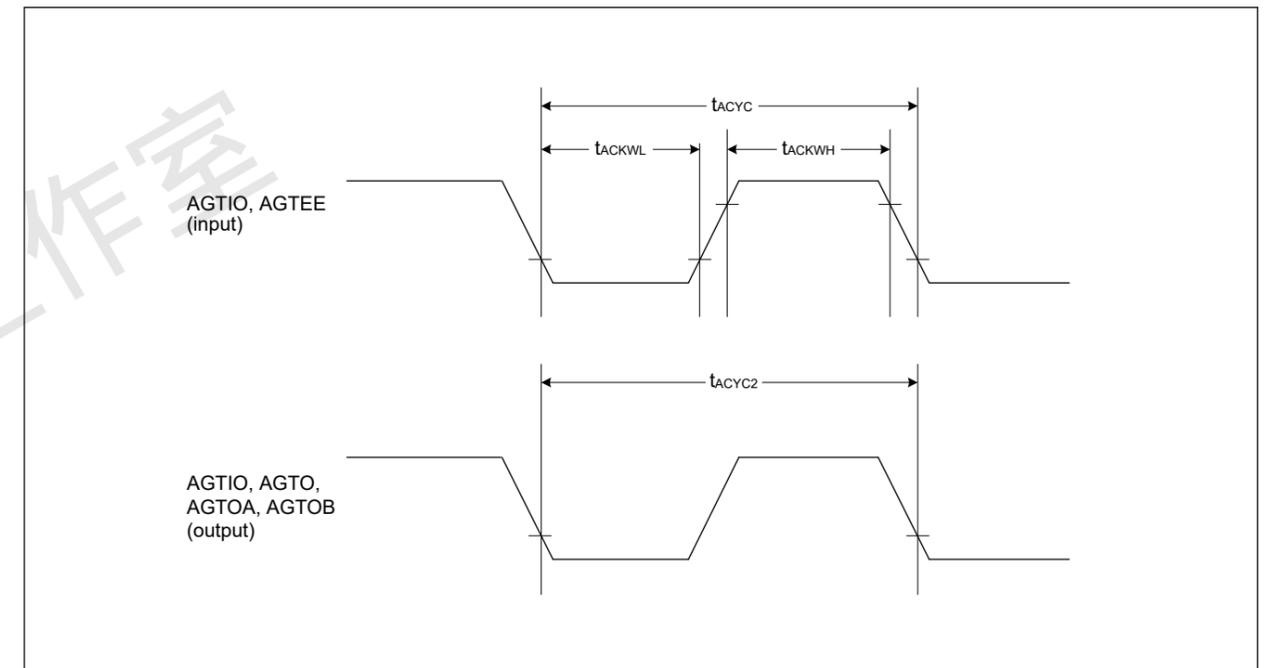


Figure 2.29 AGT input/output timing

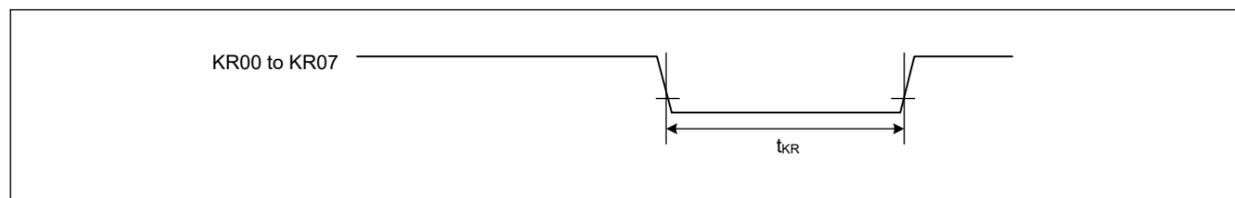


Figure 2.30 Key interrupt input timing

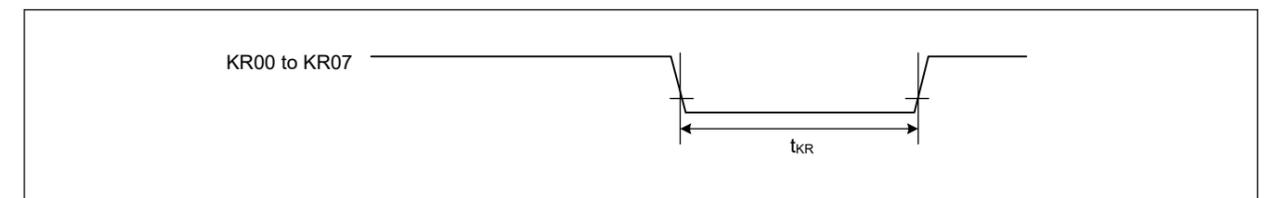


Figure 2.30 按键中断输入时序

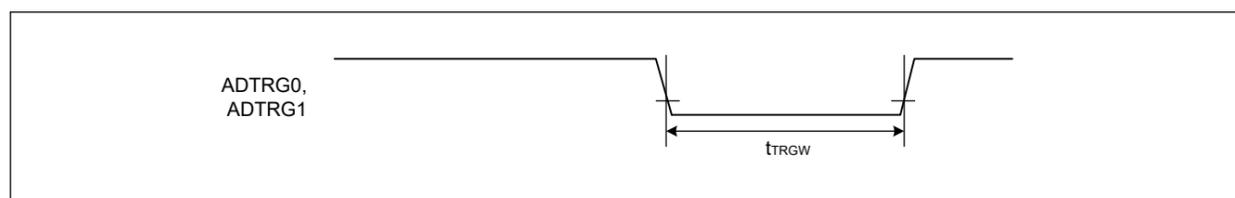


Figure 2.31 ADC trigger input timing

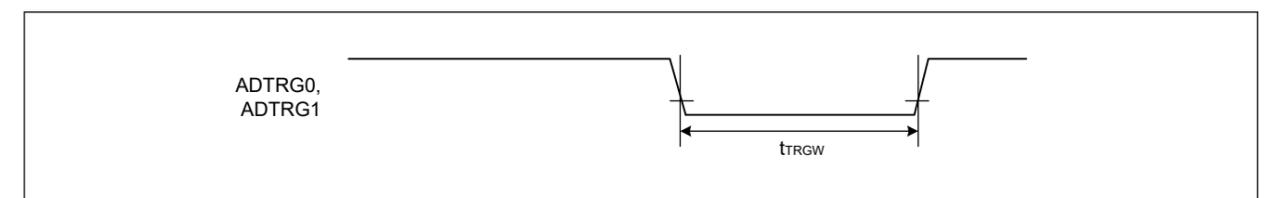


Figure 2.31 ADC触发输入时序

2.3.7 PDG Timing

Table 2.21 PDG timing

| Parameter           | Min | Typ  | Max | Unit | Test conditions  |
|---------------------|-----|------|-----|------|------------------|
| Operation frequency | 80  | —    | 200 | MHz  | —                |
| Resolution          | —   | 156  | —   | ps   | GPTCLK = 200 MHz |
| DNL*1               | —   | ±2.0 | —   | LSB  | —                |

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.8 CAC Timing

Table 2.22 CAC timing

| Parameter                       | Symbol  | Min          | Typ | Max | Unit | Test conditions |
|---------------------------------|---|--------------|-----|-----|------|-----------------|
| CAC<br>CACREF input pulse width | $t_{PBcyc} \leq t_{cac}^{*1}$<br>$t_{PBcyc} > t_{cac}^{*1}$ | $t_{CACREF}$ | —   | —   | ns   | —               |
|                                 |   |              |     |     |      |                 |

Note:  $t_{PBcyc}$ : PCLKB cycle.  
Note 1.  $t_{cac}$ : CAC count clock source cycle.

2.3.9 SCI Timing

Table 2.23 SCI timing (Asynchronous mode)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                | Symbol     | Min | Max | Unit       | Note |
|--------------------------|------------|-----|-----|------------|------|
| Input clock cycle        | $t_{Scyc}$ | 4   | —   | $t_{Tcyc}$ |      |
| Input clock pulse width  | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |      |
| Input clock rise time    | $t_{SCKr}$ | —   | 5   | ns         |      |
| Input clock fall time    | $t_{SCKf}$ | —   | 5   | ns         |      |
| Output clock cycle       | $t_{Scyc}$ | 6   | —   | $t_{Tcyc}$ |      |
| Output clock pulse width | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |      |
| Output clock rise time   | $t_{SCKr}$ | —   | 5   | ns         |      |
| Output clock fall time   | $t_{SCKf}$ | —   | 5   | ns         |      |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

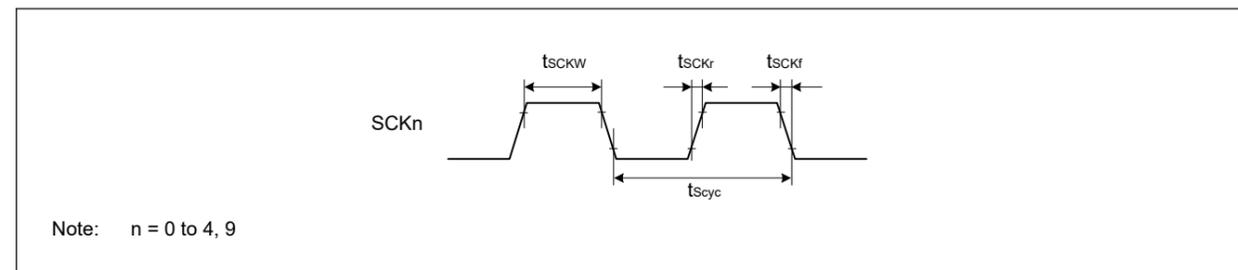


Figure 2.32 SCK clock input/output timing

Table 2.24 SCI timing (Simple SPI) (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter              | High Speed/Default | Symbol      | Min | Max   | Unit       | Note |
|------------------------|--------------------|-------------|-----|-------|------------|------|
| SCK clock cycle output | Master             | $t_{SPcyc}$ | 2   | 65536 | $t_{Tcyc}$ |      |
| SCK clock cycle input  | Slave              |             | 2   | —     |            |      |

2.3.7 PDG Timing

Table 2.21 PDG timing

| Parameter  | Min | Typ  | Max | Unit | 测试条件             |
|------------|-----|------|-----|------|------------------|
| 运行频率       | 80  | —    | 200 | MHz  | —                |
| Resolution | —   | 156  | —   | ps   | GPTCLK = 200 MHz |
| DNL*1      | —   | ±2.0 | —   | LSB  | —                |

注1.该值将1-LSB分辨率中的行之间的差异归一化。

2.3.8 CAC时序

Table 2.22 CAC计时

| Parameter           | Symbol  | Min          | Typ | Max | Unit | 测试条件 |
|---------------------|---|--------------|-----|-----|------|------|
| CAC<br>CACREF输入脉冲宽度 | $t_{PBcyc} \leq t_{cac}^{*1}$<br>$t_{PBcyc} > t_{cac}^{*1}$ | $t_{CACREF}$ | —   | —   | ns   | —    |
|                     |   |              |     |     |      |      |

Note:  $t_{PBcyc}$ : PCLKB cycle.  
注1. $t_{cac}$ : CAC计数时钟源周期。

2.3.9 SCI时序

Table 2.23 SCI时序 (异步模式)

条件: 在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | Symbol     | Min | Max | Unit       | Note |
|-----------|------------|-----|-----|------------|------|
| 输入时钟周期    | $t_{Scyc}$ | 4   | —   | $t_{Tcyc}$ |      |
| 输入时钟脉冲宽度  | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |      |
| 输入时钟上升时间  | $t_{SCKr}$ | —   | 5   | ns         |      |
| 输入时钟下降时间  | $t_{SCKf}$ | —   | 5   | ns         |      |
| 输出时钟周期    | $t_{Scyc}$ | 6   | —   | $t_{Tcyc}$ |      |
| 输出时钟脉冲宽度  | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |      |
| 输出时钟上升时间  | $t_{SCKr}$ | —   | 5   | ns         |      |
| 输出时钟下降时间  | $t_{SCKf}$ | —   | 5   | ns         |      |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

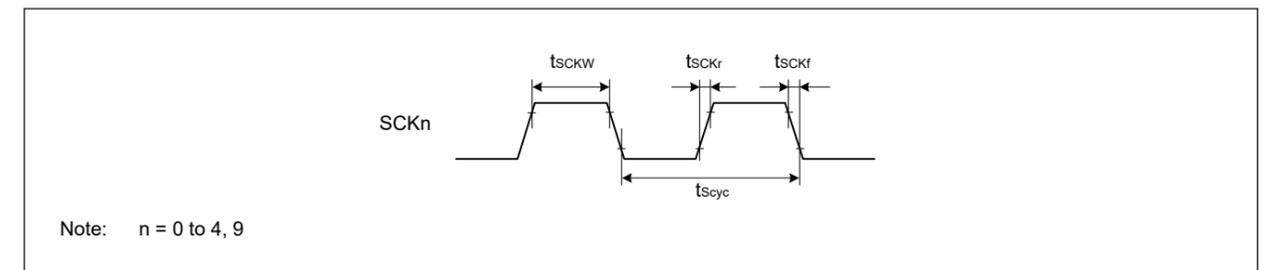


Figure 2.32 SCK时钟输入输出时序

Table 2.24 SCI时序(SimpleSPI)(1of2)

条件: 在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | High Speed/Default | Symbol      | Min | Max   | Unit       | Note |
|-----------|--------------------|-------------|-----|-------|------------|------|
| SCK时钟周期输出 | Master             | $t_{SPcyc}$ | 2   | 65536 | $t_{Tcyc}$ |      |
| SCK时钟周期输入 | Slave              |             | 2   | —     |            |      |

**Table 2.24 SCI timing (Simple SPI) (2 of 2)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                    |        | High Speed/Default | Symbol                                  | Min | Max | Unit               | Note |
|------------------------------|--------|--------------------|---|-----|-----|--------------------|------|
| SCK clock high pulse width   | Master |                    | t <sub>SPCKWH</sub>                     | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|                              | Slave  |                    |   |     |     |                    |      |
| SCK clock low pulse width    | Master |                    | t <sub>SPCKWL</sub>                     | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|                              | Slave  |                    |   |     |     |                    |      |
| SCK clock rise and fall time | Output |                    | t <sub>SPCKr</sub> , t <sub>SPCKf</sub> | —   | 5   | ns                 |      |
|                              | Input  |                    |   | —   | 1   | us                 |      |
| Data input setup time        | Master | High Speed*1       | t <sub>SU</sub>                         | 1.7 | —   | ns                 |      |
|                              |        | Default*2          |   | 3   | —   | ns                 |      |
|                              | Slave  |                    |   | 3.3 | —   | ns                 |      |
| Data input hold time         | Master | High Speed*1       | t <sub>H</sub>                          | 12  | —   | ns                 |      |
|                              |        | Default*2          |   | 14  | —   | ns                 |      |
|                              | Slave  |                    |   | 3   | —   | ns                 |      |
| Data output delay            | Master | High Speed*1       | t <sub>OD</sub>                         | —   | 5   | ns                 |      |
|                              |        | Default*2          |   | —   | 7.3 | ns                 |      |
|                              | Slave  | High Speed*1       |   | —   | 15  | ns                 |      |
|                              |        | Default*2          |   | —   | 21  | ns                 |      |
| Data output hold time        | Master |                    | t <sub>OH</sub>                         | 0   | —   | ns                 |      |
|                              | Slave  |                    |   | 0   | —   | ns                 |      |
| Data rise and fall time      | Output |                    | t <sub>Dr</sub> , t <sub>Df</sub>       | —   | 5   | ns                 |      |
|                              | Input  |                    |   | —   | 1   | ns                 |      |
| Slave access time            |        |                    | t <sub>SA</sub>                         | —   | 5   | t <sub>TCyc</sub>  |      |
| Slave output release time    |        |                    | t <sub>REL</sub>                        | —   | 5   | t <sub>TCyc</sub>  |      |

Note: t<sub>TCyc</sub>: SCITCLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance \_A, \_B, \_C, to indicate group membership. SCI0 is instance \_A, SCI2 and SCI3 are instance \_B, SCI1 and SCI9 are instance \_C, SCI4 is instance \_C and RXD is only PD14.

Note 2. All pins of group membership can be used.

**Table 2.25 SCI timing (Simple SPI mode)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                   | Symbol                                | Min | Max | Unit               | Note |
|-----------------------------|---------------------------------------|-----|-----|--------------------|------|
| SS input setup time         | t <sub>LEAD</sub>                     | 1   | —   | t <sub>SPcyc</sub> |      |
| SS input hold time          | t <sub>LAG</sub>                      | 1   | —   | t <sub>SPcyc</sub> |      |
| SS input rise and fall time | t <sub>SSLr</sub> , t <sub>SSLf</sub> | —   | 1   | us                 |      |

**Table 2.26 SCI timing (Clock synchronous mode) (1 of 2)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                  |        | High Speed/Default | Symbol              | Min | Max | Unit               | Note |
|----------------------------|--------|--------------------|---------------------|-----|-----|--------------------|------|
| SCK clock cycle output     | Master |                    | t <sub>SPcyc</sub>  | 2   | —   | t <sub>TCyc</sub>  |      |
| SCK clock cycle input      | Slave  |                    |                     | 2   | —   |                    |      |
| SCK clock high pulse width | Master |                    | t <sub>SPCKWH</sub> | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|                            | Slave  |                    |                     |     |     |                    |      |

**Table 2.24 SCI时序(SimpleSPI)(2of2)**

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter    |        | High Speed/Default | Symbol                                  | Min | Max | Unit               | Note |
|--------------|--------|--------------------|---|-----|-----|--------------------|------|
| SCK时钟高脉冲宽度   | Master |                    | t <sub>SPCKWH</sub>                     | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|              | Slave  |                    |   |     |     |                    |      |
| SCK时钟低脉冲宽度   | Master |                    | t <sub>SPCKWL</sub>                     | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|              | Slave  |                    |   |     |     |                    |      |
| SCK时钟上升和下降时间 | Output |                    | t <sub>SPCKr</sub> , t <sub>SPCKf</sub> | —   | 5   | ns                 |      |
|              | Input  |                    |   | —   | 1   | us                 |      |
| 数据输入建立时间     | Master | 高速*1               | t <sub>SU</sub>                         | 1.7 | —   | ns                 |      |
|              |        | Default*2          |   | 3   | —   | ns                 |      |
|              | Slave  |                    |   | 3.3 | —   | ns                 |      |
| 数据输入保持时间     | Master | 高速*1               | t <sub>H</sub>                          | 12  | —   | ns                 |      |
|              |        | Default*2          |   | 14  | —   | ns                 |      |
|              | Slave  |                    |   | 3   | —   | ns                 |      |
| 数据输出延迟       | Master | 高速*1               | t <sub>OD</sub>                         | —   | 5   | ns                 |      |
|              |        | Default*2          |   | —   | 7.3 | ns                 |      |
|              | Slave  | 高速*1               |   | —   | 15  | ns                 |      |
|              |        | Default*2          |   | —   | 21  | ns                 |      |
| 数据输出保持时间     | Master |                    | t <sub>OH</sub>                         | 0   | —   | ns                 |      |
|              | Slave  |                    |   | 0   | —   | ns                 |      |
| 数据上升和下降时间    | Output |                    | t <sub>Dr</sub> , t <sub>Df</sub>       | —   | 5   | ns                 |      |
|              | Input  |                    |   | —   | 1   | ns                 |      |
| 从站访问时间       |        |                    | t <sub>SA</sub>                         | —   | 5   | t <sub>TCyc</sub>  |      |
| 从机输出释放时间     |        |                    | t <sub>REL</sub>                        | —   | 5   | t <sub>TCyc</sub>  |      |

Note: t<sub>TCyc</sub>: SCITCLK cycle.

注1.必须使用名称后附有字母的引脚，例如\_A、\_B、\_C，以表示组成员身份。SCI0是实例\_A，SCI2和SCI3是实例\_B，SCI1和SCI9是实例\_C，SCI4是实例\_C，RXD只有PD14。

注2.可以使用组成员的所有引脚。

**Table 2.25 SCI时序(简单SPI模式)**

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter   | Symbol                                | Min | Max | Unit               | Note |
|-------------|---------------------------------------|-----|-----|--------------------|------|
| SS输入建立时间    | t <sub>LEAD</sub>                     | 1   | —   | t <sub>SPcyc</sub> |      |
| SS输入保持时间    | t <sub>LAG</sub>                      | 1   | —   | t <sub>SPcyc</sub> |      |
| SS输入上升和下降时间 | t <sub>SSLr</sub> , t <sub>SSLf</sub> | —   | 1   | us                 |      |

**Table 2.26 SCI时序(时钟同步模式)(1of2)**

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter  |        | High Speed/Default | Symbol              | Min | Max | Unit               | Note |
|------------|--------|--------------------|---------------------|-----|-----|--------------------|------|
| SCK时钟周期输出  | Master |                    | t <sub>SPcyc</sub>  | 2   | —   | t <sub>TCyc</sub>  |      |
| SCK时钟周期输入  | Slave  |                    |                     | 2   | —   |                    |      |
| SCK时钟高脉冲宽度 | Master |                    | t <sub>SPCKWH</sub> | 0.4 | 0.6 | t <sub>SPcyc</sub> |      |
|            | Slave  |                    |                     |     |     |                    |      |

**Table 2.26 SCI timing (Clock synchronous mode) (2 of 2)**

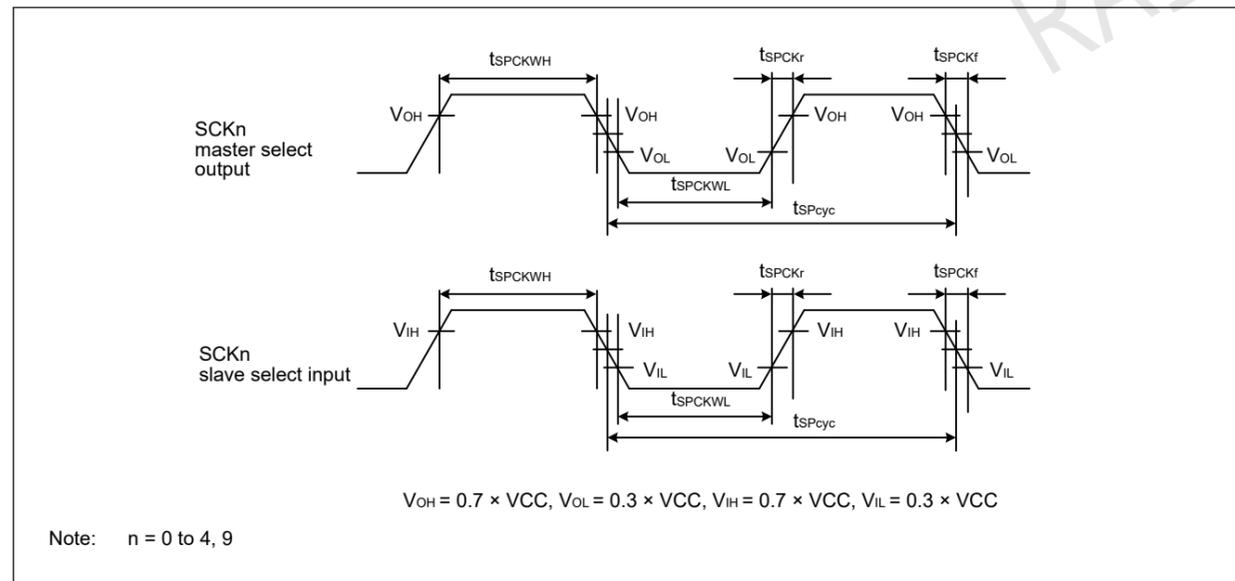
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                    |        | High Speed/Default | Symbol                 | Min | Max | Unit        | Note |
|------------------------------|--------|--------------------|------------------------|-----|-----|-------------|------|
| SCK clock low pulse width    | Master |                    | $t_{SPCKWL}$           | 0.4 | 0.6 | $t_{SPcyc}$ |      |
|                              | Slave  |                    |                        |     |     |             |      |
| SCK clock rise and fall time | Output |                    | $t_{SPCKr}, t_{SPCKf}$ | —   | 5   | ns          |      |
|                              | Input  |                    |                        |     |     |             |      |
| Data input setup time        | Master | High Speed*1       | $t_{SU}$               | 2.6 | —   | ns          |      |
|                              |        | Default*2          |                        | 2.8 | —   | ns          |      |
|                              | Slave  |                    | 3.3                    |     | ns  |             |      |
| Data input hold time         | Master | High Speed*1       | $t_H$                  | 12  | —   | ns          |      |
|                              |        | Default*2          |                        | 14  | —   | ns          |      |
|                              | Slave  |                    | 3                      |     | ns  |             |      |
| Data output delay            | Master | High Speed*1       | $t_{OD}$               | —   | 5   | ns          |      |
|                              |        | Default*2          |                        | —   | 7.3 | ns          |      |
|                              | Slave  | High Speed*1       | —                      | 15  | ns  |             |      |
|                              |        | Default*2          | —                      | 21  | ns  |             |      |
| Data output hold time        | Master |                    | $t_{OH}$               | 0   | —   | ns          |      |
|                              | Slave  |                    |                        | 0   | —   | ns          |      |
| Data rise and fall time      | Output |                    | $t_{Dr}, t_{Df}$       | —   | 5   | ns          |      |
|                              | Input  |                    |                        | —   | 5   | ns          |      |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance \_A, \_B, \_C, to indicate group membership. SCI0 is instance \_A, SCI2 and SCI3 are instance \_B, SCI1 and SCI9 are instance \_C, SCI4 is instance \_C and RXD is only PD14.

Note 2. All pins of group membership can be used.



**Figure 2.33 SCI simple SPI mode clock timing**

**Table 2.26 SCI时序 (时钟同步模式) (2of2)**

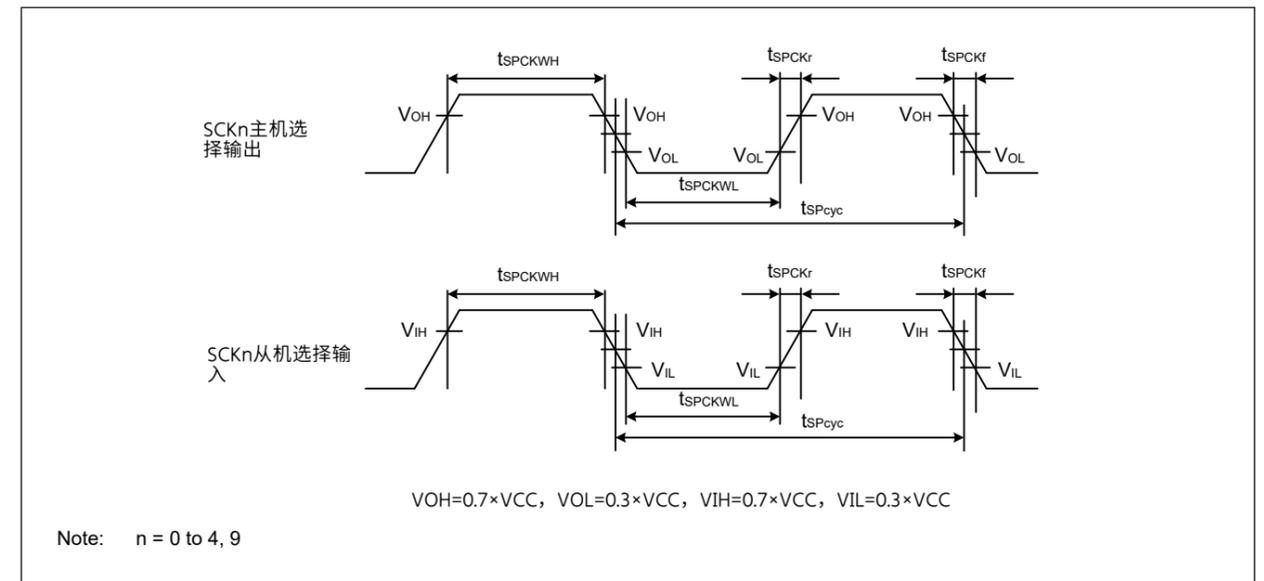
条件: 在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter    |        | High Speed/Default | Symbol                 | Min | Max | Unit        | Note |
|--------------|--------|--------------------|------------------------|-----|-----|-------------|------|
| SCK时钟低脉冲宽度   | Master |                    | $t_{SPCKWL}$           | 0.4 | 0.6 | $t_{SPcyc}$ |      |
|              | Slave  |                    |                        |     |     |             |      |
| SCK时钟上升和下降时间 | Output |                    | $t_{SPCKr}, t_{SPCKf}$ | —   | 5   | ns          |      |
|              | Input  |                    |                        |     |     |             |      |
| 数据输入建立时间     | Master | 高速*1               | $t_{SU}$               | 2.6 | —   | ns          |      |
|              |        | Default*2          |                        | 2.8 | —   | ns          |      |
|              | Slave  |                    | 3.3                    |     | ns  |             |      |
| 数据输入保持时间     | Master | 高速*1               | $t_H$                  | 12  | —   | ns          |      |
|              |        | Default*2          |                        | 14  | —   | ns          |      |
|              | Slave  |                    | 3                      |     | ns  |             |      |
| 数据输出延迟       | Master | 高速*1               | $t_{OD}$               | —   | 5   | ns          |      |
|              |        | Default*2          |                        | —   | 7.3 | ns          |      |
|              | Slave  | 高速*1               | —                      | 15  | ns  |             |      |
|              |        | Default*2          | —                      | 21  | ns  |             |      |
| 数据输出保持时间     | Master |                    | $t_{OH}$               | 0   | —   | ns          |      |
|              | Slave  |                    |                        | 0   | —   | ns          |      |
| 数据上升和下降时间    | Output |                    | $t_{Dr}, t_{Df}$       | —   | 5   | ns          |      |
|              | Input  |                    |                        | —   | 5   | ns          |      |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

注1. 必须使用名称后附有字母的引脚, 例如 \_A、\_B、\_C, 以表示组成员身份。SCI0是实例\_A, SCI2和SCI3是实例\_B, SCI1和SCI9是实例\_C, SCI4是实例\_C, RXD只有PD14。

注2. 可以使用组成员的所有引脚。



**Figure 2.33 SCI简单SPI模式时钟时序**

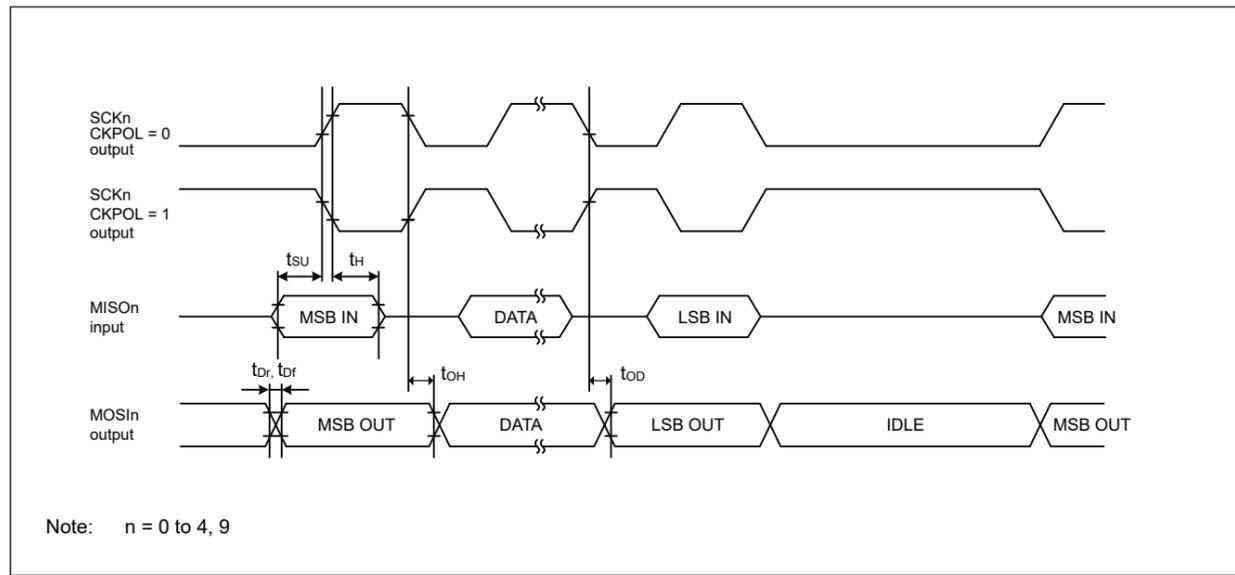


Figure 2.34 SCI simple SPI mode timing for master when CKPH = 1

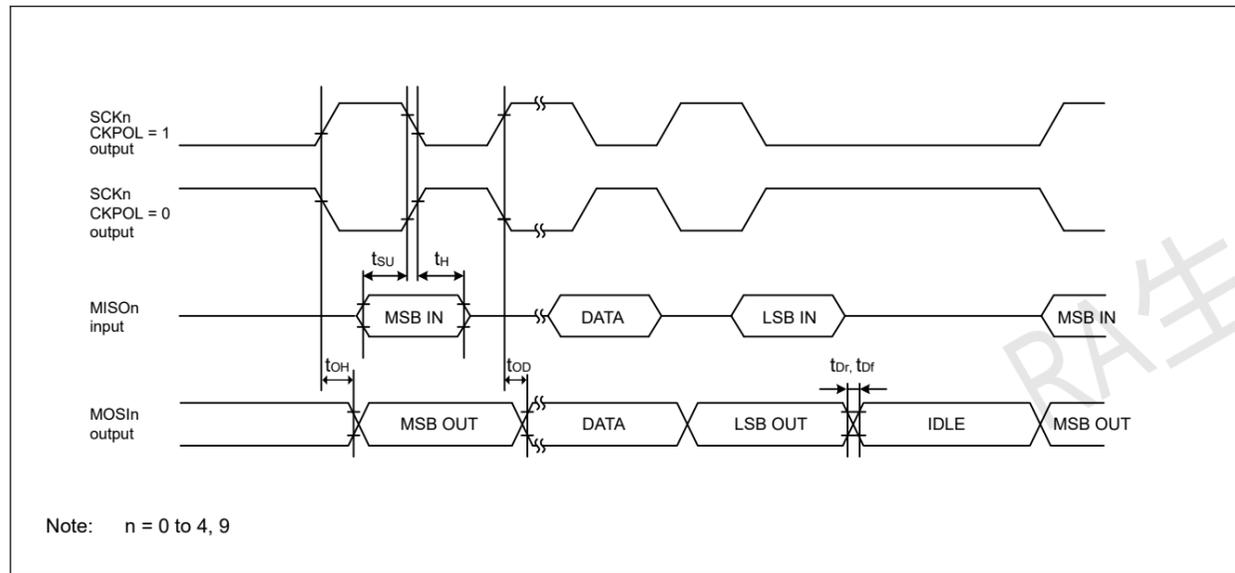


Figure 2.35 SCI simple SPI mode timing for master when CKPH = 0

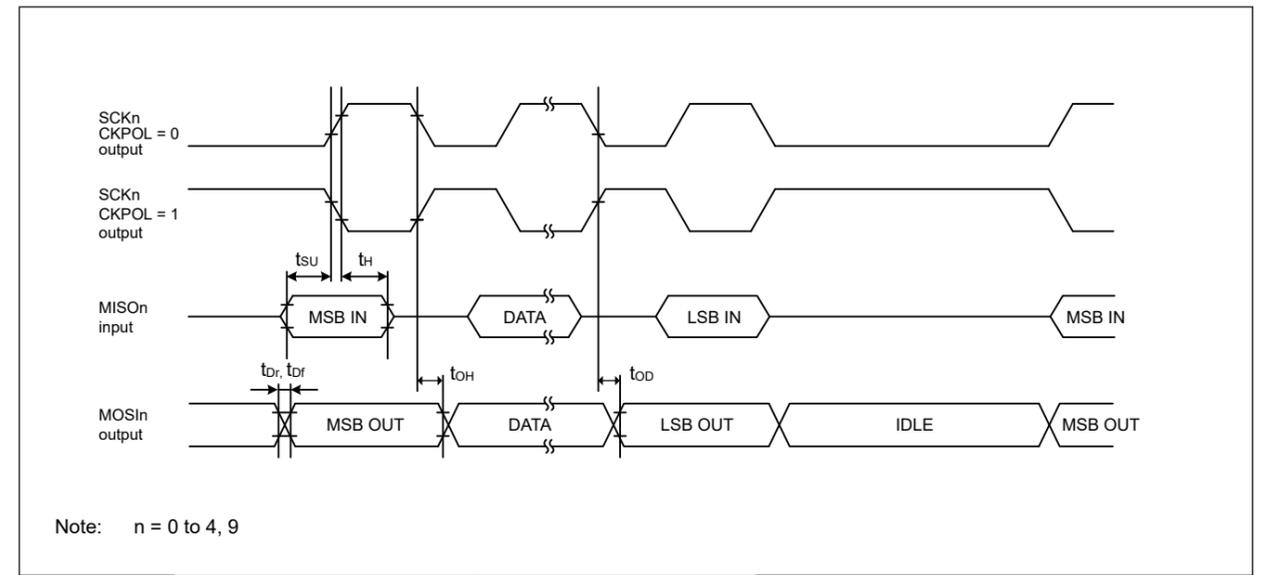


Figure 2.34 CKPH=1时主机的SCI简单SPI模式时序

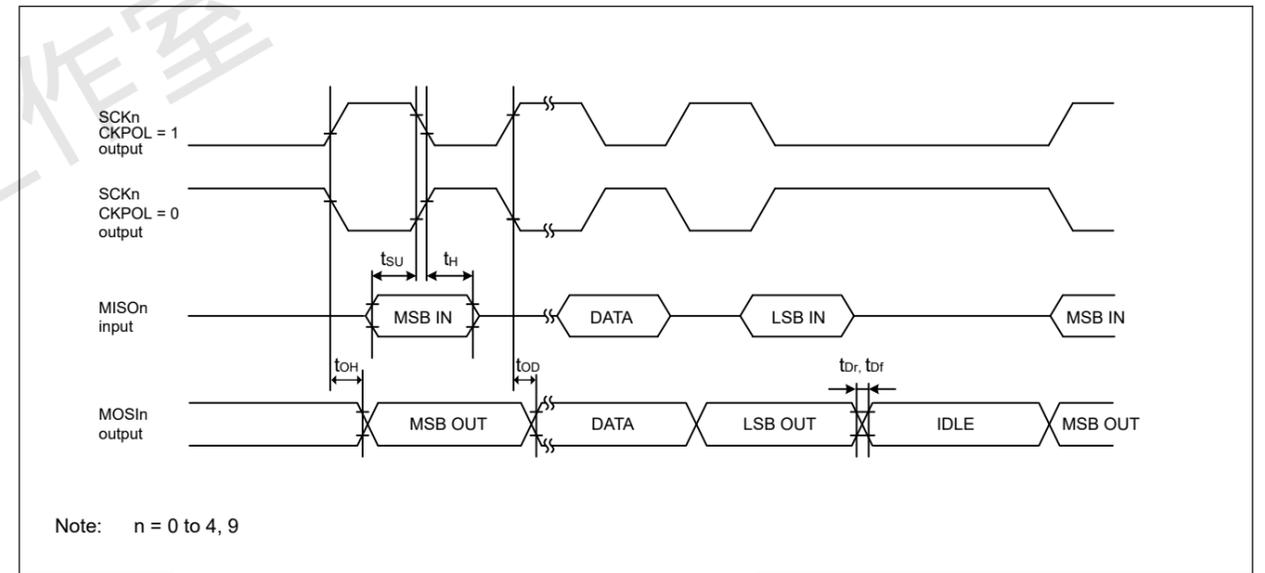


Figure 2.35 CKPH=0时主机的SCI简单SPI模式时序

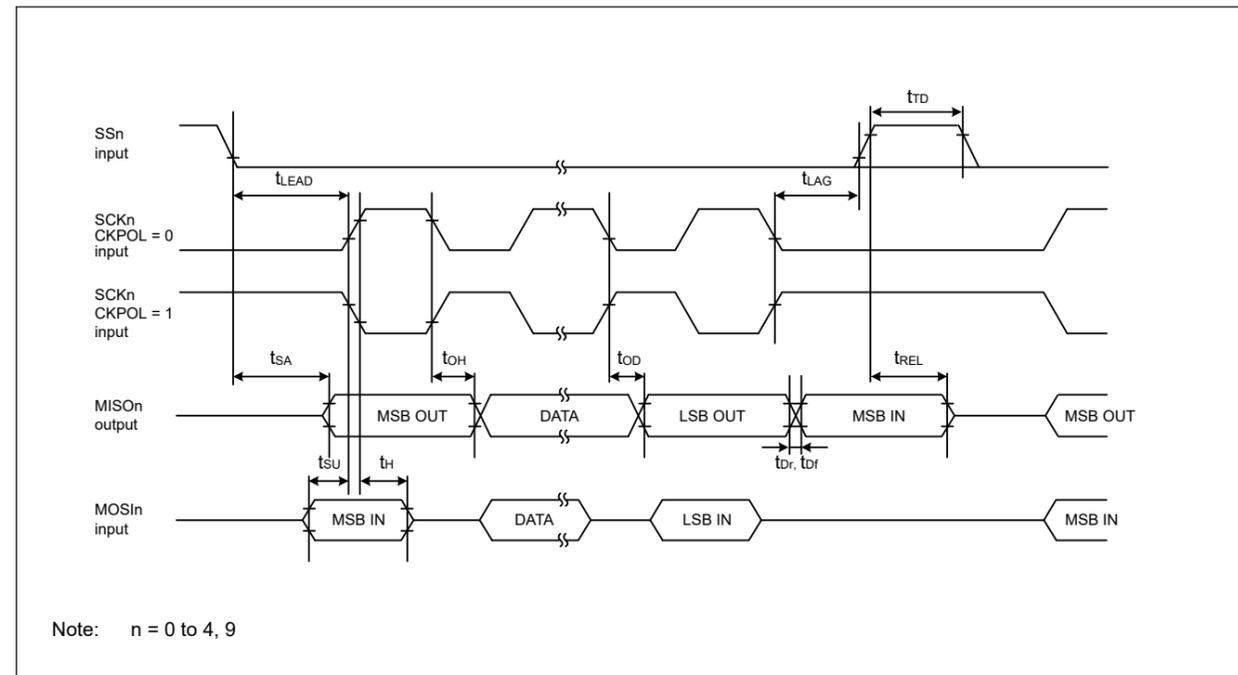


Figure 2.36 SCI simple SPI mode timing for slave when CKPH = 1

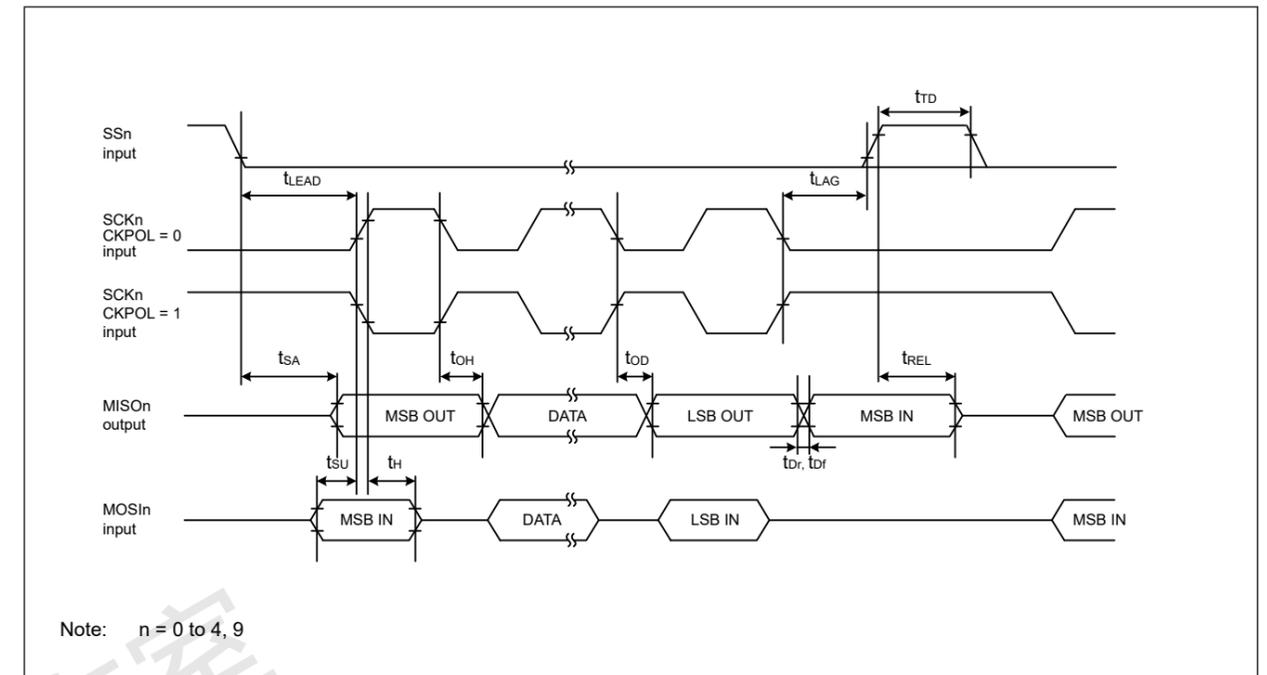


Figure 2.36 CKPH=1时从机的SCI简单SPI模式时序

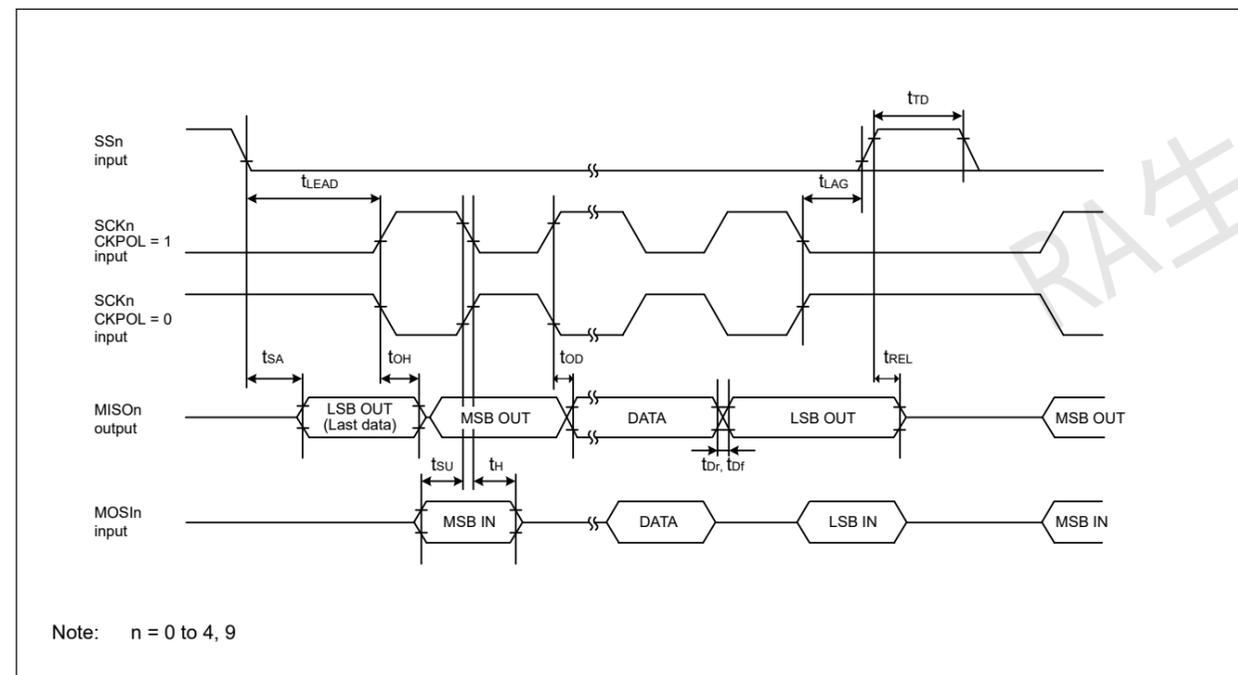


Figure 2.37 SCI simple SPI mode timing for slave when CKPH = 0

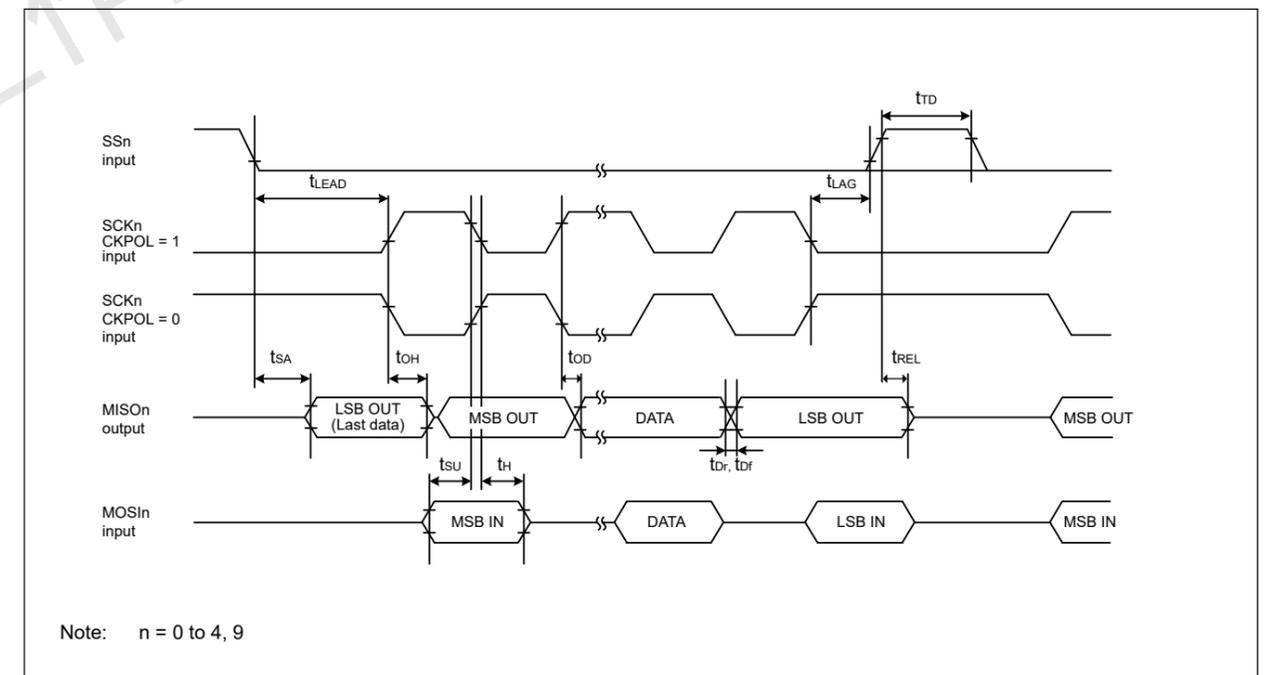


Figure 2.37 CKPH=0时从机的SCI简单SPI模式时序

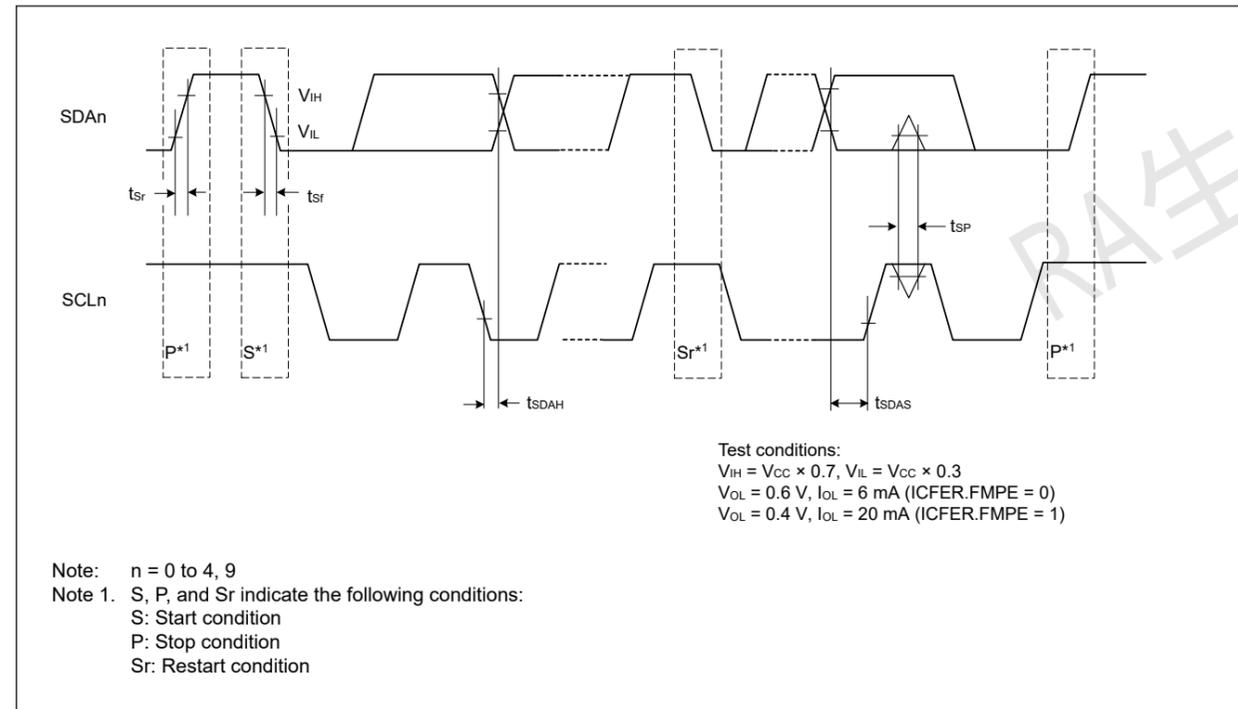
**Table 2.27 SCI timing (Simple IIC mode)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                               | Symbol                                  | Min                      | Max      | Unit                | Note |
|---|---|--------------------------|----------|---------------------|------|
| Simple IIC (Standard mode)              | SCL, SDA input rise time                | $t_{sr}$                 | —        | 1000                | ns   |
|   | SCL, SDA input fall time                | $t_{sf}$                 | —        | 300                 | ns   |
|   | SCL, SDA input spike pulse removal time | $t_{sp}$                 | 0        | $4 \times t_{Tcyc}$ | ns   |
|   | Data input setup time                   | $t_{SDAS}$               | 250      | —                   | ns   |
|   | Data input hold time                    | $t_{SDAH}$               | 0        | —                   | ns   |
|   | SCL, SDA capacitive load                | $C_b^{*1}$               | —        | 400                 | pF   |
|   | Simple IIC (Fast mode)                  | SCL, SDA input rise time | $t_{sr}$ | —                   | 300  |
| SCL, SDA input fall time                |   | $t_{sf}$                 | —        | 300                 | ns   |
| SCL, SDA input spike pulse removal time |   | $t_{sp}$                 | 0        | $4 \times t_{Tcyc}$ | ns   |
| Data input setup time                   |   | $t_{SDAS}$               | 100      | —                   | ns   |
| Data input hold time                    |   | $t_{SDAH}$               | 0        | —                   | ns   |
| SCL, SDA capacitive load                |   | $C_b^{*1}$               | —        | 400                 | pF   |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

Note 1.  $C_b$  indicates the total capacity of the bus line.



**Figure 2.38 SCI simple IIC mode timing**

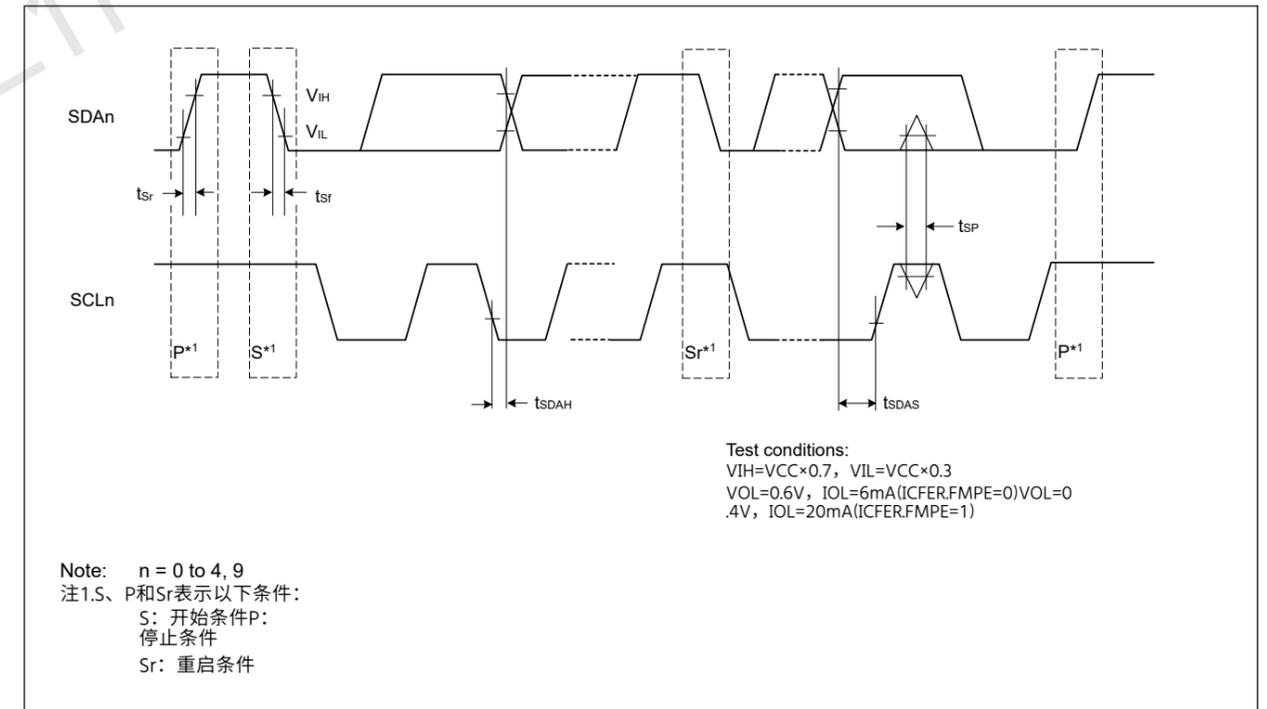
**Table 2.27 SCI时序 (简单IIC模式)**

条件: 在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter                  | Symbol                   | Min           | Max      | Unit                | Note |
|----------------------------|--------------------------|---------------|----------|---------------------|------|
| Simple IIC (Standard mode) | SCL、SDA输入上升时间            | $t_{sr}$      | —        | 1000                | ns   |
|                            | SCL、SDA输入下降时间            | $t_{sf}$      | —        | 300                 | ns   |
|                            | SCL、SDA输入尖峰脉冲去除时间        | $t_{sp}$      | 0        | $4 \times t_{Tcyc}$ | ns   |
|                            | 数据输入建立时间                 | $t_{SDAS}$    | 250      | —                   | ns   |
|                            | 数据输入保持时间                 | $t_{SDAH}$    | 0        | —                   | ns   |
|                            | SCL, SDA capacitive load | $C_b^{*1}$    | —        | 400                 | pF   |
|                            | Simple IIC (Fast mode)   | SCL、SDA输入上升时间 | $t_{sr}$ | —                   | 300  |
| SCL、SDA输入下降时间              |                          | $t_{sf}$      | —        | 300                 | ns   |
| SCL、SDA输入尖峰脉冲去除时间          |                          | $t_{sp}$      | 0        | $4 \times t_{Tcyc}$ | ns   |
| 数据输入建立时间                   |                          | $t_{SDAS}$    | 100      | —                   | ns   |
| 数据输入保持时间                   |                          | $t_{SDAH}$    | 0        | —                   | ns   |
| SCL, SDA capacitive load   |                          | $C_b^{*1}$    | —        | 400                 | pF   |

Note:  $t_{Tcyc}$ : SCITCLK cycle.

注1.  $C_b$ 表示总线的总容量。



**Figure 2.38 SCI简单IIC模式时序**

## 2.3.10 SPI Timing

Table 2.28 SPI timing (1 of 2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                      | High Speed/Default | Symbol       | VCC = 3.0 to 3.6 V, C = 15 pF               |      | VCC = 2.7 to 3.6 V, C = 30 pF               |      | Unit        | Note |
|--------------------------------|--------------------|--------------|---|------|---|------|-------------|------|
|                                |                    |              | Min   | Max  | Min   | Max  |             |      |
| RSPCK clock cycle              | Master             | $t_{SPCyc}$  | 2   | 4096 | 2   | 4096 | $t_{Tcyc}$  |      |
|                                | Slave              |              | 2   | —    | 2   | —    |             |      |
| RSPCK clock high pulse width   | Master             | $t_{SPCKWH}$ | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | ns          |      |
|                                | Slave              |              | 0.4   | 0.6  | 0.4   | 0.6  |             |      |
| RSPCK clock low pulse width    | Master             | $t_{SPCKWL}$ | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | ns          |      |
|                                | Slave              |              | 0.4   | 0.6  | 0.4   | 0.6  |             |      |
| RSPCK clock rise and fall time | Output             | $t_{SPCKr}$  | —   | 5    | —   | 5    | ns          |      |
|                                | Input              | $t_{SPCKf}$  | —   | 1    | —   | 1    |             |      |
| Data input setup time          | Master             | High Speed*1 | 0   | —    | —   | —    | ns          |      |
|                                |                    | Default*2    | —   | —    | 1.3   | —    |             |      |
|                                | Slave              |              | 2.5   | —    | 2.7   | —    | ns          |      |
| Data input hold time           | Master             | High Speed*1 | 6.2   | —    | —   | —    | ns          |      |
|                                |                    | Default*2    | —   | —    | 8   | —    |             |      |
|                                | Slave              |              | 2.5   | —    | 2.5   | —    | ns          |      |
| SSL setup time                 | Master             | $t_{LEAD}$   | 1   | 8    | 1   | 8    | $t_{SPCyc}$ |      |
|                                | Slave              |              | 6   | —    | 6   | —    |             |      |
| SSL hold time                  | Master             | $t_{LAG}$    | 1   | 8    | 1   | 8    | $t_{SPCyc}$ |      |
|                                | Slave              |              | 6   | —    | 6   | —    |             |      |
| TI SSP SS input setup time     | Slave              | $t_{TISS}$   | 2.5   | —    | 2.8   | —    | ns          |      |
| TI SSP SS input hold time      | Slave              | $t_{TISH}$   | 2.5   | —    | 2.5   | —    | ns          |      |
| TI SSP next-access time        | Slave              | $t_{TIND}$   | $2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$ | —    | $2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$ | —    | ns          |      |
| TI SSP master SS output delay  | Master             | $t_{TISSOD}$ | —   | 8.9  | —   | 8.9  | ns          |      |

## 2.3.10 SPI时序

Table 2.28 SPI时序 (1of2)

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter      | High Speed/Default | Symbol       | VCC = 3.0 to 3.6 V, C = 15 pF               |      | VCC = 2.7 to 3.6 V, C = 30 pF               |      | Unit        | Note |
|----------------|--------------------|--------------|---|------|---|------|-------------|------|
|                |                    |              | Min   | Max  | Min   | Max  |             |      |
| RSPCK时钟周期      | Master             | $t_{SPCyc}$  | 2   | 4096 | 2   | 4096 | $t_{Tcyc}$  |      |
|                | Slave              |              | 2   | —    | 2   | —    |             |      |
| RSPCK时钟高脉冲宽度   | Master             | $t_{SPCKWH}$ | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | ns          |      |
|                | Slave              |              | 0.4   | 0.6  | 0.4   | 0.6  |             |      |
| RSPCK时钟低脉冲宽度   | Master             | $t_{SPCKWL}$ | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | —    | ns          |      |
|                | Slave              |              | 0.4   | 0.6  | 0.4   | 0.6  |             |      |
| RSPCK时钟上升和下降时间 | Output             | $t_{SPCKr}$  | —   | 5    | —   | 5    | ns          |      |
|                | Input              | $t_{SPCKf}$  | —   | 1    | —   | 1    |             |      |
| 数据输入建立时间       | Master             | High Speed*1 | 0   | —    | —   | —    | ns          |      |
|                |                    | Default*2    | —   | —    | 1.3   | —    |             |      |
|                | Slave              |              | 2.5   | —    | 2.7   | —    | ns          |      |
| 数据输入保持时间       | Master             | High Speed*1 | 6.2   | —    | —   | —    | ns          |      |
|                |                    | Default*2    | —   | —    | 8   | —    |             |      |
|                | Slave              |              | 2.5   | —    | 2.5   | —    | ns          |      |
| SSL设置时间        | Master             | $t_{LEAD}$   | 1   | 8    | 1   | 8    | $t_{SPCyc}$ |      |
|                | Slave              |              | 6   | —    | 6   | —    |             |      |
| SSL保持时间        | Master             | $t_{LAG}$    | 1   | 8    | 1   | 8    | $t_{SPCyc}$ |      |
|                | Slave              |              | 6   | —    | 6   | —    |             |      |
| TISSPS输入建立时间   | Slave              | $t_{TISS}$   | 2.5   | —    | 2.8   | —    | ns          |      |
| TISSPS输入保持时间   | Slave              | $t_{TISH}$   | 2.5   | —    | 2.5   | —    | ns          |      |
| TISS下次访问时间     | Slave              | $t_{TIND}$   | $2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$ | —    | $2 \times t_{Tcyc} + SLNDL \times t_{Tcyc}$ | —    | ns          |      |
| TISS主控SS输出延迟   | Master             | $t_{TISSOD}$ | —   | 8.9  | —   | 8.9  | ns          |      |

**Table 2.28 SPI timing (2 of 2)**

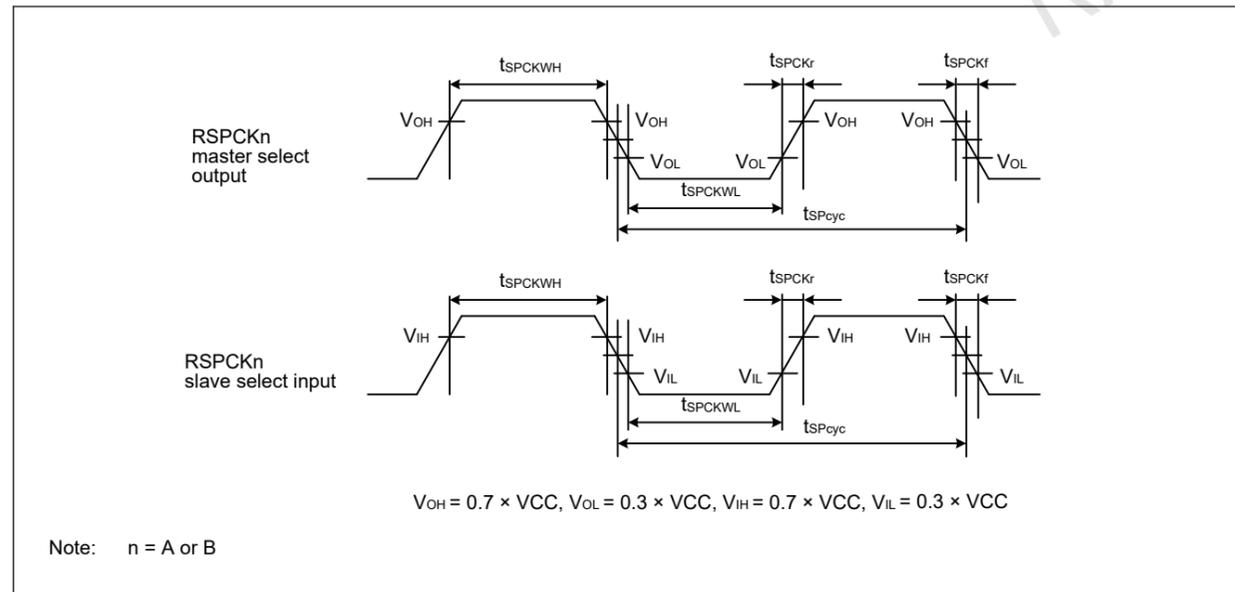
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                          | High Speed/Default | Symbol            | VCC = 3.0 to 3.6 V, C = 15 pF              |  | VCC = 2.7 to 3.6 V, C = 30 pF              |  | Unit | Note |
|------------------------------------|--------------------|-------------------|--|--|--|--|------|------|
|                                    |                    |                   | Min  | Max  | Min  | Max  |      |      |
| Data output delay time             | Master             | High Speed*1      | —  | 4.6  | —  | —  | ns   |      |
|                                    |                    | Default*2         | —  | —  | —  | 7  | ns   |      |
|                                    | Slave              | High Speed*1      | —  | 14   | —  | —  | ns   |      |
|                                    |                    | Default*2         | —  | —  | —  | 21   | ns   |      |
| Data output hold time              | Master             | t <sub>OH</sub>   | 0  | —  | 0  | —  | ns   |      |
|                                    | Slave              | t <sub>OH</sub>   | 0  | —  | 0  | —  | ns   |      |
| Successive transmission delay time | Master             | t <sub>TD</sub>   | t <sub>SPcyc</sub> + 2 × t <sub>Tcyc</sub> | 8 × t <sub>SPcyc</sub> + 2 × t <sub>Pcyc</sub> | t <sub>SPcyc</sub> + 2 × t <sub>Tcyc</sub> | 8 × t <sub>SPcyc</sub> + 2 × t <sub>Pcyc</sub> | ns   |      |
|                                    | Slave              | t <sub>TD</sub>   | t <sub>Tcyc</sub>                          | —  | t <sub>Tcyc</sub>                          | —  | ns   |      |
| MOSI and MISO rise and fall time   | Output             | t <sub>Dr</sub>   | —  | 5  | —  | 5  | ns   |      |
|                                    | Input              | t <sub>Df</sub>   | —  | 1  | —  | 1  | μs   |      |
| SSL rise and fall time             | Output             | t <sub>SSLr</sub> | —  | 5  | —  | 5  | ns   |      |
|                                    | Input              | t <sub>SSLf</sub> | —  | 1  | —  | 1  | μs   |      |
| Slave access time                  | Slave              | t <sub>SA</sub>   | —  | 20   | —  | 20   | ns   |      |
| Slave output release time          | Slave              | t <sub>REL</sub>  | —  | 20   | —  | 20   | ns   |      |

Note: t<sub>Tcyc</sub>: PCLKA or SCISPICLK cycle.

Note 1. Must use pins that have a letter appended to their name, for instance \_A, \_B, \_C, to indicate group membership. SPIA is instance \_B, SPIB is instance \_A.

Note 2. All pins of group membership can be used.



**Figure 2.39 SPI clock timing**

**Table 2.28 SPI时序 (2之2)**

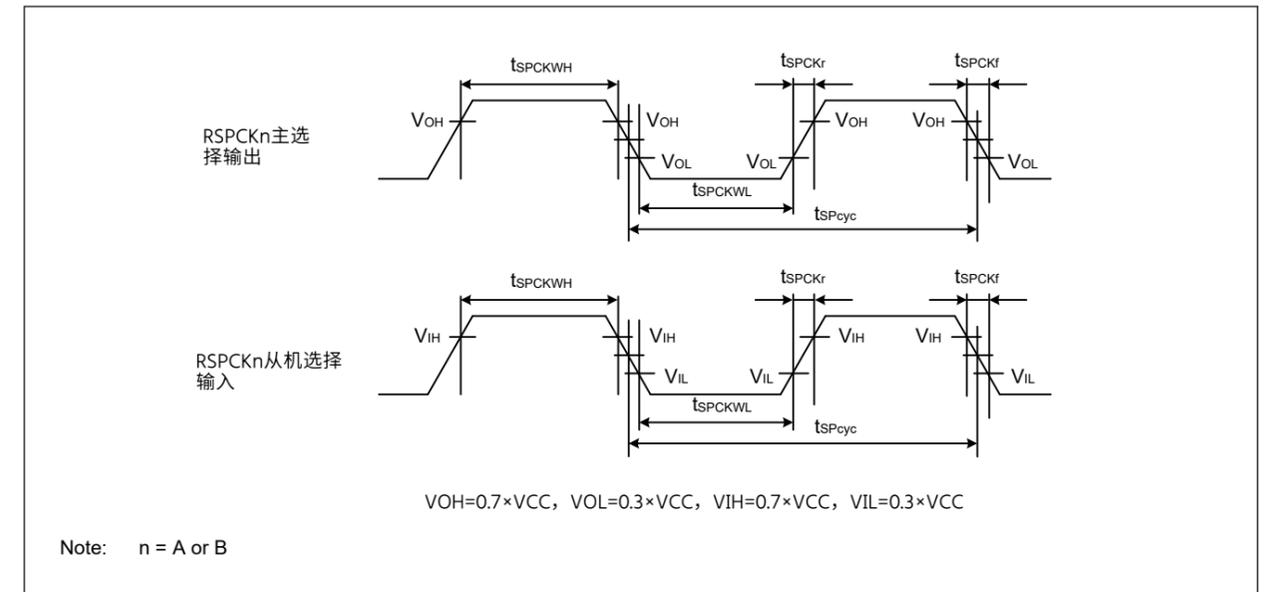
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter        | High Speed/Default | Symbol            | VCC = 3.0 to 3.6 V, C = 15 pF              |  | VCC = 2.7 to 3.6 V, C = 30 pF              |  | Unit | Note |
|------------------|--------------------|-------------------|--|--|--|--|------|------|
|                  |                    |                   | Min  | Max  | Min  | Max  |      |      |
| 数据输出延迟时间         | Master             | High Speed*1      | —  | 4.6  | —  | —  | ns   |      |
|                  |                    | Default*2         | —  | —  | —  | 7  | ns   |      |
|                  | Slave              | High Speed*1      | —  | 14   | —  | —  | ns   |      |
|                  |                    | Default*2         | —  | —  | —  | 21   | ns   |      |
| 数据输出保持时间         | Master             | t <sub>OH</sub>   | 0  | —  | 0  | —  | ns   |      |
|                  | Slave              | t <sub>OH</sub>   | 0  | —  | 0  | —  | ns   |      |
| 连续传输延迟时间         | Master             | t <sub>TD</sub>   | t <sub>SPcyc</sub> + 2 × t <sub>Tcyc</sub> | 8 × t <sub>SPcyc</sub> + 2 × t <sub>Pcyc</sub> | t <sub>SPcyc</sub> + 2 × t <sub>Tcyc</sub> | 8 × t <sub>SPcyc</sub> + 2 × t <sub>Pcyc</sub> | ns   |      |
|                  | Slave              | t <sub>TD</sub>   | t <sub>Tcyc</sub>                          | —  | t <sub>Tcyc</sub>                          | —  | ns   |      |
| MOSI和MISO上升和下降时间 | Output             | t <sub>Dr</sub>   | —  | 5  | —  | 5  | ns   |      |
|                  | Input              | t <sub>Df</sub>   | —  | 1  | —  | 1  | μs   |      |
| SSL上升和下降时间       | Output             | t <sub>SSLr</sub> | —  | 5  | —  | 5  | ns   |      |
|                  | Input              | t <sub>SSLf</sub> | —  | 1  | —  | 1  | μs   |      |
| 从站访问时间           | Slave              | t <sub>SA</sub>   | —  | 20   | —  | 20   | ns   |      |
| 从机输出释放时间         | Slave              | t <sub>REL</sub>  | —  | 20   | —  | 20   | ns   |      |

Note: t<sub>Tcyc</sub>: PCLKA或SCISPICLK周期。

注1.必须使用名称后附有字母的引脚，例如\_A、\_B、\_C，以表示组成员身份。SPIA是实例\_B，SPIB是实例\_A。

注2.可以使用组成员的所有引脚。



**Figure 2.39 SPI时钟时序**

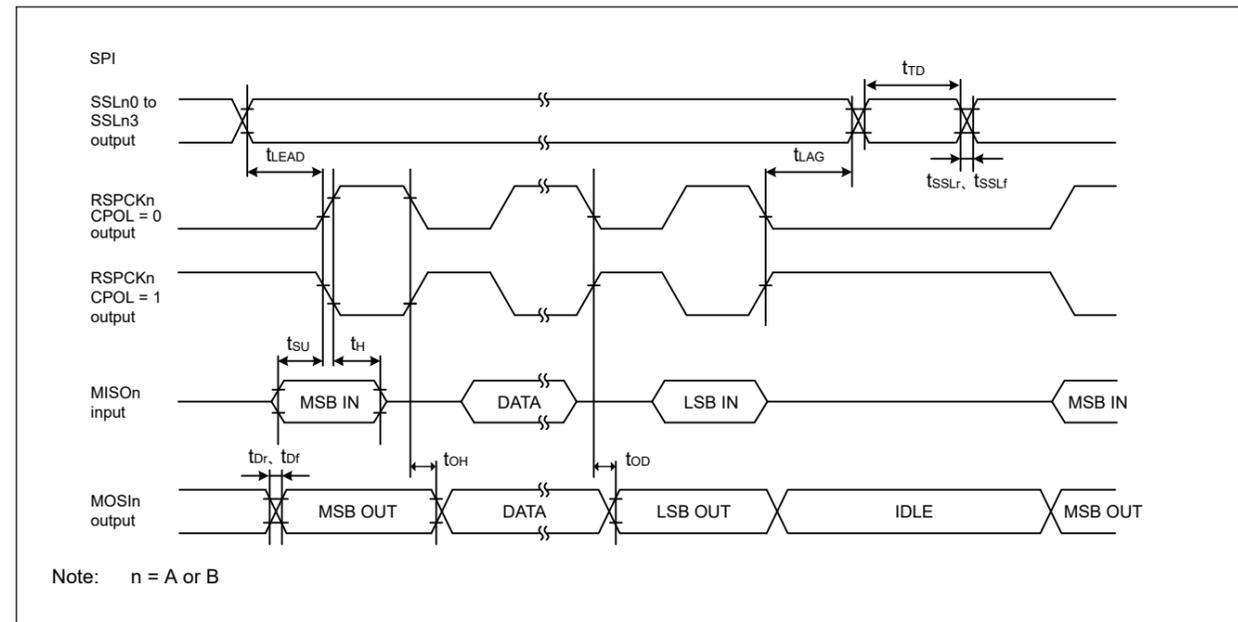


Figure 2.40 SPI timing for Motorola SPI master when CPHA = 0

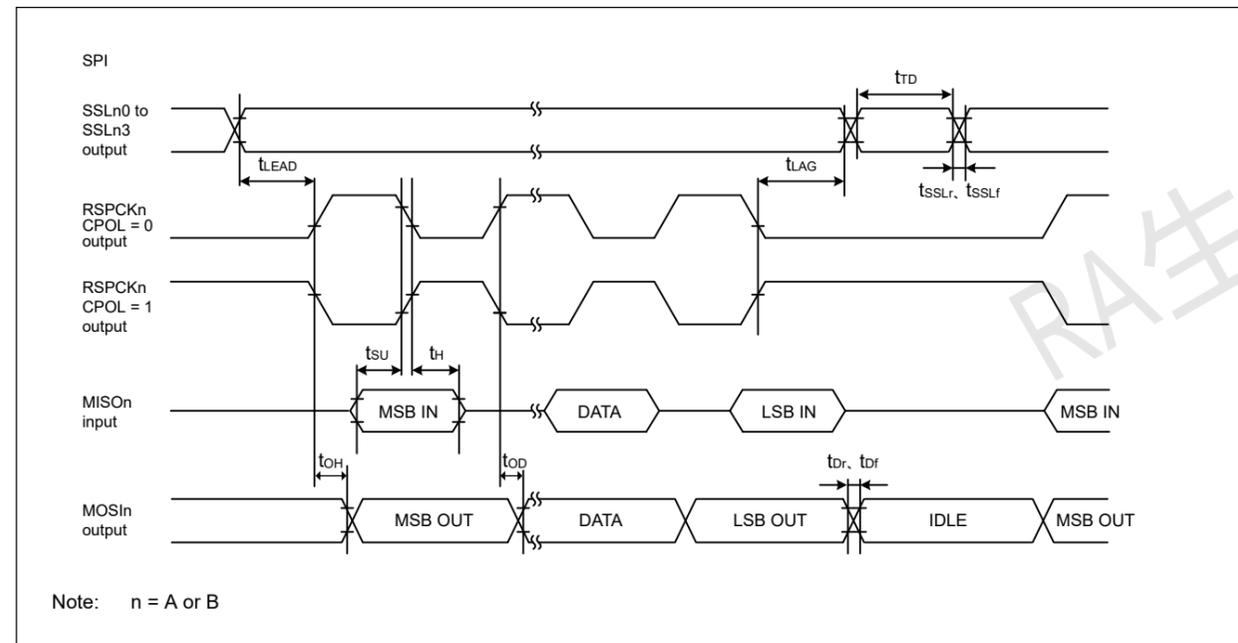


Figure 2.41 SPI timing for Motorola SPI master when CPHA = 1

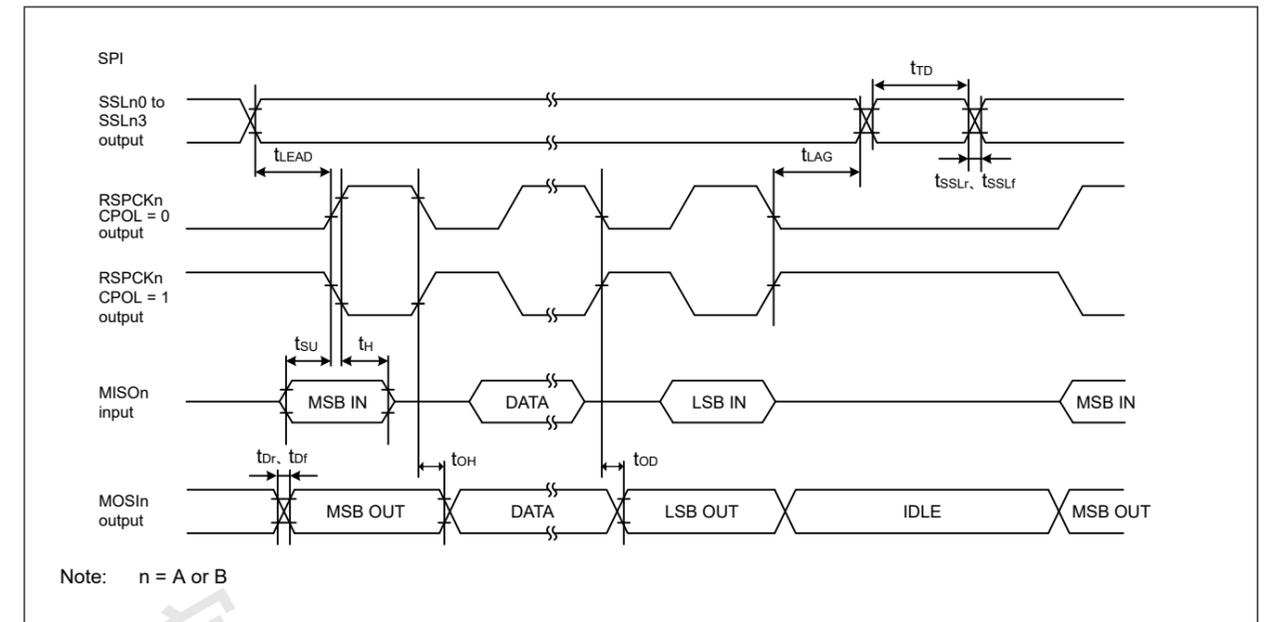


Figure 2.40 CPHA=0时MotorolaSPI主机的SPI时序

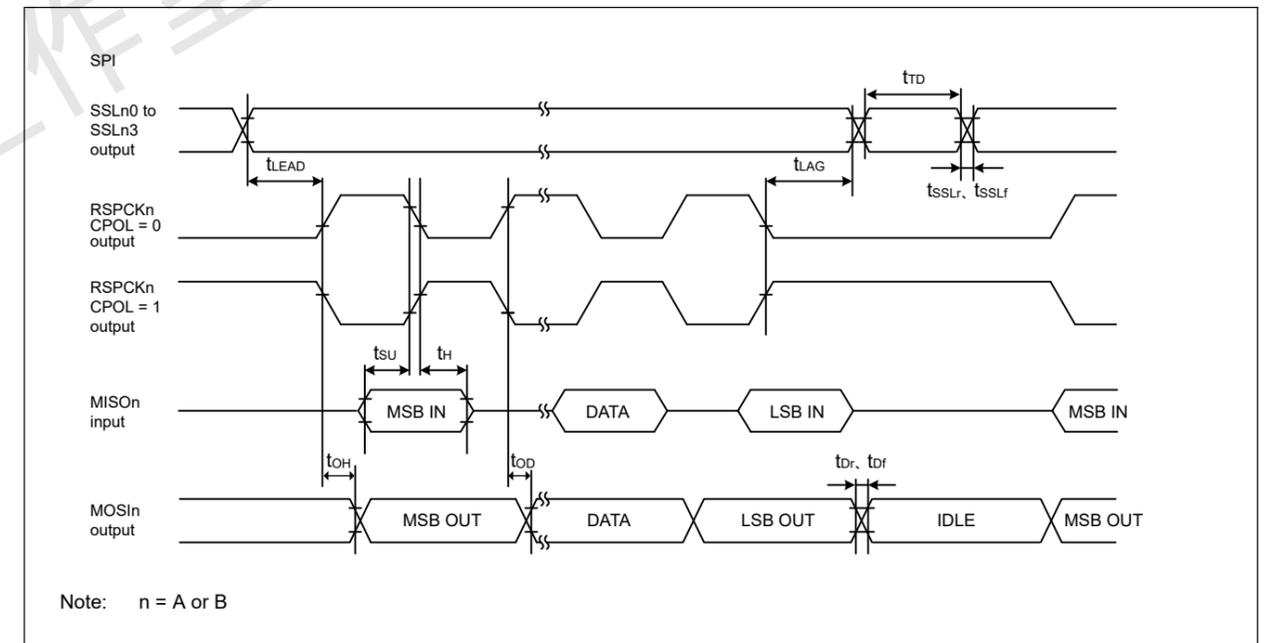


Figure 2.41 CPHA=1时摩托罗拉SPI主机的SPI时序

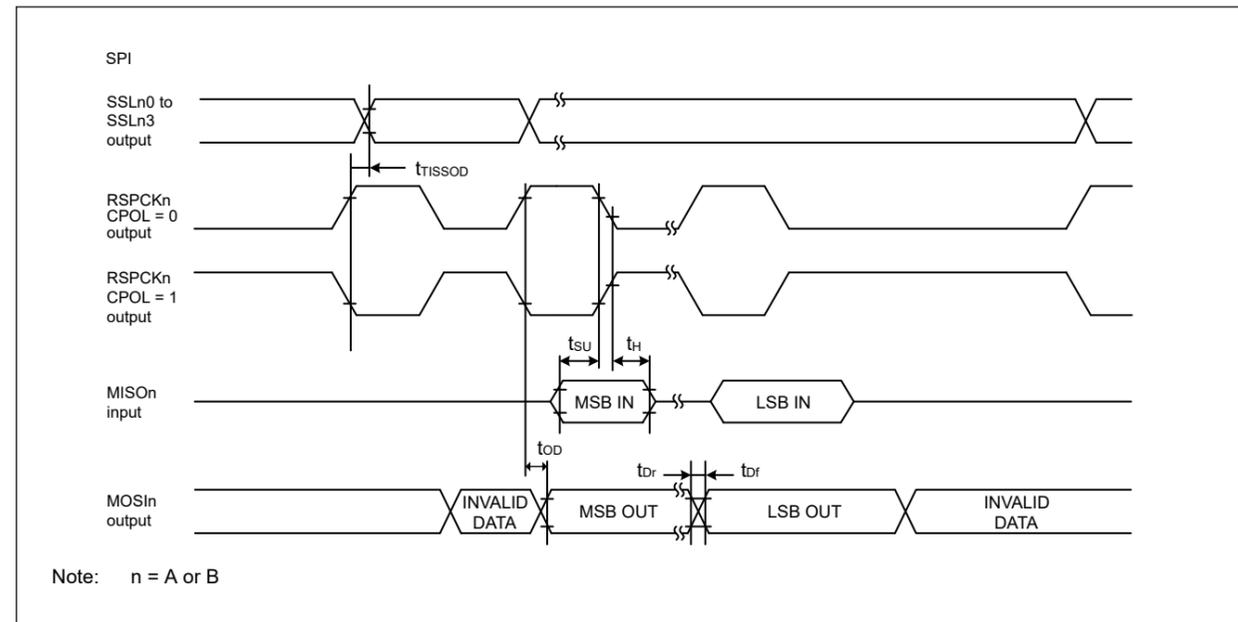


Figure 2.42 SPI timing for TI SSP master

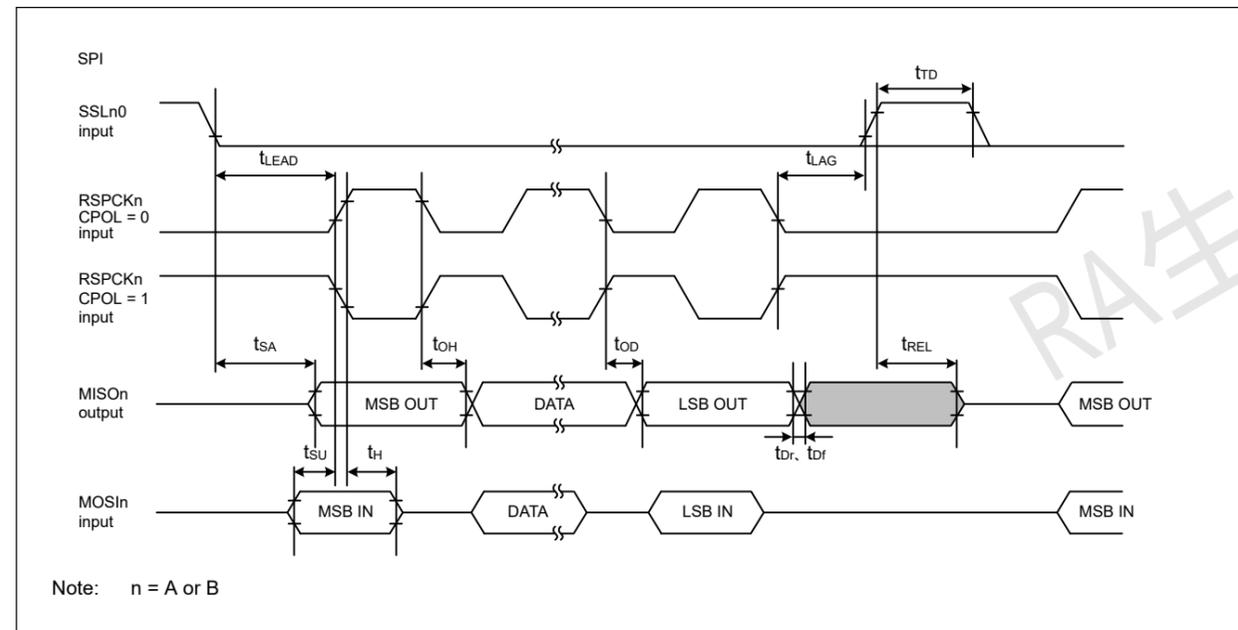


Figure 2.43 SPI timing for Motorola SPI slave when CPHA = 0

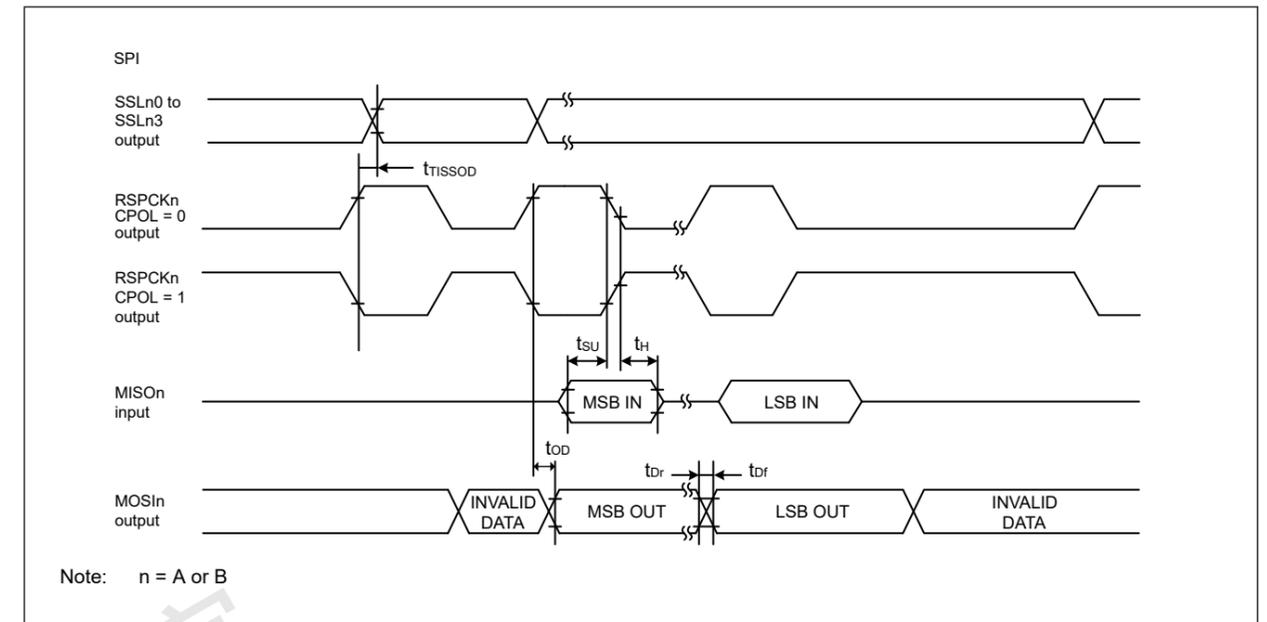


Figure 2.42 TI SSP主控的SPI时序

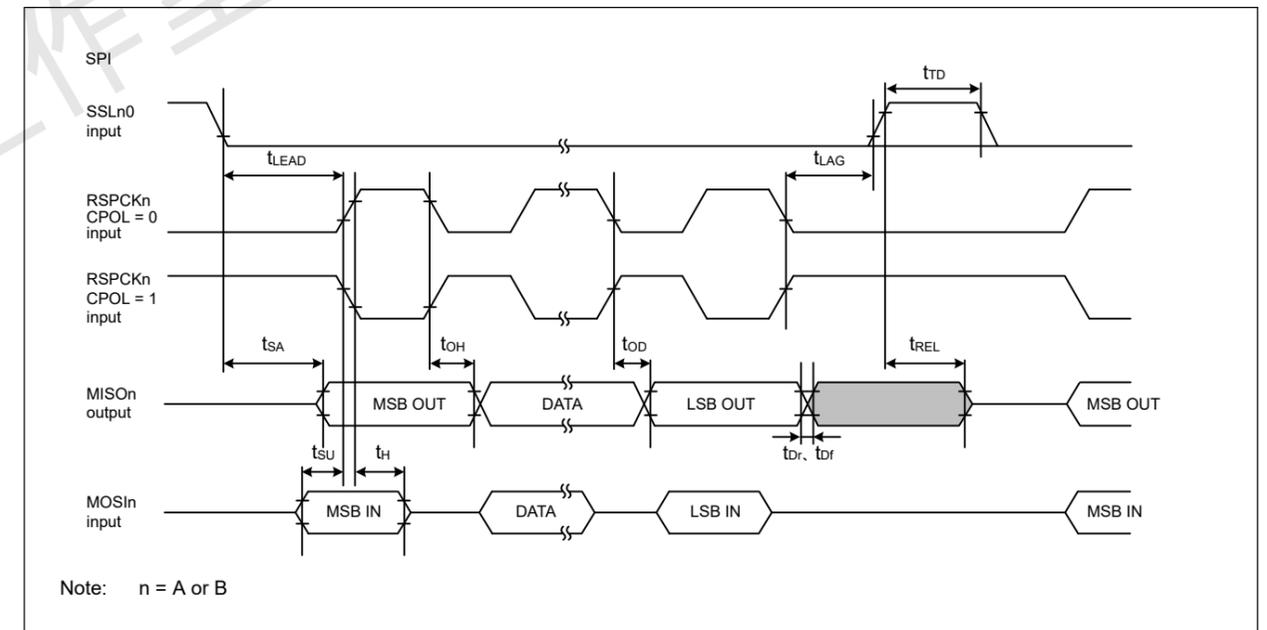


Figure 2.43 CPHA=0时Motorola SPI从机的SPI时序

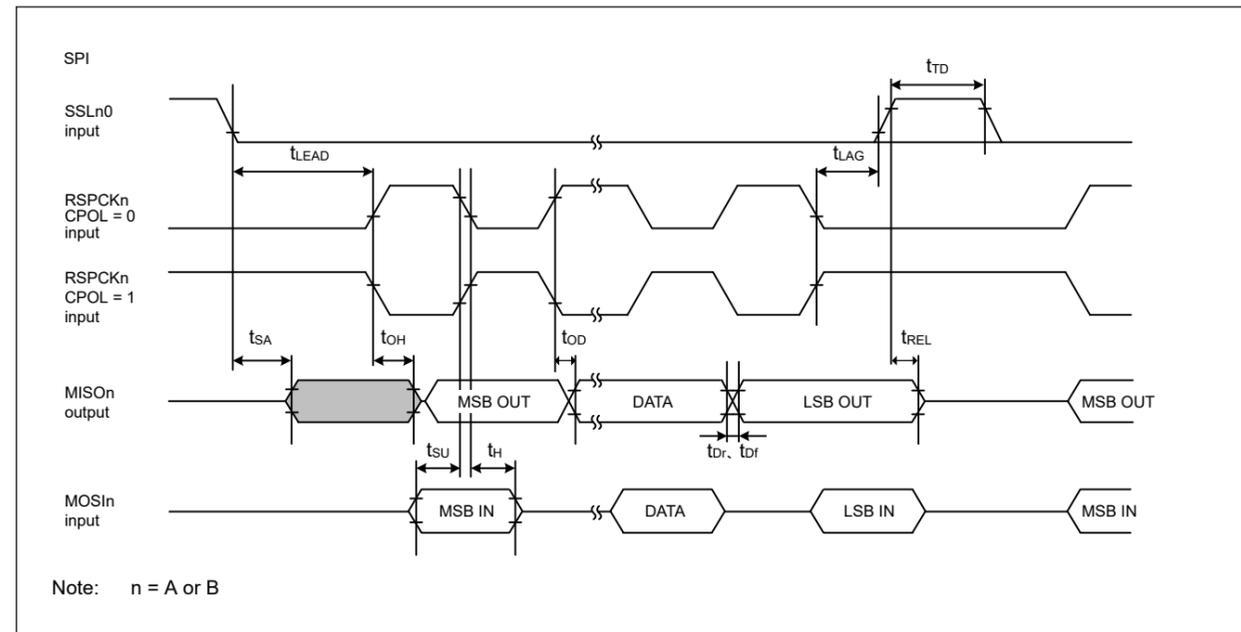


Figure 2.44 SPI timing for Motorola SPI slave when CPHA = 1

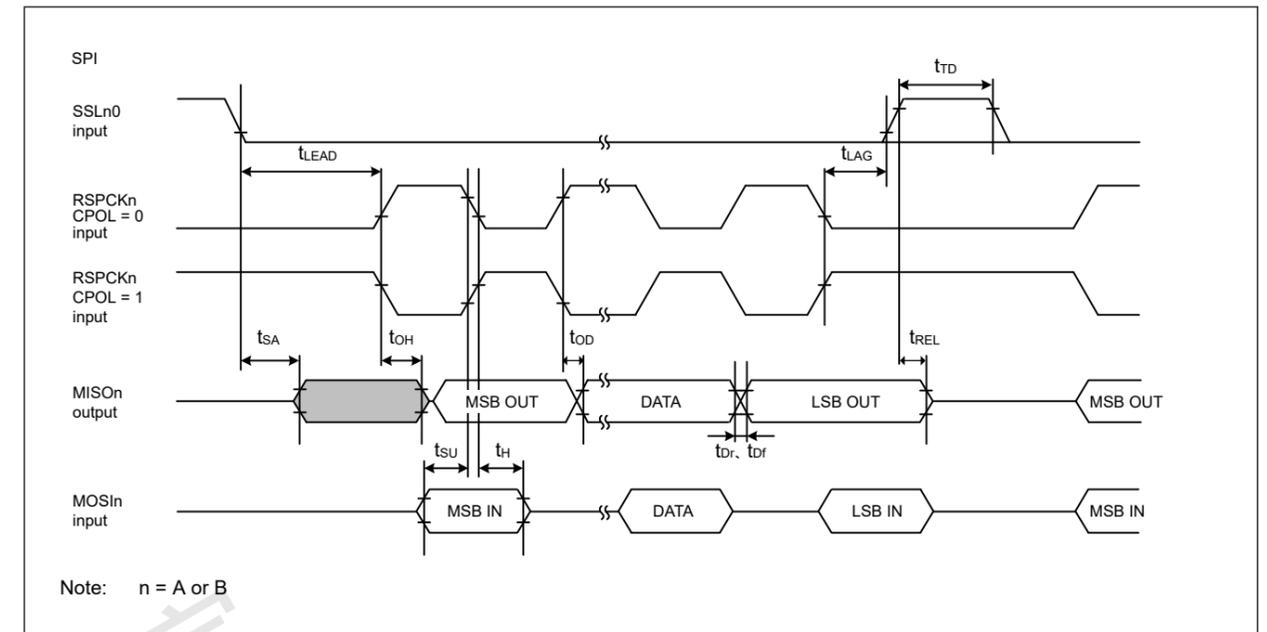


Figure 2.44 CPHA=1时摩托罗拉SPI从机的SPI时序

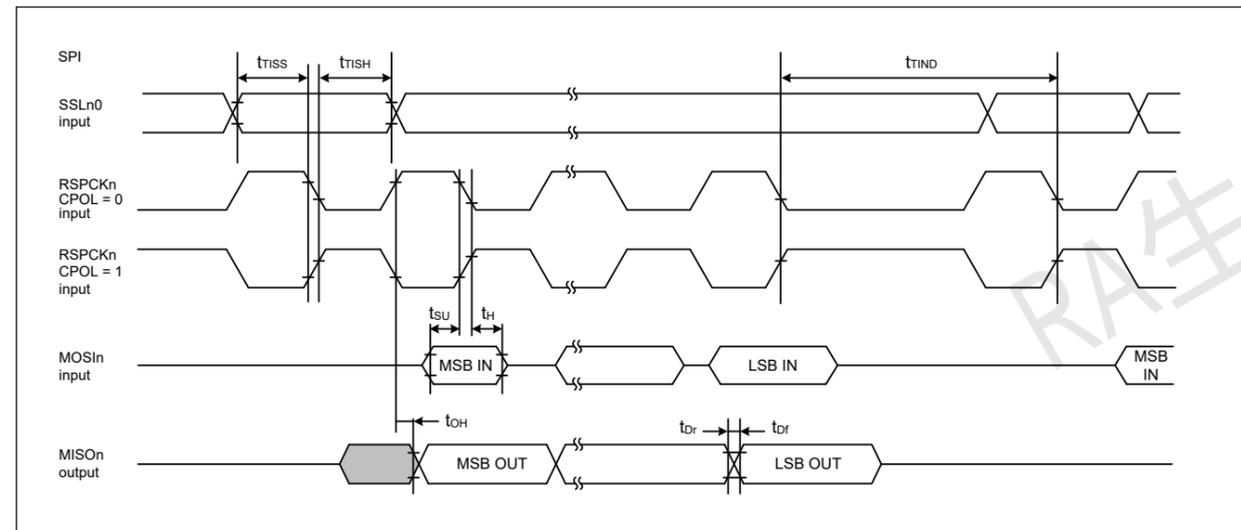


Figure 2.45 SPI timing for TI SSP slave when transmit with delay between frames

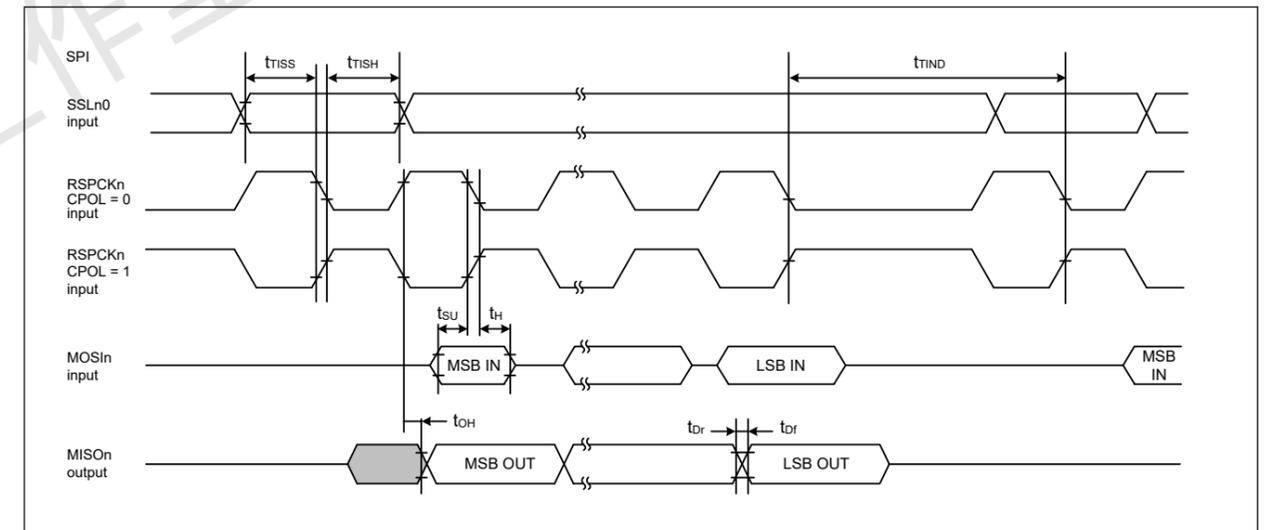


Figure 2.45 TISSP从机在帧间延迟传输时的SPI时序

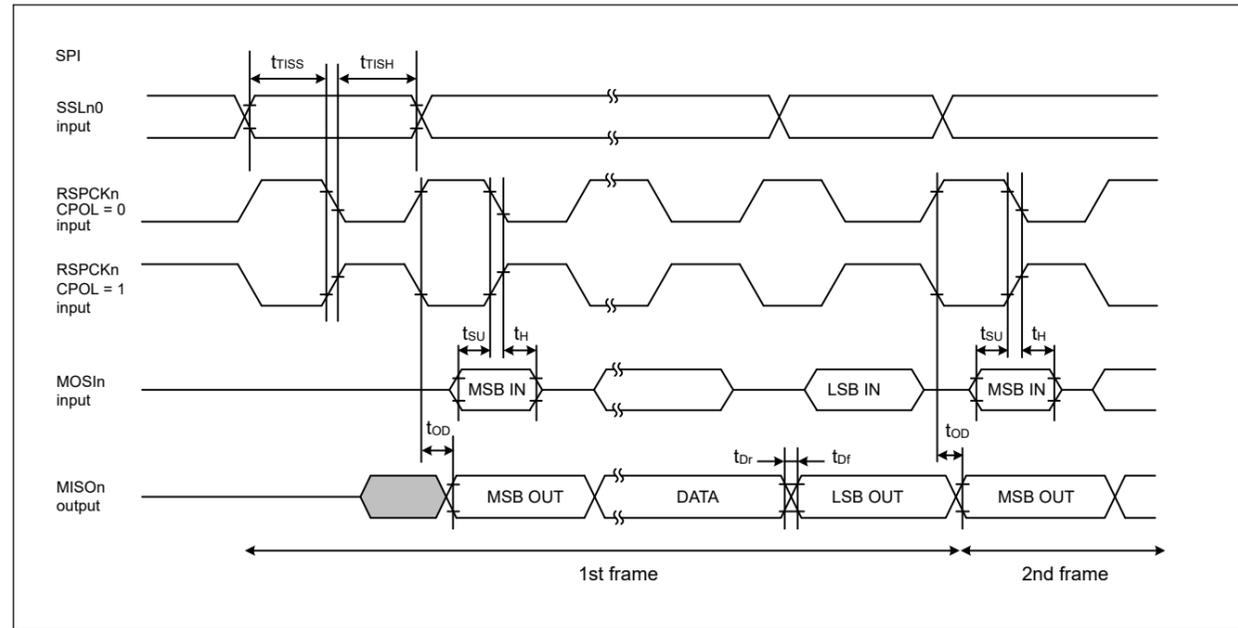


Figure 2.46 SPI timing for TI SSP slave when transmit with no delay between frames

2.3.11 IIC Timing

Table 2.29 IIC timing (1)-1

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_B, SCL1\_B, SCL0\_C, SDA0\_C, SCL0\_D, SDA0\_D, SCL0\_E, SDA0\_E, SCL0\_F, SDA0\_F, SCL1\_C, SDA1\_C, SCL1\_D, SDA1\_D, SCL1\_E, SDA1\_E.  
 (2) The following pins do not require setting: SCL0\_A, SDA0\_A, SCL1\_A, SDA1\_A.  
 (3) Use pins that have a letter appended to their names, for instance \_A or \_B or \_C or \_D or \_E or \_F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter                                 | Symbol                                    | Min        | Max                               | Unit                     | Test conditions |             |
|---|---|------------|-----------------------------------|--------------------------|-----------------|-------------|
| IIC (Standard mode, SMBus) BFCTL.FMPE = 0 | SCL input cycle time                      | $t_{SCL}$  | $10 (18) \times t_{IICyc} + 1300$ | —                        | ns              | Figure 2.47 |
|   | SCL input high pulse width                | $t_{SCLH}$ | $5 (9) \times t_{IICyc}$          | —                        | ns              |             |
|   | SCL input low pulse width                 | $t_{SCLL}$ | $5 (9) \times t_{IICyc}$          | —                        | ns              |             |
|   | SCL, SDA rise time                        | $t_{Sr}$   | —                                 | 1000                     | ns              |             |
|   | SCL, SDA fall time                        | $t_{Sf}$   | —                                 | 300                      | ns              |             |
|   | SCL, SDA input spike pulse removal time   | $t_{SP}$   | 0                                 | $1 (4) \times t_{IICyc}$ | ns              |             |
|   | SDA input bus free time                   | $t_{BUF}$  | $5 (9) \times t_{IICyc} + 300$    | —                        | ns              |             |
|   | START condition input hold time           | $t_{STAH}$ | $t_{IICyc} + 300$                 | —                        | ns              |             |
|   | Repeated START condition input setup time | $t_{STAS}$ | 1000                              | —                        | ns              |             |
|   | STOP condition input setup time           | $t_{STOS}$ | 1000                              | —                        | ns              |             |
|   | Data input setup time                     | $t_{SDAS}$ | $t_{IICyc} + 50$                  | —                        | ns              |             |
|   | Data input hold time                      | $t_{SDAH}$ | 0                                 | —                        | ns              |             |
|   | SCL, SDA capacitive load                  | $C_b^{*1}$ | —                                 | 400                      | pF              |             |

Note:  $t_{IICyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle.  
 Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.  
 Note 1.  $C_b$  indicates the total capacity of the bus line.

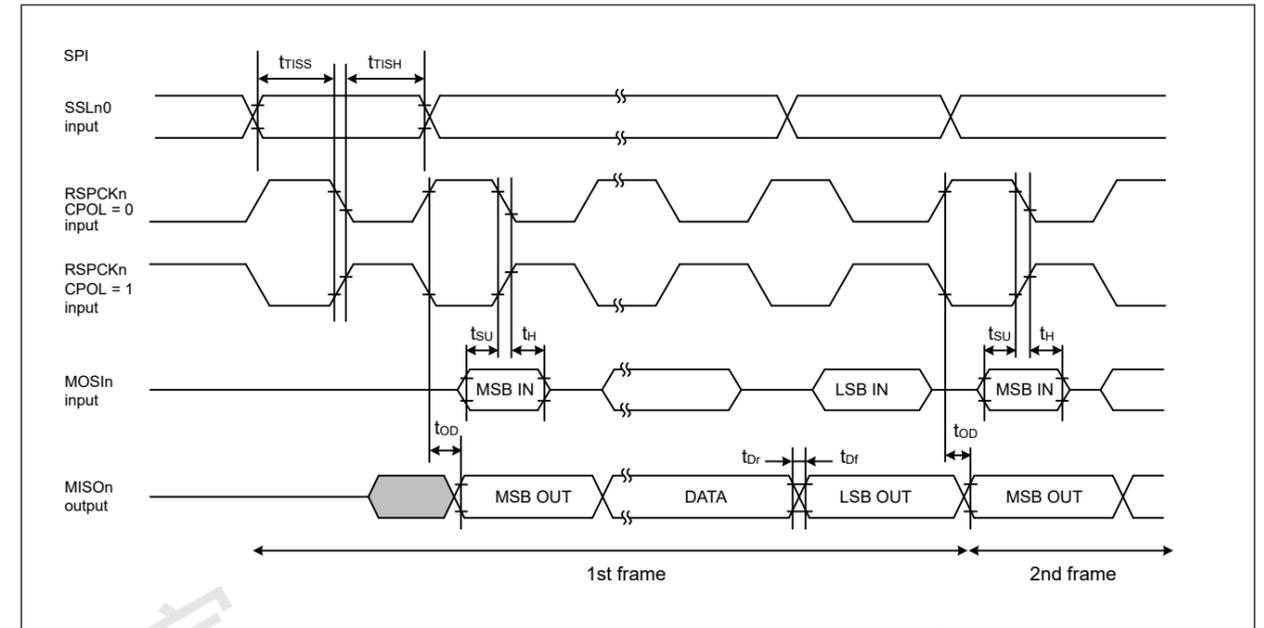


Figure 2.46 TISSP从机在帧之间无延迟传输时的SPI时序

2.3.11 IIC Timing

Table 2.29 IIC timing (1)-1

(1)条件: 在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出: SDA0\_B、SCL0\_B、SDA1\_B、SCL1\_B、SCL0\_C、SDA0\_C、SCL0\_D、SDA0\_D、SCL0\_E、SDA0\_E、SCL0\_F、SDA0\_F、SCL1\_C、SDA1\_C、SCL1\_D、SDA1\_D、SCL1\_E、SDA1\_E。(2)以下引脚不需要设置: SCL0\_A、SDA0\_A、SCL1\_A、SDA1\_A。(3)使用名称后附有字母的引脚,例如\_A或\_B或\_C或\_D或\_E或\_F,以表示组成员身份。对于IIC接口,测量每组的电气特性的交流部分。

| Parameter                                 | Symbol                   | Min        | Max                               | Unit                     | 测试条件 |             |
|---|--------------------------|------------|-----------------------------------|--------------------------|------|-------------|
| IIC (Standard mode, SMBus) BFCTL.FMPE = 0 | SCL输入周期时间                | $t_{SCL}$  | $10 (18) \times t_{IICyc} + 1300$ | —                        | ns   | Figure 2.47 |
|   | SCL输入高脉冲宽度               | $t_{SCLH}$ | $5 (9) \times t_{IICyc}$          | —                        | ns   |             |
|   | SCL输入低脉冲宽度               | $t_{SCLL}$ | $5 (9) \times t_{IICyc}$          | —                        | ns   |             |
|   | SCL、SDA上升时间              | $t_{Sr}$   | —                                 | 1000                     | ns   |             |
|   | SCL、SDA下降时间              | $t_{Sf}$   | —                                 | 300                      | ns   |             |
|   | SCL、SDA输入尖峰脉冲去除时间        | $t_{SP}$   | 0                                 | $1 (4) \times t_{IICyc}$ | ns   |             |
|   | SDA输入总线空闲时间              | $t_{BUF}$  | $5 (9) \times t_{IICyc} + 300$    | —                        | ns   |             |
|   | START条件输入保持时间            | $t_{STAH}$ | $t_{IICyc} + 300$                 | —                        | ns   |             |
|   | 重复启动条件输入建立时间             | $t_{STAS}$ | 1000                              | —                        | ns   |             |
|   | STOP条件输入建立时间             | $t_{STOS}$ | 1000                              | —                        | ns   |             |
|   | 数据输入建立时间                 | $t_{SDAS}$ | $t_{IICyc} + 50$                  | —                        | ns   |             |
|   | 数据输入保持时间                 | $t_{SDAH}$ | 0                                 | —                        | ns   |             |
|   | SCL, SDA capacitive load | $C_b^{*1}$ | —                                 | 400                      | pF   |             |

Note:  $t_{IICyc}$ : IIC内部参考时钟(IIC $\phi$ )周期。  
 Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。  
 注1.C<sub>b</sub>表示公交线路的总容量。

**Table 2.30 IIC timing (1)-2**

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_B, SCL1\_B, SCL0\_C, SDA0\_C, SCL0\_D, SDA0\_D, SCL0\_E, SDA0\_E, SCL0\_F, SDA0\_F, SCL1\_C, SDA1\_C, SCL1\_D, SDA1\_D, SCL1\_E, SDA1\_E.

(2) The following pins do not require setting: SCL0\_A, SDA0\_A, SCL1\_A, SDA1\_A.

(3) Use pins that have a letter appended to their names, for instance \_A or \_B or \_C or \_D or \_E or \_F, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter       | Symbol                                    | Min        | Max  | Unit                     | Test conditions |             |
|-----------------|---|------------|--|--------------------------|-----------------|-------------|
| IIC (Fast-mode) | SCL input cycle time                      | $t_{SCL}$  | $10 (18) \times t_{IICyc} + 600$                         | —                        | ns              | Figure 2.47 |
|                 | SCL input high pulse width                | $t_{SCLH}$ | $5 (9) \times t_{IICyc}$                                 | —                        | ns              |             |
|                 | SCL input low pulse width                 | $t_{SCLL}$ | $5 (9) \times t_{IICyc}$                                 | —                        | ns              |             |
|                 | SCL, SDA rise time                        | $t_{Sr}$   | $20 \times (\text{external pullup voltage} / 5.5V)^{*1}$ | 300                      | ns              |             |
|                 | SCL, SDA fall time                        | $t_{Sf}$   | $20 \times (\text{external pullup voltage} / 5.5V)^{*1}$ | 300                      | ns              |             |
|                 | SCL, SDA input spike pulse removal time   | $t_{SP}$   | 0  | $1 (4) \times t_{IICyc}$ | ns              |             |
|                 | SDA input bus free time                   | $t_{BUF}$  | $5 (9) \times t_{IICyc} + 300$                           | —                        | ns              |             |
|                 | START condition input hold time           | $t_{STAH}$ | $t_{IICyc} + 300$  | —                        | ns              |             |
|                 | Repeated START condition input setup time | $t_{STAS}$ | 300  | —                        | ns              |             |
|                 | STOP condition input setup time           | $t_{STOS}$ | 300  | —                        | ns              |             |
|                 | Data input setup time                     | $t_{SDAS}$ | $t_{IICyc} + 50$   | —                        | ns              |             |
|                 | Data input hold time                      | $t_{SDAH}$ | 0  | —                        | ns              |             |
|                 | SCL, SDA capacitive load                  | $C_b^{*2}$ | —  | 400                      | pF              |             |

Note:  $t_{IICyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note: Must use pins that have a letter appended to their name, for instance \_A, \_B, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Note 1. Only supported for SCL0\_A, SDA0\_A, SCL1\_A, and SDA1\_A. Other ports are depend on DC characteristics.

Note 2.  $C_b$  indicates the total capacity of the bus line.

**Table 2.30 IIC timing (1)-2**

(1)条件: 在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出: SDA0\_B、SCL0\_B、SDA1\_B、SCL1\_B、SCL0\_C、SDA0\_C、SCL0\_D、SDA0\_D、SCL0\_E、SDA0\_E、SCL0\_F、SDA0\_F、SCL1\_C、SDA1\_C、SCL1\_D、SDA1\_D、SCL1\_E、SDA1\_E。(2)以下引脚不需要设置: SCL0\_A、SDA0\_A、SCL1\_A、SDA1\_A。(3)使用名称后附有字母的引脚, 例如\_A或\_B或\_C或\_D或\_E或\_F, 以表示组成员身份。对于IIC接口, 测量每组的电气特性的交流部分。

(2)以下引脚不需要设置: SCL0\_A、SDA0\_A、SCL1\_A、SDA1\_A。(3)使用名称后附有字母的引脚, 例如\_A或\_B或\_C或\_D或\_E或\_F, 以表示组成员身份。对于IIC接口, 测量每组的电气特性的交流部分。

| Parameter       | Symbol                   | Min        | Max  | Unit                     | 测试条件 |             |
|-----------------|--------------------------|------------|--|--------------------------|------|-------------|
| IIC (Fast-mode) | SCL输入周期时间                | $t_{SCL}$  | $10 (18) \times t_{IICyc} + 600$                         | —                        | ns   | Figure 2.47 |
|                 | SCL输入高脉冲宽度               | $t_{SCLH}$ | $5 (9) \times t_{IICyc}$                                 | —                        | ns   |             |
|                 | SCL输入低脉冲宽度               | $t_{SCLL}$ | $5 (9) \times t_{IICyc}$                                 | —                        | ns   |             |
|                 | SCL、SDA上升时间              | $t_{Sr}$   | $20 \times (\text{external pullup voltage} / 5.5V)^{*1}$ | 300                      | ns   |             |
|                 | SCL、SDA下降时间              | $t_{Sf}$   | $20 \times (\text{external pullup voltage} / 5.5V)^{*1}$ | 300                      | ns   |             |
|                 | SCL、SDA输入尖峰脉冲去除时间        | $t_{SP}$   | 0  | $1 (4) \times t_{IICyc}$ | ns   |             |
|                 | SDA输入总线空闲时间              | $t_{BUF}$  | $5 (9) \times t_{IICyc} + 300$                           | —                        | ns   |             |
|                 | START条件输入保持时间            | $t_{STAH}$ | $t_{IICyc} + 300$  | —                        | ns   |             |
|                 | 重复启动条件输入建立时间             | $t_{STAS}$ | 300  | —                        | ns   |             |
|                 | STOP条件输入建立时间             | $t_{STOS}$ | 300  | —                        | ns   |             |
|                 | 数据输入建立时间                 | $t_{SDAS}$ | $t_{IICyc} + 50$   | —                        | ns   |             |
|                 | 数据输入保持时间                 | $t_{SDAH}$ | 0  | —                        | ns   |             |
|                 | SCL, SDA capacitive load | $C_b^{*2}$ | —  | 400                      | pF   |             |

Note:  $t_{IICyc}$ : IIC内部参考时钟(IIC $\phi$ )周期。

Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。

Note: 必须使用名称后附有字母的引脚, 例如\_A、\_B, 以表明组成员身份。对于IIC接口, 测量每组的电气特性的交流部分。

注1.仅支持SCL0\_A、SDA0\_A、SCL1\_A和SDA1\_A。其他端口取决于直流特性。

注2. $C_b$ 表示公交线路的总容量。

Table 2.31 IIC timing (1)-3

Setting of the SCL0\_A, SDA0\_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter                             | Symbol                                    | Min        | Max                               | Unit                      | Test conditions |             |
|---------------------------------------|---|------------|-----------------------------------|---------------------------|-----------------|-------------|
| IIC<br>(Fast-mode+)<br>BFCTL.FMPE = 1 | SCL input cycle time                      | $t_{SCL}$  | $10 (18) \times t_{IICcyc} + 240$ | —                         | ns              | Figure 2.47 |
|                                       | SCL input high pulse width                | $t_{SCLH}$ | $5 (9) \times t_{IICcyc}$         | —                         | ns              |             |
|                                       | SCL input low pulse width                 | $t_{SCLL}$ | $5 (9) \times t_{IICcyc}$         | —                         | ns              |             |
|                                       | SCL, SDA rise time                        | $t_{Sr}$   | —                                 | 120                       | ns              |             |
|                                       | SCL, SDA fall time                        | $t_{Sf}$   | —                                 | 120                       | ns              |             |
|                                       | SCL, SDA input spike pulse removal time   | $t_{SP}$   | 0                                 | $1 (4) \times t_{IICcyc}$ | ns              |             |
|                                       | SDA input bus free time                   | $t_{BUF}$  | $5 (9) \times t_{IICcyc} + 120$   | —                         | ns              |             |
|                                       | START condition input hold time           | $t_{STAH}$ | $t_{IICcyc} + 120$                | —                         | ns              |             |
|                                       | Repeated START condition input setup time | $t_{STAS}$ | 120                               | —                         | ns              |             |
|                                       | STOP condition input setup time           | $t_{STOS}$ | 120                               | —                         | ns              |             |
|                                       | Data input setup time                     | $t_{SDAS}$ | $t_{IICcyc} + 30$                 | —                         | ns              |             |
|                                       | Data input hold time                      | $t_{SDAH}$ | 0                                 | —                         | ns              |             |
|                                       | SCL, SDA capacitive load                  | $C_b^{*1}$ | —                                 | 550                       | pF              |             |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note: Targets are SCL0\_A and SDA0\_A.

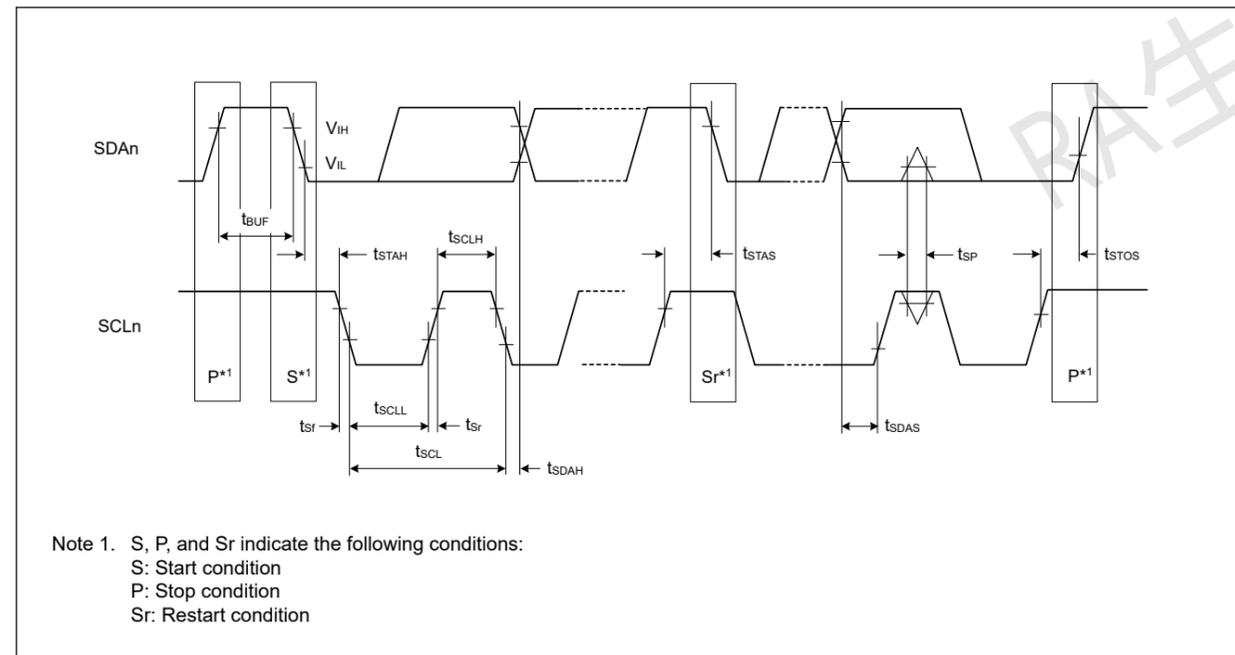
Note 1.  $C_b$  indicates the total capacity of the bus line.Figure 2.47 I<sup>2</sup>C bus interface input/output timing

Table 2.31 IIC timing (1)-3

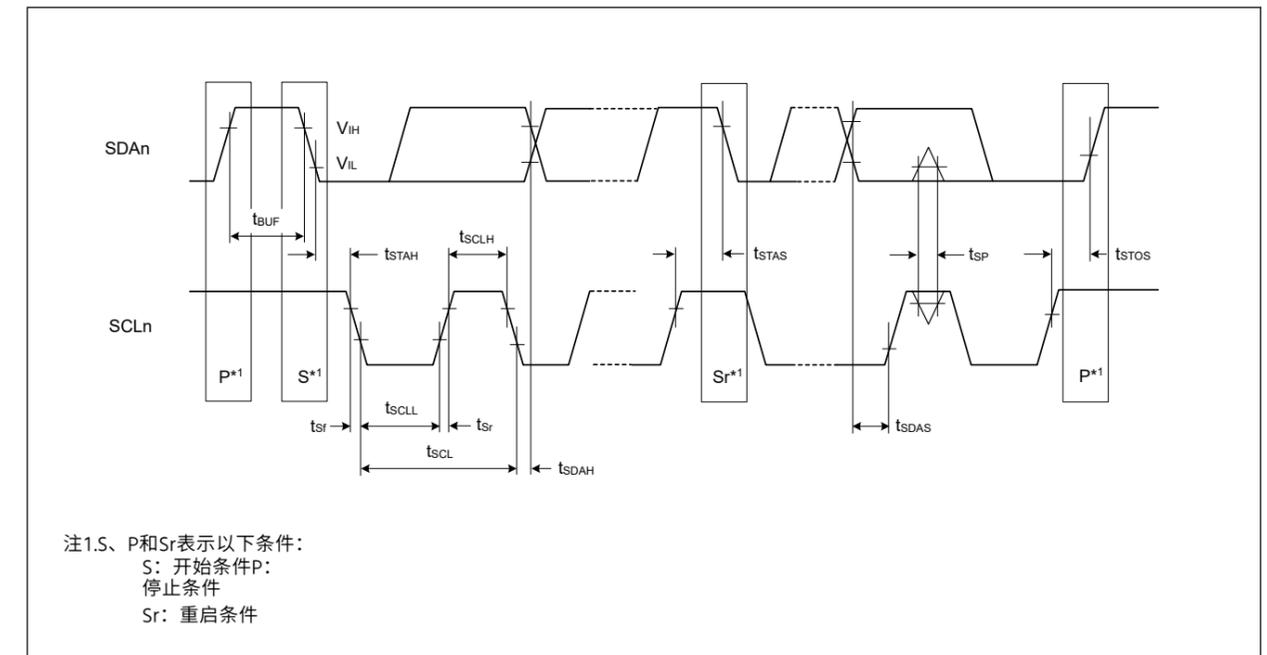
PmnPFS寄存器中的端口驱动能力位不需要设置SCL0\_A、SDA0\_A引脚。

| Parameter                             | Symbol                   | Min        | Max                               | Unit                      | 测试条件 |             |
|---------------------------------------|--------------------------|------------|-----------------------------------|---------------------------|------|-------------|
| IIC<br>(Fast-mode+)<br>BFCTL.FMPE = 1 | SCL输入周期时间                | $t_{SCL}$  | $10 (18) \times t_{IICcyc} + 240$ | —                         | ns   | Figure 2.47 |
|                                       | SCL输入高脉冲宽度               | $t_{SCLH}$ | $5 (9) \times t_{IICcyc}$         | —                         | ns   |             |
|                                       | SCL输入低脉冲宽度               | $t_{SCLL}$ | $5 (9) \times t_{IICcyc}$         | —                         | ns   |             |
|                                       | SCL、SDA上升时间              | $t_{Sr}$   | —                                 | 120                       | ns   |             |
|                                       | SCL、SDA下降时间              | $t_{Sf}$   | —                                 | 120                       | ns   |             |
|                                       | SCL、SDA输入尖峰脉冲去除时间        | $t_{SP}$   | 0                                 | $1 (4) \times t_{IICcyc}$ | ns   |             |
|                                       | SDA输入总线空闲时间              | $t_{BUF}$  | $5 (9) \times t_{IICcyc} + 120$   | —                         | ns   |             |
|                                       | START条件输入保持时间            | $t_{STAH}$ | $t_{IICcyc} + 120$                | —                         | ns   |             |
|                                       | 重复启动条件输入建立时间             | $t_{STAS}$ | 120                               | —                         | ns   |             |
|                                       | STOP条件输入建立时间             | $t_{STOS}$ | 120                               | —                         | ns   |             |
|                                       | 数据输入建立时间                 | $t_{SDAS}$ | $t_{IICcyc} + 30$                 | —                         | ns   |             |
|                                       | 数据输入保持时间                 | $t_{SDAH}$ | 0                                 | —                         | ns   |             |
|                                       | SCL, SDA capacitive load | $C_b^{*1}$ | —                                 | 550                       | pF   |             |

Note:  $t_{IICcyc}$ : IIC内部参考时钟(IIC $\phi$ )周期。

Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。

Note: 目标是SCL0\_A和SDA0\_A。

注1.  $C_b$ 表示公交线路的总容量。Figure 2.47 I<sup>2</sup>C总线接口输入输出时序

**Table 2.32 IIC timing (2)**

Setting of the SCL0\_A, SDA0\_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter                       | Symbol                                    | Min                  | Max                              | Unit                      | Test conditions |             |    |
|---------------------------------|---|----------------------|----------------------------------|---------------------------|-----------------|-------------|----|
| IIC (Hs-mode)<br>BFCTL.HSME = 1 | SCL input cycle time                      | $t_{SCL}$            | $10 (12) \times t_{IICcyc} + 80$ | —                         | ns              | Figure 2.48 |    |
|                                 | SCL input high pulse width                | $t_{SCLH}$           | $5 (6) \times t_{IICcyc}$        | —                         | ns              |             |    |
|                                 | SCL input low pulse width                 | $t_{SCLL}$           | $5 (6) \times t_{IICcyc}$        | —                         | ns              |             |    |
|                                 | SCL rise time                             | $t_{SrCL}$           | $C_b = 400\text{pF}$             | —                         | 80              |             | ns |
|                                 |   |                      | $C_b = 100\text{pF}$             | —                         | 40              |             | ns |
|                                 | SDA rise time                             | $t_{SrDA}$           | $C_b = 400\text{pF}$             | —                         | 160             |             | ns |
|                                 |   |                      | $C_b = 100\text{pF}$             | —                         | 80              |             | ns |
|                                 | SCL fall time                             | $t_{SfCL}$           | $C_b = 400\text{pF}$             | —                         | 80              |             | ns |
|                                 |   |                      | $C_b = 100\text{pF}$             | —                         | 40              |             | ns |
|                                 | SDA fall time                             | $t_{SfDA}$           | $C_b = 400\text{pF}$             | —                         | 160             |             | ns |
|                                 |   |                      | $C_b = 100\text{pF}$             | —                         | 80              |             | ns |
|                                 | SCL, SDA input spike pulse removal time   | $t_{SP}$             | 0                                | $1 (1) \times t_{IICcyc}$ | ns              |             |    |
|                                 | Repeated START condition input setup time | $t_{STAS}$           | 40                               | —                         | ns              |             |    |
|                                 | STOP condition input setup time           | $t_{STOS}$           | 40                               | —                         | ns              |             |    |
| Data input setup time           | $t_{SDAS}$                                | 10                   | —                                | ns                        |                 |             |    |
| Data input hold time            | $t_{SDAH}$                                | $C_b = 400\text{pF}$ | 0                                | 150                       | ns              |             |    |
|                                 |   | $C_b = 100\text{pF}$ | 0                                | 70                        | ns              |             |    |
| SCL, SDA capacitive load        | $C_b^{*1}$                                | —                    | 400                              | pF                        |                 |             |    |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IICφ) cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note: Targets are SCL0\_A and SDA0\_A.

Note 1.  $C_b$  indicates the total capacity of the bus line.

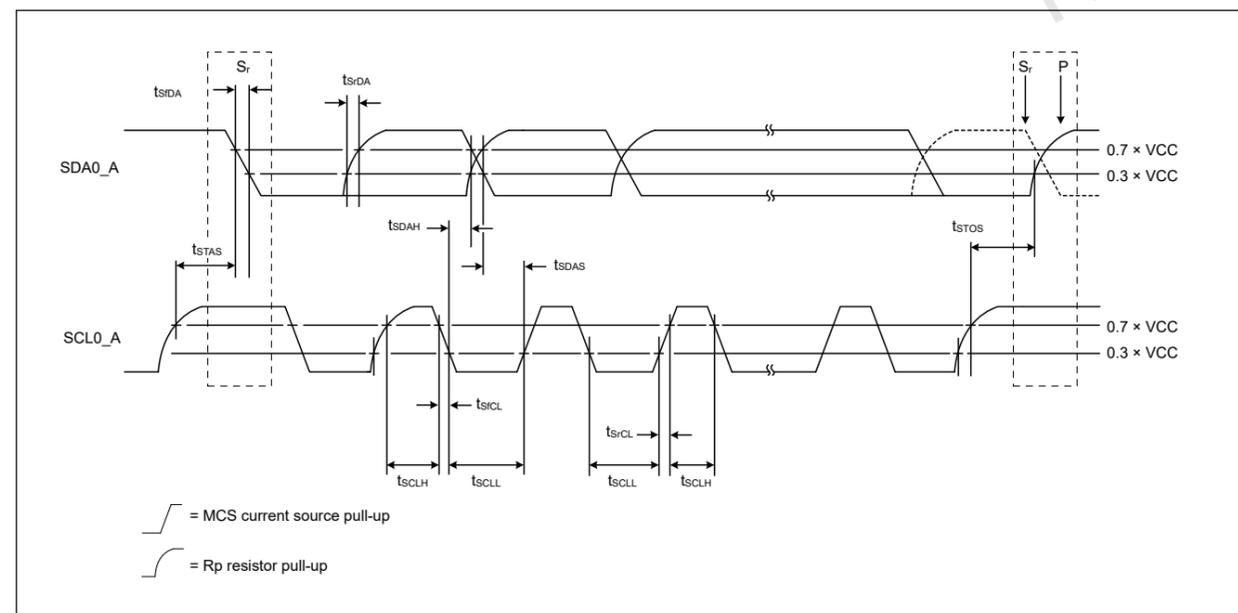


Figure 2.48 I<sup>2</sup>C bus interface input/output timing (Hs-mode)

**Table 2.32 IIC timing (2)**

PmnPFS寄存器中的端口驱动能力位不需要设置SCL0\_A、SDA0\_A引脚。

| Parameter                       | Symbol            | Min                  | Max                              | Unit                      | 测试条件 |             |    |
|---------------------------------|-------------------|----------------------|----------------------------------|---------------------------|------|-------------|----|
| IIC (Hs-mode)<br>BFCTL.HSME = 1 | SCL输入周期时间         | $t_{SCL}$            | $10 (12) \times t_{IICcyc} + 80$ | —                         | ns   | Figure 2.48 |    |
|                                 | SCL输入高脉冲宽度        | $t_{SCLH}$           | $5 (6) \times t_{IICcyc}$        | —                         | ns   |             |    |
|                                 | SCL输入低脉冲宽度        | $t_{SCLL}$           | $5 (6) \times t_{IICcyc}$        | —                         | ns   |             |    |
|                                 | SCL上升时间           | $t_{SrCL}$           | $C_b = 400\text{pF}$             | —                         | 80   |             | ns |
|                                 |                   |                      | $C_b = 100\text{pF}$             | —                         | 40   |             | ns |
|                                 | SDA上升时间           | $t_{SrDA}$           | $C_b = 400\text{pF}$             | —                         | 160  |             | ns |
|                                 |                   |                      | $C_b = 100\text{pF}$             | —                         | 80   |             | ns |
|                                 | SCL下降时间           | $t_{SfCL}$           | $C_b = 400\text{pF}$             | —                         | 80   |             | ns |
|                                 |                   |                      | $C_b = 100\text{pF}$             | —                         | 40   |             | ns |
|                                 | SDA下降时间           | $t_{SfDA}$           | $C_b = 400\text{pF}$             | —                         | 160  |             | ns |
|                                 |                   |                      | $C_b = 100\text{pF}$             | —                         | 80   |             | ns |
|                                 | SCL、SDA输入尖峰脉冲去除时间 | $t_{SP}$             | 0                                | $1 (1) \times t_{IICcyc}$ | ns   |             |    |
|                                 | 重复启动条件输入建立时间      | $t_{STAS}$           | 40                               | —                         | ns   |             |    |
|                                 | STOP条件输入建立时间      | $t_{STOS}$           | 40                               | —                         | ns   |             |    |
| 数据输入建立时间                        | $t_{SDAS}$        | 10                   | —                                | ns                        |      |             |    |
| 数据输入保持时间                        | $t_{SDAH}$        | $C_b = 400\text{pF}$ | 0                                | 150                       | ns   |             |    |
|                                 |                   | $C_b = 100\text{pF}$ | 0                                | 70                        | ns   |             |    |
| SCL, SDA capacitive load        | $C_b^{*1}$        | —                    | 400                              | pF                        |      |             |    |

Note:  $t_{IICcyc}$ : IIC内部参考时钟(IICφ)周期。

Note: 括号中的值适用于INCTL.DNFS[3:0]设置为0011b且数字滤波器启用且INCTL.DNFE设置为1的情况。

Note: 目标是SCL0\_A和SDA0\_A。

注1.  $C_b$ 表示公交线路的总容量。

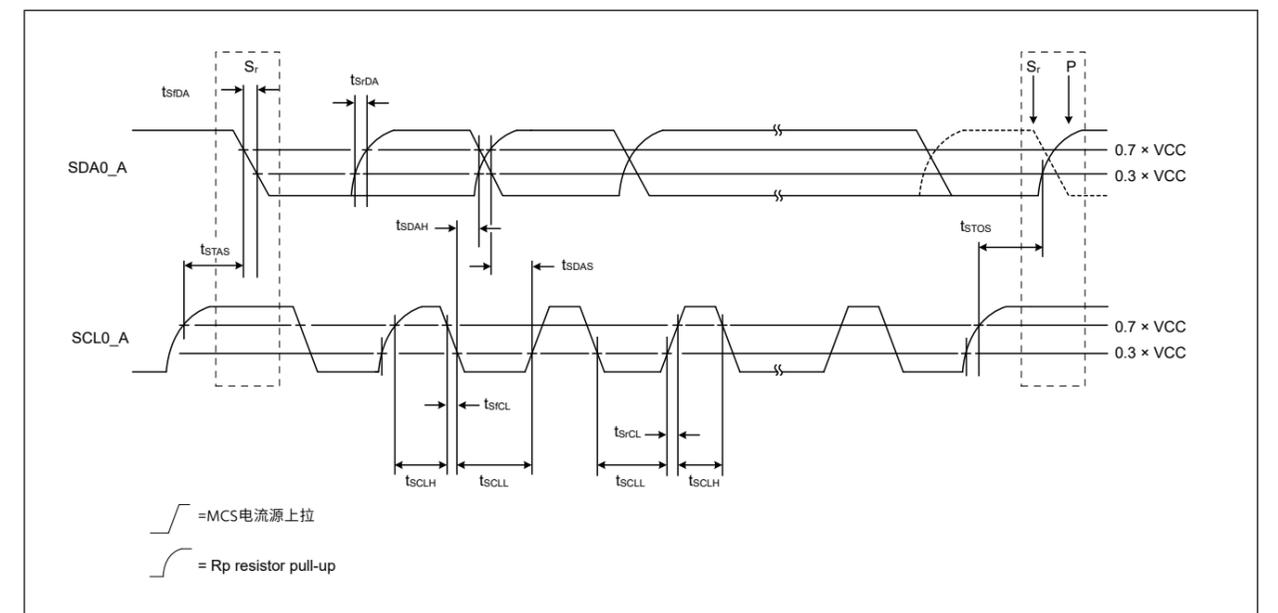


Figure 2.48 I<sup>2</sup>C总线接口输入输出时序 (Hs-mode)

2.3.12 CANFD Timing

Table 2.33 CANFD interface timing

| Parameter           | Symbol     | CAN |     | CAN-FD |     | Unit | Test conditions |
|---------------------|------------|-----|-----|--------|-----|------|-----------------|
|                     |            | Min | Max | Min    | Max |      |                 |
| Internal delay time | $t_{node}$ | —   | 100 | —      | 75  | ns   | Figure 2.49     |
| Transmission rate   |            | —   | 1   | —      | 5   | Mbps |                 |

Note:  $t_{node} = t_{output} + t_{input}$

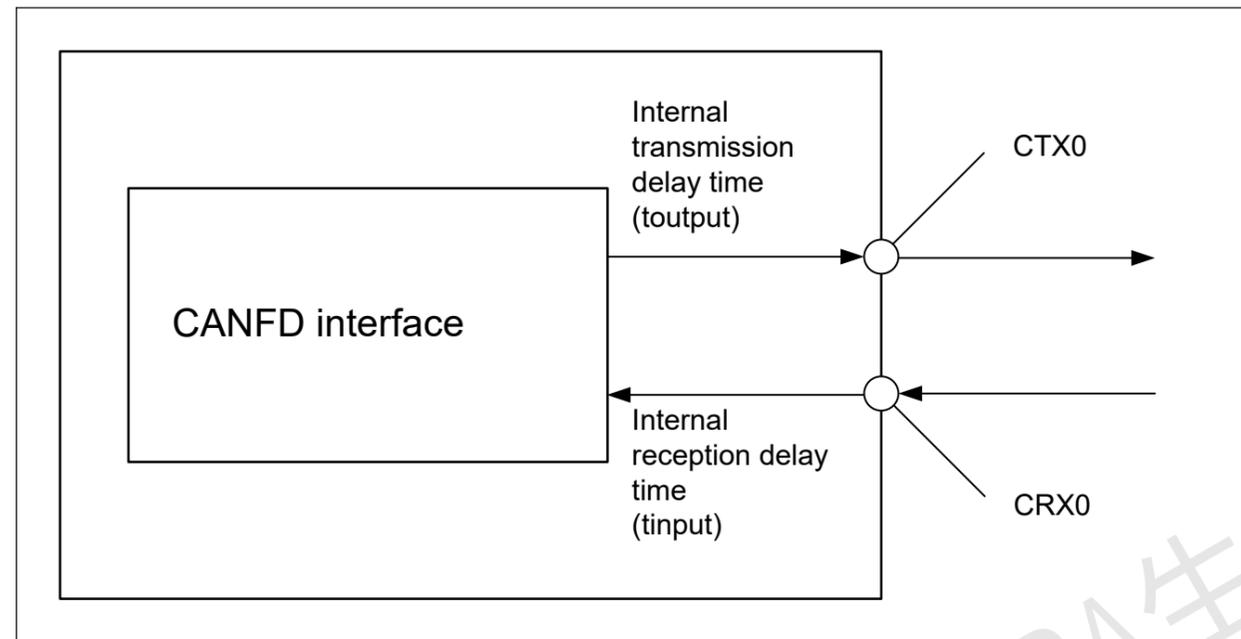


Figure 2.49 CANFD interface condition

2.4 ADC Characteristics

Table 2.34 A/D conversion characteristics (Common) (1 of 2)

| Parameter                                  | Min                    | Typ   | Max                        | Unit | Test conditions |    |  |
|--|------------------------|---|----------------------------|------|-----------------|----|--|
| A/D conversion clock frequency(ADCLK)      | 25                     | 50  | 60                         | MHz  |                 |    |  |
| Quantization error                         | —                      | ±0.5  | —                          | LSB  |                 |    |  |
| Successive approximation time              | 100                    | —   | 140                        | ns   |                 |    |  |
| A/D sampling time                          | During calibration     | 400   | —                          | —    | ns              |    |  |
|  | In self-diagnosis mode |   | $1 \times t_{ADcyc} + 40$  | —    | —               | ns |  |
|  | During A/D conversion  | Channel-dedicated sample-and-hold circuits in use (AN000 to AN005) (AN006 to AN011) | $1 \times t_{ADcyc} + 160$ | —    | —               | ns |  |
|  |                        | High-speed channels (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)              | $1 \times t_{ADcyc} + 40$  | —    | —               | ns |  |
|  |                        | High-precision channels (AN012 to AN017)  | 180                        | —    | —               | ns |  |
| Normal-precision channels (AN020 to AN028) |                        | 400   | —                          | —    | ns              |    |  |

2.3.12 CANFD Timing

Table 2.33 CANFD接口时序

| Parameter | Symbol     | CAN |     | CAN-FD |     | Unit | 测试条件        |
|-----------|------------|-----|-----|--------|-----|------|-------------|
|           |            | Min | Max | Min    | Max |      |             |
| 内部延迟时间    | $t_{node}$ | —   | 100 | —      | 75  | ns   | Figure 2.49 |
| 传输速率      |            | —   | 1   | —      | 5   | Mbps |             |

Note:  $t_{节点} = t_{输出} + t_{输入}$

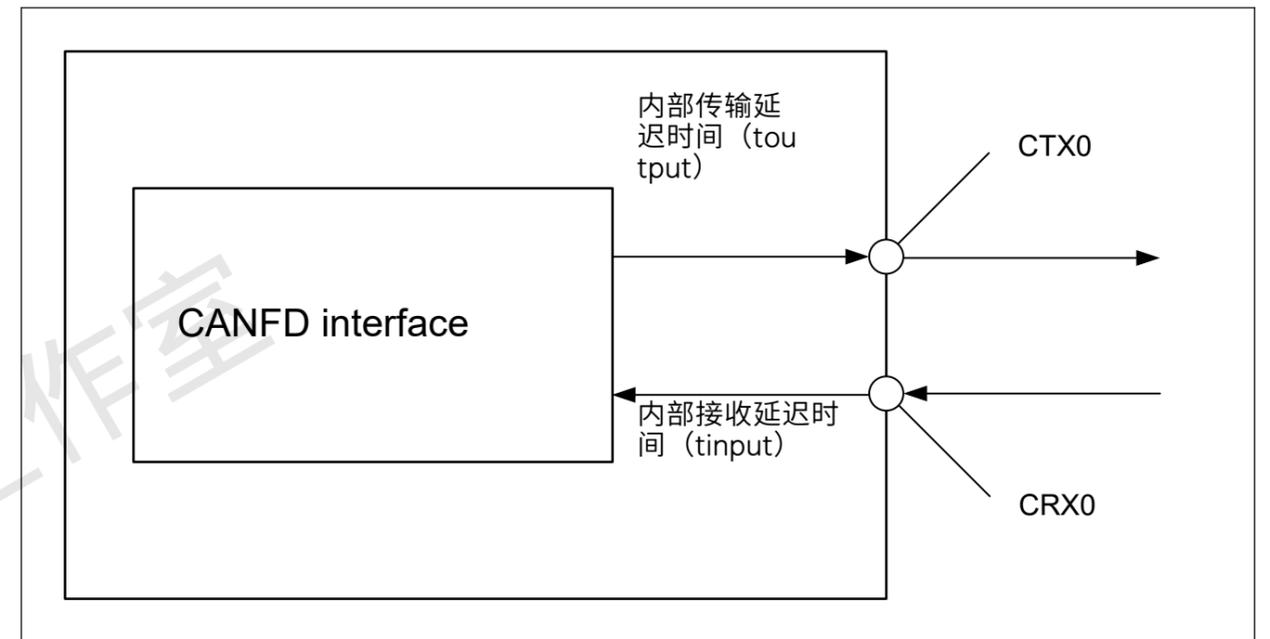


Figure 2.49 CANFD接口情况

2.4 ADC Characteristics

Table 2.34 AD转换特性(Common)(1of2)

| Parameter                                  | Min     | Typ  | Max                        | Unit | 测试条件 |    |  |
|--|---------|--|----------------------------|------|------|----|--|
| AD转换时钟频率(ADCLK)                            | 25      | 50   | 60                         | MHz  |      |    |  |
| 量化误差                                       | —       | ±0.5   | —                          | LSB  |      |    |  |
| 逐次逼近时间                                     | 100     | —  | 140                        | ns   |      |    |  |
| AD采样时间                                     | 校准期间    |  | 400                        | —    | —    | ns |  |
|  | 处于自诊断模式 |  | $1 \times t_{ADcyc} + 40$  | —    | —    | ns |  |
|  | 在AD转换期间 | 使用中的通道专用采样保持电路 (AN000 to AN005) (AN006 to AN011)                       | $1 \times t_{ADcyc} + 160$ | —    | —    | ns |  |
|  |         | High-speed channels (AN000 to AN005) (AN006 to AN011) (AN018 to AN019) | $1 \times t_{ADcyc} + 40$  | —    | —    | ns |  |
|  |         | High-precision channels (AN012 to AN017)                               | 180                        | —    | —    | ns |  |
| Normal-precision channels (AN020 to AN028) |         | 400  | —                          | —    | ns   |    |  |

Table 2.34 A/D conversion characteristics (Common) (2 of 2)

| Parameter                                  | Min  | Typ | Max    | Unit | Test conditions |
|--|--|-----|--------|------|-----------------|
| Channel-dedicated sample-and-hold circuits | Sampling time during calibration                         | 400 | —      | —    | ns              |
|  | Sampling time during A/D conversion                      | 400 | —      | —    | ns              |
|  | Hold mode switching time                                 | 40  | —      | —    | ns              |
|  | Hold time  | —   | —      | 5    | μs              |
| Operation stabilization time               | A/D start-up time  | 2.0 | —      | —    | us              |
|  | Channel-dedicated sample-and-hold circuits start-up time | 2.0 | —      | —    | us              |
|  | A/D shut-down time                                       | 1.0 | —      | —    | us              |
| Analog input voltage range                 | VREFL0   | —   | VREFH0 | V    |                 |

Note:  $t_{ADcyc}$ : ADCLK cycle

Table 2.35 A/D conversion characteristics (1 of 2)

| Parameter   | Min   | Typ  | Max        | Unit       | Test conditions |  |
|---|---|------|------------|------------|-----------------|--|
| Resolution  | —   | —    | 12         | bit        |                 |  |
| Channel-dedicated sample-and-hold circuits in use (AN000 to AN005) (AN006 to AN011) | Conversion time*1 (operation at ADCLK = 50 MHz) | 0.70 | —          | —          | μs              | <ul style="list-style-type: none"> <li>Sampling time of channel-dedicated sample-and-hold circuits: 20 ADCLK</li> <li>Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK</li> <li>Sampling time: 8 ADCLK</li> <li>Successive approximation time: 5 ADCLK</li> </ul> |
|   | Offset error                                    | —    | ±0.5       | ±1.0       | LSB             |  |
|   | Full-scale error                                | —    | ±1.0       | ±1.5       | LSB             |  |
|   | Absolute accuracy                               | —    | ±5.0       | ±7.0       | LSB             |  |
|   | DNL pseudo-differential nonlinearity error      | —    | -1 to +1.5 | -1 to +2.5 | LSB             |  |
|   | INL integral nonlinearity error                 | —    | ±2.0       | ±3.0       | LSB             |  |
| High-speed channels (AN000 to AN005) (AN006 to AN011) (AN018 to AN019)*2            | Conversion time*1 (operation at ADCLK = 50 MHz) | 0.16 | —          | —          | μs              | <ul style="list-style-type: none"> <li>Sampling time: 3 ADCLK</li> <li>Successive approximation time: 5 ADCLK</li> </ul>   |
|   | Offset error                                    | —    | ±1.0       | ±3.0       | LSB             |  |
|   | Full-scale error                                | —    | ±1.5       | ±2.5       | LSB             |  |
|   | Absolute accuracy                               | —    | ±5.5       | ±7.0       | LSB             |  |
|   | DNL pseudo-differential nonlinearity error      | —    | -1 to +1.5 | -1 to +2.5 | LSB             |  |
|   | INL integral nonlinearity error                 | —    | ±2.0       | ±3.0       | LSB             |  |
| High-precision channels (AN012 to AN017)  | Conversion time*1 (operation at ADCLK = 50 MHz) | 0.28 | —          | —          | μs              | <ul style="list-style-type: none"> <li>Sampling time: 9 ADCLK</li> <li>Successive approximation time: 5 ADCLK</li> </ul>   |
|   | Offset error                                    | —    | ±1.0       | ±1.5       | LSB             |  |
|   | Full-scale error                                | —    | ±1.0       | ±2.5       | LSB             |  |
|   | Absolute accuracy                               | —    | ±4.0       | ±7.0       | LSB             |  |
|   | DNL pseudo-differential nonlinearity error      | —    | -1 to +1.5 | -1 to +2.5 | LSB             |  |
|   | INL integral nonlinearity error                 | —    | ±2.0       | ±3.0       | LSB             |  |

Table 2.34 AD转换特性(Common)(2of2)

| Parameter                                  | Min                | Typ | Max    | Unit | 测试条件 |
|--|--------------------|-----|--------|------|------|
| Channel-dedicated sample-and-hold circuits | 校准期间的采样时间          | 400 | —      | —    | ns   |
|  | AD转换期间的采样时间        | 400 | —      | —    | ns   |
|  | 保持模式切换时间           | 40  | —      | —    | ns   |
|  | 保持时间               | —   | —      | 5    | μs   |
| 运行稳定时间                                     | A/D start-up time  | 2.0 | —      | —    | us   |
|  | 通道专用采样保持电路的启动时间    | 2.0 | —      | —    | us   |
|  | A/D shut-down time | 1.0 | —      | —    | us   |
| 模拟输入电压范围                                   | VREFL0             | —   | VREFH0 | V    |      |

Note:  $t_{ADcyc}$ : ADCLK cycle

Table 2.35 AD转换特性(1of2)

| Parameter                                     | Min  | Typ  | Max        | Unit       | 测试条件 |  |
|---|--|------|------------|------------|------|--|
| Resolution                                    | —  | —    | 12         | bit        |      |  |
| 使用中的通道专用采样保持电路 (AN000至AN005) (AN006至AN011)    | 转换时间*1 (operation at ADCLK = 50 MHz)       | 0.70 | —          | —          | μs   | <ul style="list-style-type: none"> <li>通道专用采样保持电路的采样时间: 20ADCLK</li> <li>通道专用采样保持电路的保持模式切换时间: 2ADCLK</li> <li>Sampling time: 8 ADCLK</li> <li>逐次逼近时间: 5 ADCLK</li> </ul> |
|   | 偏移误差                                       | —    | ±0.5       | ±1.0       | LSB  |  |
|   | Full-scale error                           | —    | ±1.0       | ±1.5       | LSB  |  |
|   | 绝对精度                                       | —    | ±5.0       | ±7.0       | LSB  |  |
|   | DNL pseudo-differential nonlinearity error | —    | -1 to +1.5 | -1 to +2.5 | LSB  |  |
|   | INL积分非线性误差                                 | —    | ±2.0       | ±3.0       | LSB  |  |
| 高速通道(AN000至AN005)(AN006至AN011)(AN018至AN019)*2 | 转换时间*1 (operation at ADCLK = 50 MHz)       | 0.16 | —          | —          | μs   | <ul style="list-style-type: none"> <li>Sampling time: 3 ADCLK</li> <li>逐次逼近时间: 5 ADCLK</li> </ul>  |
|   | 偏移误差                                       | —    | ±1.0       | ±3.0       | LSB  |  |
|   | Full-scale error                           | —    | ±1.5       | ±2.5       | LSB  |  |
|   | 绝对精度                                       | —    | ±5.5       | ±7.0       | LSB  |  |
|   | DNL pseudo-differential nonlinearity error | —    | -1 to +1.5 | -1 to +2.5 | LSB  |  |
|   | INL积分非线性误差                                 | —    | ±2.0       | ±3.0       | LSB  |  |
| 高精度通道 (AN012至AN017)                           | 转换时间*1 (operation at ADCLK = 50 MHz)       | 0.28 | —          | —          | μs   | <ul style="list-style-type: none"> <li>Sampling time: 9 ADCLK</li> <li>逐次逼近时间: 5 ADCLK</li> </ul>  |
|   | 偏移误差                                       | —    | ±1.0       | ±1.5       | LSB  |  |
|   | Full-scale error                           | —    | ±1.0       | ±2.5       | LSB  |  |
|   | 绝对精度                                       | —    | ±4.0       | ±7.0       | LSB  |  |
|   | DNL pseudo-differential nonlinearity error | —    | -1 to +1.5 | -1 to +2.5 | LSB  |  |
|   | INL积分非线性误差                                 | —    | ±2.0       | ±3.0       | LSB  |  |

Table 2.35 A/D conversion characteristics (2 of 2)

| Parameter                                  |   |  | Min  | Typ        | Max        | Unit | Test conditions   |
|--|---|--|------|------------|------------|------|---|
| Normal-precision channels (AN020 to AN028) | Conversion time*1 (operation at ADCLK = 50 MHz) | Permissible signal source impedance Max. = 50Ω | 0.50 | —          | —          | μs   | <ul style="list-style-type: none"> <li>Sampling time: 20 ADCLK</li> <li>Successive approximation time: 5 ADCLK</li> </ul> |
|  | Offset error                                    |  | —    | ±1.0       | ±2.5       | LSB  |   |
|  | Full-scale error                                |  | —    | ±1.5       | ±2.5       | LSB  |   |
|  | Absolute accuracy                               |  | —    | ±5.5       | ±8.0       | LSB  |   |
|  | DNL pseudo-differential nonlinearity error      |  | —    | -1 to +1.5 | -1 to +2.5 | LSB  |   |
|  | INL integral nonlinearity error                 |  | —    | ±2.0       | ±4.0       | LSB  |   |

Note 1. Channel-dedicated sample-and-hold circuits in use; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Channel-dedicated sample-and-hold circuits not in use; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 2. These channels cannot be used with Channel-dedicated sample-and-hold circuits.

Table 2.36 A/D internal reference voltage characteristics

| Parameter                      | Min  | Typ  | Max  | Unit | Test conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V    |                 |
| Sampling time                  | 4.15 | —    | —    | μs   |                 |

Table 2.37 A/D with D/A conversion characteristics

| Parameter     | Min | Typ | Max | Unit | Test conditions |
|---------------|-----|-----|-----|------|-----------------|
| Sampling time | 1   | —   | —   | μs   |                 |

## 2.5 DAC12 Characteristics

Table 2.38 D/A conversion characteristics

| Parameter                | Min | Typ  | Max         | Unit | Test conditions                            |
|--------------------------|-----|------|-------------|------|--|
| Resolution               | —   | —    | 12          | Bits | —  |
| Without output amplifier |     |      |             |      |  |
| Absolute accuracy        | —   | —    | ±24         | LSB  | Resistive load 2 MΩ                        |
| INL                      | —   | ±2.0 | ±8.0        | LSB  | Resistive load 2 MΩ                        |
| DNL                      | —   | ±1.0 | ±2.0        | LSB  | —  |
| Output impedance         | —   | 8.5  | —           | kΩ   | —  |
| Conversion time          | —   | —    | 3           | μs   | Resistive load 2 MΩ, Capacitive load 20 pF |
| Output voltage range     | 0   | —    | AVCC0       | V    | —  |
| With output amplifier    |     |      |             |      |  |
| INL                      | —   | ±2.0 | ±4.0        | LSB  | —  |
| DNL                      | —   | ±1.0 | ±2.0        | LSB  | —  |
| Conversion time          | —   | —    | 4.0         | μs   | —  |
| Resistive load           | 5   | —    | —           | kΩ   | —  |
| Capacitive load          | —   | —    | 50          | pF   | —  |
| Output voltage range     | 0.2 | —    | AVCC0 - 0.2 | V    | —  |

Table 2.35 AD转换特性(2of2)

| Parameter             |  |                   | Min  | Typ        | Max        | Unit | 测试条件   |
|-----------------------|--|-------------------|------|------------|------------|------|--|
| 普通精度通道 (A NO20至AN028) | 转换时间*1 (operation at ADCLK = 50 MHz)       | 允许的信号源阻抗 Max.=50Ω | 0.50 | —          | —          | μs   | <ul style="list-style-type: none"> <li>Sampling time: 20 ADCLK</li> <li>逐次逼近时间: 5 ADCLK</li> </ul> |
|                       | 偏移误差                                       |                   | —    | ±1.0       | ±2.5       | LSB  |  |
|                       | Full-scale error                           |                   | —    | ±1.5       | ±2.5       | LSB  |  |
|                       | 绝对精度                                       |                   | —    | ±5.5       | ±8.0       | LSB  |  |
|                       | DNL pseudo-differential nonlinearity error |                   | —    | -1 to +1.5 | -1 to +2.5 | LSB  |  |
|                       | INL积分非线性误差                                 |                   | —    | ±2.0       | ±4.0       | LSB  |  |

注1.使用中的通道专用采样保持电路; 转换时间是通道专用采样保持电路的采样时间、保持模式切换时间、采样时间和逐次逼近时间之和。上述每种状态均针对测试条件进行指示。未使用通道专用的采样保持电路; 转换时间是采样时间和逐次逼近时间之和。上述每种状态均针对测试条件进行指示。

注2.这些通道不能与通道专用的采样保持电路一起使用。

Table 2.36 AD内部参考电压特性

| Parameter | Min  | Typ  | Max  | Unit | 测试条件 |
|-----------|------|------|------|------|------|
| AD内部参考电压  | 1.13 | 1.18 | 1.23 | V    |      |
| 采样时间      | 4.15 | —    | —    | μs   |      |

Table 2.37 AD具有DA转换特性

| Parameter | Min | Typ | Max | Unit | 测试条件 |
|-----------|-----|-----|-----|------|------|
| 采样时间      | 1   | —   | —   | μs   |      |

## 2.5 DAC12 Characteristics

Table 2.38 DA转换特性

| Parameter       | Min | Typ  | Max         | Unit | 测试条件              |
|-----------------|-----|------|-------------|------|-------------------|
| Resolution      | —   | —    | 12          | Bits | —                 |
| 无输出放大器          |     |      |             |      |                   |
| 绝对精度            | —   | —    | ±24         | LSB  | 阻性负载2MΩ           |
| INL             | —   | ±2.0 | ±8.0        | LSB  | 阻性负载2MΩ           |
| DNL             | —   | ±1.0 | ±2.0        | LSB  | —                 |
| 输出阻抗            | —   | 8.5  | —           | kΩ   | —                 |
| 转换时间            | —   | —    | 3           | μs   | 电阻负载2MΩ, 电容负载20pF |
| 输出电压范围          | 0   | —    | AVCC0       | V    | —                 |
| 带输出放大器          |     |      |             |      |                   |
| INL             | —   | ±2.0 | ±4.0        | LSB  | —                 |
| DNL             | —   | ±1.0 | ±2.0        | LSB  | —                 |
| 转换时间            | —   | —    | 4.0         | μs   | —                 |
| 阻性负载            | 5   | —    | —           | kΩ   | —                 |
| Capacitive load | —   | —    | 50          | pF   | —                 |
| 输出电压范围          | 0.2 | —    | AVCC0 - 0.2 | V    | —                 |

## 2.6 TSN Characteristics

Table 2.39 TSN characteristics

| Parameter                     | Symbol             | Min  | Typ   | Max | Unit  | Test conditions |
|-------------------------------|--------------------|------|-------|-----|-------|-----------------|
| Relative accuracy             | —                  | —    | ± 1.0 | —   | °C    | —               |
| Temperature slope             | —                  | —    | 4.0   | —   | mV/°C | —               |
| Output voltage (at 25 °C)     | —                  | —    | 1.24  | —   | V     | —               |
| Temperature sensor start time | t <sub>START</sub> | —    | —     | 30  | μs    | —               |
| Sampling time                 | —                  | 4.15 | —     | —   | μs    | —               |

## 2.7 ACMPHS Characteristics

Table 2.40 ACMPHS characteristics

| Parameter   | Symbol              | Min | Typ | Max   | Unit | Test conditions                 |
|---|---------------------|-----|-----|-------|------|---------------------------------|
| Input offset voltage  | V <sub>IO</sub>     | —   | —   | 40    | mV   |                                 |
| Reference voltage range   | V <sub>REF</sub>    | 0   | —   | AVCC0 | V    |                                 |
| Input voltage range   | V <sub>I</sub>      | 0   | —   | AVCC0 | V    |                                 |
| Output delay  | t <sub>tot(r)</sub> | —   | —   | 200   | ns   | VOD = 100 mV<br>CMPCTL.CDFS = 0 |
|   | t <sub>tot(f)</sub> | —   | —   | 200   | ns   |                                 |
| Waiting time for stabilization following switching of the input | t <sub>wait</sub>   | 300 | —   | —     | ns   |                                 |
| Operation stabilization time                                    | t <sub>cmp</sub>    | —   | —   | 1     | us   |                                 |

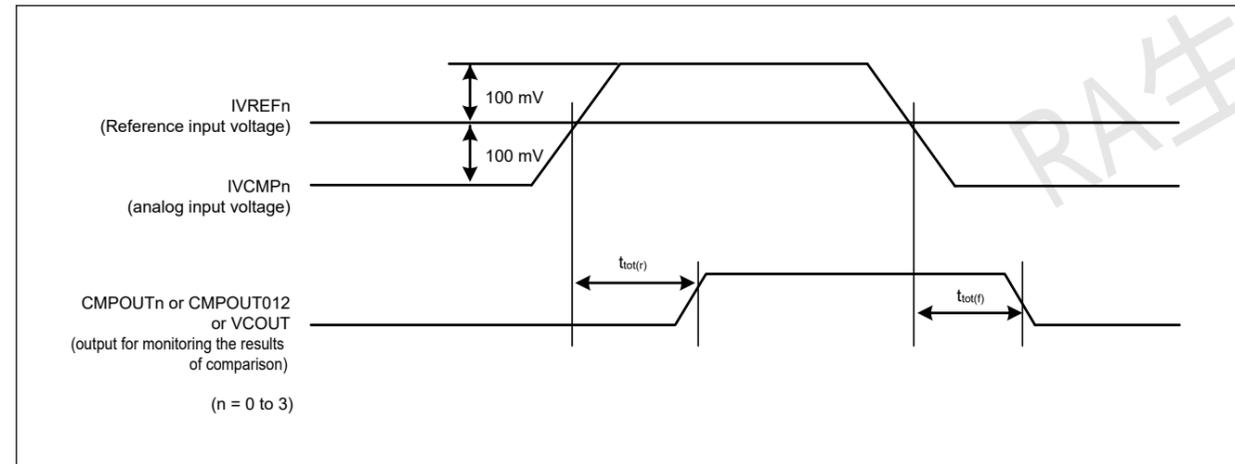


Figure 2.50 Comparator Response Time

## 2.8 PGA Characteristics

Table 2.41 PGA characteristics in single mode (1 of 3)

| Parameter    | Symbol           | Min | Typ | Max | Unit | Test conditions |
|--------------|------------------|-----|-----|-----|------|-----------------|
| Offset error | V <sub>off</sub> | -8  | —   | 8   | mV   |                 |

## 2.6 TSN Characteristics

Table 2.39 TSN characteristics

| Parameter    | Symbol             | Min  | Typ   | Max | Unit  | 测试条件 |
|--------------|--------------------|------|-------|-----|-------|------|
| 相对精度         | —                  | —    | ± 1.0 | —   | °C    | —    |
| 温度斜率         | —                  | —    | 4.0   | —   | mV/°C | —    |
| 输出电压 (25°C时) | —                  | —    | 1.24  | —   | V     | —    |
| 温度传感器启动时间    | t <sub>START</sub> | —    | —     | 30  | μs    | —    |
| 采样时间         | —                  | 4.15 | —     | —   | μs    | —    |

## 2.7 ACMPHS Characteristics

Table 2.40 ACMPHS characteristics

| Parameter    | Symbol              | Min | Typ | Max   | Unit | 测试条件                            |
|--------------|---------------------|-----|-----|-------|------|---------------------------------|
| 输入失调电压       | V <sub>IO</sub>     | —   | —   | 40    | mV   |                                 |
| 参考电压范围       | V <sub>REF</sub>    | 0   | —   | AVCC0 | V    |                                 |
| 输入电压范围       | V <sub>I</sub>      | 0   | —   | AVCC0 | V    |                                 |
| 输出延迟         | t <sub>tot(r)</sub> | —   | —   | 200   | ns   | VOD = 100 mV<br>CMPCTL.CDFS = 0 |
|              | t <sub>tot(f)</sub> | —   | —   | 200   | ns   |                                 |
| 输入切换后的稳定等待时间 | t <sub>wait</sub>   | 300 | —   | —     | ns   |                                 |
| 运行稳定时间       | t <sub>cmp</sub>    | —   | —   | 1     | us   |                                 |

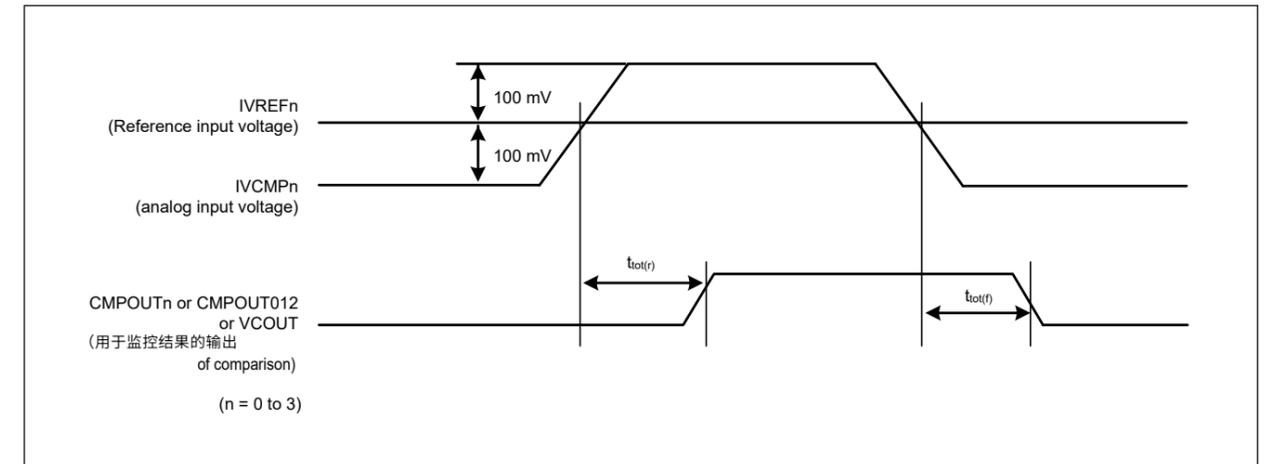


Figure 2.50 比较器响应时间

## 2.8 PGA特性

Table 2.41 单模PGA特性 (3个中的1个)

| Parameter | Symbol           | Min | Typ | Max | Unit | 测试条件 |
|-----------|------------------|-----|-----|-----|------|------|
| 偏移误差      | V <sub>off</sub> | -8  | —   | 8   | mV   |      |

Table 2.41 PGA characteristics in single mode (2 of 3)

| Parameter                          | Symbol                | Min                  | Typ                 | Max                  | Unit | Test conditions |
|------------------------------------|-----------------------|----------------------|---------------------|----------------------|------|-----------------|
| PGAVSS input voltage range         | PGAVSS                | 0                    | —                   | 0                    | V    |                 |
|                                    | AIN0 (G = 2.000)      | $0.05 \times AVCC0$  | —                   | $0.45 \times AVCC0$  | V    |                 |
|                                    | AIN1 (G = 2.500)      | $0.047 \times AVCC0$ | —                   | $0.36 \times AVCC0$  | V    |                 |
|                                    | AIN2 (G = 2.667)      | $0.046 \times AVCC0$ | —                   | $0.337 \times AVCC0$ | V    |                 |
|                                    | AIN3 (G = 2.857)      | $0.046 \times AVCC0$ | —                   | $0.32 \times AVCC0$  | V    |                 |
|                                    | AIN4 (G = 3.077)      | $0.045 \times AVCC0$ | —                   | $0.292 \times AVCC0$ | V    |                 |
|                                    | AIN5 (G = 3.333)      | $0.044 \times AVCC0$ | —                   | $0.265 \times AVCC0$ | V    |                 |
|                                    | AIN6 (G = 3.636)      | $0.042 \times AVCC0$ | —                   | $0.247 \times AVCC0$ | V    |                 |
|                                    | AIN7 (G = 4.000)      | $0.04 \times AVCC0$  | —                   | $0.212 \times AVCC0$ | V    |                 |
|                                    | AIN8 (G = 4.444)      | $0.036 \times AVCC0$ | —                   | $0.191 \times AVCC0$ | V    |                 |
|                                    | AIN9 (G = 5.000)      | $0.033 \times AVCC0$ | —                   | $0.17 \times AVCC0$  | V    |                 |
|                                    | AIN10 (G = 5.714)     | $0.031 \times AVCC0$ | —                   | $0.148 \times AVCC0$ | V    |                 |
|                                    | AIN11 (G = 6.667)     | $0.029 \times AVCC0$ | —                   | $0.127 \times AVCC0$ | V    |                 |
|                                    | AIN12 (G = 8.000)     | $0.027 \times AVCC0$ | —                   | $0.09 \times AVCC0$  | V    |                 |
|                                    | AIN13 (G = 10.000)    | $0.025 \times AVCC0$ | —                   | $0.08 \times AVCC0$  | V    |                 |
| AIN14 (G = 13.333)                 | $0.023 \times AVCC0$  | —                    | $0.06 \times AVCC0$ | V                    |      |                 |
| Output voltage range <sup>*1</sup> | PGAOUT0 (G = 2.000)   | $0.100 \times AVCC0$ | —                   | $0.900 \times AVCC0$ | V    |                 |
|                                    | PGAOUT1 (G = 2.500)   | $0.118 \times AVCC0$ | —                   | $0.900 \times AVCC0$ | V    |                 |
|                                    | PGAOUT2 (G = 2.667)   | $0.123 \times AVCC0$ | —                   | $0.899 \times AVCC0$ | V    |                 |
|                                    | PGAOUT3 (G = 2.857)   | $0.131 \times AVCC0$ | —                   | $0.914 \times AVCC0$ | V    |                 |
|                                    | PGAOUT4 (G = 3.077)   | $0.138 \times AVCC0$ | —                   | $0.898 \times AVCC0$ | V    |                 |
|                                    | PGAOUT5 (G = 3.333)   | $0.147 \times AVCC0$ | —                   | $0.883 \times AVCC0$ | V    |                 |
|                                    | PGAOUT6 (G = 3.636)   | $0.153 \times AVCC0$ | —                   | $0.898 \times AVCC0$ | V    |                 |
|                                    | PGAOUT7 (G = 4.000)   | $0.160 \times AVCC0$ | —                   | $0.848 \times AVCC0$ | V    |                 |
|                                    | PGAOUT8 (G = 4.444)   | $0.160 \times AVCC0$ | —                   | $0.849 \times AVCC0$ | V    |                 |
|                                    | PGAOUT9 (G = 5.000)   | $0.165 \times AVCC0$ | —                   | $0.850 \times AVCC0$ | V    |                 |
|                                    | PGAOUT10 (G = 5.714)  | $0.177 \times AVCC0$ | —                   | $0.846 \times AVCC0$ | V    |                 |
|                                    | PGAOUT11 (G = 6.667)  | $0.193 \times AVCC0$ | —                   | $0.847 \times AVCC0$ | V    |                 |
|                                    | PGAOUT12 (G = 8.000)  | $0.216 \times AVCC0$ | —                   | $0.720 \times AVCC0$ | V    |                 |
|                                    | PGAOUT13 (G = 10.000) | $0.250 \times AVCC0$ | —                   | $0.800 \times AVCC0$ | V    |                 |
|                                    | PGAOUT14 (G = 13.333) | $0.307 \times AVCC0$ | —                   | $0.800 \times AVCC0$ | V    |                 |

Table 2.41 单模PGA特性(2of3)

| Parameter            | Symbol                | Min                  | Typ                 | Max                  | Unit | 测试条件 |
|----------------------|-----------------------|----------------------|---------------------|----------------------|------|------|
| PGAVSS输入电压范围         | PGAVSS                | 0                    | —                   | 0                    | V    |      |
|                      | AIN0 (G = 2.000)      | $0.05 \times AVCC0$  | —                   | $0.45 \times AVCC0$  | V    |      |
|                      | AIN1 (G = 2.500)      | $0.047 \times AVCC0$ | —                   | $0.36 \times AVCC0$  | V    |      |
|                      | AIN2 (G = 2.667)      | $0.046 \times AVCC0$ | —                   | $0.337 \times AVCC0$ | V    |      |
|                      | AIN3 (G = 2.857)      | $0.046 \times AVCC0$ | —                   | $0.32 \times AVCC0$  | V    |      |
|                      | AIN4 (G = 3.077)      | $0.045 \times AVCC0$ | —                   | $0.292 \times AVCC0$ | V    |      |
|                      | AIN5 (G = 3.333)      | $0.044 \times AVCC0$ | —                   | $0.265 \times AVCC0$ | V    |      |
|                      | AIN6 (G = 3.636)      | $0.042 \times AVCC0$ | —                   | $0.247 \times AVCC0$ | V    |      |
|                      | AIN7 (G = 4.000)      | $0.04 \times AVCC0$  | —                   | $0.212 \times AVCC0$ | V    |      |
|                      | AIN8 (G = 4.444)      | $0.036 \times AVCC0$ | —                   | $0.191 \times AVCC0$ | V    |      |
|                      | AIN9 (G = 5.000)      | $0.033 \times AVCC0$ | —                   | $0.17 \times AVCC0$  | V    |      |
|                      | AIN10 (G = 5.714)     | $0.031 \times AVCC0$ | —                   | $0.148 \times AVCC0$ | V    |      |
|                      | AIN11 (G = 6.667)     | $0.029 \times AVCC0$ | —                   | $0.127 \times AVCC0$ | V    |      |
|                      | AIN12 (G = 8.000)     | $0.027 \times AVCC0$ | —                   | $0.09 \times AVCC0$  | V    |      |
|                      | AIN13 (G = 10.000)    | $0.025 \times AVCC0$ | —                   | $0.08 \times AVCC0$  | V    |      |
| AIN14 (G = 13.333)   | $0.023 \times AVCC0$  | —                    | $0.06 \times AVCC0$ | V                    |      |      |
| 输出电压范围 <sup>*1</sup> | PGAOUT0 (G = 2.000)   | $0.100 \times AVCC0$ | —                   | $0.900 \times AVCC0$ | V    |      |
|                      | PGAOUT1 (G = 2.500)   | $0.118 \times AVCC0$ | —                   | $0.900 \times AVCC0$ | V    |      |
|                      | PGAOUT2 (G = 2.667)   | $0.123 \times AVCC0$ | —                   | $0.899 \times AVCC0$ | V    |      |
|                      | PGAOUT3 (G = 2.857)   | $0.131 \times AVCC0$ | —                   | $0.914 \times AVCC0$ | V    |      |
|                      | PGAOUT4 (G = 3.077)   | $0.138 \times AVCC0$ | —                   | $0.898 \times AVCC0$ | V    |      |
|                      | PGAOUT5 (G = 3.333)   | $0.147 \times AVCC0$ | —                   | $0.883 \times AVCC0$ | V    |      |
|                      | PGAOUT6 (G = 3.636)   | $0.153 \times AVCC0$ | —                   | $0.898 \times AVCC0$ | V    |      |
|                      | PGAOUT7 (G = 4.000)   | $0.160 \times AVCC0$ | —                   | $0.848 \times AVCC0$ | V    |      |
|                      | PGAOUT8 (G = 4.444)   | $0.160 \times AVCC0$ | —                   | $0.849 \times AVCC0$ | V    |      |
|                      | PGAOUT9 (G = 5.000)   | $0.165 \times AVCC0$ | —                   | $0.850 \times AVCC0$ | V    |      |
|                      | PGAOUT10 (G = 5.714)  | $0.177 \times AVCC0$ | —                   | $0.846 \times AVCC0$ | V    |      |
|                      | PGAOUT11 (G = 6.667)  | $0.193 \times AVCC0$ | —                   | $0.847 \times AVCC0$ | V    |      |
|                      | PGAOUT12 (G = 8.000)  | $0.216 \times AVCC0$ | —                   | $0.720 \times AVCC0$ | V    |      |
|                      | PGAOUT13 (G = 10.000) | $0.250 \times AVCC0$ | —                   | $0.800 \times AVCC0$ | V    |      |
|                      | PGAOUT14 (G = 13.333) | $0.307 \times AVCC0$ | —                   | $0.800 \times AVCC0$ | V    |      |

Table 2.41 PGA characteristics in single mode (3 of 3)

| Parameter                    | Symbol              | Min  | Typ | Max | Unit | Test conditions |
|------------------------------|---------------------|------|-----|-----|------|-----------------|
| Gain error                   | Gerr0 (G = 2.000)   | -1.0 | —   | 1.0 | %    |                 |
|                              | Gerr1 (G = 2.500)   | -1.0 | —   | 1.0 | %    |                 |
|                              | Gerr2 (G = 2.667)   | -1.0 | —   | 1.0 | %    |                 |
|                              | Gerr3 (G = 2.857)   | -1.0 | —   | 1.0 | %    |                 |
|                              | Gerr4 (G = 3.007)   | -1.0 | —   | 1.0 | %    |                 |
|                              | Gerr5 (G = 3.333)   | -1.5 | —   | 1.5 | %    |                 |
|                              | Gerr6 (G = 3.636)   | -1.5 | —   | 1.5 | %    |                 |
|                              | Gerr7 (G = 4.000)   | -1.5 | —   | 1.5 | %    |                 |
|                              | Gerr8 (G = 4.444)   | -2.0 | —   | 2.0 | %    |                 |
|                              | Gerr9 (G = 5.000)   | -2.0 | —   | 2.0 | %    |                 |
|                              | Gerr10 (G = 5.714)  | -2.0 | —   | 2.0 | %    |                 |
|                              | Gerr11 (G = 6.667)  | -2.0 | —   | 2.0 | %    |                 |
|                              | Gerr12 (G = 8.000)  | -2.0 | —   | 2.0 | %    |                 |
|                              | Gerr13 (G = 10.000) | -2.0 | —   | 2.0 | %    |                 |
| Gerr14 (G = 13.333)          | -2.0                | —    | 2.0 | %   |      |                 |
| Operation stabilization time | t <sub>start</sub>  | —    | —   | 5   | μs   |                 |

Note 1. Calculate with the following formula. (n = 0 to 14)

$$PGAOUT_n = AIN_n \times G$$

Actual output range includes gain error.

$$PGAOUT_n = (AIN_n \times G) \times (Gerr + 100\%)$$

Table 2.42 PGA characteristics in differential mode

| Parameter                        | Symbol             | Min   | Typ | Max   | Unit | Test conditions |
|----------------------------------|--------------------|-------|-----|-------|------|-----------------|
| Offset error                     | V <sub>off</sub>   | -20   | —   | 20    | mV   |                 |
| PGAVSS input voltage range       | PGAVSS             | -0.5  | —   | 0.3   | V    |                 |
| Differential input voltage range | G = 1.500          | -0.5  | —   | 0.5   | V    |                 |
|                                  | G = 2.333          | -0.4  | —   | 0.4   | V    |                 |
|                                  | G = 4.000          | -0.2  | —   | 0.2   | V    |                 |
|                                  | G = 5.667          | -0.15 | —   | 0.15  | V    |                 |
| Output voltage range*1           | G = 1.500          | 0.600 | —   | 2.550 | V    |                 |
|                                  | G = 2.333          | 0.417 | —   | 2.733 | V    |                 |
|                                  | G = 4.000          | 0.550 | —   | 2.600 | V    |                 |
|                                  | G = 5.667          | 0.500 | —   | 2.650 | V    |                 |
| Gain error                       | G = 1.500          | -1.0  | —   | 1.0   | %    |                 |
|                                  | G = 2.333          | -1.0  | —   | 1.0   | %    |                 |
|                                  | G = 4.000          | -1.0  | —   | 1.0   | %    |                 |
|                                  | G = 5.667          | -1.0  | —   | 1.0   | %    |                 |
| Operation stabilization time     | t <sub>start</sub> | —     | —   | 5     | μs   |                 |

Note 1. Calculate with the following formula.

$$V_{OR} = (AIN - PGAVSS) \times G + (0.5 \times AVCC0)$$

Actual output range includes gain error.

$$V_{OR} = (AIN - PGAVSS) \times G \times (Gerr + 100\%) + (0.5 \times AVCC0)$$

Table 2.41 单模PGA特性 (3个中的3个)

| Parameter           | Symbol              | Min  | Typ | Max | Unit | 测试条件 |
|---------------------|---------------------|------|-----|-----|------|------|
| 增益误差                | Gerr0 (G = 2.000)   | -1.0 | —   | 1.0 | %    |      |
|                     | Gerr1 (G = 2.500)   | -1.0 | —   | 1.0 | %    |      |
|                     | Gerr2 (G = 2.667)   | -1.0 | —   | 1.0 | %    |      |
|                     | Gerr3 (G = 2.857)   | -1.0 | —   | 1.0 | %    |      |
|                     | Gerr4 (G = 3.007)   | -1.0 | —   | 1.0 | %    |      |
|                     | Gerr5 (G = 3.333)   | -1.5 | —   | 1.5 | %    |      |
|                     | Gerr6 (G = 3.636)   | -1.5 | —   | 1.5 | %    |      |
|                     | Gerr7 (G = 4.000)   | -1.5 | —   | 1.5 | %    |      |
|                     | Gerr8 (G = 4.444)   | -2.0 | —   | 2.0 | %    |      |
|                     | Gerr9 (G = 5.000)   | -2.0 | —   | 2.0 | %    |      |
|                     | Gerr10 (G = 5.714)  | -2.0 | —   | 2.0 | %    |      |
|                     | Gerr11 (G = 6.667)  | -2.0 | —   | 2.0 | %    |      |
|                     | Gerr12 (G = 8.000)  | -2.0 | —   | 2.0 | %    |      |
|                     | Gerr13 (G = 10.000) | -2.0 | —   | 2.0 | %    |      |
| Gerr14 (G = 13.333) | -2.0                | —    | 2.0 | %   |      |      |
| 运行稳定时间              | t <sub>start</sub>  | —    | —   | 5   | μs   |      |

注1.用下列公式计算。(n=0到14)

$$PGAOUT_n = AIN_n \times G$$

实际输出范围包括增益误差。

$$PGAOUT_n = (AIN_n \times G) \times (Gerr + 100\%)$$

Table 2.42 差模下的PGA特性

| Parameter    | Symbol             | Min   | Typ | Max   | Unit | 测试条件 |
|--------------|--------------------|-------|-----|-------|------|------|
| 偏移误差         | V <sub>off</sub>   | -20   | —   | 20    | mV   |      |
| PGAVSS输入电压范围 | PGAVSS             | -0.5  | —   | 0.3   | V    |      |
| 差分输入电压范围     | G = 1.500          | -0.5  | —   | 0.5   | V    |      |
|              | G = 2.333          | -0.4  | —   | 0.4   | V    |      |
|              | G = 4.000          | -0.2  | —   | 0.2   | V    |      |
|              | G = 5.667          | -0.15 | —   | 0.15  | V    |      |
| 输出电压范围*1     | G = 1.500          | 0.600 | —   | 2.550 | V    |      |
|              | G = 2.333          | 0.417 | —   | 2.733 | V    |      |
|              | G = 4.000          | 0.550 | —   | 2.600 | V    |      |
|              | G = 5.667          | 0.500 | —   | 2.650 | V    |      |
| 增益误差         | G = 1.500          | -1.0  | —   | 1.0   | %    |      |
|              | G = 2.333          | -1.0  | —   | 1.0   | %    |      |
|              | G = 4.000          | -1.0  | —   | 1.0   | %    |      |
|              | G = 5.667          | -1.0  | —   | 1.0   | %    |      |
| 运行稳定时间       | t <sub>start</sub> | —     | —   | 5     | μs   |      |

注1.用下列公式计算。

$$V_{OR} = (AIN - PGAVSS) \times G + (0.5 \times AVCC0)$$

实际输出范围包括增益误差。

$$V_{OR} = (AIN - PGAVSS) \times G \times (Gerr + 100\%) + (0.5 \times AVCC0)$$

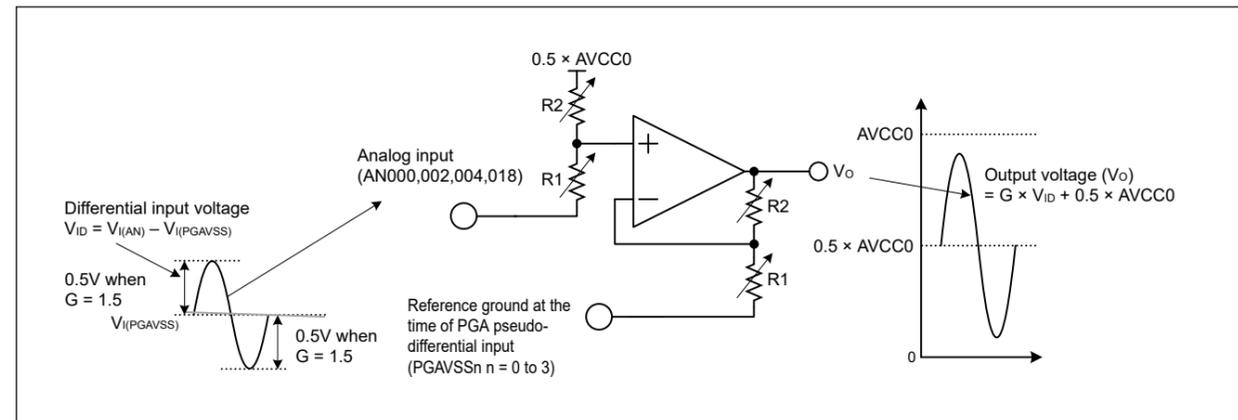


Figure 2.51 Input and Output Signal Levels with the PGA's Pseudo-Differential Setting

2.9 OSC Stop Detect Characteristics

Table 2.43 Oscillation stop detection circuit characteristics

| Parameter      | Symbol   | Min | Typ | Max | Unit | Test conditions |
|----------------|----------|-----|-----|-----|------|-----------------|
| Detection time | $t_{dr}$ | —   | —   | 1   | ms   | Figure 2.52     |

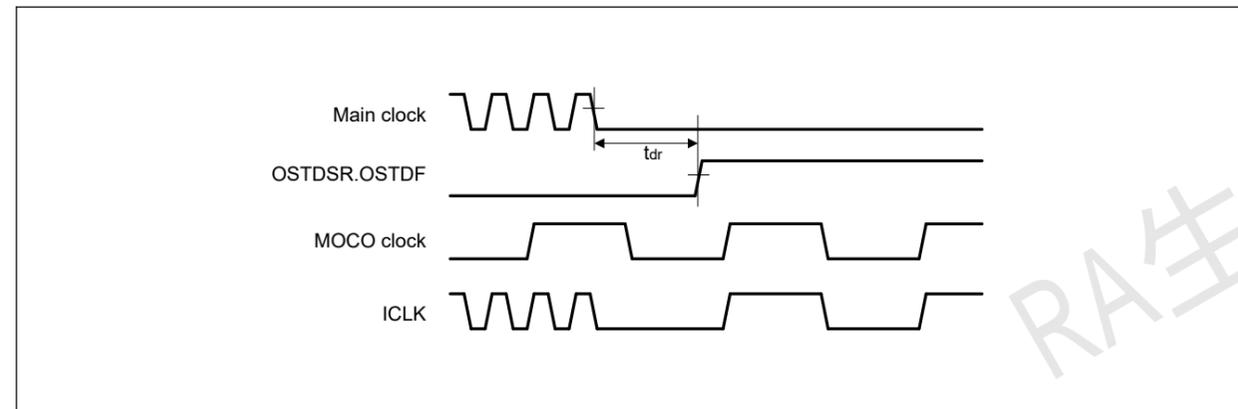


Figure 2.52 Oscillation stop detection timing

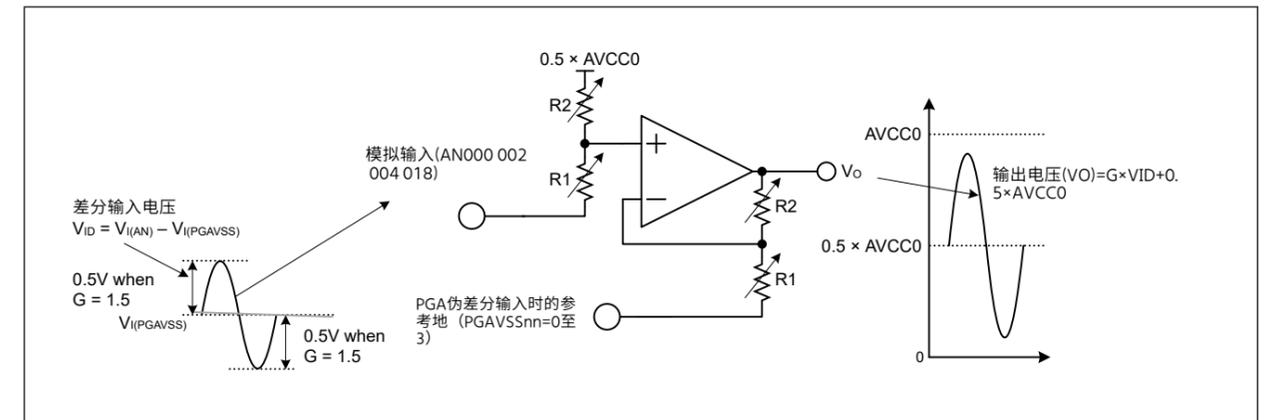


Figure 2.51 具有PGA伪差分设置的输入和输出信号电平

2.9 OSC停止检测特性

Table 2.43 振荡停止检测电路特性

| Parameter | Symbol   | Min | Typ | Max | Unit | 测试条件        |
|-----------|----------|-----|-----|-----|------|-------------|
| 检测时间      | $t_{dr}$ | —   | —   | 1   | ms   | Figure 2.52 |

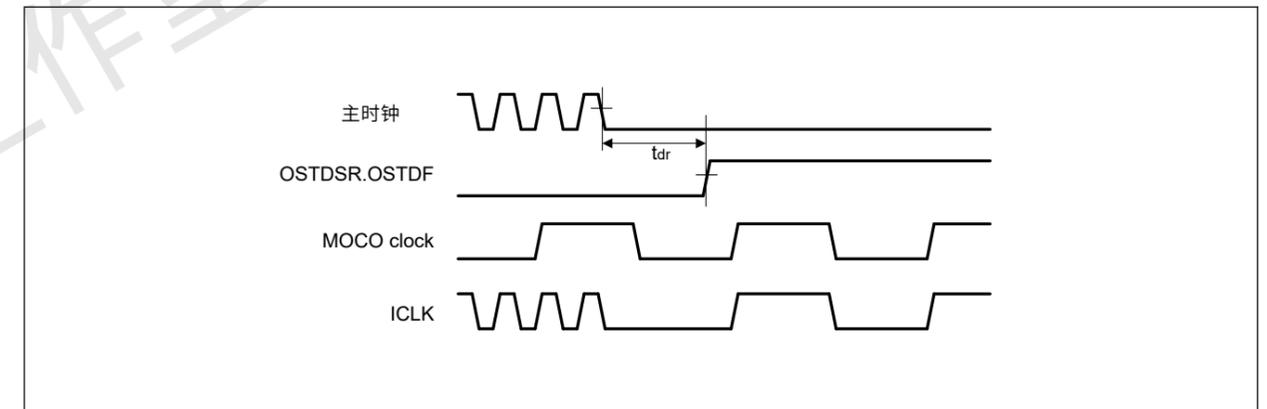


Figure 2.52 振荡停止检测时机

2.10 POR and LVD Characteristics

Table 2.44 Power-on reset circuit and voltage detection circuit characteristics (1)

| Parameter   | Symbol                           | Min                                | Typ              | Max  | Unit | Test conditions |                            |             |
|---|----------------------------------|------------------------------------|------------------|------|------|-----------------|----------------------------|-------------|
| Voltage detection level                                 | Power-on reset (POR)             | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | V <sub>POR</sub> | 2.5  | 2.6  | 2.7             | V                          | Figure 2.53 |
|   |                                  | DPSBYCR.DEEPCUT[1:0] = 11b.        |                  | 1.8  | 2.25 | 2.7             |                            |             |
|   | Voltage detection circuit (LVD0) | V <sub>det0_1</sub>                | 2.84             | 2.94 | 3.04 |                 | Figure 2.54                |             |
|   |                                  | V <sub>det0_2</sub>                | 2.77             | 2.87 | 2.97 |                 |                            |             |
|   |                                  | V <sub>det0_3</sub>                | 2.70             | 2.80 | 2.90 |                 |                            |             |
|   | Voltage detection circuit (LVD1) | V <sub>det1_1</sub>                | 2.89             | 2.99 | 3.09 |                 | Figure 2.55                |             |
|   |                                  | V <sub>det1_2</sub>                | 2.82             | 2.92 | 3.02 |                 |                            |             |
|   |                                  | V <sub>det1_3</sub>                | 2.75             | 2.85 | 2.95 |                 |                            |             |
|   | Voltage detection circuit (LVD2) | V <sub>det2_1</sub>                | 2.89             | 2.99 | 3.09 |                 | Figure 2.56                |             |
|   |                                  | V <sub>det2_2</sub>                | 2.82             | 2.92 | 3.02 |                 |                            |             |
|   |                                  | V <sub>det2_3</sub>                | 2.75             | 2.85 | 2.95 |                 |                            |             |
|   | Internal reset time              | Power-on reset time                | t <sub>POR</sub> | —    | 4.5  | —               | ms                         | Figure 2.53 |
| LVD0 reset time   |                                  | t <sub>LVD0</sub>                  | —                | 0.51 | —    |                 | Figure 2.54                |             |
| LVD1 reset time   |                                  | t <sub>LVD1</sub>                  | —                | 0.38 | —    |                 | Figure 2.55                |             |
| LVD2 reset time   |                                  | t <sub>LVD2</sub>                  | —                | 0.38 | —    |                 | Figure 2.56                |             |
| Minimum VCC down time*1                                 | t <sub>VOFF</sub>                | 200                                | —                | —    | —    | μs              | Figure 2.53, Figure 2.54   |             |
| Response delay  | t <sub>det</sub>                 | —                                  | —                | 200  | —    | μs              | Figure 2.54 to Figure 2.56 |             |
| LVD operation stabilization time (after LVD is enabled) | t <sub>d(E-A)</sub>              | —                                  | —                | 10   | —    | μs              | Figure 2.55, Figure 2.56   |             |
| Hysteresis width (LVD1 and LVD2)                        | V <sub>LVH</sub>                 | —                                  | 70               | —    | —    | mV              |                            |             |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V<sub>POR</sub>, V<sub>det0</sub>, V<sub>det1</sub>, and V<sub>det2</sub> for POR and LVD.

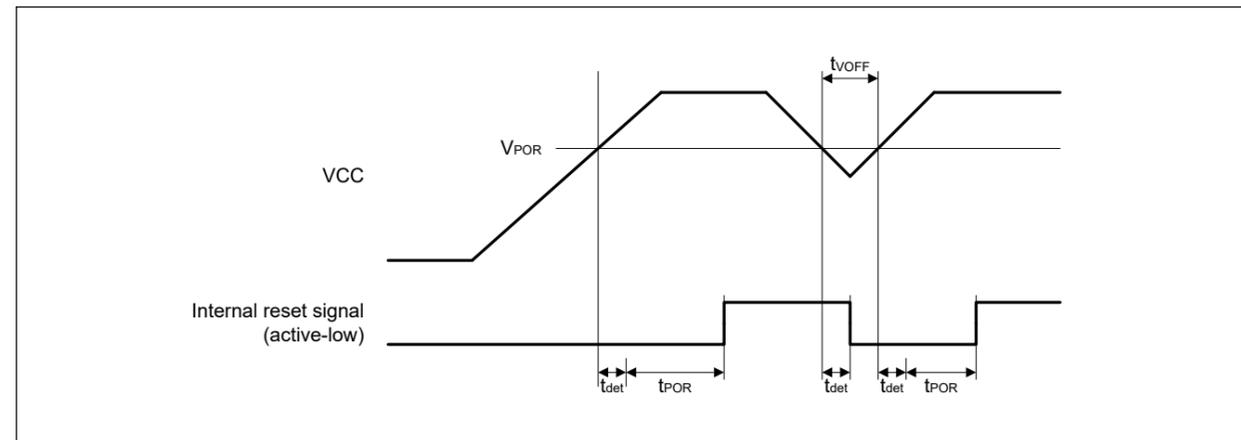


Figure 2.53 Power-on reset timing

2.10 POR和LVD特性

Table 2.44 上电复位电路及电压检测电路特性 (一)

| Parameter          | Symbol               | Min                                | Typ              | Max  | Unit | Test conditions |                          |             |
|--------------------|----------------------|------------------------------------|------------------|------|------|-----------------|--------------------------|-------------|
| 电压检测电平             | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | V <sub>POR</sub> | 2.5  | 2.6  | 2.7             | V                        | Figure 2.53 |
|                    |                      | DPSBYCR.DEEPCUT[1:0] = 11b.        |                  | 1.8  | 2.25 | 2.7             |                          |             |
|                    | 电压检测电路 (LVD0)        | V <sub>det0_1</sub>                | 2.84             | 2.94 | 3.04 |                 | Figure 2.54              |             |
|                    |                      | V <sub>det0_2</sub>                | 2.77             | 2.87 | 2.97 |                 |                          |             |
|                    |                      | V <sub>det0_3</sub>                | 2.70             | 2.80 | 2.90 |                 |                          |             |
|                    | 电压检测电路 (LVD1)        | V <sub>det1_1</sub>                | 2.89             | 2.99 | 3.09 |                 | Figure 2.55              |             |
|                    |                      | V <sub>det1_2</sub>                | 2.82             | 2.92 | 3.02 |                 |                          |             |
|                    |                      | V <sub>det1_3</sub>                | 2.75             | 2.85 | 2.95 |                 |                          |             |
|                    | 电压检测电路 (LVD2)        | V <sub>det2_1</sub>                | 2.89             | 2.99 | 3.09 |                 | Figure 2.56              |             |
|                    |                      | V <sub>det2_2</sub>                | 2.82             | 2.92 | 3.02 |                 |                          |             |
|                    |                      | V <sub>det2_3</sub>                | 2.75             | 2.85 | 2.95 |                 |                          |             |
|                    | 内部复位时间               | 上电复位时间                             | t <sub>POR</sub> | —    | 4.5  | —               | ms                       | Figure 2.53 |
| LVD0复位时间           |                      | t <sub>LVD0</sub>                  | —                | 0.51 | —    |                 | Figure 2.54              |             |
| LVD1复位时间           |                      | t <sub>LVD1</sub>                  | —                | 0.38 | —    |                 | Figure 2.55              |             |
| LVD2复位时间           |                      | t <sub>LVD2</sub>                  | —                | 0.38 | —    |                 | Figure 2.56              |             |
| 最小VCC停机时间*1        | t <sub>VOFF</sub>    | 200                                | —                | —    | —    | μs              | Figure 2.53, Figure 2.54 |             |
| 响应延迟               | t <sub>det</sub>     | —                                  | —                | 200  | —    | μs              | 图2.54至 Figure 2.56       |             |
| LVD操作稳定时间 (启用LVD后) | t <sub>d(E-A)</sub>  | —                                  | —                | 10   | —    | μs              | Figure 2.55, Figure 2.56 |             |
| 迟滞宽度 (LVD1和LVD2)   | V <sub>LVH</sub>     | —                                  | 70               | —    | —    | mV              |                          |             |

注1.最小VCC停机时间是指VCC低于电压检测电平V<sub>POR</sub>、V<sub>det0</sub>、V<sub>det1</sub>和V<sub>det2</sub>用于POR和LVD。

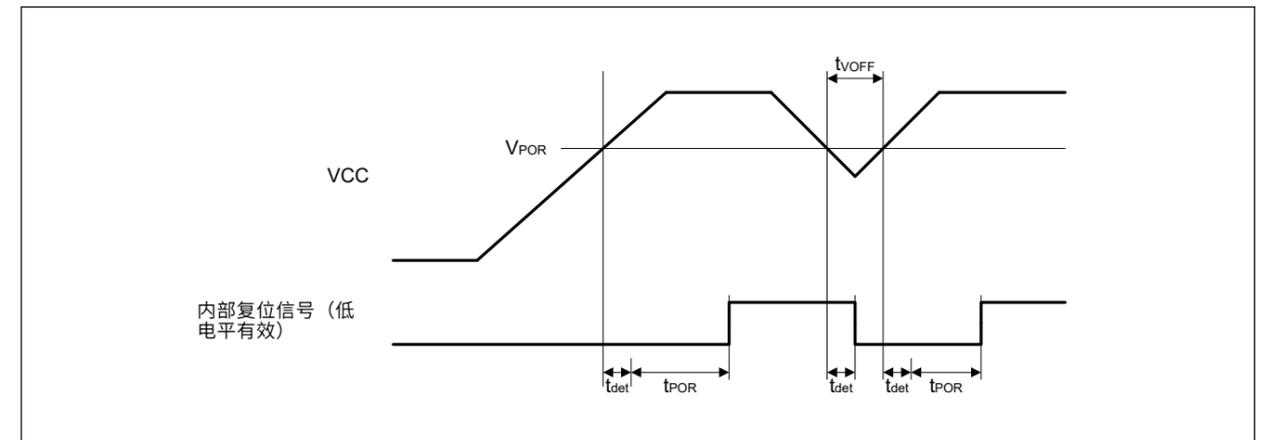


Figure 2.53 上电复位时序

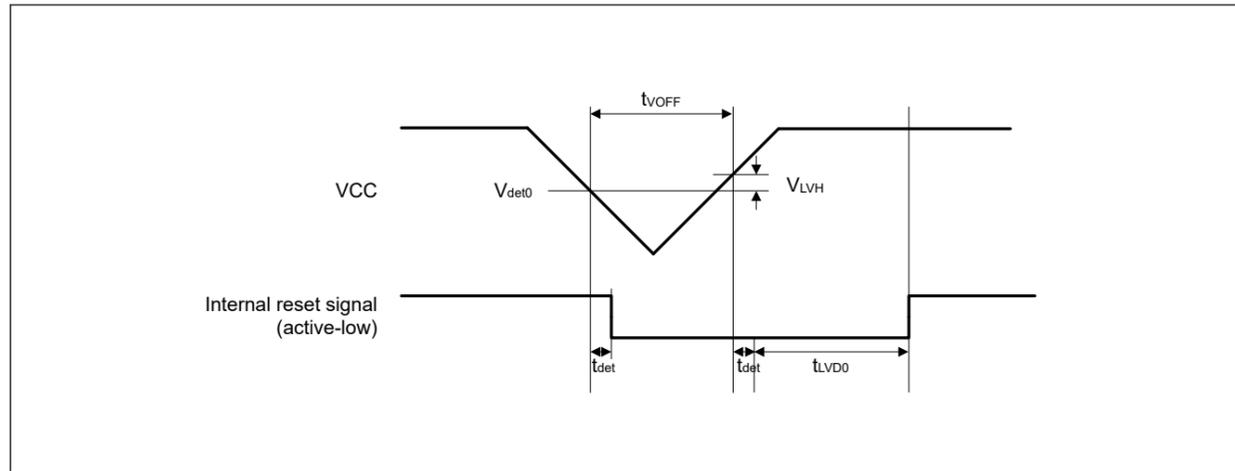


Figure 2.54 Voltage detection circuit timing ( $V_{det0}$ )

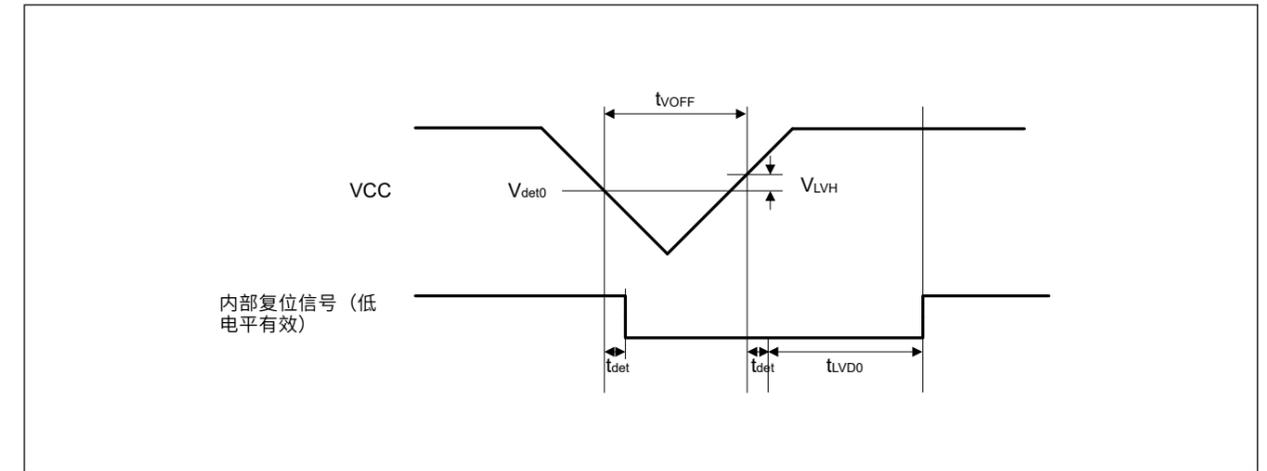


Figure 2.54 电压检测电路时序 ( $V_{det0}$ )

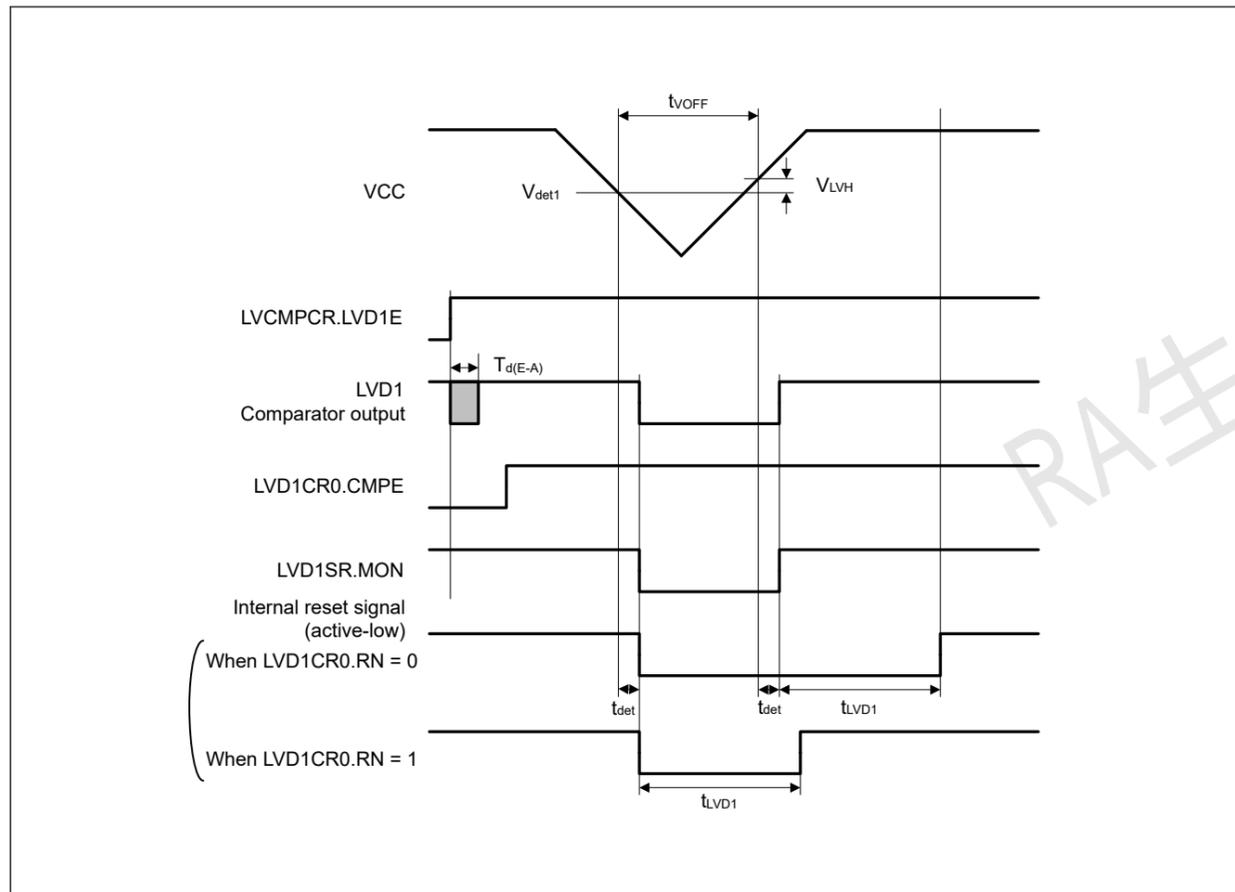


Figure 2.55 Voltage detection circuit timing ( $V_{det1}$ )

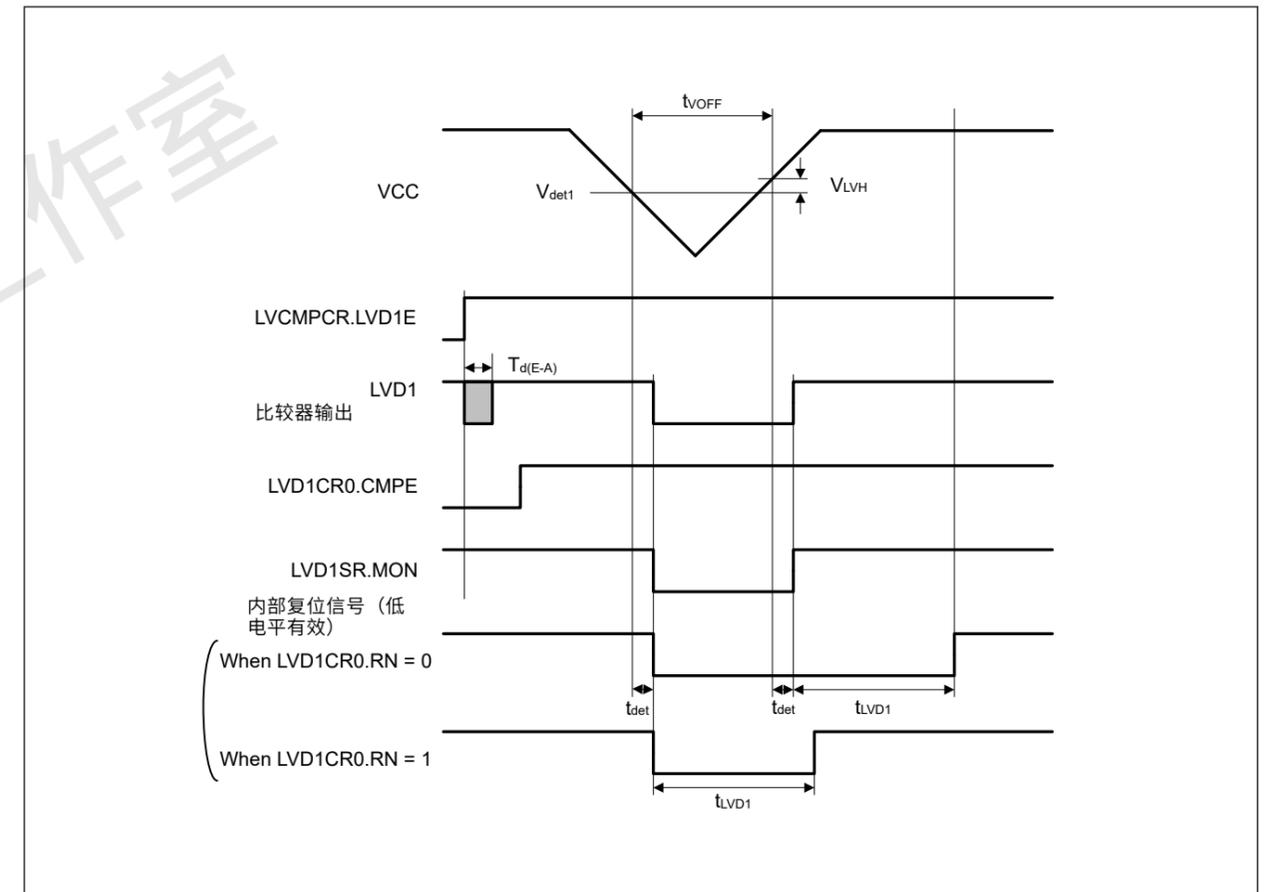


Figure 2.55 电压检测电路时序 ( $V_{det1}$ )

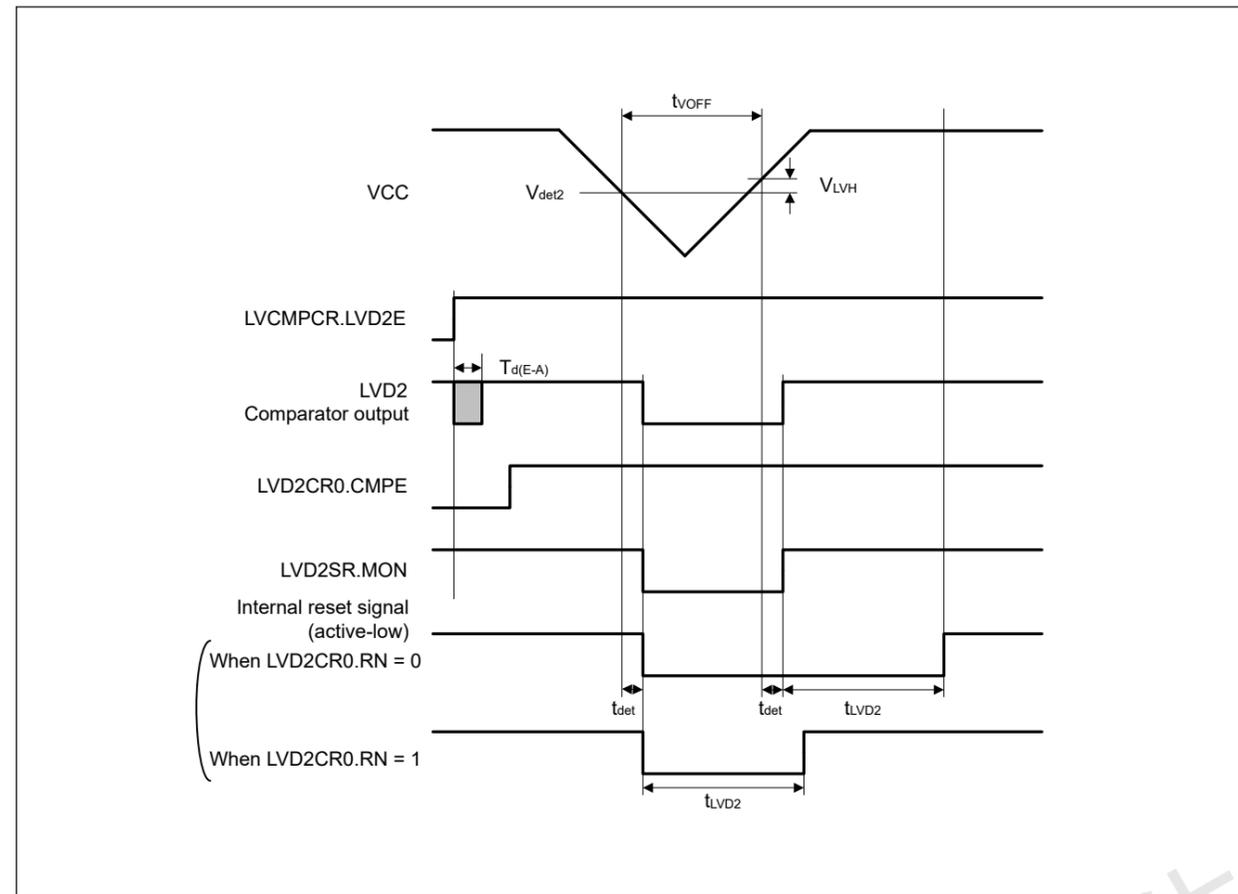


Figure 2.56 Voltage detection circuit timing (Vdet2)

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.45 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz  
Read: FCLK ≤ 60 MHz

| Parameter                            | Symbol   | FCLK = 4 MHz |       |      | 20 MHz ≤ FCLK ≤ 60 MHz |       |      | Unit | Test conditions |
|--------------------------------------|----------|--------------|-------|------|------------------------|-------|------|------|-----------------|
|                                      |          | Min          | Typ*6 | Max  | Min                    | Typ*6 | Max  |      |                 |
| Programming time<br>NPEC ≤ 100 times | 128-byte | tP128        | —     | 0.75 | 13.2                   | —     | 0.34 | 6.0  | ms              |
|                                      | 8-KB     | tP8K         | —     | 49   | 176                    | —     | 22   | 80   | ms              |
|                                      | 32-KB    | tP32K        | —     | 194  | 704                    | —     | 88   | 320  | ms              |
| Programming time<br>NPEC > 100 times | 128-byte | tP128        | —     | 0.91 | 15.8                   | —     | 0.41 | 7.2  | ms              |
|                                      | 8-KB     | tP8K         | —     | 60   | 212                    | —     | 27   | 96   | ms              |
|                                      | 32-KB    | tP32K        | —     | 234  | 848                    | —     | 106  | 384  | ms              |
| Erasure time<br>NPEC ≤ 100 times     | 8-KB     | tE8K         | —     | 78   | 216                    | —     | 43   | 120  | ms              |
|                                      | 32-KB    | tE32K        | —     | 283  | 864                    | —     | 157  | 480  | ms              |
| Erasure time<br>NPEC > 100 times     | 8-KB     | tE8K         | —     | 94   | 260                    | —     | 52   | 144  | ms              |
|                                      | 32-KB    | tE32K        | —     | 341  | 1040                   | —     | 189  | 576  | ms              |
| Reprogramming/erasure cycle*4        | NPEC     | 10000*1      | —     | —    | 10000*1                | —     | —    | —    | Times           |

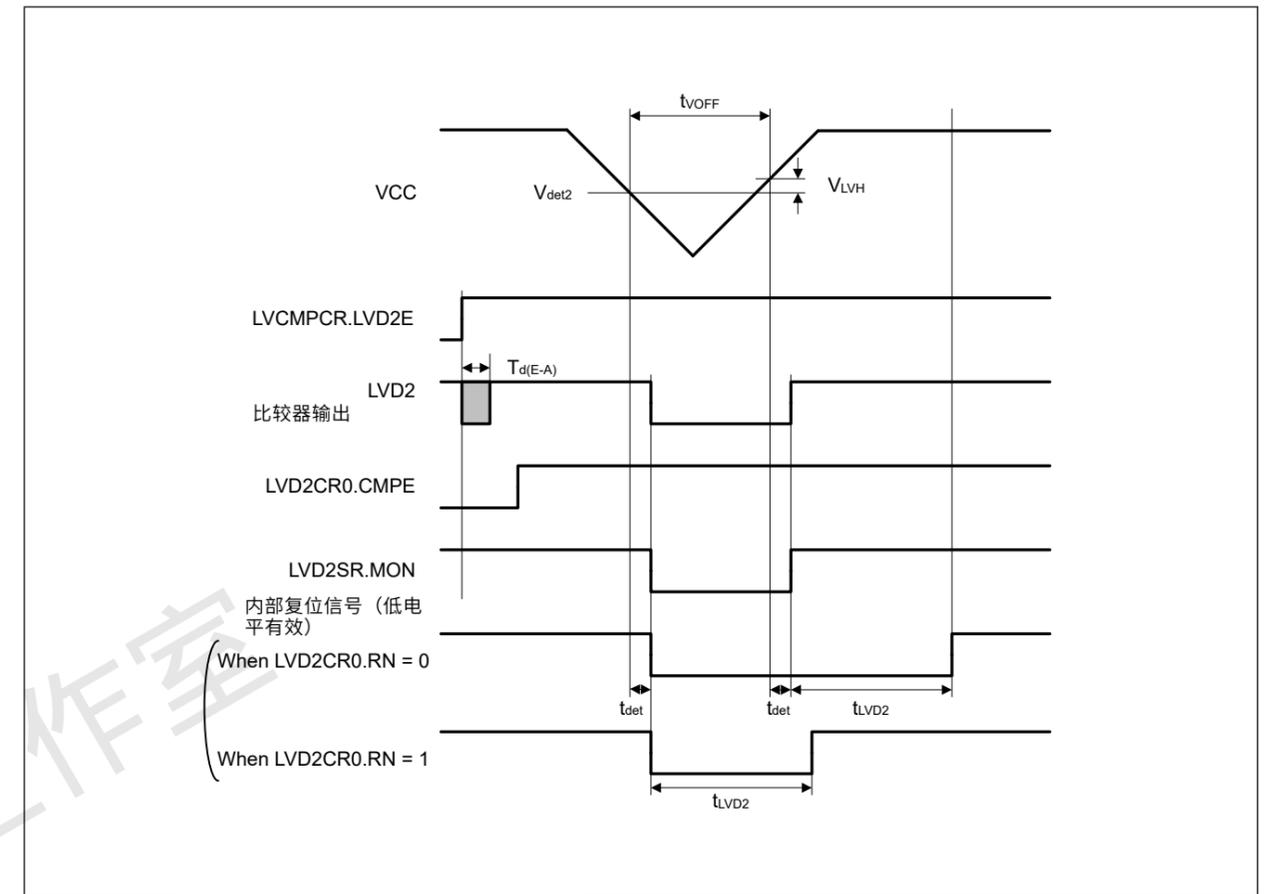


Figure 2.56 电压检测电路时序 (Vdet2)

2.11 闪存特性

2.11.1 代码闪存特性

Table 2.45 代码闪存特性(1of2)

条件: 编程或擦除: FCLK=4至60MHz  
Read: FCLK ≤ 60 MHz

| Parameter                     | Symbol   | FCLK = 4 MHz |       |      | 20 MHz ≤ FCLK ≤ 60 MHz |       |      | Unit | 测试条件  |
|-------------------------------|----------|--------------|-------|------|------------------------|-------|------|------|-------|
|                               |          | Min          | Typ*6 | Max  | Min                    | Typ*6 | Max  |      |       |
| 编程时间NPEC≤10<br>0次             | 128-byte | tP128        | —     | 0.75 | 13.2                   | —     | 0.34 | 6.0  | ms    |
|                               | 8-KB     | tP8K         | —     | 49   | 176                    | —     | 22   | 80   | ms    |
|                               | 32-KB    | tP32K        | —     | 194  | 704                    | —     | 88   | 320  | ms    |
| 编程时间NPEC>10<br>0次             | 128-byte | tP128        | —     | 0.91 | 15.8                   | —     | 0.41 | 7.2  | ms    |
|                               | 8-KB     | tP8K         | —     | 60   | 212                    | —     | 27   | 96   | ms    |
|                               | 32-KB    | tP32K        | —     | 234  | 848                    | —     | 106  | 384  | ms    |
| 擦除时间<br>NPEC≤100次             | 8-KB     | tE8K         | —     | 78   | 216                    | —     | 43   | 120  | ms    |
|                               | 32-KB    | tE32K        | —     | 283  | 864                    | —     | 157  | 480  | ms    |
| 擦除时间<br>NPEC>100次             | 8-KB     | tE8K         | —     | 94   | 260                    | —     | 52   | 144  | ms    |
|                               | 32-KB    | tE32K        | —     | 341  | 1040                   | —     | 189  | 576  | ms    |
| Reprogramming/erasure cycle*4 | NPEC     | 10000*1      | —     | —    | 10000*1                | —     | —    | —    | Times |

**Table 2.45 Code flash memory characteristics (2 of 2)**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

| Parameter   | Symbol | FCLK = 4 MHz |       |     | 20 MHz ≤ FCLK ≤ 60 MHz |       |     | Unit  | Test conditions |
|---|--------|--------------|-------|-----|------------------------|-------|-----|-------|-----------------|
|   |        | Min          | Typ*6 | Max | Min                    | Typ*6 | Max |       |                 |
| Suspend delay during programming                                    | tSPD   | —            | —     | 264 | —                      | —     | 120 | μs    |                 |
| Programming resume time   | tPRT   | —            | —     | 110 | —                      | —     | 50  | μs    |                 |
| First suspend delay during erasure in suspend priority mode         | tSESD1 | —            | —     | 216 | —                      | —     | 120 | μs    |                 |
| Second suspend delay during erasure in suspend priority mode        | tSESD2 | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |                 |
| Suspend delay during erasure in erasure priority mode               | tSEED  | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |                 |
| First erasing resume time during erasure in suspend priority mode*5 | tREST1 | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |                 |
| Second erasing resume time during erasure in suspend priority mode  | tREST2 | —            | —     | 144 | —                      | —     | 80  | μs    |                 |
| Erasing resume time during erasure in erasure priority mode         | tREET  | —            | —     | 144 | —                      | —     | 80  | μs    |                 |
| Forced stop command   | tFD    | —            | —     | 32  | —                      | —     | 20  | μs    |                 |
| Data hold time*2  | tDRP   | 10*2*3       | —     | —   | 10*2*3                 | —     | —   | Years | Ta = +85°C      |
|   |        | 30*2*3       | —     | —   | 30*2*3                 | —     | —   |       |                 |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Note 6. The reference value at VCC = 3.3V and room temperature.

**Table 2.45 代码闪存特性(2of2)**

条件: 编程或擦除: FCLK=4至60MHz

Read: FCLK ≤ 60 MHz

| Parameter              | Symbol | FCLK = 4 MHz |       |     | 20 MHz ≤ FCLK ≤ 60 MHz |       |     | Unit  | 测试条件       |
|------------------------|--------|--------------|-------|-----|------------------------|-------|-----|-------|------------|
|                        |        | Min          | Typ*6 | Max | Min                    | Typ*6 | Max |       |            |
| 编程期间暂停延迟               | tSPD   | —            | —     | 264 | —                      | —     | 120 | μs    |            |
| 编程恢复时间                 | tPRT   | —            | —     | 110 | —                      | —     | 50  | μs    |            |
| 挂起优先模式下擦除期间的第一个挂起延迟    | tSESD1 | —            | —     | 216 | —                      | —     | 120 | μs    |            |
| 挂起优先模式下擦除期间的第二挂起延迟     | tSESD2 | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |            |
| 擦除优先模式下擦除期间的挂起延迟       | tSEED  | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |            |
| 挂起优先模式擦除期间的第一次擦除恢复时间*5 | tREST1 | —            | —     | 1.7 | —                      | —     | 1.7 | ms    |            |
| 挂起优先模式下擦除期间的第二次擦除恢复时间  | tREST2 | —            | —     | 144 | —                      | —     | 80  | μs    |            |
| 在擦除优先模式下擦除期间擦除恢复时间     | tREET  | —            | —     | 144 | —                      | —     | 80  | μs    |            |
| 强制停止命令                 | tFD    | —            | —     | 32  | —                      | —     | 20  | μs    |            |
| 数据保持时间*2               | tDRP   | 10*2*3       | —     | —   | 10*2*3                 | —     | —   | Years | Ta = +85°C |
|                        |        | 30*2*3       | —     | —   | 30*2*3                 | —     | —   |       |            |

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

注2.这表示在指定范围内执行重新编程时特性的最小值。

注3: 此结果来自可靠性测试。

注4.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次 (n=10 000) 时, 可以对每个块执行n次擦除。例如, 当对8KB块中的不同地址执行64次128字节编程, 然后擦除整个块时, 重新编程擦除周期计为1。但是, 不能将同一地址多次编程为一次擦除。禁止覆盖。

注5.恢复时间包括重新应用暂停时切断的擦除脉冲 (最多1个完整脉冲) 的时间。

注6.VCC=3.3V和室温下的参考值。

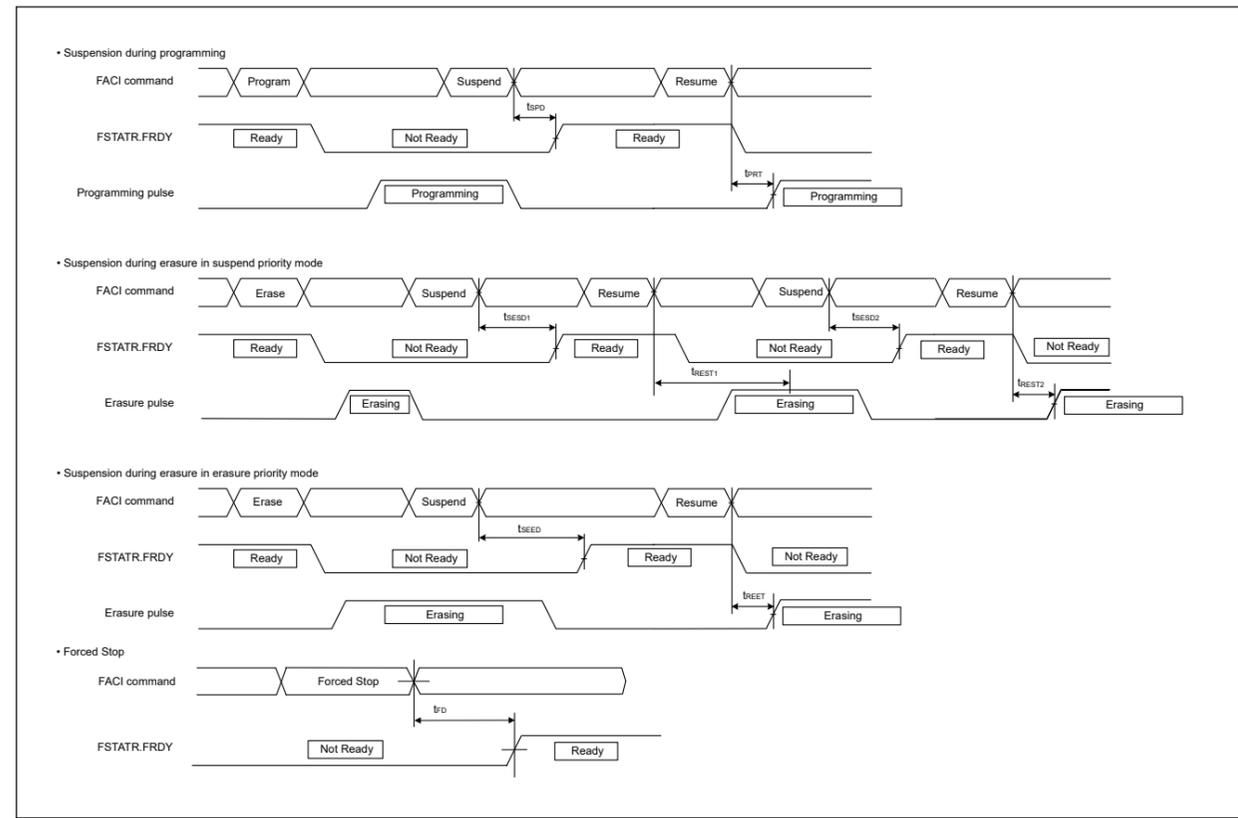


Figure 2.57 Suspension and forced stop timing for flash memory programming and erasure

2.11.2 Data Flash Memory Characteristics

Table 2.46 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz  
Read: FCLK ≤ 60 MHz

| Parameter   | Symbol            | FCLK = 4 MHz        |       |      | 20 MHz ≤ FCLK ≤ 60 MHz |       |      | Unit | Test conditions |
|---|-------------------|---------------------|-------|------|------------------------|-------|------|------|-----------------|
|   |                   | Min                 | Typ*6 | Max  | Min                    | Typ*6 | Max  |      |                 |
| Programming time  | 4-byte            | t <sub>DP4</sub>    | —     | 0.36 | 3.8                    | —     | 0.16 | 1.7  | ms              |
|   | 8-byte            | t <sub>DP8</sub>    | —     | 0.38 | 4.0                    | —     | 0.17 | 1.8  |                 |
|   | 16-byte           | t <sub>DP16</sub>   | —     | 0.42 | 4.5                    | —     | 0.19 | 2.0  |                 |
| Erasure time  | 64-byte           | t <sub>DE64</sub>   | —     | 3.1  | 18                     | —     | 1.7  | 10   | ms              |
|   | 128-byte          | t <sub>DE128</sub>  | —     | 4.7  | 27                     | —     | 2.6  | 15   |                 |
|   | 256-byte          | t <sub>DE256</sub>  | —     | 8.9  | 50                     | —     | 4.9  | 28   |                 |
| Blank check time  | 4-byte            | t <sub>DBC4</sub>   | —     | —    | 84                     | —     | —    | 30   | μs              |
| Reprogramming/erasure cycle*1                               | N <sub>DPEC</sub> | 125000*2            | —     | —    | 125000*2               | —     | —    | —    | —               |
| Suspend delay during programming                            | 4-byte            | t <sub>DSPD</sub>   | —     | —    | 264                    | —     | —    | 120  | μs              |
|   | 8-byte            |                     | —     | —    | 264                    | —     | —    | 120  |                 |
|   | 16-byte           |                     | —     | —    | 264                    | —     | —    | 120  |                 |
| Programming resume time                                     |                   | t <sub>DPRT</sub>   | —     | —    | 110                    | —     | —    | 50   | μs              |
| First suspend delay during erasure in suspend priority mode | 64-byte           | t <sub>DSESD1</sub> | —     | —    | 216                    | —     | —    | 120  | μs              |
|   | 128-byte          |                     | —     | —    | 216                    | —     | —    | 120  |                 |
|   | 256-byte          |                     | —     | —    | 216                    | —     | —    | 120  |                 |

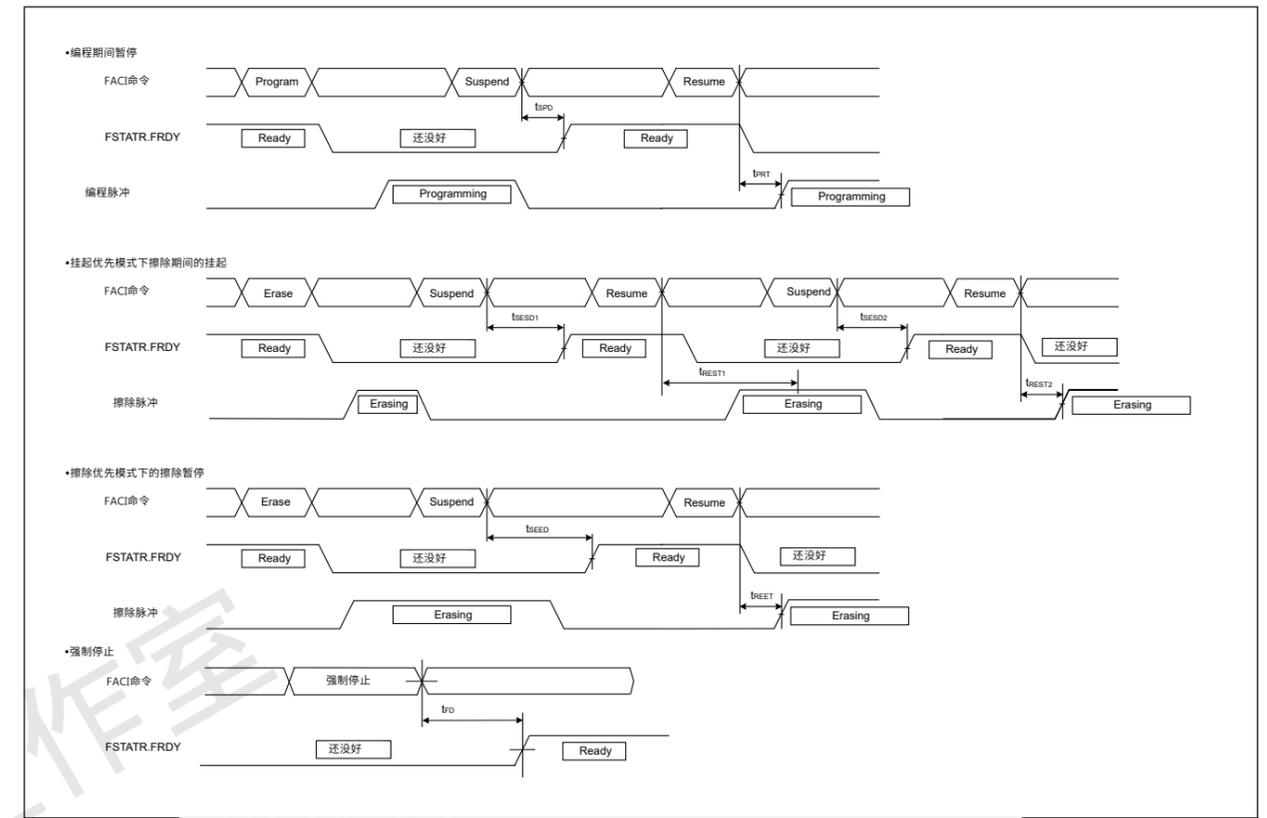


Figure 2.57 闪存编程和擦除的暂停和强制停止时序

2.11.2 数据闪存特性

Table 2.46 数据闪存特性(1of2)

条件：编程或擦除：FCLK=4至60MHz  
Read: FCLK ≤ 60 MHz

| Parameter                     | Symbol            | FCLK = 4 MHz        |            |      | 20 MHz ≤ FCLK ≤ 60 MHz |       |      | Unit | 测试条件 |
|-------------------------------|-------------------|---------------------|------------|------|------------------------|-------|------|------|------|
|                               |                   | Min                 | 典型*6最大值最小值 | Max  | Min                    | Typ*6 | Max  |      |      |
| 编程时间                          | 4-byte            | t <sub>DP4</sub>    | —          | 0.36 | 3.8                    | —     | 0.16 | 1.7  | ms   |
|                               | 8-byte            | t <sub>DP8</sub>    | —          | 0.38 | 4.0                    | —     | 0.17 | 1.8  |      |
|                               | 16-byte           | t <sub>DP16</sub>   | —          | 0.42 | 4.5                    | —     | 0.19 | 2.0  |      |
| 擦除时间                          | 64-byte           | t <sub>DE64</sub>   | —          | 3.1  | 18                     | —     | 1.7  | 10   | ms   |
|                               | 128-byte          | t <sub>DE128</sub>  | —          | 4.7  | 27                     | —     | 2.6  | 15   |      |
|                               | 256-byte          | t <sub>DE256</sub>  | —          | 8.9  | 50                     | —     | 4.9  | 28   |      |
| 空白检查时间                        | 4-byte            | t <sub>DBC4</sub>   | —          | —    | 84                     | —     | —    | 30   | μs   |
| Reprogramming/erasure cycle*1 | N <sub>DPEC</sub> | 125000*2            | —          | —    | 125000*2               | —     | —    | —    | —    |
| 编程期间暂停延迟                      | 4-byte            | t <sub>DSPD</sub>   | —          | —    | 264                    | —     | —    | 120  | μs   |
|                               | 8-byte            |                     | —          | —    | 264                    | —     | —    | 120  |      |
|                               | 16-byte           |                     | —          | —    | 264                    | —     | —    | 120  |      |
| 编程恢复时间                        |                   | t <sub>DPRT</sub>   | —          | —    | 110                    | —     | —    | 50   | μs   |
| 挂起优先模式下擦除期间的第一个挂起延迟           | 64-byte           | t <sub>DSESD1</sub> | —          | —    | 216                    | —     | —    | 120  | μs   |
|                               | 128-byte          |                     | —          | —    | 216                    | —     | —    | 120  |      |
|                               | 256-byte          |                     | —          | —    | 216                    | —     | —    | 120  |      |

**Table 2.46 Data flash memory characteristics (2 of 2)**

Conditions: Program or erase: FCLK = 4 to 60 MHz  
Read: FCLK ≤ 60 MHz

| Parameter   | Symbol              | FCLK = 4 MHz        |                   |     | 20 MHz ≤ FCLK ≤ 60 MHz |                   |     | Unit | Test conditions |
|---|---------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|------|-----------------|
|   |                     | Min                 | Typ <sup>*6</sup> | Max | Min                    | Typ <sup>*6</sup> | Max |      |                 |
| Second suspend delay during erasure in suspend priority mode  | 64-byte             | —                   | —                 | 300 | —                      | —                 | 300 | μs   |                 |
|   | 128-byte            | —                   | —                 | 390 | —                      | —                 | 390 |      |                 |
|   | 256-byte            | —                   | —                 | 570 | —                      | —                 | 570 |      |                 |
| Suspend delay during erasing in erasure priority mode   | 64-byte             | —                   | —                 | 300 | —                      | —                 | 300 | μs   |                 |
|   | 128-byte            | —                   | —                 | 390 | —                      | —                 | 390 |      |                 |
|   | 256-byte            | —                   | —                 | 570 | —                      | —                 | 570 |      |                 |
| First erasing resume time during erasure in suspend priority mode <sup>*5</sup>   | t <sub>DREST1</sub> | —                   | —                 | 300 | —                      | —                 | 300 | μs   |                 |
| Second erasing resume time during erasure in suspend priority mode<br>First erasing resume time during erasure in suspend priority mode | t <sub>DREST2</sub> | —                   | —                 | 126 | —                      | —                 | 70  | μs   |                 |
| Erasing resume time during erasure in erasure priority mode   | t <sub>DREET</sub>  | —                   | —                 | 126 | —                      | —                 | 70  | μs   |                 |
| Forced stop command   | t <sub>FD</sub>     | —                   | —                 | 32  | —                      | —                 | 20  | μs   |                 |
| Data hold time <sup>*3</sup>  | t <sub>DRP</sub>    | 10 <sup>*3</sup> *4 | —                 | —   | 10 <sup>*3</sup> *4    | —                 | —   | Year |                 |
|   |                     | 30 <sup>*3</sup> *4 | —                 | —   | 30 <sup>*3</sup> *4    | —                 | —   |      |                 |

- Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
- Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
- Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
- Note 4. This result is obtained from reliability testing.
- Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
- Note 6. The reference value at VCC = 3.3 V and room temperature.

2.11.3 Option Setting Memory Characteristics

**Table 2.47 Option setting memory characteristics**

Conditions: Program: FCLK = 4 to 60 MHz  
Read: FCLK ≤ 60 MHz

| Parameter  | Symbol           | FCLK = 4 MHz        |                   |     | 20 MHz ≤ FCLK ≤ 60 MHz |                   |     | Unit  | Test conditions |
|--|------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|-------|-----------------|
|  |                  | Min                 | Typ <sup>*4</sup> | Max | Min                    | Typ <sup>*4</sup> | Max |       |                 |
| Programming time<br>N <sub>OPC</sub> ≤ 100 times | t <sub>OP</sub>  | —                   | 83                | 309 | —                      | 45                | 162 | ms    |                 |
| Programming time<br>N <sub>OPC</sub> > 100 times | t <sub>OP</sub>  | —                   | 100               | 371 | —                      | 55                | 195 | ms    |                 |
| Reprogramming cycle                              | N <sub>OPC</sub> | 20000 <sup>*1</sup> | —                 | —   | 20000 <sup>*1</sup>    | —                 | —   | Times |                 |
| Data hold time <sup>*2</sup>                     | t <sub>DRP</sub> | 10 <sup>*2</sup> *3 | —                 | —   | 10 <sup>*2</sup> *3    | —                 | —   | Years |                 |
|  |                  | 30 <sup>*2</sup> *3 | —                 | —   | 30 <sup>*2</sup> *3    | —                 | —   |       |                 |

- Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
- Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
- Note 3. This result is obtained from reliability testing.
- Note 4. The reference value at VCC = 3.3 V and room temperature.

2.12 Boundary Scan

**Table 2.46 数据闪存特性(2of2)**

条件: 编程或擦除: FCLK=4至60MHz  
Read: FCLK ≤ 60 MHz

| Parameter                                      | Symbol              | FCLK = 4 MHz        |            |     | 20 MHz ≤ FCLK ≤ 60 MHz |                   |     | Unit | 测试条件 |
|--|---------------------|---------------------|------------|-----|------------------------|-------------------|-----|------|------|
|  |                     | Min                 | 典型+6最大值最小值 | Max | Min                    | Typ <sup>*6</sup> | Max |      |      |
| 挂起优先模式下擦除期间的第二挂起延迟                             | 64-byte             | —                   | —          | 300 | —                      | —                 | 300 | μs   |      |
|  | 128-byte            | —                   | —          | 390 | —                      | —                 | 390 |      |      |
|  | 256-byte            | —                   | —          | 570 | —                      | —                 | 570 |      |      |
| 在擦除优先模式下擦除期间暂停延迟                               | 64-byte             | —                   | —          | 300 | —                      | —                 | 300 | μs   |      |
|  | 128-byte            | —                   | —          | 390 | —                      | —                 | 390 |      |      |
|  | 256-byte            | —                   | —          | 570 | —                      | —                 | 570 |      |      |
| 挂起优先模式擦除期间的第一次擦除恢复时间*5                         | t <sub>DREST1</sub> | —                   | —          | 300 | —                      | —                 | 300 | μs   |      |
| 挂起优先模式下擦除期间的第二次擦除恢复时间<br>挂起优先模式下擦除期间的第二次擦除恢复时间 | t <sub>DREST2</sub> | —                   | —          | 126 | —                      | —                 | 70  | μs   |      |
| 在擦除优先模式下擦除期间擦除恢复时间                             | t <sub>DREET</sub>  | —                   | —          | 126 | —                      | —                 | 70  | μs   |      |
| 强制停止命令   | t <sub>FD</sub>     | —                   | —          | 32  | —                      | —                 | 20  | μs   |      |
| 数据保持时间*3                                       | t <sub>DRP</sub>    | 10 <sup>*3</sup> *4 | —          | —   | 10 <sup>*3</sup> *4    | —                 | —   | Year |      |
|  |                     | 30 <sup>*3</sup> *4 | —          | —   | 30 <sup>*3</sup> *4    | —                 | —   |      |      |

- 注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次 (n=125 000) 时,可以对每个块执行n次擦除。例如,当对64字节块中的不同地址执行16次4字节编程,然后擦除整个块时,重新编程擦除周期计为1。但是,不能将同一地址多次编程为一次擦除。禁止覆盖。
- 注2.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
- 注3.这表示在指定范围内执行重新编程时特性的最小值。
- 注4: 此结果来自可靠性测试。
- 注5.恢复时间包括重新应用暂停时切断的擦除脉冲(最多1个完整脉冲)的时间。
- 注6.VCC=3.3V和室温下的参考值。

2.11.3 选项设置内存特性

**Table 2.47 选项设置内存特性**

Conditions: Program: FCLK = 4 to 60 MHz  
Read: FCLK ≤ 60 MHz

| Parameter                  | Symbol           | FCLK = 4 MHz        |                   |     | 20 MHz ≤ FCLK ≤ 60 MHz |                   |     | Unit  | 测试条件 |
|----------------------------|------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|-------|------|
|                            |                  | Min                 | Typ <sup>*4</sup> | Max | Min                    | Typ <sup>*4</sup> | Max |       |      |
| 编程时间N <sub>OPC</sub> ≤100次 | t <sub>OP</sub>  | —                   | 83                | 309 | —                      | 45                | 162 | ms    |      |
| 编程时间N <sub>OPC</sub> >100次 | t <sub>OP</sub>  | —                   | 100               | 371 | —                      | 55                | 195 | ms    |      |
| 重编程周期                      | N <sub>OPC</sub> | 20000 <sup>*1</sup> | —                 | —   | 20000 <sup>*1</sup>    | —                 | —   | Times |      |
| 数据保持时间*2                   | t <sub>DRP</sub> | 10 <sup>*2</sup> *3 | —                 | —   | 10 <sup>*2</sup> *3    | —                 | —   | Years |      |
|                            |                  | 30 <sup>*2</sup> *3 | —                 | —   | 30 <sup>*2</sup> *3    | —                 | —   |       |      |

- 注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
- 注2.这表示在指定范围内执行重新编程时特性的最小值。
- 注3: 此结果来自可靠性测试。
- 注4.VCC=3.3V和室温下的参考值。

2.12 边界扫描

Table 2.48 Boundary scan characteristics

| Parameter                            | Symbol       | Min         | Typ | Max | Unit | Test conditions |
|--------------------------------------|--------------|-------------|-----|-----|------|-----------------|
| TCK clock cycle time                 | $t_{TCKcyc}$ | 100         | —   | —   | ns   | Figure 2.58     |
| TCK clock high pulse width           | $t_{TCKH}$   | 45          | —   | —   | ns   |                 |
| TCK clock low pulse width            | $t_{TCKL}$   | 45          | —   | —   | ns   |                 |
| TCK clock rise time                  | $t_{TCKr}$   | —           | —   | 5   | ns   |                 |
| TCK clock fall time                  | $t_{TCKf}$   | —           | —   | 5   | ns   |                 |
| TMS setup time                       | $t_{TMSS}$   | 20          | —   | —   | ns   | Figure 2.59     |
| TMS hold time                        | $t_{TMSh}$   | 20          | —   | —   | ns   |                 |
| TDI setup time                       | $t_{TDIS}$   | 20          | —   | —   | ns   |                 |
| TDI hold time                        | $t_{TDIH}$   | 20          | —   | —   | ns   |                 |
| TDO data delay                       | $t_{TDOD}$   | —           | —   | 40  | ns   | Figure 2.60     |
| Boundary scan circuit startup time*1 | $T_{BSSTUP}$ | $t_{RESWP}$ | —   | —   | —    |                 |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

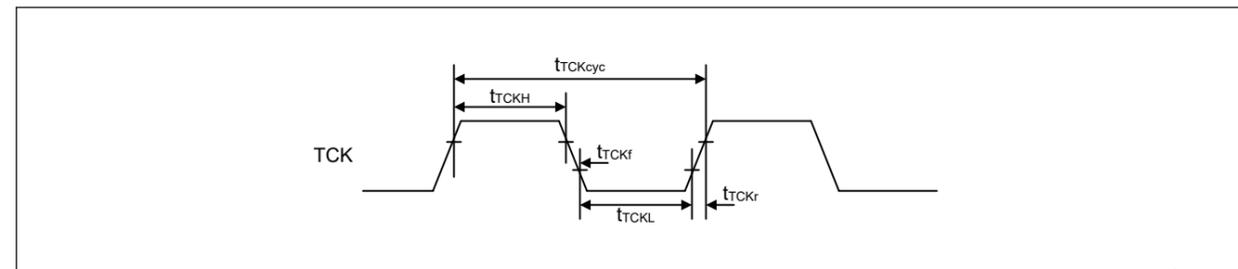


Figure 2.58 Boundary scan TCK timing

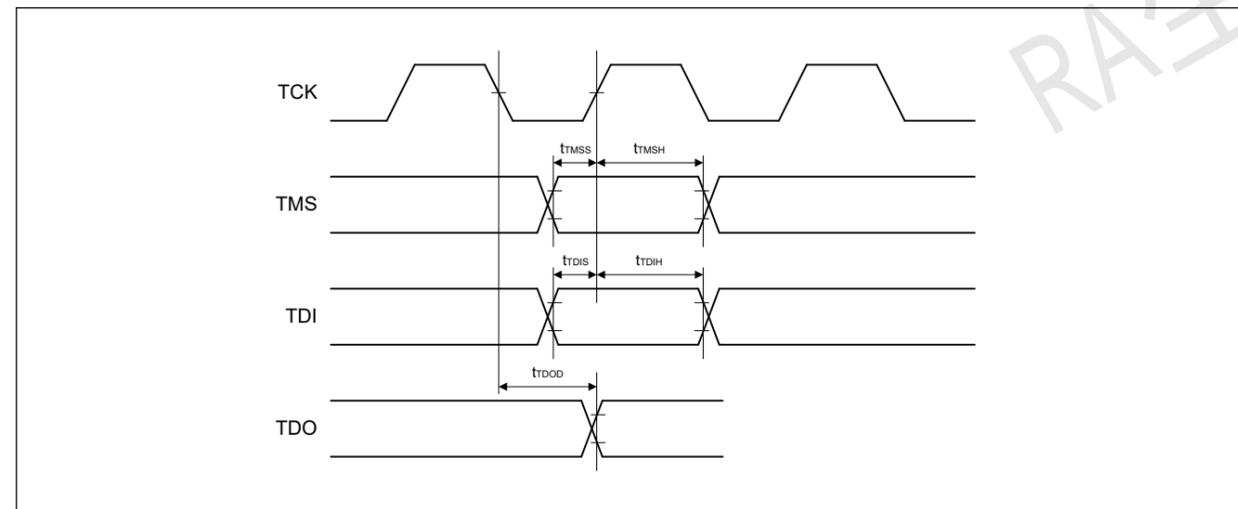


Figure 2.59 Boundary scan input/output timing

Table 2.48 边界扫描特性

| Parameter    | Symbol       | Min         | Typ | Max | Unit | 测试条件        |
|--------------|--------------|-------------|-----|-----|------|-------------|
| TCK时钟周期时间    | $t_{TCKcyc}$ | 100         | —   | —   | ns   | Figure 2.58 |
| TCK时钟高脉冲宽度   | $t_{TCKH}$   | 45          | —   | —   | ns   |             |
| TCK时钟低脉冲宽度   | $t_{TCKL}$   | 45          | —   | —   | ns   |             |
| TCK时钟上升时间    | $t_{TCKr}$   | —           | —   | 5   | ns   |             |
| TCK时钟下降时间    | $t_{TCKf}$   | —           | —   | 5   | ns   |             |
| TMS设置时间      | $t_{TMSS}$   | 20          | —   | —   | ns   | Figure 2.59 |
| TMS保持时间      | $t_{TMSh}$   | 20          | —   | —   | ns   |             |
| TDI建立时间      | $t_{TDIS}$   | 20          | —   | —   | ns   |             |
| TDI保持时间      | $t_{TDIH}$   | 20          | —   | —   | ns   |             |
| TDO数据延迟      | $t_{TDOD}$   | —           | —   | 40  | ns   | Figure 2.60 |
| 边界扫描电路启动时间*1 | $T_{BSSTUP}$ | $t_{RESWP}$ | —   | —   | —    |             |

注1.在上电复位变为负值之前，边界扫描不起作用。

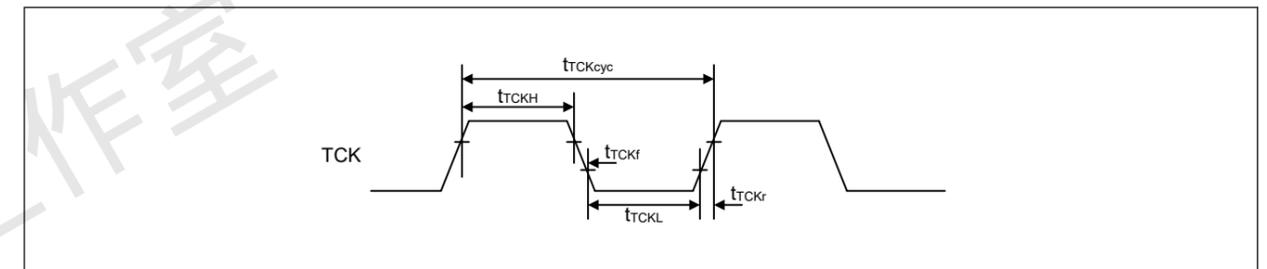


Figure 2.58 边界扫描TCK时序

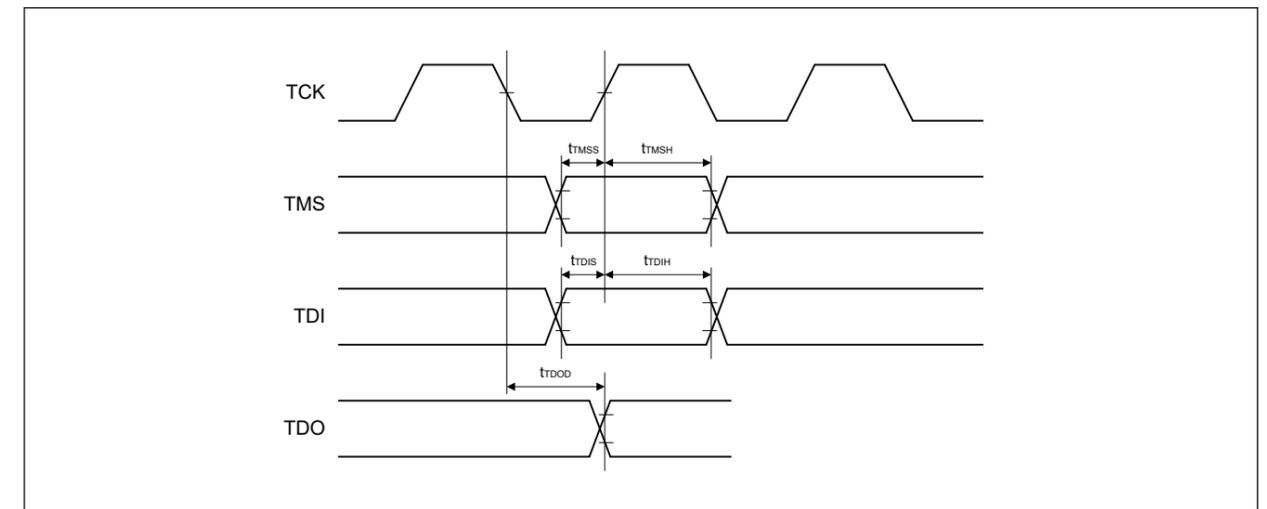


Figure 2.59 边界扫描输入输出时序

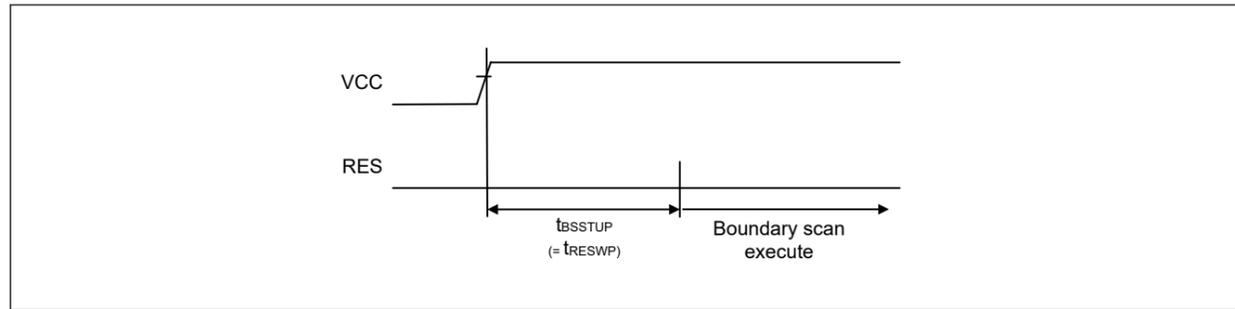


Figure 2.60 Boundary scan circuit startup timing

2.13 Joint Test Action Group (JTAG)

Table 2.49 JTAG

| Parameter                  | Symbol       | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time       | $t_{TCKcyc}$ | 40  | —   | —   | ns   | Figure 2.61     |
| TCK clock high pulse width | $t_{TCKH}$   | 15  | —   | —   | ns   |                 |
| TCK clock low pulse width  | $t_{TCKL}$   | 15  | —   | —   | ns   |                 |
| TCK clock rise time        | $t_{TCKr}$   | —   | —   | 5   | ns   |                 |
| TCK clock fall time        | $t_{TCKf}$   | —   | —   | 5   | ns   |                 |
| TMS setup time             | $t_{TMSS}$   | 8   | —   | —   | ns   | Figure 2.62     |
| TMS hold time              | $t_{TMSH}$   | 8   | —   | —   | ns   |                 |
| TDI setup time             | $t_{TDIS}$   | 8   | —   | —   | ns   |                 |
| TDI hold time              | $t_{TDIH}$   | 8   | —   | —   | ns   |                 |
| TDO data delay time        | $t_{TDOD}$   | —   | —   | 20  | ns   |                 |

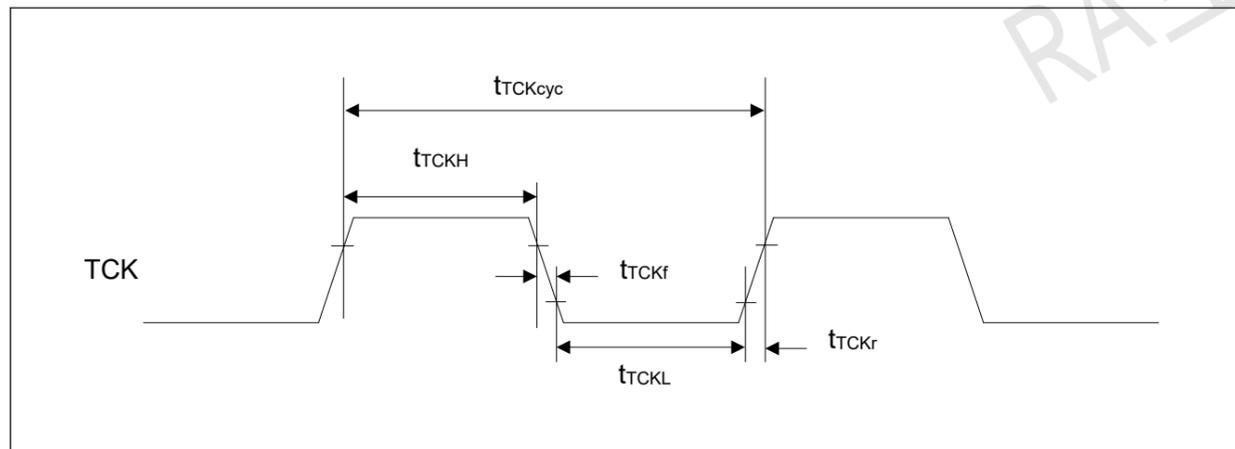


Figure 2.61 JTAG TCK timing

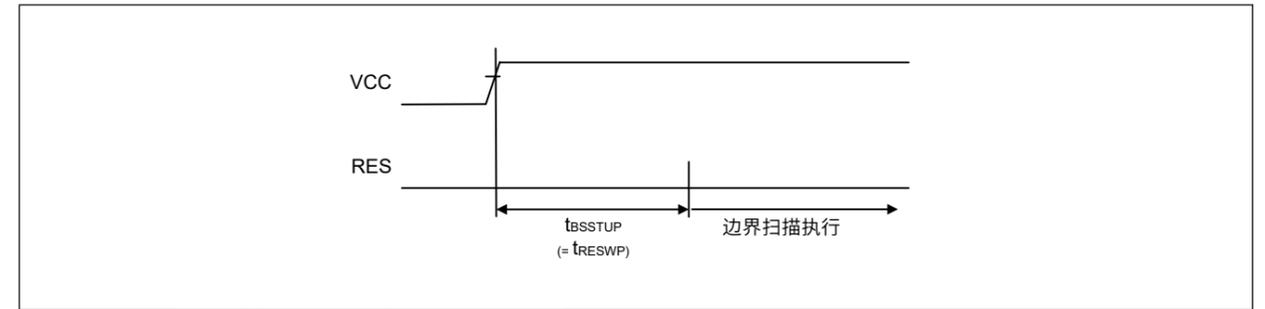


Figure 2.60 边界扫描电路启动时序

2.13 联合测试行动组(JTAG)

Table 2.49 JTAG

| Parameter  | Symbol       | Min | Typ | Max | Unit | 测试条件        |
|------------|--------------|-----|-----|-----|------|-------------|
| TCK时钟周期时间  | $t_{TCKcyc}$ | 40  | —   | —   | ns   | Figure 2.61 |
| TCK时钟高脉冲宽度 | $t_{TCKH}$   | 15  | —   | —   | ns   |             |
| TCK时钟低脉冲宽度 | $t_{TCKL}$   | 15  | —   | —   | ns   |             |
| TCK时钟上升时间  | $t_{TCKr}$   | —   | —   | 5   | ns   |             |
| TCK时钟下降时间  | $t_{TCKf}$   | —   | —   | 5   | ns   |             |
| TMS设置时间    | $t_{TMSS}$   | 8   | —   | —   | ns   | Figure 2.62 |
| TMS保持时间    | $t_{TMSH}$   | 8   | —   | —   | ns   |             |
| TDI建立时间    | $t_{TDIS}$   | 8   | —   | —   | ns   |             |
| TDI保持时间    | $t_{TDIH}$   | 8   | —   | —   | ns   |             |
| TDO数据延迟时间  | $t_{TDOD}$   | —   | —   | 20  | ns   |             |

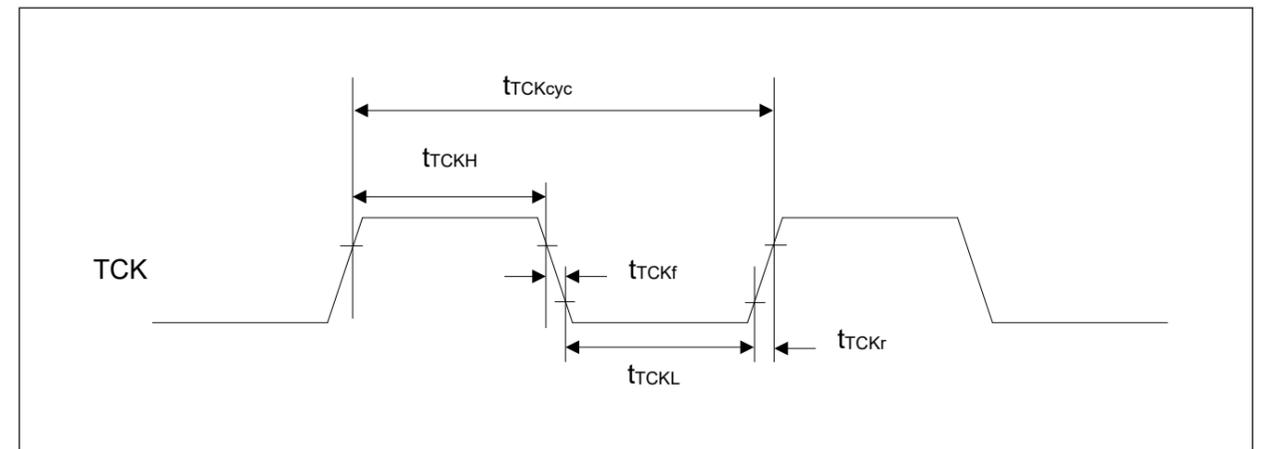


Figure 2.61 JTAG TCK timing

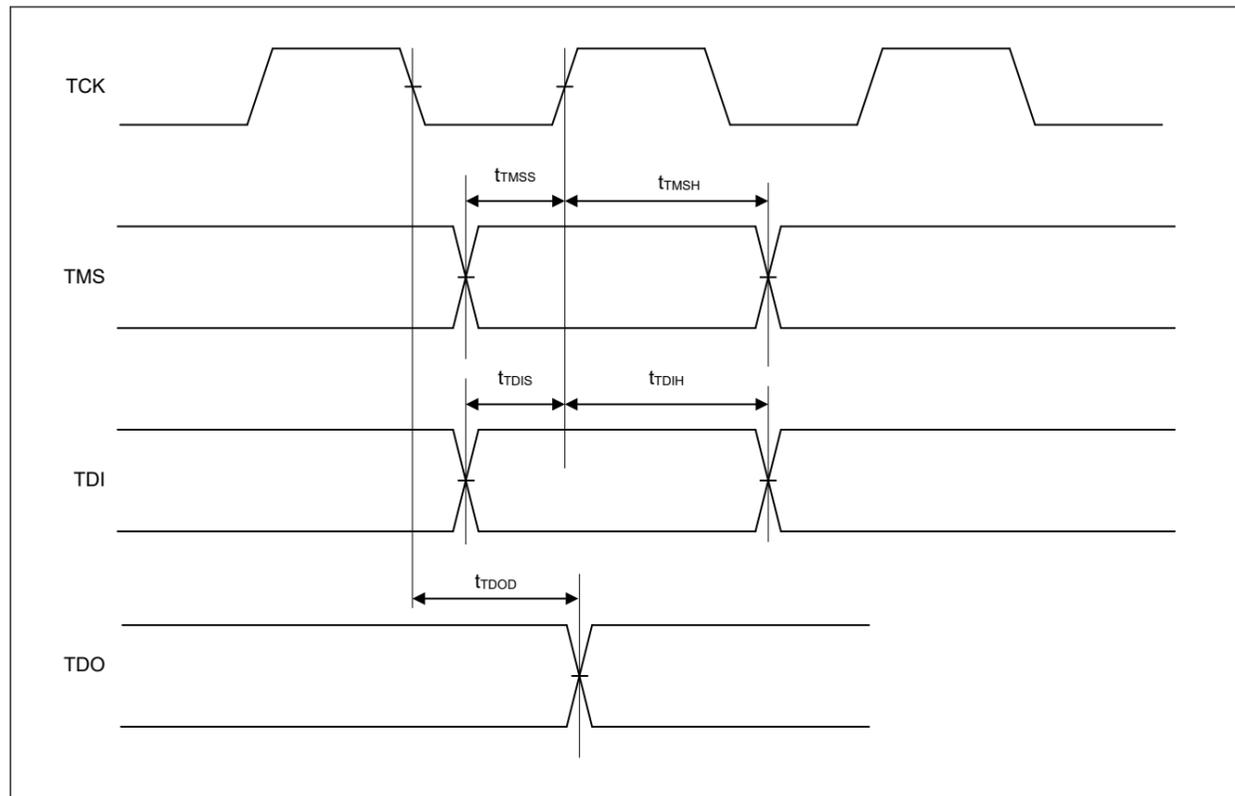


Figure 2.62 JTAG input/output timing

2.14 Serial Wire Debug (SWD)

Table 2.50 SWD

| Parameter                    | Symbol         | Min | Typ | Max | Unit | Test conditions |
|------------------------------|----------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time       | $t_{SWCLKcyc}$ | 40  | —   | —   | ns   | Figure 2.63     |
| SWCLK clock high pulse width | $t_{SWCKH}$    | 15  | —   | —   | ns   |                 |
| SWCLK clock low pulse width  | $t_{SWCKL}$    | 15  | —   | —   | ns   |                 |
| SWCLK clock rise time        | $t_{SWCKr}$    | —   | —   | 5   | ns   |                 |
| SWCLK clock fall time        | $t_{SWCKf}$    | —   | —   | 5   | ns   |                 |
| SWDIO setup time             | $t_{SWDS}$     | 8   | —   | —   | ns   | Figure 2.64     |
| SWDIO hold time              | $t_{SWDH}$     | 8   | —   | —   | ns   |                 |
| SWDIO data delay time        | $t_{SWDD}$     | 2   | —   | 28  | ns   |                 |

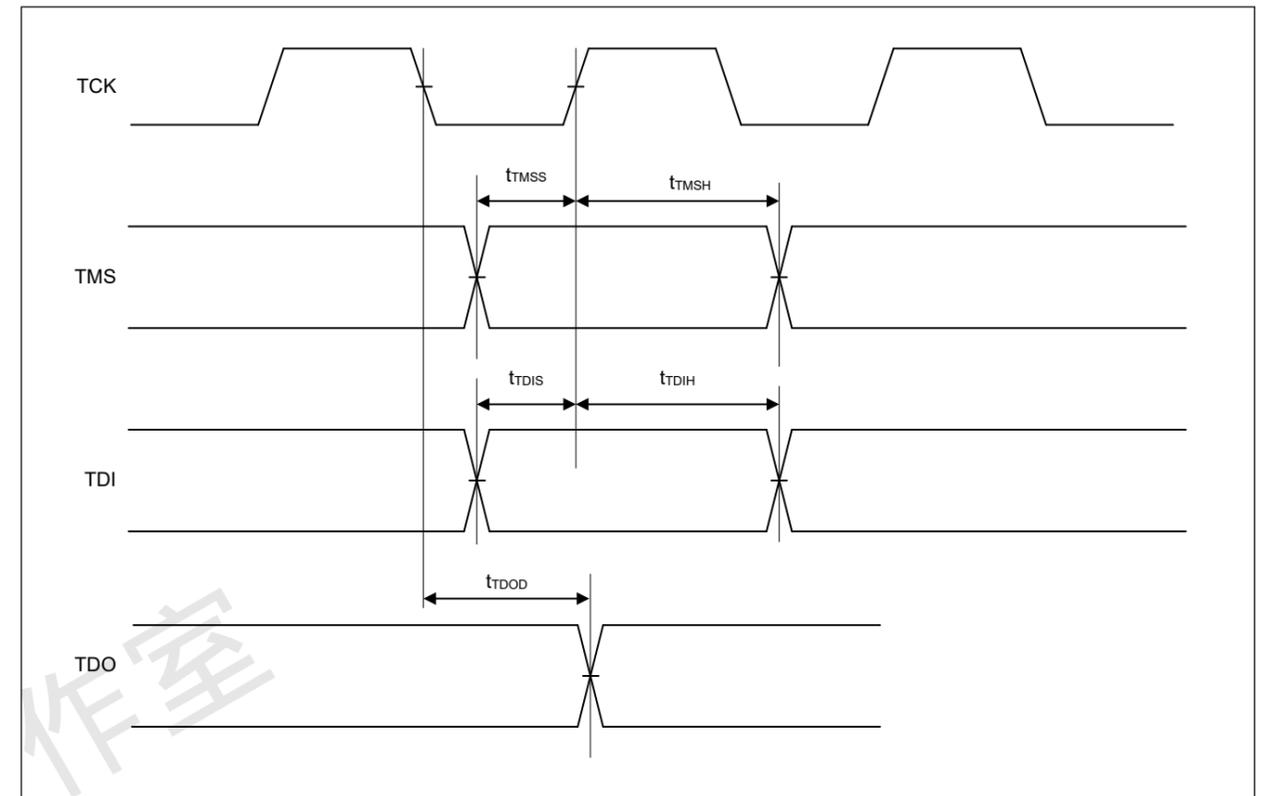


Figure 2.62 JTAG input/output timing

2.14 串行线调试(SWD)

Table 2.50 SWD

| Parameter    | Symbol         | Min | Typ | Max | Unit | 测试条件        |
|--------------|----------------|-----|-----|-----|------|-------------|
| SWCLK时钟周期时间  | $t_{SWCLKcyc}$ | 40  | —   | —   | ns   | Figure 2.63 |
| SWCLK时钟高脉冲宽度 | $t_{SWCKH}$    | 15  | —   | —   | ns   |             |
| SWCLK时钟低脉冲宽度 | $t_{SWCKL}$    | 15  | —   | —   | ns   |             |
| SWCLK时钟上升时间  | $t_{SWCKr}$    | —   | —   | 5   | ns   |             |
| SWCLK时钟下降时间  | $t_{SWCKf}$    | —   | —   | 5   | ns   |             |
| SWDIO设置时间    | $t_{SWDS}$     | 8   | —   | —   | ns   | Figure 2.64 |
| SWDIO保持时间    | $t_{SWDH}$     | 8   | —   | —   | ns   |             |
| SWDIO数据延迟时间  | $t_{SWDD}$     | 2   | —   | 28  | ns   |             |

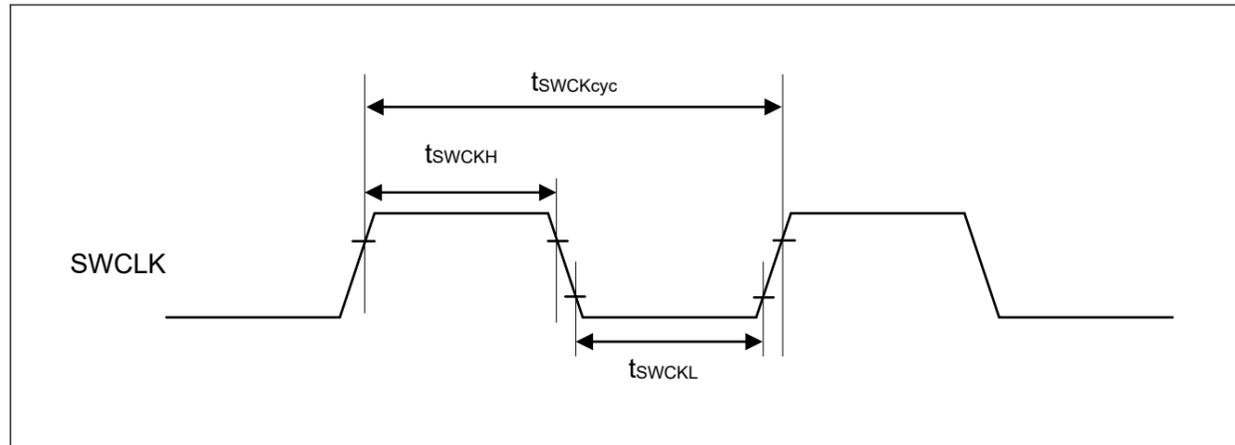


Figure 2.63 SWD SWCLK timing

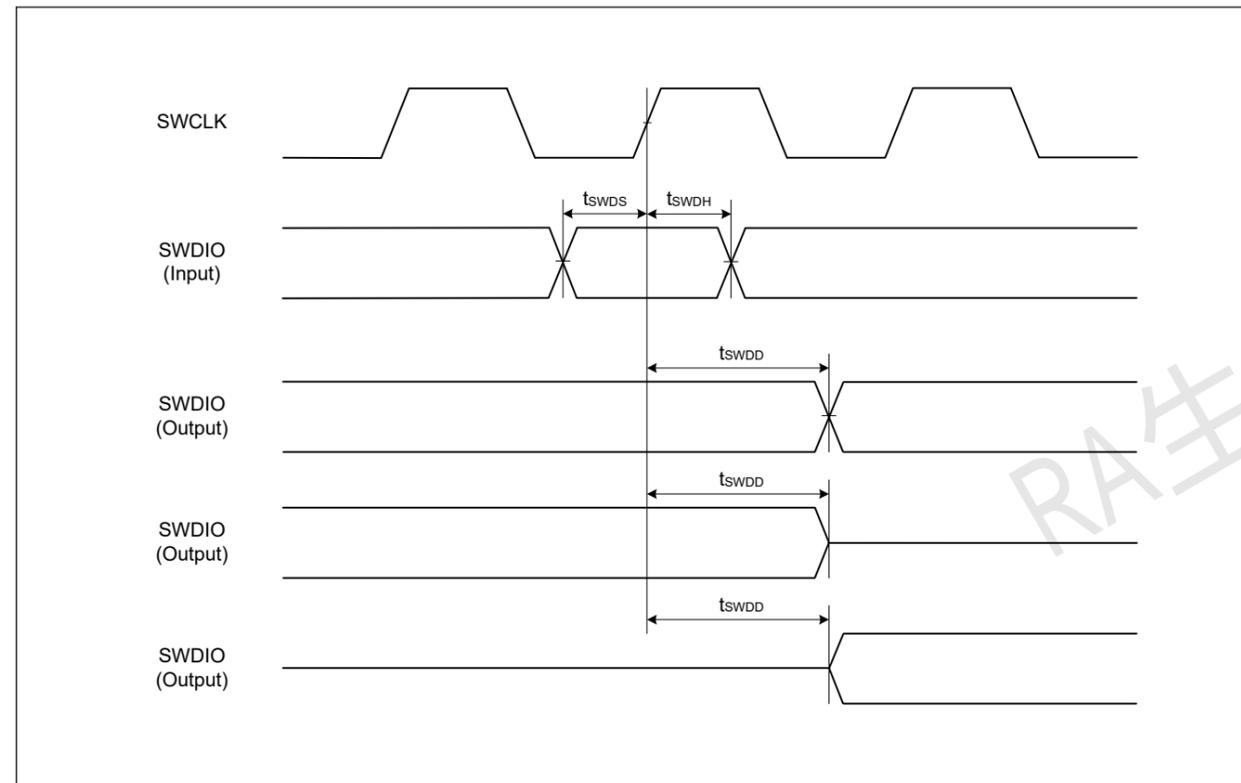


Figure 2.64 SWD input/output timing

2.15 Embedded Trace Macro Interface (ETM)

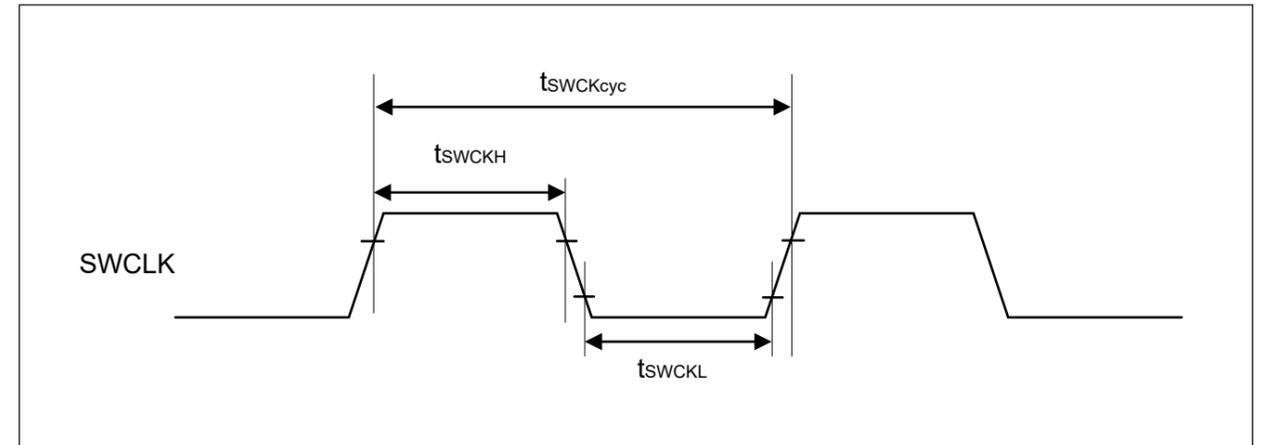


Figure 2.63 SWD SWCLK timing

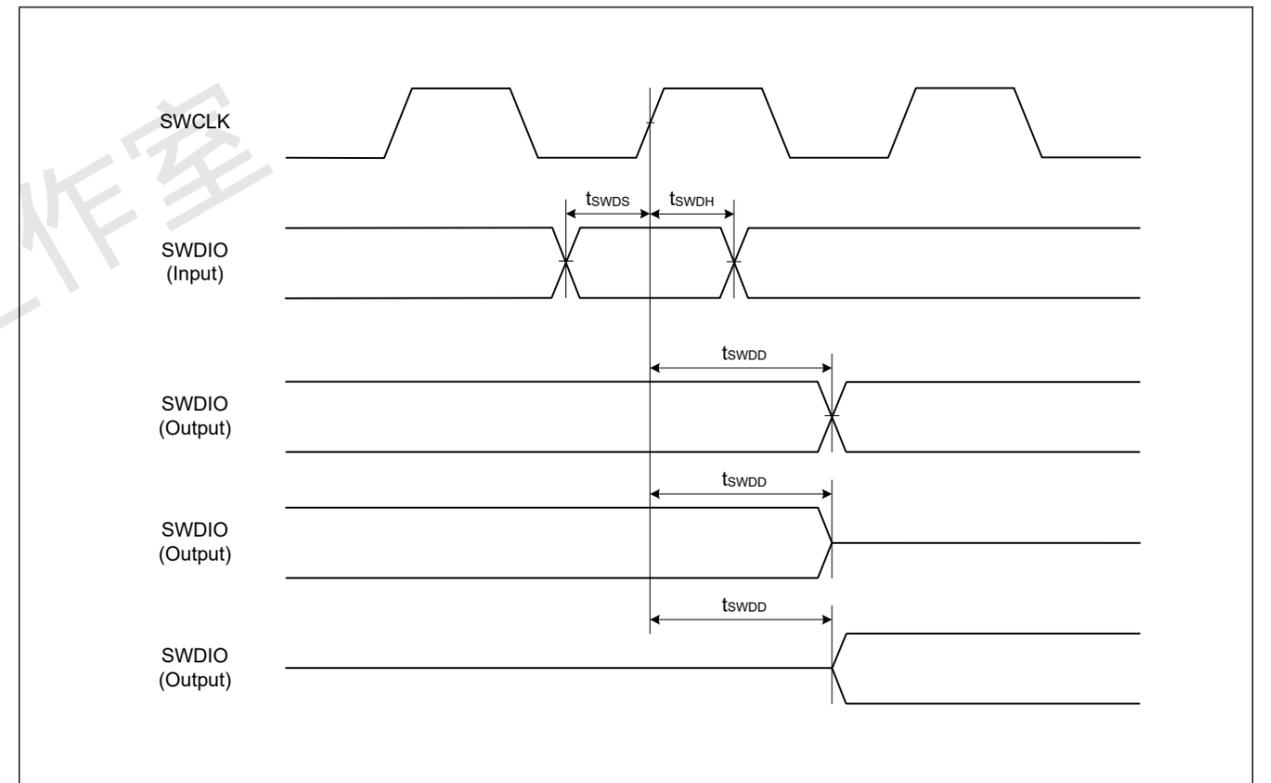


Figure 2.64 SWD input/output timing

2.15 嵌入式跟踪宏接口(ETM)

**Table 2.51 ETM**

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                    | Symbol        | Min  | Typ | Max | Unit | Test conditions |
|------------------------------|---------------|------|-----|-----|------|-----------------|
| TCLK clock cycle time        | $t_{TCLKcyc}$ | 16.7 | —   | —   | ns   | Figure 2.65     |
| TCLK clock high pulse width  | $t_{TCLKH}$   | 7.35 | —   | —   | ns   |                 |
| TCLK clock low pulse width   | $t_{TCLKL}$   | 7.35 | —   | —   | ns   |                 |
| TCLK clock rise time         | $t_{TCLKr}$   | —    | —   | 1   | ns   |                 |
| TCLK clock fall time         | $t_{TCLKf}$   | —    | —   | 1   | ns   |                 |
| TDATA[3:0] output setup time | $t_{TRDS}$    | 2.5  | —   | —   | ns   | Figure 2.66     |
| TDATA[3:0] output hold time  | $t_{TRDH}$    | 1.5  | —   | —   | ns   |                 |

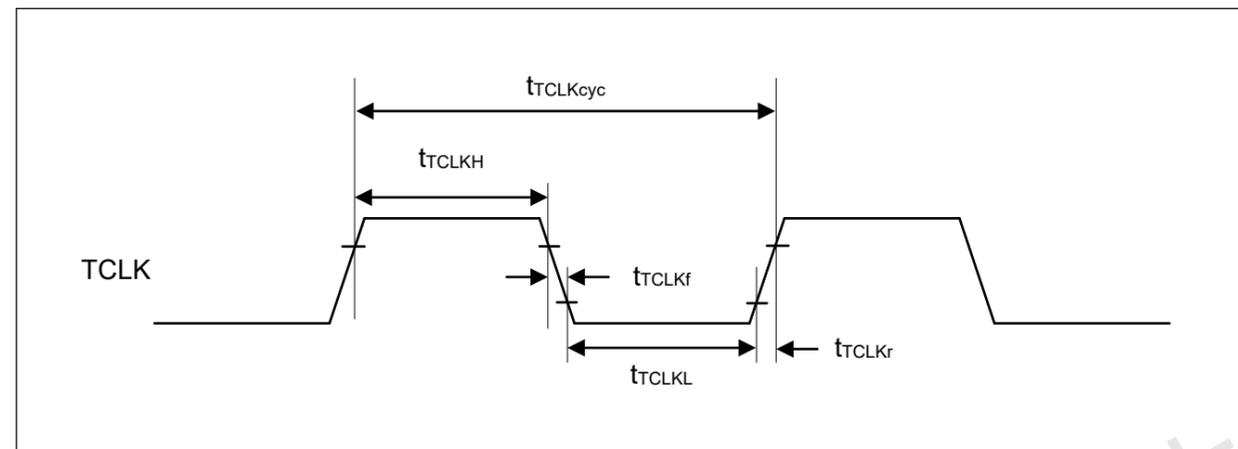


Figure 2.65 ETM TCLK timing

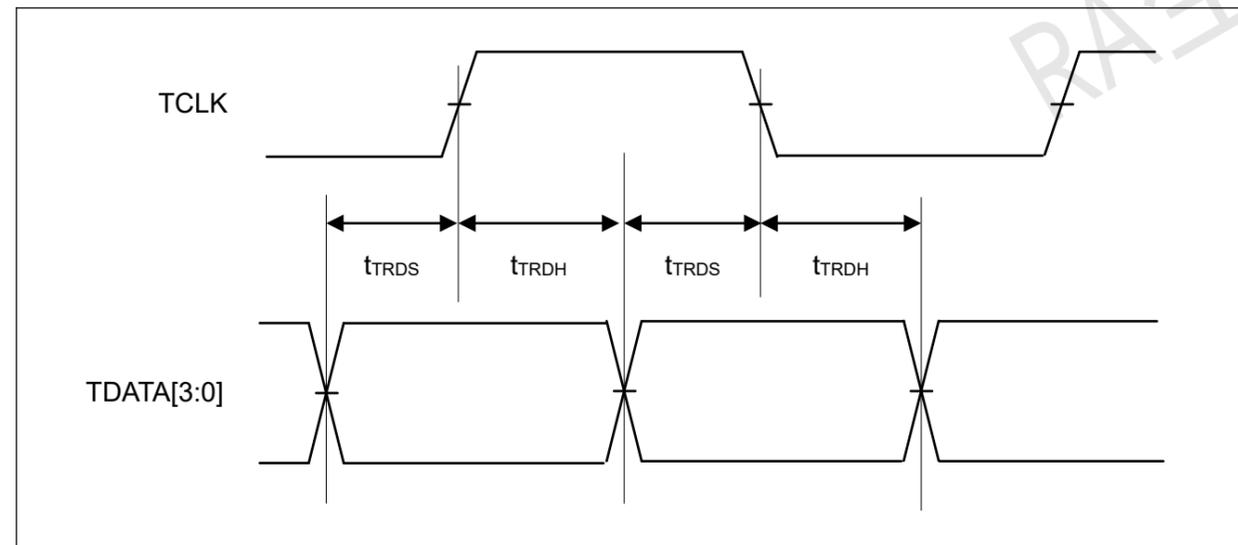


Figure 2.66 ETM output timing

**Table 2.51 ETM**

条件：在PmnPFS寄存器的端口驱动能力位中选择高速高驱动输出。

| Parameter        | Symbol        | Min  | Typ | Max | Unit | 测试条件        |
|------------------|---------------|------|-----|-----|------|-------------|
| TCLK时钟周期时间       | $t_{TCLKcyc}$ | 16.7 | —   | —   | ns   | Figure 2.65 |
| TCLK时钟高脉冲宽度      | $t_{TCLKH}$   | 7.35 | —   | —   | ns   |             |
| TCLK时钟低脉冲宽度      | $t_{TCLKL}$   | 7.35 | —   | —   | ns   |             |
| TCLK时钟上升时间       | $t_{TCLKr}$   | —    | —   | 1   | ns   |             |
| TCLK时钟下降时间       | $t_{TCLKf}$   | —    | —   | 1   | ns   |             |
| TDATA[3:0]输出建立时间 | $t_{TRDS}$    | 2.5  | —   | —   | ns   | Figure 2.66 |
| TDATA[3:0]输出保持时间 | $t_{TRDH}$    | 1.5  | —   | —   | ns   |             |

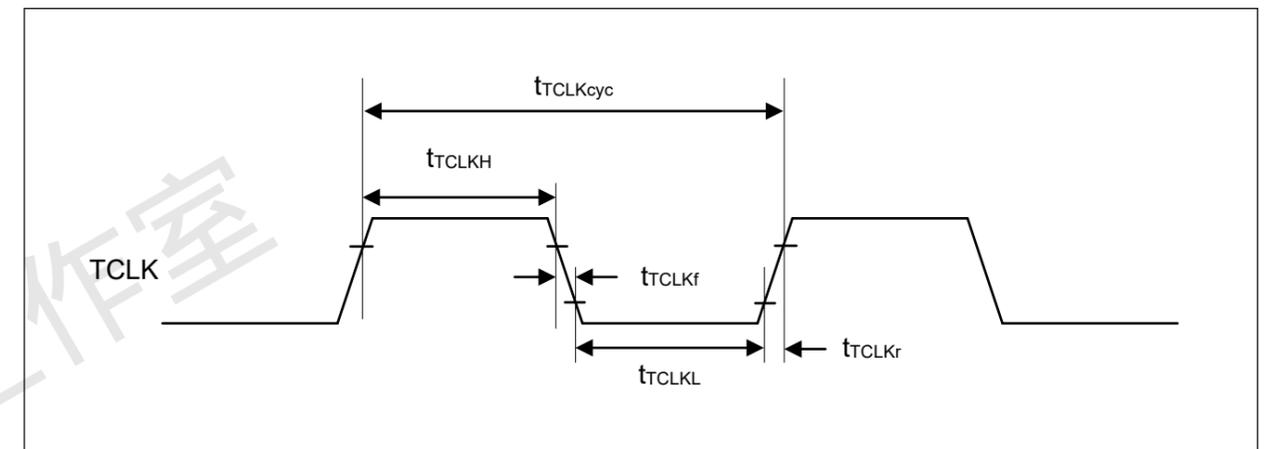


Figure 2.65 ETM TCLK timing

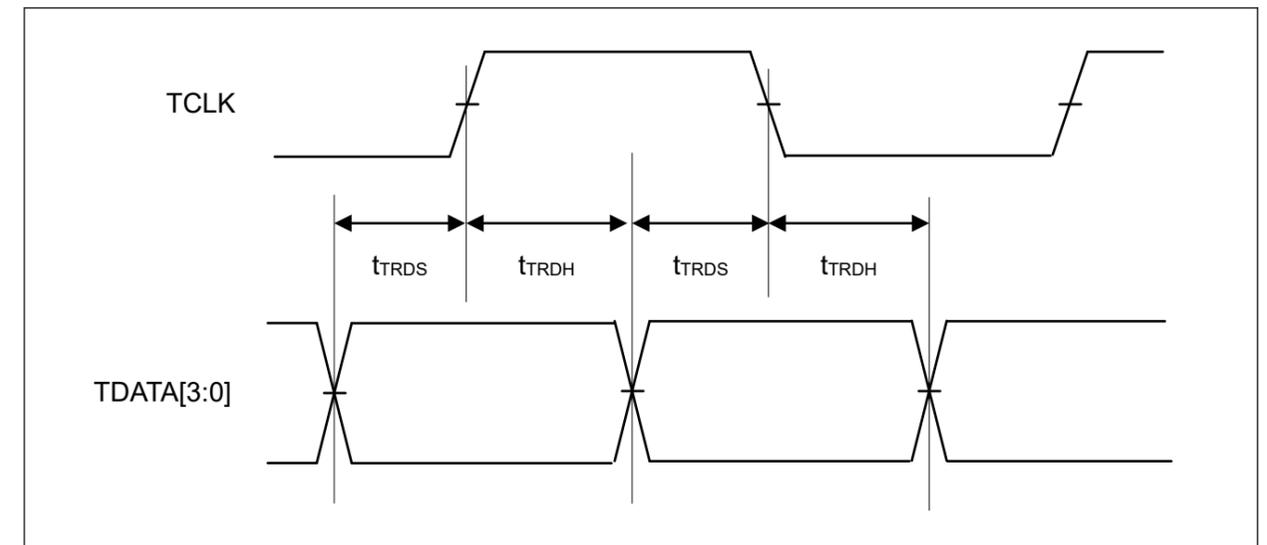


Figure 2.66 ETM输出时序

## Appendix 1. Port States in Each Processing Mode

| Function | Pin function                              | Reset                 | Software Standby mode                                      | Deep Software Standby mode   | After Deep Software Standby mode is canceled (return to startup mode) |                              |
|----------|---|-----------------------|--|------------------------------|---|------------------------------|
|          |   |                       |  |                              | IOKEEP = 0  | IOKEEP = 1 <sup>*1</sup>     |
| Mode     | MD  | Pull-up               | Keep-O   | Keep                         | Hi-Z  | Keep                         |
| JTAG     | TCK/TMS/TDI                               | Pull-up               | Keep-O   | Keep                         | Hi-Z  | Keep                         |
|          | TDO                                       | TDO output            | Keep-O   | Keep                         | TDO output  | Keep                         |
| Trace    | TCLK/TDATAx                               | Hi-Z                  | Keep-O   | Keep                         | Hi-Z  | Keep                         |
| IRQ      | IRQx                                      | Hi-Z                  | Keep-O <sup>*2</sup>                                       | Keep                         | Hi-Z  | Keep                         |
|          | IRQx-DS                                   | Hi-Z                  | Keep-O <sup>*2</sup>                                       | Keep <sup>*3</sup>           | Hi-Z  | Keep                         |
| KINT     | KRxx                                      | Hi-Z                  | Keep-O <sup>*2</sup>                                       | Keep                         | Hi-Z  | Keep                         |
| AGT      | AGTIO <sub>n</sub>                        | Hi-Z                  | Keep-O <sup>*2</sup>                                       | Keep                         | Hi-Z  | Keep                         |
| IIC      | SCL <sub>n</sub> /SDA <sub>n</sub>        | Hi-Z                  | Keep-O <sup>*2</sup>                                       | Keep                         | Hi-Z  | Keep                         |
| CLKOUT   | CLKOUT                                    | Hi-Z                  | [CLKOUT selected]<br>CLKOUT output                         | Keep                         | Hi-Z  | Keep                         |
| ACMPHS   | VCOUT, CMPOUT <sub>m</sub> ,<br>CMPOUT012 | Hi-Z                  | Hi-Z (Keep-O)  | Hi-Z (Keep-O)                | Hi-Z  | Keep                         |
|          | IVREF <sub>n</sub>                        | Hi-Z                  | Hi-Z (Keep-O)  | Hi-Z (Keep-O)                | Hi-Z  | Hi-Z                         |
|          | IVCMP <sub>m</sub>                        | Hi-Z                  | Hi-Z (Keep-O)  | Hi-Z (Keep-O)                | Hi-Z  | Hi-Z                         |
| DAC12    | DA <sub>n</sub>                           | Hi-Z                  | [DA <sub>n</sub> output (DAOE = 1)]<br>D/A output retained | Keep                         | Hi-Z  | Keep                         |
| ADC      | AN <sub>xxx</sub>                         | Hi-Z                  | Hi-Z   | Hi-Z                         | Hi-Z  | Hi-Z                         |
|          | PGAIN <sub>n</sub>                        | Hi-Z                  | Hi-Z   | Hi-Z                         | Hi-Z  | Hi-Z                         |
|          | PGA <sub>VSSn</sub>                       | Pull-up <sup>*4</sup> | Pull-up <sup>*5</sup> / Keep                               | Pull-up <sup>*5</sup> / Keep | Pull-up <sup>*5</sup> / Keep  | Pull-up <sup>*5</sup> / Keep |
|          | PGAOUT <sub>n</sub>                       | Hi-Z                  | Hi-Z   | Hi-Z                         | Hi-Z  | Hi-Z                         |
| Others   | —   | Hi-Z                  | Keep-O   | Keep                         | Hi-Z  | Keep                         |

Note: H: High-level  
L: Low-level  
Hi-Z: High-impedance  
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.  
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.

Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.

Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Note 4. The built-in pull-up is turned on to protect the circuit from negative potential inputs.

Note 5. Regardless of whether the PGA is enabled or disabled, when the PGA is set to pseudo-differential mode, the built-in pull-up is turned on to protect the circuit from negative potential inputs. To turn off the built-in pull-up, turn off the PGA's pseudo-differential mode and set it to single mode.

## Appendix 1. 每种处理模式下的端口状态

| Function | 引脚功能                                      | Reset                 | 软件待机模式                                 | 深度软件待机模式                     | 取消深度软件待机模式后 (返回启动模式)         |                              |
|----------|---|-----------------------|--|------------------------------|------------------------------|------------------------------|
|          |   |                       |  |                              | IOKEEP = 0                   | IOKEEP = 1 <sup>*1</sup>     |
| Mode     | MD  | Pull-up               | Keep-O                                 | Keep                         | Hi-Z                         | Keep                         |
| JTAG     | TCK/TMS/TDI                               | Pull-up               | Keep-O                                 | Keep                         | Hi-Z                         | Keep                         |
|          | TDO                                       | TDO输出                 | Keep-O                                 | Keep                         | TDO输出                        | Keep                         |
| Trace    | TCLK/TDATAx                               | Hi-Z                  | Keep-O                                 | Keep                         | Hi-Z                         | Keep                         |
| IRQ      | IRQx                                      | Hi-Z                  | Keep-O <sup>*2</sup>                   | Keep                         | Hi-Z                         | Keep                         |
|          | IRQx-DS                                   | Hi-Z                  | Keep-O <sup>*2</sup>                   | Keep <sup>*3</sup>           | Hi-Z                         | Keep                         |
| KINT     | KRxx                                      | Hi-Z                  | Keep-O <sup>*2</sup>                   | Keep                         | Hi-Z                         | Keep                         |
| AGT      | AGTIO <sub>n</sub>                        | Hi-Z                  | Keep-O <sup>*2</sup>                   | Keep                         | Hi-Z                         | Keep                         |
| IIC      | SCL <sub>n</sub> /SDA <sub>n</sub>        | Hi-Z                  | Keep-O <sup>*2</sup>                   | Keep                         | Hi-Z                         | Keep                         |
| CLKOUT   | CLKOUT                                    | Hi-Z                  | [CLKOUT selected]<br>CLKOUT output     | Keep                         | Hi-Z                         | Keep                         |
| ACMPHS   | VCOUT, CMPOUT <sub>m</sub> ,<br>CMPOUT012 | Hi-Z                  | Hi-Z (Keep-O)                          | Hi-Z (Keep-O)                | Hi-Z                         | Keep                         |
|          | IVREF <sub>n</sub>                        | Hi-Z                  | Hi-Z (Keep-O)                          | Hi-Z (Keep-O)                | Hi-Z                         | Hi-Z                         |
|          | IVCMP <sub>m</sub>                        | Hi-Z                  | Hi-Z (Keep-O)                          | Hi-Z (Keep-O)                | Hi-Z                         | Hi-Z                         |
| DAC12    | DA <sub>n</sub>                           | Hi-Z                  | [DA <sub>n</sub> 输出(DAOE=1)]DA<br>输出保留 | Keep                         | Hi-Z                         | Keep                         |
| ADC      | AN <sub>xxx</sub>                         | Hi-Z                  | Hi-Z                                   | Hi-Z                         | Hi-Z                         | Hi-Z                         |
|          | PGAIN <sub>n</sub>                        | Hi-Z                  | Hi-Z                                   | Hi-Z                         | Hi-Z                         | Hi-Z                         |
|          | PGA <sub>VSSn</sub>                       | Pull-up <sup>*4</sup> | Pull-up <sup>*5</sup> / Keep           | Pull-up <sup>*5</sup> / Keep | Pull-up <sup>*5</sup> / Keep | Pull-up <sup>*5</sup> / Keep |
|          | PGAOUT <sub>n</sub>                       | Hi-Z                  | Hi-Z                                   | Hi-Z                         | Hi-Z                         | Hi-Z                         |
| Others   | —   | Hi-Z                  | Keep-O                                 | Keep                         | Hi-Z                         | Keep                         |

Note: H: High-level  
L: Low-level  
Hi-Z: High-impedance  
Keep-O: 输出引脚保留其先前的值。输入引脚变为高阻抗。  
保持: 在软件待机模式期间保持引脚状态。

注1. 保持IO端口状态直到DPSBYCR.IOKEEP位被清除为0。

注2. 如果引脚被指定为软件待机取消源, 同时它被用作外部中断引脚, 则输入被启用。

注3. 如果引脚被指定为深度软件待机取消源, 则启用输入。

注4. 内置上拉电阻打开以保护电路免受负电位输入的影响。

注5. 无论PGA启用还是禁用, 当PGA设置为伪差分模式时, 内置上拉电阻会打开以保护电路免受负电位输入的影响。要关闭内置上拉, 关闭PGA的伪差分模式并将其设置为单模式。

### Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in Packages on the Renesas Electronics Corporation website.

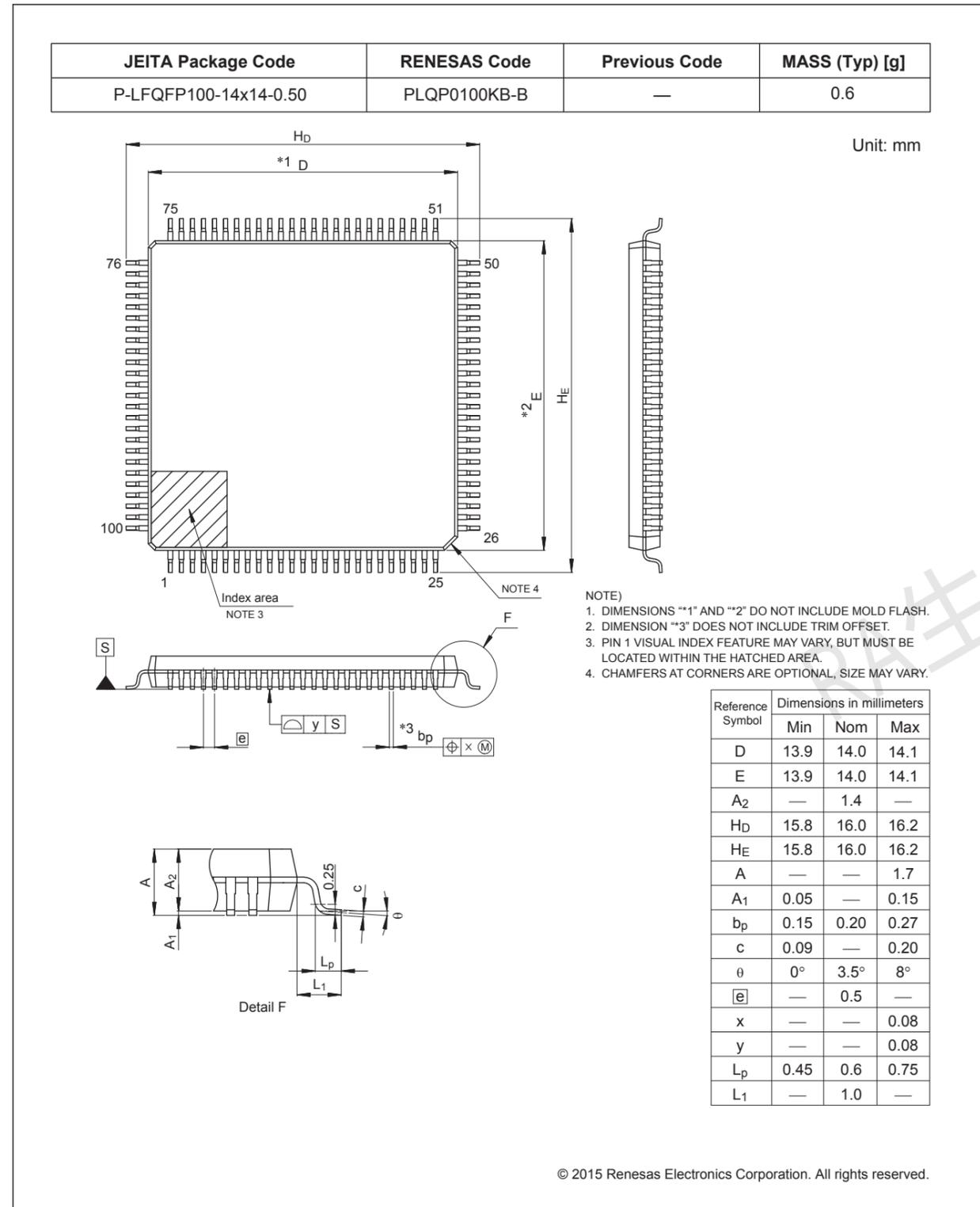


Figure 2.1 LQFP 100-pin

### Appendix 2. 包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨的封装中电子公司网站。

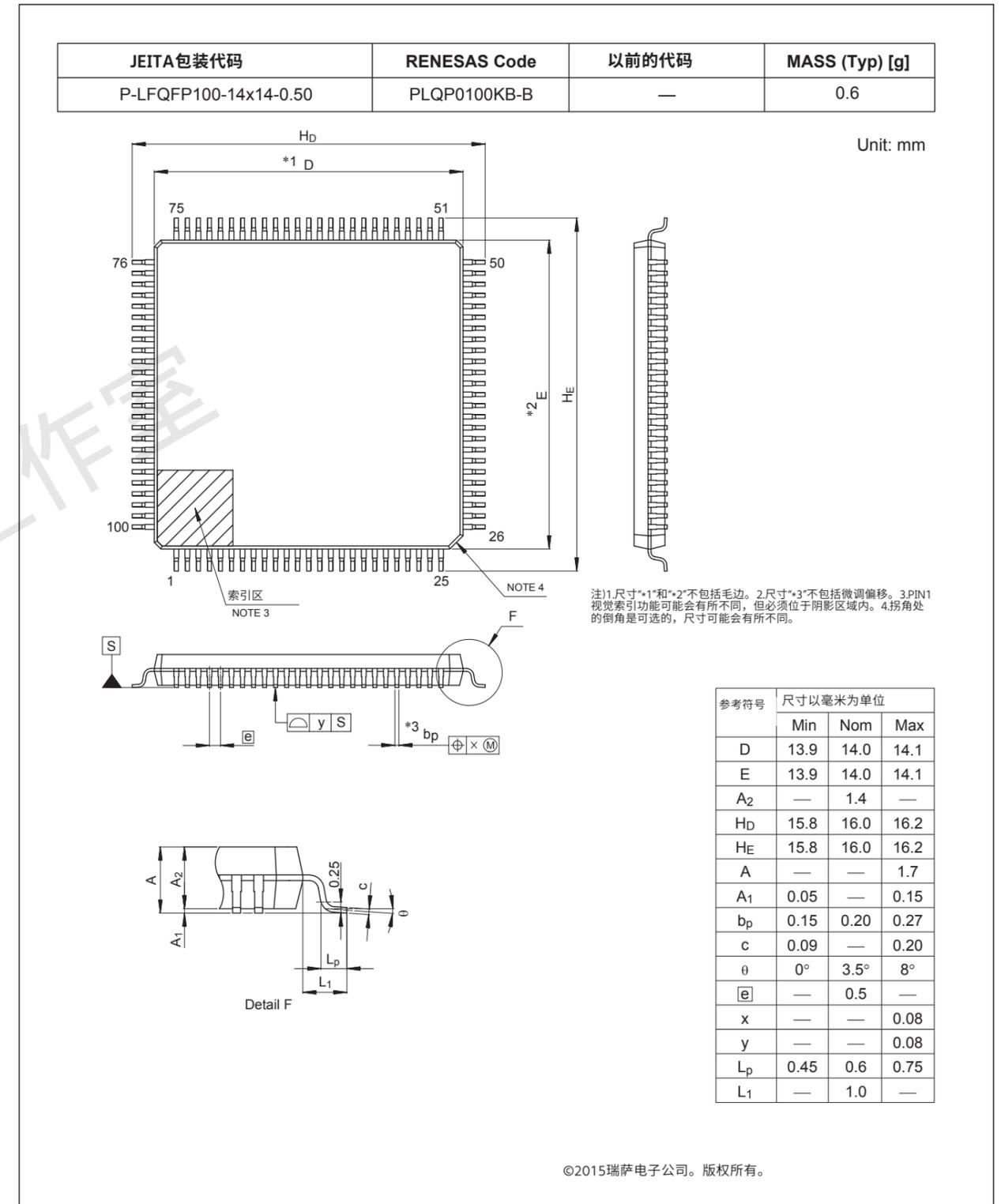
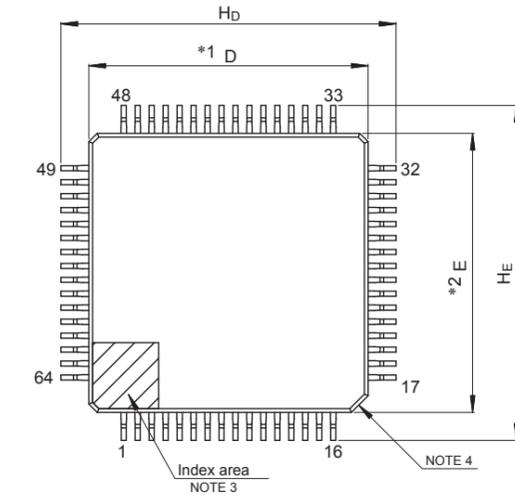


Figure 2.1 LQFP 100-pin

| JEITA Package Code   | RENESAS Code | Previous Code | MASS (Typ) [g] |
|----------------------|--------------|---------------|----------------|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | —             | 0.3            |

Unit: mm



- NOTE)
1. DIMENSIONS "1" AND "2" DO NOT INCLUDE MOLD FLASH.
  2. DIMENSION "3" DOES NOT INCLUDE TRIM OFFSET.
  3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
  4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

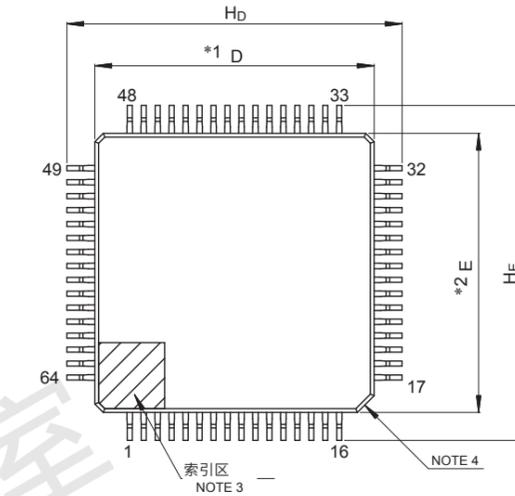
| Reference Symbol | Dimensions in millimeters |      |      |
|------------------|---------------------------|------|------|
|                  | Min                       | Nom  | Max  |
| D                | 9.9                       | 10.0 | 10.1 |
| E                | 9.9                       | 10.0 | 10.1 |
| A <sub>2</sub>   | —                         | 1.4  | —    |
| H <sub>D</sub>   | 11.8                      | 12.0 | 12.2 |
| H <sub>E</sub>   | 11.8                      | 12.0 | 12.2 |
| A                | —                         | —    | 1.7  |
| A <sub>1</sub>   | 0.05                      | —    | 0.15 |
| b <sub>p</sub>   | 0.15                      | 0.20 | 0.27 |
| c                | 0.09                      | —    | 0.20 |
| θ                | 0°                        | 3.5° | 8°   |
| e                | —                         | 0.5  | —    |
| x                | —                         | —    | 0.08 |
| y                | —                         | —    | 0.08 |
| L <sub>p</sub>   | 0.45                      | 0.6  | 0.75 |
| L <sub>1</sub>   | —                         | 1.0  | —    |

© 2015 Renesas Electronics Corporation. All rights reserved.

Figure 2.2 LQFP 64-pin

| JEITA 包装代码           | RENESAS Code | 以前的代码 | MASS (Typ) [g] |
|----------------------|--------------|-------|----------------|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | —     | 0.3            |

Unit: mm



- 注)1.尺寸"1"和"2"不包括毛边。2.尺寸"3"不包括微调偏移。3.PIN1 视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

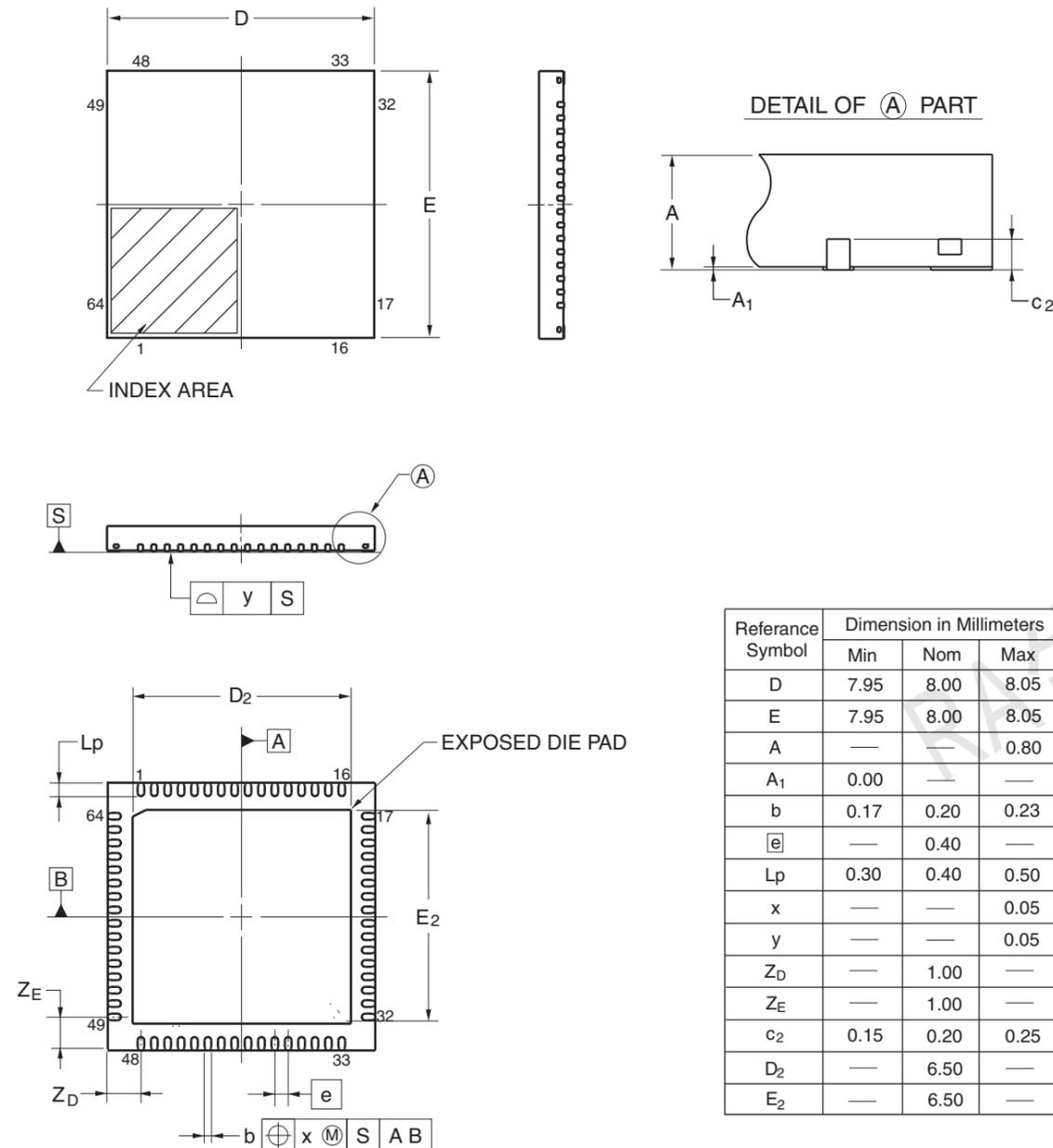
| 参考符号           | 尺寸以毫米为单位 |      |      |
|----------------|----------|------|------|
|                | Min      | Nom  | Max  |
| D              | 9.9      | 10.0 | 10.1 |
| E              | 9.9      | 10.0 | 10.1 |
| A <sub>2</sub> | —        | 1.4  | —    |
| H <sub>D</sub> | 11.8     | 12.0 | 12.2 |
| H <sub>E</sub> | 11.8     | 12.0 | 12.2 |
| A              | —        | —    | 1.7  |
| A <sub>1</sub> | 0.05     | —    | 0.15 |
| b <sub>p</sub> | 0.15     | 0.20 | 0.27 |
| c              | 0.09     | —    | 0.20 |
| θ              | 0°       | 3.5° | 8°   |
| e              | —        | 0.5  | —    |
| x              | —        | —    | 0.08 |
| y              | —        | —    | 0.08 |
| L <sub>p</sub> | 0.45     | 0.6  | 0.75 |
| L <sub>1</sub> | —        | 1.0  | —    |

©2015瑞萨电子公司。版权所有。

Figure 2.2 LQFP 64-pin

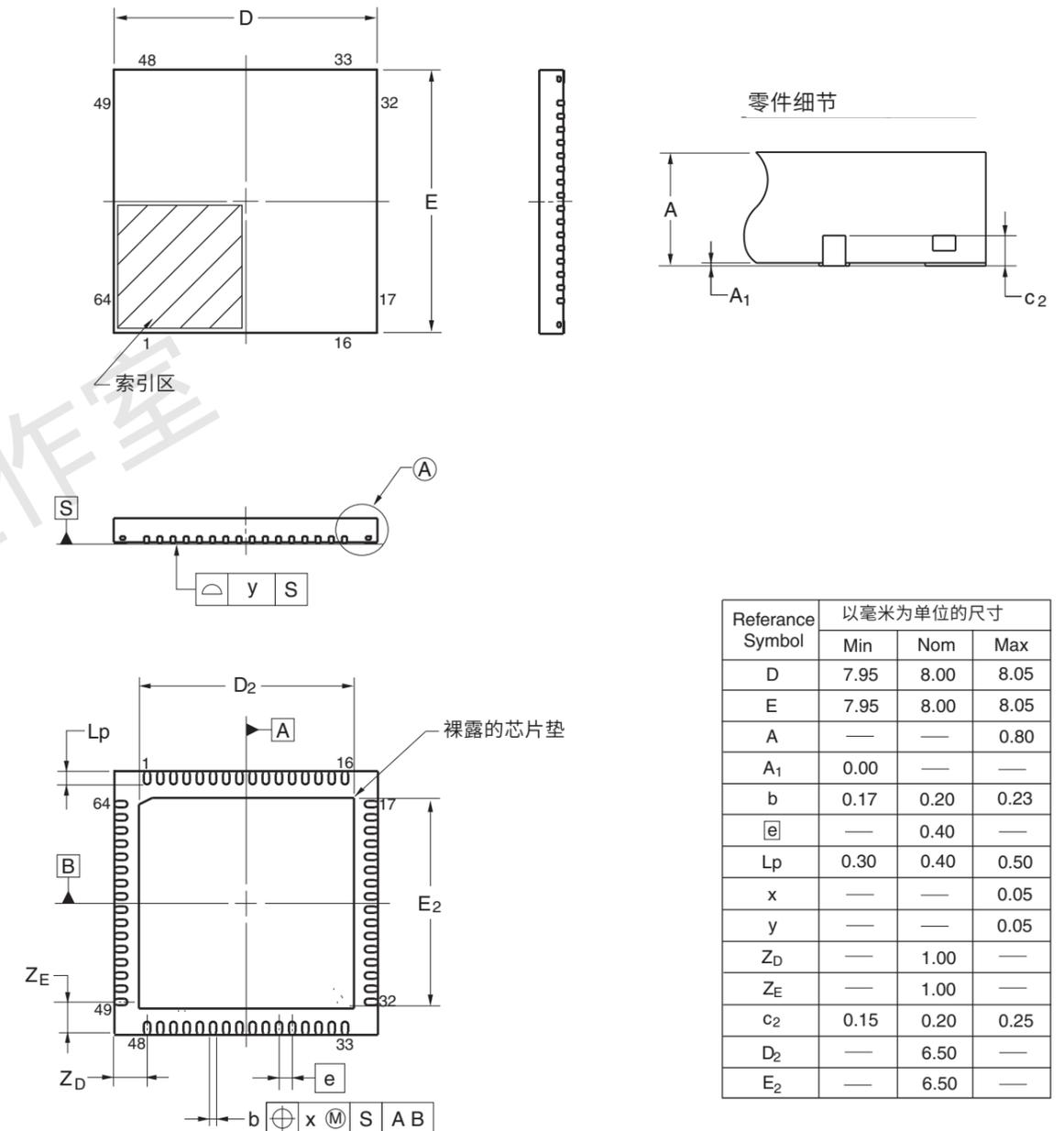
| JEITA Package code | RENESAS code | Previous code  | MASS(TYP.)[g] |
|--------------------|--------------|----------------|---------------|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-3 | 0.16          |

| JEITA包装代码          | RENESAS code | 以前的代码          | MASS(TYP.)[g] |
|--------------------|--------------|----------------|---------------|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-3 | 0.16          |



©2013 Renesas Electronics Corporation. All rights reserved.

Figure 2.3 QFN 64-pin



©2013瑞萨电子公司。版权所有。

Figure 2.3 QFN 64-pin

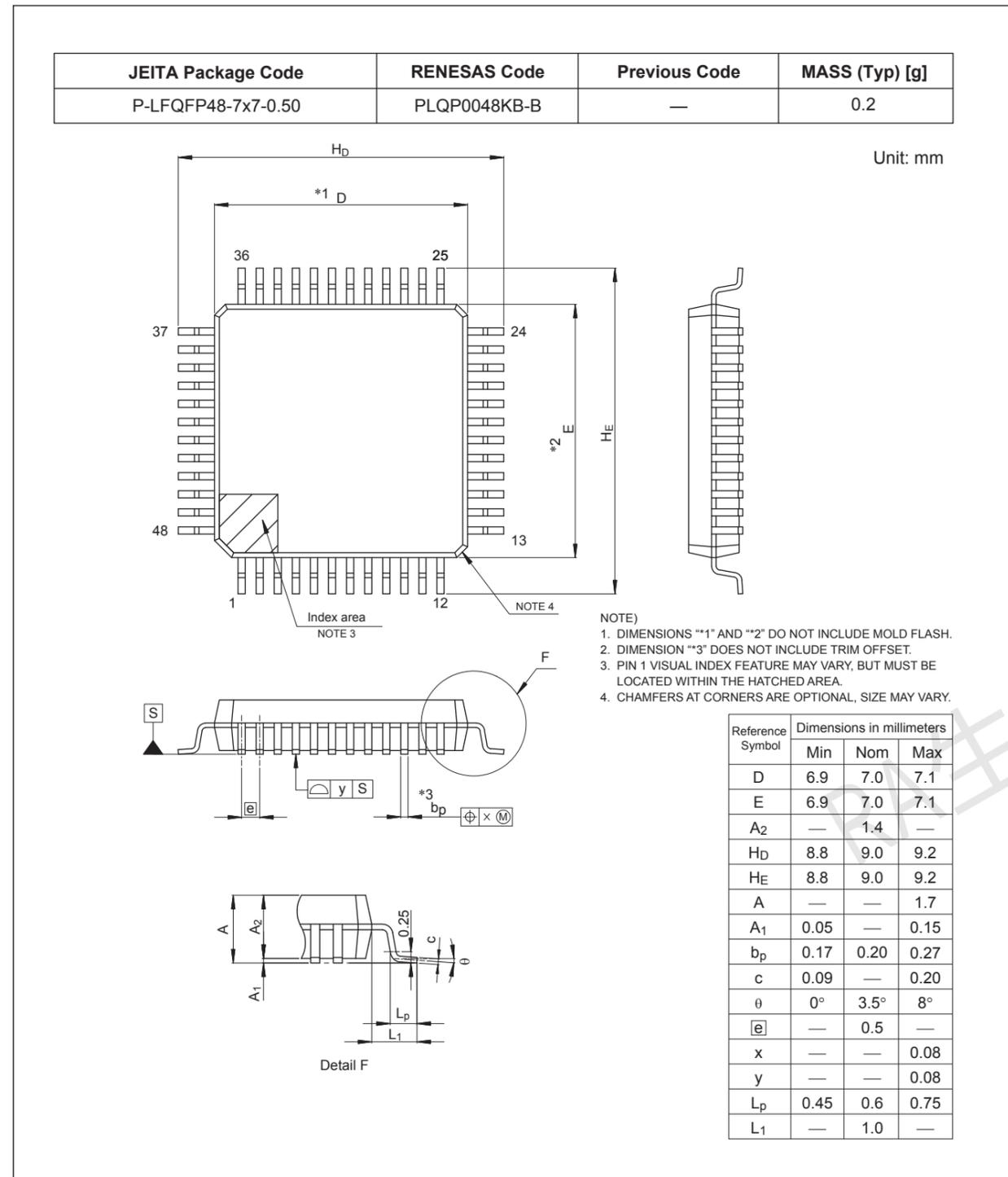


Figure 2.4 LQFP 48-pin

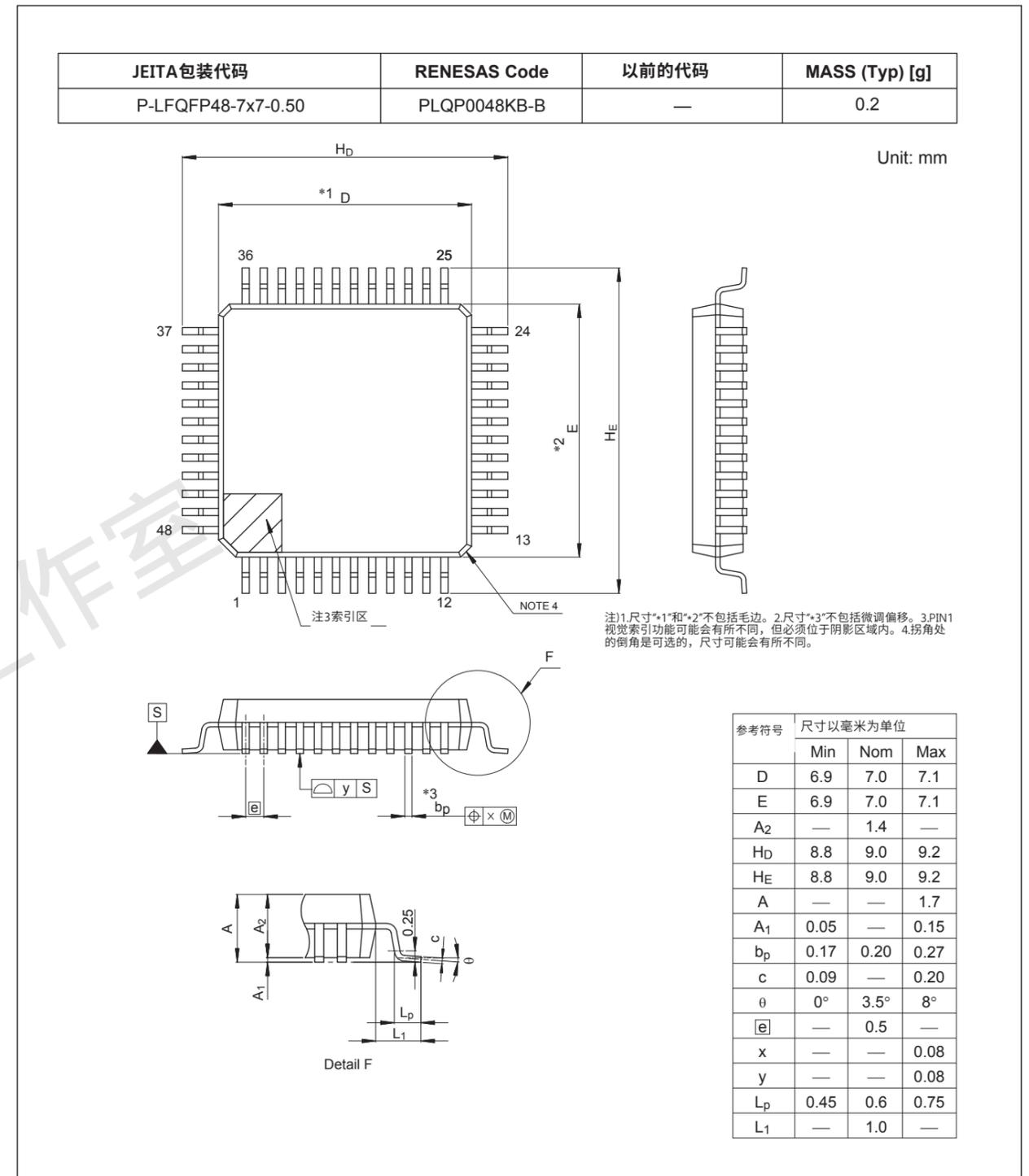


Figure 2.4 LQFP 48-pin

©2015瑞萨电子公司。版权所有。

| JEITA Package code | RENESAS code | Previous code             | MASS(TYP.)[g] |
|--------------------|--------------|---------------------------|---------------|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13          |

| JEITA包装代码          | RENESAS code | 以前的代码                     | MASS(TYP.)[g] |
|--------------------|--------------|---------------------------|---------------|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13          |

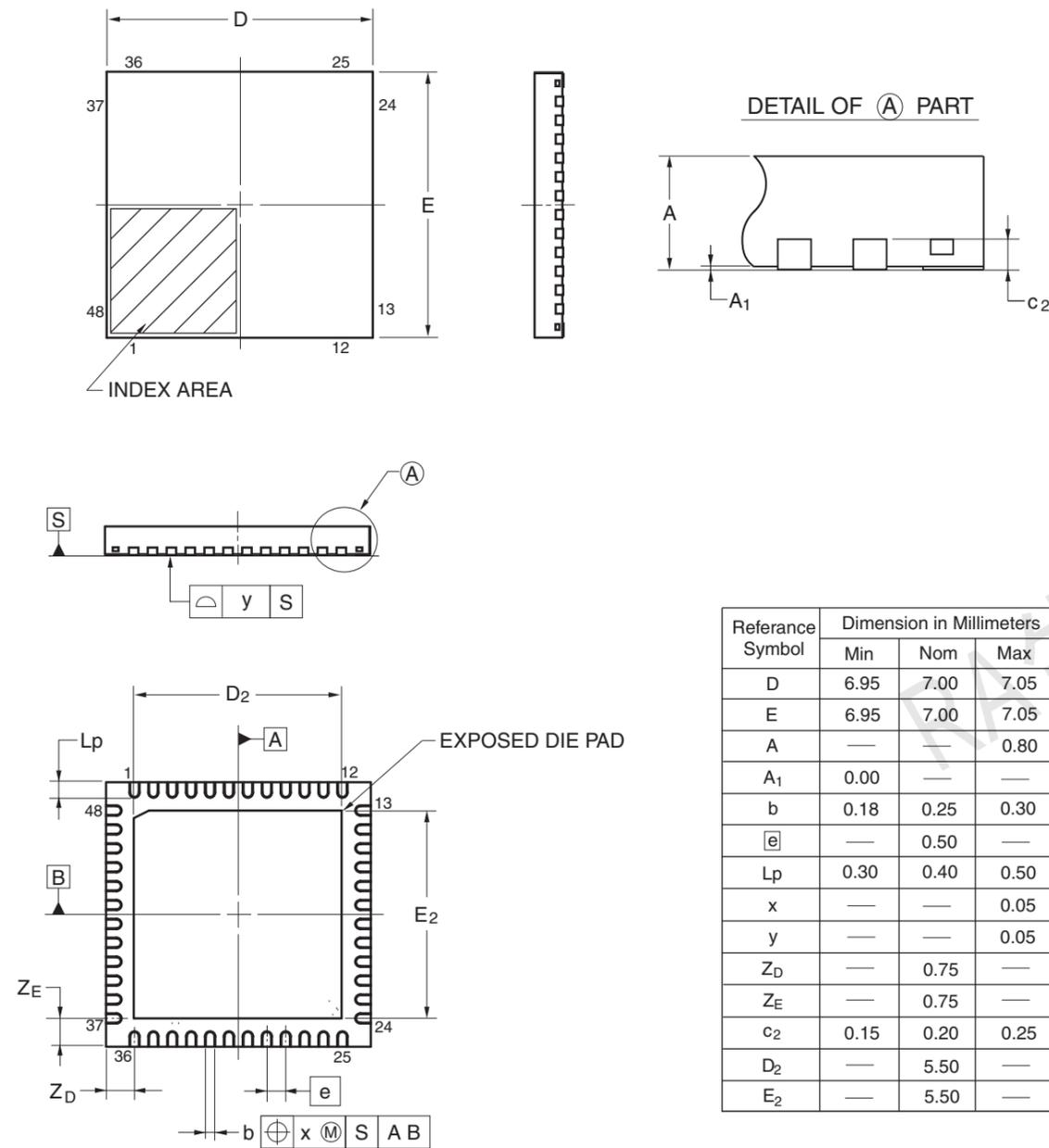


Figure 2.5 QFN 48-pin

© 2013 Renesas Electronics Corporation. All rights reserved.

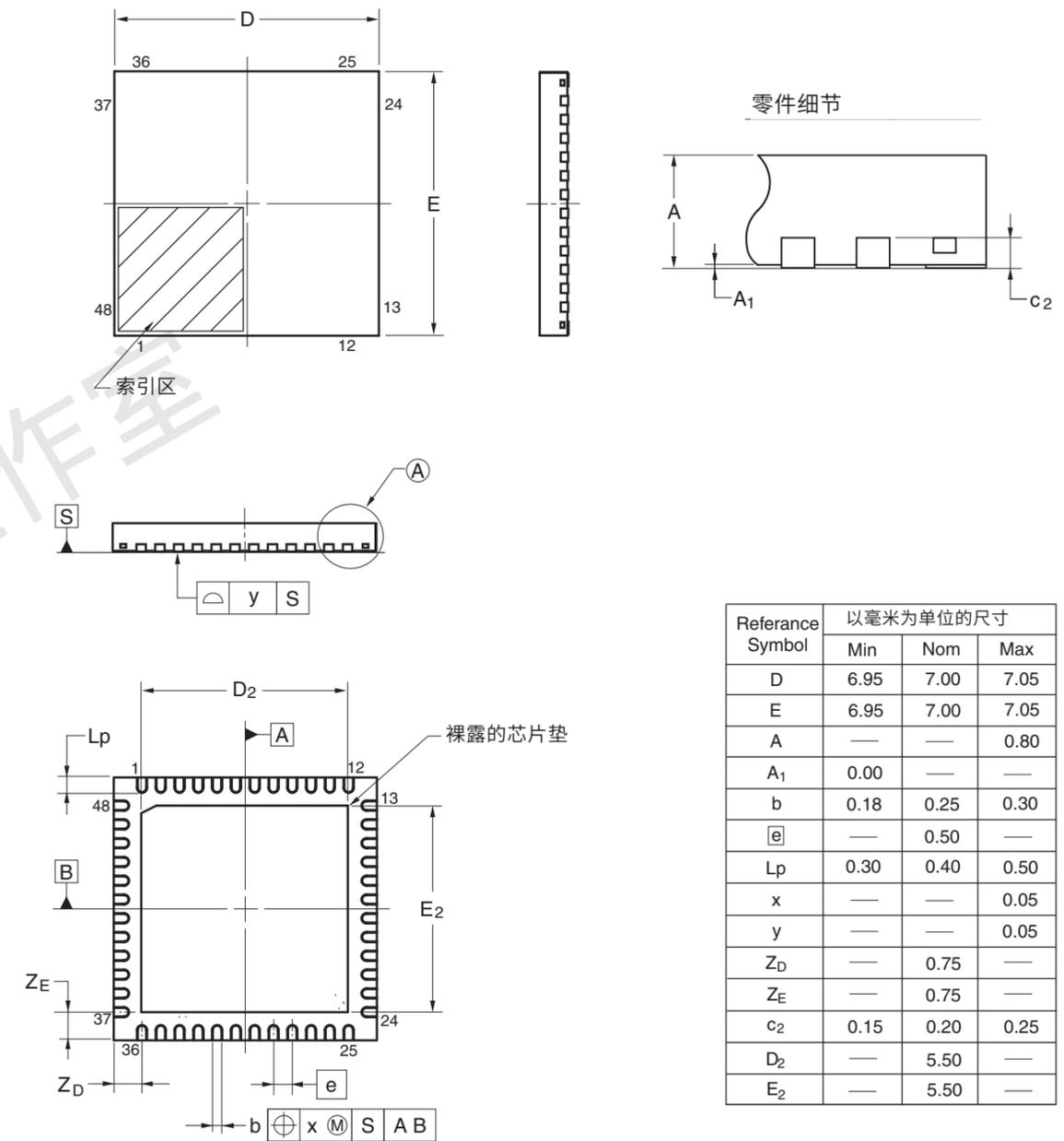


Figure 2.5 QFN 48-pin

© 2013 瑞萨电子公司。版权所有。

## Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

### 3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

**Table 3.1 Peripheral base address (1 of 3)**

| Name   | Description                                  | Base address |
|--------|--|--------------|
| RMPU   | Renesas Memory Protection Unit               | 0x4000_0000  |
| TZF    | TrustZone Filter                             | 0x4000_0E00  |
| SRAM   | SRAM Control                                 | 0x4000_2000  |
| BUS    | BUS Control                                  | 0x4000_3000  |
| DMAC0  | Direct memory access controller 0            | 0x4000_5000  |
| DMAC1  | Direct memory access controller 1            | 0x4000_5040  |
| DMAC2  | Direct memory access controller 2            | 0x4000_5080  |
| DMAC3  | Direct memory access controller 3            | 0x4000_50C0  |
| DMAC4  | Direct memory access controller 4            | 0x4000_5100  |
| DMAC5  | Direct memory access controller 5            | 0x4000_5140  |
| DMAC6  | Direct memory access controller 6            | 0x4000_5180  |
| DMAC7  | Direct memory access controller 7            | 0x4000_51C0  |
| DMA    | DMAC Module Activation                       | 0x4000_5200  |
| DTC    | Data Transfer Controller                     | 0x4000_5400  |
| ICU    | Interrupt Controller                         | 0x4000_6000  |
| CACHE  | CACHE  | 0x4000_7000  |
| CPSCU  | CPU System Security Control Unit             | 0x4000_8000  |
| DBG    | Debug Function                               | 0x4001_B000  |
| FCACHE | Flash Cache                                  | 0x4001_C100  |
| SYSC   | System Control                               | 0x4001_E000  |
| PORT0  | Port 0 Control Registers                     | 0x4001_F000  |
| PORT2  | Port 2 Control Registers                     | 0x4001_F040  |
| PORTA  | Port A Control Registers                     | 0x4001_F140  |
| PORTB  | Port B Control Registers                     | 0x4001_F160  |
| PORTC  | Port C Control Registers                     | 0x4001_F180  |
| PORTD  | Port D Control Registers                     | 0x4001_F1A0  |
| PORTE  | Port E Control Registers                     | 0x4001_F1C0  |
| PFS_B  | Pmn Pin Function Control Register            | 0x4001_F800  |
| IIRFA  | IIR Filter Accelerator                       | 0x4002_0000  |
| TFU    | Trigonometric Function Unit                  | 0x4002_1000  |
| ELC_B  | Event Link Controller                        | 0x4008_2000  |
| IWDT   | Independent Watchdog Timer                   | 0x4008_3200  |
| WDT    | Watchdog Timer                               | 0x4008_3400  |
| CAC    | Clock Frequency Accuracy Measurement Circuit | 0x4008_3600  |
| MSTP   | Module Stop Control A, B, C, D, E            | 0x4008_4000  |

## Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址和访问周期。

### 3.1 外设基地址

本节提供本手册中描述的外设的基地址。表3.1显示了每个外设的名称、描述和基地址。

**Table 3.1 外设基地址(1of3)**

| Name   | Description      | 基址          |
|--------|------------------|-------------|
| RMPU   | 瑞萨内存保护单元         | 0x4000_0000 |
| TZF    | TrustZone Filter | 0x4000_0E00 |
| SRAM   | SRAM Control     | 0x4000_2000 |
| BUS    | 总线控制             | 0x4000_3000 |
| DMAC0  | 直接内存访问控制器0       | 0x4000_5000 |
| DMAC1  | 直接内存访问控制器1       | 0x4000_5040 |
| DMAC2  | 直接内存访问控制器2       | 0x4000_5080 |
| DMAC3  | 直接内存访问控制器3       | 0x4000_50C0 |
| DMAC4  | 直接内存访问控制器4       | 0x4000_5100 |
| DMAC5  | 直接内存访问控制器5       | 0x4000_5140 |
| DMAC6  | 直接内存访问控制器6       | 0x4000_5180 |
| DMAC7  | 直接内存访问控制器7       | 0x4000_51C0 |
| DMA    | DMAC模块激活         | 0x4000_5200 |
| DTC    | 数据传输控制器          | 0x4000_5400 |
| ICU    | 中断控制器            | 0x4000_6000 |
| CACHE  | CACHE            | 0x4000_7000 |
| CPSCU  | CPU系统安全控制单元      | 0x4000_8000 |
| DBG    | 调试功能             | 0x4001_B000 |
| FCACHE | 闪存缓存             | 0x4001_C100 |
| SYSC   | 系统控制             | 0x4001_E000 |
| PORT0  | 端口0控制寄存器         | 0x4001_F000 |
| PORT2  | 端口2控制寄存器         | 0x4001_F040 |
| PORTA  | 端口A控制寄存器         | 0x4001_F140 |
| PORTB  | 端口B控制寄存器         | 0x4001_F160 |
| PORTC  | 端口C控制寄存器         | 0x4001_F180 |
| PORTD  | 端口D控制寄存器         | 0x4001_F1A0 |
| PORTE  | 端口E控制寄存器         | 0x4001_F1C0 |
| PFS_B  | Pmn引脚功能控制寄存器     | 0x4001_F800 |
| IIRFA  | IIR滤波器加速器        | 0x4002_0000 |
| TFU    | 三角函数单元           | 0x4002_1000 |
| ELC_B  | 事件链接控制器          | 0x4008_2000 |
| IWDT   | 独立看门狗定时器         | 0x4008_3200 |
| WDT    | 看门狗定时器           | 0x4008_3400 |
| CAC    | 时钟频率精度测量电路       | 0x4008_3600 |
| MSTP   | 模块停止控制A、B、C、D、E  | 0x4008_4000 |

Table 3.1 Peripheral base address (2 of 3)

| Name      | Description                                    | Base address |
|-----------|--|--------------|
| KINT      | Key Interrupt Function                         | 0x4008_5000  |
| POEG      | Port Output Enable for GPT                     | 0x4008_A000  |
| IIC0WU_B  | Inter-Integrated Circuit 0 Wake-up Unit        | 0x4009_F098  |
| CANFD_B   | CANFD Module Control                           | 0x400B_0000  |
| PSCU      | Peripheral Security Control Unit               | 0x400E_0000  |
| AGTW_B0   | Low Power Asynchronous General purpose Timer 0 | 0x400E_8000  |
| AGTW_B1   | Low Power Asynchronous General purpose Timer 1 | 0x400E_8100  |
| TSN       | Temperature Sensor                             | 0x400F_3000  |
| ACMPHS0   | High-Speed Analog Comparator                   | 0x400F_4000  |
| ACMPHS1   | High-Speed Analog Comparator                   | 0x400F_4100  |
| ACMPHS2   | High-Speed Analog Comparator                   | 0x400F_4200  |
| ACMPHS3   | High-Speed Analog Comparator                   | 0x400F_4300  |
| CRC       | Cyclic Redundancy Check                        | 0x4010_8000  |
| DOC_B     | Data Operation Circuit                         | 0x4010_9000  |
| SCI_B0    | Serial Communication Interface 0               | 0x4011_8000  |
| SCI_B1    | Serial Communication Interface 1               | 0x4011_8100  |
| SCI_B2    | Serial Communication Interface 2               | 0x4011_8200  |
| SCI_B3    | Serial Communication Interface 3               | 0x4011_8300  |
| SCI_B4    | Serial Communication Interface 4               | 0x4011_8400  |
| SCI_B9    | Serial Communication Interface 9               | 0x4011_8900  |
| SPI_B0    | Serial Peripheral Interface 0                  | 0x4011_A000  |
| SPI_B1    | Serial Peripheral Interface 1                  | 0x4011_A100  |
| IIC_B0    | Inter-Integrated Circuit 0                     | 0x4011_F000  |
| IIC_B1    | Inter-Integrated Circuit 1                     | 0x4011_F400  |
| ECCMB     | CANFD ECC Module                               | 0x4012_F200  |
| SCE5_B    | Secure Cryptographic Engine                    | 0x4016_1000  |
| GPT0      | General PWM Timer 0                            | 0x4016_9000  |
| GPT1      | General PWM Timer 1                            | 0x4016_9100  |
| GPT2      | General PWM Timer 2                            | 0x4016_9200  |
| GPT3      | General PWM Timer 3                            | 0x4016_9300  |
| GPT4      | General PWM Timer 4                            | 0x4016_9400  |
| GPT5      | General PWM Timer 5                            | 0x4016_9500  |
| GPT6      | General PWM Timer 6                            | 0x4016_9600  |
| GPT7      | General PWM Timer 7                            | 0x4016_9700  |
| GPT8      | General PWM Timer 8                            | 0x4016_9800  |
| GPT9      | General PWM Timer 9                            | 0x4016_9900  |
| GPT_OPS   | Output Phase Switching Controller              | 0x4016_9A00  |
| GPT_GTCLK | General PWM Timer                              | 0x4016_9B00  |
| PDG       | PWM Delay Generation                           | 0x4016_A000  |
| ADC_B     | 12-Bit A/D Converter                           | 0x4017_0000  |
| DAC120    | 12-bit D/A converter                           | 0x4017_2000  |
| DAC121    | 12-bit D/A converter                           | 0x4017_2100  |

Table 3.1 外设基地址 (2个, 共3个)

| Name      | Description                | 基址          |
|-----------|----------------------------|-------------|
| KINT      | 按键中断功能                     | 0x4008_5000 |
| POEG      | GPT的端口输出使能                 | 0x4008_A000 |
| IIC0WU_B  | 内部集成电路0唤醒单元                | 0x4009_F098 |
| CANFD_B   | CANFD模块控制                  | 0x400B_0000 |
| PSCU      | 外围安全控制单元                   | 0x400E_0000 |
| AGTW_B0   | 低功耗异步通用定时器0                | 0x400E_8000 |
| AGTW_B1   | 低功耗异步通用定时器1                | 0x400E_8100 |
| TSN       | 温度感应器                      | 0x400F_3000 |
| ACMPHS0   | 高速模拟比较器                    | 0x400F_4000 |
| ACMPHS1   | 高速模拟比较器                    | 0x400F_4100 |
| ACMPHS2   | 高速模拟比较器                    | 0x400F_4200 |
| ACMPHS3   | 高速模拟比较器                    | 0x400F_4300 |
| CRC       | 循环冗余校验                     | 0x4010_8000 |
| DOC_B     | 数据运算电路                     | 0x4010_9000 |
| SCI_B0    | 串行通讯接口0                    | 0x4011_8000 |
| SCI_B1    | 串行通讯接口1                    | 0x4011_8100 |
| SCI_B2    | 串行通讯接口2                    | 0x4011_8200 |
| SCI_B3    | 串行通讯接口3                    | 0x4011_8300 |
| SCI_B4    | 串行通讯接口4                    | 0x4011_8400 |
| SCI_B9    | 串行通讯接口9                    | 0x4011_8900 |
| SPI_B0    | 串行外设接口0                    | 0x4011_A000 |
| SPI_B1    | 串行外设接口1                    | 0x4011_A100 |
| IIC_B0    | Inter-Integrated Circuit 0 | 0x4011_F000 |
| IIC_B1    | Inter-Integrated Circuit 1 | 0x4011_F400 |
| ECCMB     | CANFD ECC Module           | 0x4012_F200 |
| SCE5_B    | 安全加密引擎                     | 0x4016_1000 |
| GPT0      | 通用PWM定时器0                  | 0x4016_9000 |
| GPT1      | 通用PWM定时器1                  | 0x4016_9100 |
| GPT2      | 通用PWM定时器2                  | 0x4016_9200 |
| GPT3      | 通用PWM定时器3                  | 0x4016_9300 |
| GPT4      | 通用PWM定时器4                  | 0x4016_9400 |
| GPT5      | 通用PWM定时器5                  | 0x4016_9500 |
| GPT6      | 通用PWM定时器6                  | 0x4016_9600 |
| GPT7      | 通用PWM定时器7                  | 0x4016_9700 |
| GPT8      | 通用PWM定时器8                  | 0x4016_9800 |
| GPT9      | 通用PWM定时器9                  | 0x4016_9900 |
| GPT_OPS   | 输出相位切换控制器                  | 0x4016_9A00 |
| GPT_GTCLK | 通用PWM定时器                   | 0x4016_9B00 |
| PDG       | PWM延迟生成                    | 0x4016_A000 |
| ADC_B     | 12-Bit A/D Converter       | 0x4017_0000 |
| DAC120    | 12-bit D/A converter       | 0x4017_2000 |
| DAC121    | 12-bit D/A converter       | 0x4017_2100 |

Table 3.1 Peripheral base address (3 of 3)

| Name | Description                         | Base address |
|------|-------------------------------------|--------------|
| FLAD | Data Flash                          | 0x407F_C000  |
| FACI | Flash Application Command Interface | 0x407F_E000  |

Note: Name = Peripheral name  
Description = Peripheral functionality  
Base address = Lowest reserved address or address used by the peripheral

### 3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

| Peripherals                                | Address     |             | Number of access cycles |       |                           |        | Cycle Unit | Related function   |
|--|-------------|-------------|-------------------------|-------|---------------------------|--------|------------|--|
|  |             |             | ICLK = PCLK             |       | ICLK > PCLK <sup>*1</sup> |        |            |  |
|  |             |             | Read                    | Write | Read                      | Write  |            |  |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 4                       | 3     | 4                         | 3      | ICLK       | Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller |
| CACHE                                      | 0x4000_7000 | 0x4000_7FFF | 4                       | 5     | 4                         | 5      | ICLK       | CACHE  |
| CPSCU, DBG, FCACHE                         | 0x4000_8000 | 0x4001_CFFF | 4                       | 3     | 4                         | 3      | ICLK       | CPU System Security Control Unit, Debug Function, Flash Cache  |
| SYSC                                       | 0x4001_E000 | 0x4001_E3FF | 5                       | 4     | 5                         | 4      | ICLK       | System Control   |
| SYSC                                       | 0x4001_E400 | 0x4001_E5FF | 9                       | 8     | 5 to 8                    | 5 to 8 | PCLKB      | System Control   |
| PORTn                                      | 0x4001_F000 | 0x4001_F7FF | 5                       | 3     | 5                         | 3      | ICLK       | PORTn Control Register 1/3/4   |
| PORTn (PCNTR2)                             | 0x4001_F000 | 0x4001_F7FF | 8                       | 3     | 8                         | 3      | ICLK       | PORTn Control Register 2   |
| PFS  | 0x4001_F800 | 0x4001_FFFF | 8                       | 3     | 8                         | 3      | ICLK       | Pmn Pin Function Control Register  |
| IIRFA                                      | 0x4002_0000 | 0x4002_03FF | 4                       | 3     | 4                         | 3      | ICLK       | IIR Filter Accelerator   |
| IIRFA                                      | 0x4002_0400 | 0x4002_0FFF | 6                       | 3     | 6                         | 3      | ICLK       | IIR Filter Accelerator   |

Table 3.1 外设基地址(3of3)

| Name | Description | 基址          |
|------|-------------|-------------|
| FLAD | 数据闪存        | 0x407F_C000 |
| FACI | Flash应用命令接口 | 0x407F_E000 |

Note: 名称=外设名称  
描述=外围功能  
基址=外设使用的最低保留地址或地址

### 3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

- 寄存器按相关模块分组。
- 访问周期数是指基于指定参考时钟的周期数。
- 在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。
- IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。
- 当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。
- 当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。
- 写访问周期数是指非缓冲写访问所获得的周期数。

Note: 这适用于当来自CPU的访问与来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 访问周期(1of3)

| Peripherals                                | Address     |             | 访问周期数       |       |                           |        | Cycle Unit | 相关功能   |
|--|-------------|-------------|-------------|-------|---------------------------|--------|------------|--|
|  |             |             | ICLK = PCLK |       | ICLK > PCLK <sup>*1</sup> |        |            |  |
|  |             |             | Read        | Write | Read                      | Write  |            |  |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 4           | 3     | 4                         | 3      | ICLK       | 瑞萨内存保护单元、TrustZone过滤器、SRAM控制、总线控制、直接内存访问控制器n、DMAC模块激活、DTC控制寄存器、中断控制器 |
| CACHE                                      | 0x4000_7000 | 0x4000_7FFF | 4           | 5     | 4                         | 5      | ICLK       | CACHE  |
| CPSCU, DBG, FCACHE                         | 0x4000_8000 | 0x4001_CFFF | 4           | 3     | 4                         | 3      | ICLK       | CPU系统安全控制单元，调试功能，闪存  |
| SYSC                                       | 0x4001_E000 | 0x4001_E3FF | 5           | 4     | 5                         | 4      | ICLK       | 系统控制   |
| SYSC                                       | 0x4001_E400 | 0x4001_E5FF | 9           | 8     | 5 to 8                    | 5 to 8 | PCLKB      | 系统控制   |
| PORTn                                      | 0x4001_F000 | 0x4001_F7FF | 5           | 3     | 5                         | 3      | ICLK       | PORTn控制寄存器134  |
| PORTn (PCNTR2)                             | 0x4001_F000 | 0x4001_F7FF | 8           | 3     | 8                         | 3      | ICLK       | PORTn Control Register 2   |
| PFS  | 0x4001_F800 | 0x4001_FFFF | 8           | 3     | 8                         | 3      | ICLK       | Pmn引脚功能控制寄存器   |
| IIRFA                                      | 0x4002_0000 | 0x4002_03FF | 4           | 3     | 4                         | 3      | ICLK       | IIR滤波器加速器  |
| IIRFA                                      | 0x4002_0400 | 0x4002_0FFF | 6           | 3     | 6                         | 3      | ICLK       | IIR滤波器加速器  |

Table 3.2 Access cycles (2 of 3)

| Peripherals                         | Address     |             | Number of access cycles |       |                           |        | Cycle Unit | Related function   |
|-------------------------------------|-------------|-------------|-------------------------|-------|---------------------------|--------|------------|--|
|                                     |             |             | ICLK = PCLK             |       | ICLK > PCLK <sup>*1</sup> |        |            |  |
|                                     |             |             | Read                    | Write | Read                      | Write  |            |  |
| TFU                                 | 0x4002_1000 | 0x4002_1FFF | 4                       | 3     | 4                         | 3      | ICLK       | Trigonometric Function Unit  |
| ELC                                 | 0x4008_2000 | 0x4008_2FFF | 5                       | 4     | 3 to 5                    | 2 to 4 | PCLKB      | Event Link Controller  |
| IWDT, WDT, CAC                      | 0x4008_3000 | 0x4008_3FFF | 5                       | 4     | 3 to 5                    | 2 to 4 | PCLKB      | Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit |
| MSTP                                | 0x4008_4000 | 0x4008_4FFF | 5                       | 4     | 2 to 4                    | 2 to 4 | PCLKB      | Module Stop Control  |
| KINT                                | 0x4008_5000 | 0x4008_5FFF | 4                       | 3     | 1 to 4                    | 1 to 3 | PCLKB      | Key Interrupt Function   |
| POEG                                | 0x4008_A000 | 0x4008_AFFF | 5                       | 4     | 3 to 5                    | 2 to 4 | PCLKB      | Port Output Enable for GPT   |
| CANFD                               | 0x400B_0000 | 0x400C_1FFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKB      | CANFD Module   |
| PSCU                                | 0x400E_0000 | 0x400E_0FFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKB      | Peripheral Security Control Unit   |
| AGTn                                | 0x400E_8000 | 0x400E_8FFF | 7                       | 4     | 4 to 7                    | 2 to 4 | PCLKB      | Low Power Asynchronous General Purpose Timer n   |
| TSN                                 | 0x400F_3000 | 0x400F_3FFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKB      | Temperature Sensor   |
| ACMPHSn                             | 0x400F_4000 | 0x400F_4FFF | 4                       | 3     | 1 to 3                    | 1 to 3 | PCLKB      | High-Speed Analog Comparator   |
| CRC, DOC                            | 0x4010_8000 | 0x4010_9FFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKA      | Cyclic Redundancy Check, Data Operation Circuit  |
| SCIn                                | 0x4011_8000 | 0x4011_8FFF | 5                       | 4     | 2 to 4                    | 2 to 4 | PCLKA      | Serial Communication Interface n   |
| SPIIn                               | 0x4011_A000 | 0x4011_AFFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKA      | Serial Peripheral Interface n  |
| IICn                                | 0x4011_F000 | 0x4011_FFFF | 5                       | 4     | 2 to 4                    | 2 to 4 | PCLKA      | Inter-Integrated Circuit n   |
| CANFD ECC                           | 0x4012_F200 | 0x4012_FFFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKA      | CANFD ECC Module   |
| SCE5                                | 0x4016_1000 | 0x4016_1FFF | 6                       | 4     | 3 to 6                    | 2 to 4 | PCLKA      | Secure Cryptographic Engine  |
| GPTn, GPT_OPS (core clock = PCLKD)  | 0x4016_9000 | 0x4016_9FFF | 8                       | 5     | 5 to 8                    | 3 to 5 | PCLKA      | General PWM Timer n, Output Phase Switching Controller                                   |
| GPTn, GPT_OPS (core clock = GPTCLK) | 0x4016_9000 | 0x4016_9FFF | 10                      | 7     | 7 to 10                   | 5 to 7 | PCLKA      | General PWM Timer n, Output Phase Switching Controller                                   |
| GPT (GTCKCR)                        | 0x4016_9B00 | 0x4016_9B00 | 5                       | 4     | 2 to 4                    | 2 to 4 | PCLKA      | GPT Clock Control Register   |
| PDG                                 | 0x4016_A000 | 0x4016_AFFF | 4                       | 3     | 1 to 3                    | 1 to 3 | PCLKA      | PWM Delay Generation   |
| ADC                                 | 0x4017_0000 | 0x4017_0FFF | 5                       | 4     | 2 to 5                    | 2 to 4 | PCLKA      | 12-bit A/D Converter   |
| ADC                                 | 0x4017_1000 | 0x4017_1FFF | 4                       | 3     | 1 to 3                    | 1 to 3 | PCLKA      | 12-bit A/D Converter   |
| DAC12n                              | 0x4017_2000 | 0x4017_2FFF | 5                       | 4     | 2 to 4                    | 2 to 4 | PCLKA      | 12-bit D/A Converter   |

Table 3.2 访问周期 (2个, 共3个)

| Peripherals                         | Address     |             | 访问周期数       |       |                           |        | Cycle Unit | 相关功能   |
|-------------------------------------|-------------|-------------|-------------|-------|---------------------------|--------|------------|--|
|                                     |             |             | ICLK = PCLK |       | ICLK > PCLK <sup>*1</sup> |        |            |  |
|                                     |             |             | Read        | Write | Read                      | Write  |            |  |
| TFU                                 | 0x4002_1000 | 0x4002_1FFF | 4           | 3     | 4                         | 3      | ICLK       | 三角函数单元   |
| ELC                                 | 0x4008_2000 | 0x4008_2FFF | 5           | 4     | 3 to 5                    | 2 to 4 | PCLKB      | 事件链接控制器  |
| IWDT, WDT, CAC                      | 0x4008_3000 | 0x4008_3FFF | 5           | 4     | 3 to 5                    | 2 to 4 | PCLKB      | Independent 看门狗定时器, 看门狗定时器, 时钟频率 Accuracy 测量电路 |
| MSTP                                | 0x4008_4000 | 0x4008_4FFF | 5           | 4     | 2 to 4                    | 2 to 4 | PCLKB      | 模块停止控制   |
| KINT                                | 0x4008_5000 | 0x4008_5FFF | 4           | 3     | 1 to 4                    | 1 to 3 | PCLKB      | 按键中断功能   |
| POEG                                | 0x4008_A000 | 0x4008_AFFF | 5           | 4     | 3 to 5                    | 2 to 4 | PCLKB      | 端口输出使能 GPT                                     |
| CANFD                               | 0x400B_0000 | 0x400C_1FFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKB      | CANFD Module                                   |
| PSCU                                | 0x400E_0000 | 0x400E_0FFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKB      | 外围安全控制单元                                       |
| AGTn                                | 0x400E_8000 | 0x400E_8FFF | 7           | 4     | 4 to 7                    | 2 to 4 | PCLKB      | 低电量 Asynchronous 一般用途 Timer n                  |
| TSN                                 | 0x400F_3000 | 0x400F_3FFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKB      | 温度感应器  |
| ACMPHSn                             | 0x400F_4000 | 0x400F_4FFF | 4           | 3     | 1 to 3                    | 1 to 3 | PCLKB      | High-Speed Analog Comparator                   |
| CRC, DOC                            | 0x4010_8000 | 0x4010_9FFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKA      | 循环冗余检查, 数据运算电路                                 |
| SCIn                                | 0x4011_8000 | 0x4011_8FFF | 5           | 4     | 2 to 4                    | 2 to 4 | PCLKA      | 串行通信 Interface n                               |
| SPIIn                               | 0x4011_A000 | 0x4011_AFFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKA      | 串行外设 Interface n                               |
| IICn                                | 0x4011_F000 | 0x4011_FFFF | 5           | 4     | 2 to 4                    | 2 to 4 | PCLKA      | Inter-Integrated Circuit n                     |
| CANFD ECC                           | 0x4012_F200 | 0x4012_FFFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKA      | CANFD ECC Module                               |
| SCE5                                | 0x4016_1000 | 0x4016_1FFF | 6           | 4     | 3 to 6                    | 2 to 4 | PCLKA      | 安全密码学 Engine                                   |
| GPTn, GPT_OPS (core clock = PCLKD)  | 0x4016_9000 | 0x4016_9FFF | 8           | 5     | 5 to 8                    | 3 to 5 | PCLKA      | 通用PWM定时器n, 输出相位切换控制器                           |
| GPTn, GPT_OPS (core clock = GPTCLK) | 0x4016_9000 | 0x4016_9FFF | 10          | 7     | 7 to 10                   | 5 to 7 | PCLKA      | 通用PWM定时器n, 输出相位切换控制器                           |
| GPT (GTCKCR)                        | 0x4016_9B00 | 0x4016_9B00 | 5           | 4     | 2 to 4                    | 2 to 4 | PCLKA      | GPT时钟控制 Register                               |
| PDG                                 | 0x4016_A000 | 0x4016_AFFF | 4           | 3     | 1 to 3                    | 1 to 3 | PCLKA      | PWM延迟生成  |
| ADC                                 | 0x4017_0000 | 0x4017_0FFF | 5           | 4     | 2 to 5                    | 2 to 4 | PCLKA      | 12-bit A/D Converter                           |
| ADC                                 | 0x4017_1000 | 0x4017_1FFF | 4           | 3     | 1 to 3                    | 1 to 3 | PCLKA      | 12-bit A/D Converter                           |
| DAC12n                              | 0x4017_2000 | 0x4017_2FFF | 5           | 4     | 2 to 4                    | 2 to 4 | PCLKA      | 12-bit D/A Converter                           |

Table 3.2 Access cycles (3 of 3)

| Peripherals | Address     |             | Number of access cycles |       |                           |        | Cycle Unit | Related function                                |
|-------------|-------------|-------------|-------------------------|-------|---------------------------|--------|------------|---|
|             |             |             | ICLK = FCLK             |       | ICLK > FCLK <sup>*1</sup> |        |            |   |
|             |             |             | Read                    | Write | Read                      | Write  |            |   |
| FLAD, FACL  | 0x407F_C000 | 0x407F_EFFF | 5                       | 4     | 2 to 5                    | 2 to 4 | FCLK       | Data Flash, Flash Application Command Interface |

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.

Table 3.2 访问周期 (3个, 共3个)

| Peripherals | Address     |             | 访问周期数       |       |                           |        | Cycle Unit | 相关功能          |
|-------------|-------------|-------------|-------------|-------|---------------------------|--------|------------|---------------|
|             |             |             | ICLK = FCLK |       | ICLK > FCLK <sup>*1</sup> |        |            |               |
|             |             |             | Read        | Write | Read                      | Write  |            |               |
| FLAD, FACL  | 0x407F_C000 | 0x407F_EFFF | 5           | 4     | 2 to 5                    | 2 to 4 | FCLK       | 数据闪存、闪存应用命令接口 |

注1.如果PCLK或FCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2.5是1到3。

## Appendix 4. Peripheral Variant

Table 4.1 shows the correspondence between the module name used in this manual and the Peripheral Variant.

**Table 4.1 Module name vs Peripheral Variant**

| Module name | Peripheral Variant |
|-------------|--------------------|
| ELC         | ELC_B              |
| AGTW        | AGTW_B             |
| SCI         | SCI_B              |
| IIC         | IIC_B              |
| CANFD       | CANFD_B            |
| SPI         | SPI_B              |
| SCE5        | SCE5_B             |
| ADC         | ADC_B              |
| DOC         | DOC_B              |

## Appendix 4. 外设变体

表4.1显示了本手册中使用的模块名称与PeripheralVariant之间的对应关系。

**Table 4.1 模块名称与外设变体**

| 模块名称  | 外设变体    |
|-------|---------|
| ELC   | ELC_B   |
| AGTW  | AGTW_B  |
| SCI   | SCI_B   |
| IIC   | IIC_B   |
| CANFD | CANFD_B |
| SPI   | SPI_B   |
| SCE5  | SCE5_B  |
| ADC   | ADC_B   |
| DOC   | DOC_B   |

RA生态工作室

## Appendix 5. Related Documents

| Component               | Document Type                    | Description  |
|-------------------------|----------------------------------|--|
| Microcontrollers        | Data sheet                       | Features, overview, and electrical characteristics of the MCU  |
|                         | User's Manual: Hardware          | MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions   |
|                         | Application Notes                | Technical notes, board design guidelines, and software migration information   |
|                         | Technical Update (TU)            | Preliminary reports on product specifications such as restriction and errata   |
| Software                | User's Manual: Software          | Command set, API reference and programming information   |
|                         | Application Notes                | Project files, guidelines for software programming, and application examples to develop embedded software applications   |
| Tools & Kits, Solutions | User's Manual: Development Tools | User's manuals and quick start guides for developing embedded software applications with Software Packages, Development Kits, Starter Kits, Promotion Kits, Product Examples, and Application Examples |
|                         | Quick Start Guide                |  |
|                         | Application Notes                | Project files, guidelines for software programming, and application examples to develop embedded software applications   |

## Appendix 5. 相关文件

| Component        | 文件类型                    | Description   |
|------------------|-------------------------|---|
| Microcontrollers | 数据表                     | MCU的特性、概述和电气特性  |
|                  | User's Manual: Hardware | MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述                 |
|                  | 应用笔记                    | 技术说明、电路板设计指南和软件迁移信息                                   |
|                  | 技术更新(TU)                | 限制、勘误等产品规格的初步报告                                       |
| Software         | User's Manual: Software | 命令集、API参考和编程信息  |
|                  | 应用笔记                    | 用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例                      |
| 工具和套件 解决方案       | 用户手册：开发工具               | 使用软件包、开发套件、入门套件、促销套件、产品示例和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南 |
|                  | 快速入门指南                  |   |
|                  | 应用笔记                    | Examples<br>用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例          |

## Revision History

Revision 1.10 — Dec 9, 2021

First edition, issued

## 修订记录

1.10版——2021年12月9日

第一版，已发行

RA生态工作室

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- Precaution against Electrostatic Discharge (ESD)**

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
- Processing at power-on**

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
- Input of signal during power-off state**

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
- Handling of unused pins**

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
- Clock signals**

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
- Voltage application waveform at input pin**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).
- Prohibition of access to reserved addresses**

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
- Differences between products**

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

## 处理微处理单元和微控制器的一般注意事项 单位产品

以下使用说明适用于瑞萨的所有微处理单元和微控制器单元产品。有关详细的使用说明本文档所涵盖的产品，请参阅文档的相关部分以及为产品发布的任何技术更新。

- 防止静电放电(ESD)**

当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
- 上电处理**

通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态在通过片内上电复位功能复位的产品中，从供电时间到供电达到指定重置的级别。
- 断电状态下的信号输入**

请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
- 处理未使用的引脚**

按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。
- 时钟信号**

应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。
- 输入引脚的电压施加波形**

由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在 $V_{IL}$ 之间的区域(Max.)和 $V_{IH}$ (Min.)由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，输入电平是固定的，并且在输入电平通过 $V_{IL}$ (Max.)和 $V_{IH}$ (Min.)之间的区域时的过渡期间也是如此。
- 禁止访问保留地址**

禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些不能保证LSI的正确操作。
- 产品之间的差异**

在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。同一组中的微处理单元或微控制器单元产品的特性，但具有不同的部件号，其特性可能会有所不同内部存储器容量，布局模式和其他因素，这些因素会影响电气特性的范围，例如特性值，工作裕度、抗噪声能力和辐射噪声量。当更改为具有不同部件号的产品时，实施系统-给定产品的评估测试。

## Notice

- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
- Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
- No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
- You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
- Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
- Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
- No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
- When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
- Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
- Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
- It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
- Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan

[www.renesas.com](http://www.renesas.com)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

## Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

[www.renesas.com/contact/](http://www.renesas.com/contact/).

## Notice

- 本文中対电路、软件和其他相关信息的描述仅用于说明半导体产品的操作和应用示例。您对在您的产品或系统设计中使用或以任何其他方式使用电路、软件和信息负全部责任。对于您或第三方因使用这些电路、软件或信息而遭受的任何损失和损害，瑞萨电子不承担任何责任。

- 瑞萨电子特此明确声明，对于因使用本文中描述的瑞萨电子产品或技术信息（包括但不限于产品数据、图纸、图表、程序、算法和应用示例。

- 瑞萨电子或其他方的任何专利、版权或其他知识产权在此未授予任何明示、暗示或其他许可。

- 您应负责确定需要从任何第三方获得哪些许可证，并在需要时为合法进口、出口、制造、销售、使用、分销或以其他方式处置任何包含瑞萨电子产品的产品获取此类许可证。
- 您不得全部或部分更改、修改、复制或反向工程任何瑞萨电子产品。对于您或第三方因此类更改、修改、复制或逆向工程而遭受的任何损失或损害，瑞萨电子不承担任何责任。
- 瑞萨电子产品根据以下两个质量等级进行分类：“标准”和“高质量”。每个瑞萨电子产品的预期应用取决于产品的质量等级，如下所示。

“标准”：计算机；办公用品;通讯设备；测试和测量设备；视听设备；家用电器；机械工具;个人电子设备；工业机器人；等“高品质”：运输设备（汽车、火车、轮船等）；交通管制（红绿灯）；大型通讯设备；关键金融终端系统；安全控制设备；除非在瑞萨电子数据表或其他瑞萨电子文档中明确指定为高可靠性产品或适用于恶劣环境的产品，否则瑞萨电子产品不得用于或授权用于可能对人类构成直接威胁的产品或系统生命或身体伤害（人工生命支持设备或系统；外科植入物等），或可能造成严重财产损失（空间系统；海底中继器；核电控制系统；飞机控制系统；关键工厂系统；军事装备等）。)。对于您或任何第三方因使用与任何瑞萨电子数据表、用户手册或其他瑞萨电子文档不一致的任何瑞萨电子产品而导致的任何损害或损失，瑞萨电子不承担任何责任。

- 没有半导体产品是绝对安全的。尽管瑞萨电子硬件或软件产品中可能实施任何安全措施或功能，但瑞萨电子绝对不承担因任何漏洞或安全漏洞引起的任何责任，包括但不限于任何未经授权访问或使用瑞萨电子产品或使用瑞萨电子产品的系统。瑞萨电子不保证或保证瑞萨电子产品或使用创建的任何系统

- 瑞萨电子产品将无懈可击或不受腐败、攻击、病毒、干扰、黑客攻击、数据丢失或盗窃或其他安全入侵（“漏洞问题”）。瑞萨电子不承担任何和由任何漏洞问题引起或与之相关的所有责任或义务。此外，在某种程度上在适用法律允许的情况下，瑞萨电子不提供任何明示或暗示的保证，包括关于本文档和任何相关或随附的软件或硬件，包括但不限于对适销性或特定用途适用性的默示保证。
- 使用瑞萨电子产品时，请参阅最新的产品信息（数据表、用户手册、应用说明、“通用说明处理和使用半导体器件”在可靠性手册等），并确保使用条件在规定的范围内瑞萨电子关于最大额定值、工作电源电压范围、散热特性、安装等方面的信息。瑞萨电子不对因在上述规定范围之外使用瑞萨电子产品而引起的任何故障、故障或事故承担任何责任。

9.尽管瑞萨电子努力提高瑞萨电子产品的质量和可靠性，但半导体产品具有特定的特性，例如以一定的速率发生故障以及在特定的使用条件下发生故障。除非在瑞萨电子数据表或其他瑞萨电子文档中指定为高可靠性产品或适用于恶劣环境的产品，否则瑞萨电子产品不受抗辐射设计的约束。您有责任实施安全措施，以防止在瑞萨电子产品出现故障或故障时可能造成人身伤害、火灾造成的伤害或损害以及/或对公众造成危险，例如硬件和软件的安全设计，包括但不限于冗余、火灾控制和故障预防、老化退化的适当处理或任何其他适当的措施。因为单单评估微机软件是非常困难和不切实际的，您有责任评估您制造的最终产品或系统的安全性。10.请联系瑞萨电子销售办事处了解有关环境问题的详细信息，例如每个瑞萨电子产品的环境兼容性。您有责任仔细、充分地调查适用于管制物质的包含或使用的法律和法规，包括但不限于欧盟RoHS指令，并按照所有这些适用的法律和法规使用瑞萨电子产品。瑞萨电子对因您不遵守适用法律和法规而造成的损害或损失不承担任何责任。11.瑞萨电子的产品和技术不得用于或整合到任何适用的国内或国外法律或法规禁止制造、使用或销售的产品或系统中。您应遵守对各方或交易主张管辖权的任何国家/地区的政府颁布和管理的任何适用的出口管制法律和法规。12.瑞萨电子产品的购买者或分销商，或将产品分销、处置或以其他方式出售或转让给第三方的任何其他方，有责任提前通知该第三方有关内容和条件本文件中规定。13.未经瑞萨电子事先书面同意，不得以任何形式全部或部分翻印、复制或复制本文档。14.如果您对本文档中包含的信息或瑞萨电子产品有任何疑问，请联系瑞萨电子销售办事处。

(Note1) 本文中使用的“瑞萨电子”是指瑞萨电子公司，还包括其直接或间接控制的子公司。

(Note2) “瑞萨电子产品”是指由瑞萨电子开发或制造或为瑞萨电子开发或制造的任何产品。

(Rev.5.0-1 October 2020)

## 公司总部

TOYOSU FORESIA, 3-2-24 Toyosu,  
日本东京都江东区135-0061

[www.renesas.com](http://www.renesas.com)

## Trademarks

瑞萨和瑞萨标识是瑞萨电子公司的商标。所有商标和注册商标均为其各自所有者的财产。

## 联系信息

有关产品、技术、文档的最新版本或离您最近的销售办事处的更多信息，请访问：[www.renesas.com](http://www.renesas.com)联系方式。