

Leading-performance 100 MHz Arm Cortex-M33 core, up to 512 KB code flash memory with background operation, 8 KB Data flash memory, and 128 KB SRAM with Parity. High-integration with USB 2.0 Full-Speed, Quad SPI, and advanced analog.

Features

- Arm® Cortex®-M33 Core
 - Armv8-M architecture with the main extension
 - Maximum operating frequency: 100 MHz
 - Arm Memory Protection Unit (Arm MPU)
 - Protected Memory System Architecture (PMSAv8)
 - Secure MPU (MPU_S): 8 regions
 - Non-secure MPU (MPU_NS): 8 regions
 - SysTick timer
 - Embeds two Systick timers: Secure and Non-secure instance
 - Driven by LOCO or system clock
 - CoreSight™ ETM-M33
- Memory
 - Up to 512-KB code flash memory
 - 8-KB data flash memory (100,000 program/erase (P/E) cycles)
 - 128-KB SRAM
- Connectivity
 - Serial Communications Interface (SCI) × 4
 - Asynchronous interfaces
 - 8-bit clock synchronous interface
 - Smart card interface
 - Simple IIC
 - Simple SPI
 - Manchester coding (SCI3, SCI4)
 - I²C bus interface (IIC)
 - Serial Peripheral Interface (SPI)
 - Quad Serial Peripheral Interface (QSPI)
 - USB 2.0 Full-Speed Module (USBFS)
 - Control Area Network module (CAN)
- Analog
 - 12-bit A/D Converter (ADC12)
 - 12-bit D/A Converter (DAC12)
- Timers
 - General PWM Timer 32-bit (GPT32) × 2
 - General PWM Timer 16-bit (GPT16) × 2
 - Low Power Asynchronous General Purpose Timer (AGT) × 5
- Security and Encryption
 - Arm® TrustZone®
 - Up to three regions for the code flash
 - Up to two regions for the data flash
 - Up to three regions for the SRAM
 - Individual secure or non-secure security attribution for each peripheral
- System and Power Management
 - Low power modes
 - Battery backup function (VBATT)
 - Realtime Clock (RTC) with calendar and VBATT support
 - Event Link Controller (ELC)
 - Data Transfer Controller (DTC)
 - DMA Controller (DMAC) × 8
 - Power-on reset
 - Low Voltage Detection (LVD) with voltage settings
 - Watchdog Timer (WDT)
 - Independent Watchdog Timer (IWDT)
- Multiple Clock Sources
 - Main clock oscillator (MOSC) (8 to 24 MHz)
 - Sub-clock oscillator (SOSC) (32.768 kHz)
 - High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
 - Middle-speed on-chip oscillator (MOCO) (8 MHz)
 - Low-speed on-chip oscillator (LOCO) (32.768 kHz)
 - IWDT-dedicated on-chip oscillator (15 kHz)
 - Clock trim function for HOCO/MOCO/LOCO
 - PLL/PLL2
 - Clock out support

性能领先的100MHzArmCortex-M33内核，高达512KB代码闪存，带后台操作，8KB数据闪存和带奇偶校验的128KBSRAM。与USB2.0全速、四路SPI和高级模拟的高度集成。

Features

- Arm® Cortex®-M33内核
 - 带有主扩展的Armv8-M架构
 - 最大工作频率: 100MHz
 - Arm内存保护单元 (ArmMPU)
- 受保护的内存系统架构(PMSAv8) 安全MPU(MPU_S): 8个区域 非安全MPU(MPU_NS): 8个区域
 - Systick计时器
 - 嵌入两个Systick计时器: 安全和非安全实例 由LOCO或系统时钟驱动
 - CoreSight ETM-M33
- Memory
 - 高达512-KB代码闪存
 - 8-KB数据闪存 (100 000次程序擦除(PE)周期)
 - 128-KB SRAM
- Connectivity
 - 串行通信接口(SCI)×4-异步接口-8位时钟同步接口-智能卡接口-简单I²C-简单SPI-曼彻斯特编码(SCI3 SCI4)
 - I²C总线接口(I²C)
 - 串行外设接口(SPI)●四路串行外设接口(QSPI)
 - USB2.0全速模块(USBFS)
 - 控制区域网络模块(CAN)
- Analog
 - 12-bit A/D Converter (ADC12)
 - 12-bit D/A Converter (DAC12)
- Timers
 - 通用PWM定时器32位(GPT32)×2
 - 通用PWM定时器16位(GPT16)×2
 - 低功耗异步通用定时器(AGT)×5
- 安全和加密
 - Arm® TrustZone®
 - 代码闪存最多三个区域 数据闪存最多两个区域 SRAM最多三个区域 每个外设的单独安全或非安全属性
- 系统和电源管理
 - 低功耗模式
 - 电池备份功能(VBATT)
 - 支持日历和VBATT的实时时钟(RTC)
 - 事件链接控制器(ELC)
 - 数据传输控制器(DTC)
 - DMA控制器(DMAC)×8
 - 上电复位
 - 具有电压设置的低电压检测(LVD)
 - 看门狗定时器(WDT)
 - 独立看门狗定时器(IWDT)
- 多个时钟源
 - 主时钟振荡器 (MOSC) (8至24MHz)
 - 副时钟振荡器 (SOSC) (32.768kHz)
 - 高速片上振荡器 (HOCO) (161820MHz)
 - 中速片上振荡器(MOCO)(8MHz)
 - 低速片上振荡器(LOCO)(32.768kHz)
 - IWDT专用片上振荡器(15kHz)
 - HOCOMOCOLOCO的时钟微调功能
 - PLL/PLL2
 - 时钟输出支持

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 100 MHz with the following features:

- Up to 512 KB code flash memory
- 128 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- USBFS
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

| Feature | Functional description |
|---------------------|--|
| Arm Cortex-M33 core | <ul style="list-style-type: none"> ● Maximum operating frequency: up to 100 MHz ● Arm Cortex-M33 core: <ul style="list-style-type: none"> - Armv8-M architecture with security extension - Revision: r0p4-00rel0 ● Arm Memory Protection Unit (Arm MPU) <ul style="list-style-type: none"> - Protected Memory System Architecture (PMSAv8) - Secure MPU (MPU_S): 8 regions - Non-secure MPU (MPU_NS): 8 regions ● SysTick timer <ul style="list-style-type: none"> - Embeds two Systick timers: Secure and Non-secure instance - Driven by SysTick timer clock (SYSTICKCLK) or system clock (ICLK) ● CoreSight™ ETM-M33 |

Table 1.2 Memory

| Feature | Functional description |
|-----------------------|--|
| Code flash memory | Maximum 512 KB of code flash memory. |
| Data flash memory | 8 KB of data flash memory. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. |
| SRAM | On-chip high-speed SRAM with or without parity bit. |

Table 1.3 System (1 of 2)

| Feature | Functional description |
|-----------------------------|--|
| Operating modes | Two operating modes: <ul style="list-style-type: none"> ● Single-chip mode ● SCI/USB boot mode |
| Resets | The MCU provides 13 resets. |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. |

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外围设备可促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达100MHz的高性能ArmCortex®-M33内核，具有以下特性：

- 高达512KB的代码闪存
- 128 KB SRAM
- 四路串行外设接口(QSPI)
- USBFS
- 模拟外设
- 安全和安全功能

1.1 功能概要

Table 1.1 脚芯

| Feature | 功能说明 |
|-----------------|---|
| ArmCortex-M33内核 | <ul style="list-style-type: none"> ● 最大工作频率：高达100MHz ● Arm Cortex-M33 core: <ul style="list-style-type: none"> - 带有安全扩展的Armv8-M架构 - Revision: r0p4-00rel0 ● Arm内存保护单元（ArmMPU） <ul style="list-style-type: none"> - 受保护的内存系统架构(PMSAv8) - 安全MPU(MPU_S): 8个区域 - 非安全MPU (MPU_NS): 8 regions ● SysTick timer <ul style="list-style-type: none"> - 嵌入两个Systick计时器：安全和非安全实例 - 由SysTick定时器时钟(SYSTICKCLK)或系统时钟(ICLK)驱动 ● CoreSight™ ETM-M33 |

Table 1.2 Memory

| Feature | 功能说明 |
|-----------------------|---------------------|
| 代码闪存 | 最大512KB的代码闪存。 |
| 数据闪存 | 8KB数据闪存。 |
| Option-setting memory | 选项设置存储器确定复位后MCU的状态。 |
| SRAM | 带或不带奇偶校验的片上高速SRAM。 |

Table 1.3 系统(1of2)

| Feature | 功能说明 |
|------------|--|
| 操作模式 | 两种操作模式：● <ul style="list-style-type: none"> ● SCI/USB启动模式 |
| Resets | MCU提供13次复位。 |
| 低电压检测(LVD) | 低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器(LVD0、LVD1、LVD2)组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。 |

Table 1.3 System (2 of 2)

| Feature | Functional description |
|--|--|
| Clocks | <ul style="list-style-type: none"> Main clock oscillator (MOSC) Sub-clock oscillator (SOSC) High-speed on-chip oscillator (HOCO) Middle-speed on-chip oscillator (MOCO) Low-speed on-chip oscillator (LOCO) IWDT-dedicated on-chip oscillator PLL/PLL2 Clock out support |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. |
| Low power modes | Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. |
| Register write protection | The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). |
| Memory Protection Unit (MPU) | The MCU has one Memory Protection Unit (MPU). |

Table 1.4 Event link

| Feature | Functional description |
|-----------------------------|--|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. |

Table 1.5 Direct memory access

| Feature | Functional description |
|--------------------------------|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. |
| DMA Controller (DMAC) | The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. |

Table 1.6 External bus interface

| Feature | Functional description |
|--------------|--|
| External bus | <ul style="list-style-type: none"> QSPI area (EQBIU): Connected to the QSPI (external device interface) |

Table 1.7 Timers (1 of 2)

| Feature | Functional description |
|-----------------------------------|--|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 2 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. |
| Port Output Enable for GPT (POEG) | The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state |

Table 1.3 系统(2之2)

| Feature | 功能说明 |
|-----------------|---|
| Clocks | <ul style="list-style-type: none"> 主时钟振荡器(MOSC) Sub-clock oscillator (SOSC) High-speed on-chip oscillator (HOCO) Middle-speed on-chip oscillator (MOCO) Low-speed on-chip oscillator (LOCO) IWDT-dedicated on-chip oscillator PLL/PLL2 打卡支持 |
| 时钟频率精度测量电路(CAC) | 时钟频率精度测量电路(CAC)在被选为测量基准的时钟(测量基准时钟)产生的时间内对要测量的时钟(测量目标时钟)的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。 |
| 中断控制器单元(ICU) | 中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量。中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。 |
| 低功耗模式 | 可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。 |
| 电池备份功能 | 提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、备份存储器以及VCC和VBATT之间的切换。 |
| 寄存器写保护 | 寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PR CR)设置。 |
| 内存保护单元(MPU) | MCU有一个内存保护单元(MPU)。 |

Table 1.4 活动链接

| Feature | 功能说明 |
|--------------|--|
| 事件链接控制器(ELC) | EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。 |

Table 1.5 直接内存访问

| Feature | 功能说明 |
|-----------------------|--|
| 数据传输控制器(DTC) | 数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。 |
| DMA Controller (DMAC) | MCU包括一个8通道直接内存访问控制器(DMAC)，无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。 |

Table 1.6 外部总线接口

| Feature | 功能说明 |
|---------|--|
| 外部总线 | <ul style="list-style-type: none"> QSPI区(EQBIU)：连接到QSPI(外部设备接口) |

Table 1.7 计时器(1of2)

| Feature | 功能说明 |
|------------------|--|
| 通用PWM定时器(GPT) | 通用PWM定时器(GPT)是一个32位定时器，具有GPT32×2通道和一个16位定时器，具有GPT16×2通道。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。 |
| GPT(POEG)的端口输出使能 | 端口输出使能(POEG)功能可以将通用PWM定时器(GPT)输出引脚置于输出禁用状态 |

Table 1.7 Timers (2 of 2)

| Feature | Functional description |
|--|--|
| Low power Asynchronous General Purpose Timer (AGT) | The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. |
| Realtime Clock (RTC) | The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. |
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. |

Table 1.8 Communication interfaces

| Feature | Functional description |
|---|--|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) × 4 channels have asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) 8-bit clock synchronous interface Simple IIC (master-only) Simple SPI Smart card interface Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3, 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. |
| I ² C bus interface (IIC) | The I ² C bus interface (IIC) has 1 channel. The IIC module conforms with and provides a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions. |
| Serial Peripheral Interface (SPI) | The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. |
| Control Area Network (CAN) | The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver. |
| USB 2.0 Full-Speed module (USBFS) | The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. |
| Quad Serial Peripheral Interface (QSPI) | The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. |

Table 1.7 计时器 (2个中的2个)

| Feature | 功能说明 |
|-------------------|---|
| 低功耗异步通用目的定时器(AGT) | 低功耗异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。 |
| 实时时钟(RTC) | 实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。 |
| 看门狗定时器(WDT) | 看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。 |
| 独立看门狗定时器(IWDT) | 独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。 |

Table 1.8 通讯接口

| Feature | 功能说明 |
|---------------------------|---|
| 串行通信接口(SCI) | 串行通信接口(SCI)×4通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） <ul style="list-style-type: none"> 8位时钟同步接口 Simple IIC (master-only) 简单的SPI 智能卡接口 曼彻斯特界面 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0 3 4 9)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。 |
| I ² C总线接口(IIC) | I ² C总线接口(IIC)有1个通道。I ² C模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集。 |
| 串行外设接口(SPI) | 串行外设接口(SPI)有1个通道。SPI提供与多个处理器和外围设备的高速全双工同步串行通信。 |
| 控制区域网络(CAN) | 控制器局域网(CAN)模块使用基于消息的协议在电磁噪声应用中的多个从机和主机之间接收和传输数据。该模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。CAN模块需要额外的外部CAN收发器。 |
| USB2.0全速模块(USBFS) | USB2.0全速模块(USBFS)可以作为主机控制器或设备控制器运行。该模块支持全速和低速（仅限主机控制器）传输，如通用串行总线规范2.0。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据您的系统为管道1到9分配任何端点编号。 |
| 四路串行外设接口(QSPI) | QuadSerialPeripheralInterface(QSPI)是一种存储器控制器，用于连接具有SPI兼容接口的串行ROM（非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM）。 |

Table 1.9 Analog

| Feature | Functional description |
|------------------------------|--|
| 12-bit A/D Converter (ADC12) | A 12-bit successive approximation A/D converter is provided. Up to 9 analog input channels are selectable. |
| 12-bit D/A Converter (DAC12) | A 12-bit D/A converter (DAC12) is provided. |

Table 1.10 Data processing

| Feature | Functional description |
|--|--|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. |

Table 1.9 Analog

| Feature | 功能说明 |
|------------------------------|----------------------------------|
| 12-bit A/D Converter (ADC12) | 提供了一个12位逐次逼近模数转换器。最多可选择9个模拟输入通道。 |
| 12-bit D/A Converter (DAC12) | 提供了一个12位DA转换器(DAC12)。 |

Table 1.10 数据处理

| Feature | 功能说明 |
|----------------|---|
| 循环冗余校验(CRC)计算器 | 循环冗余校验(CRC)生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。 |
| 数据运算电路(DOC) | 数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。 |

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

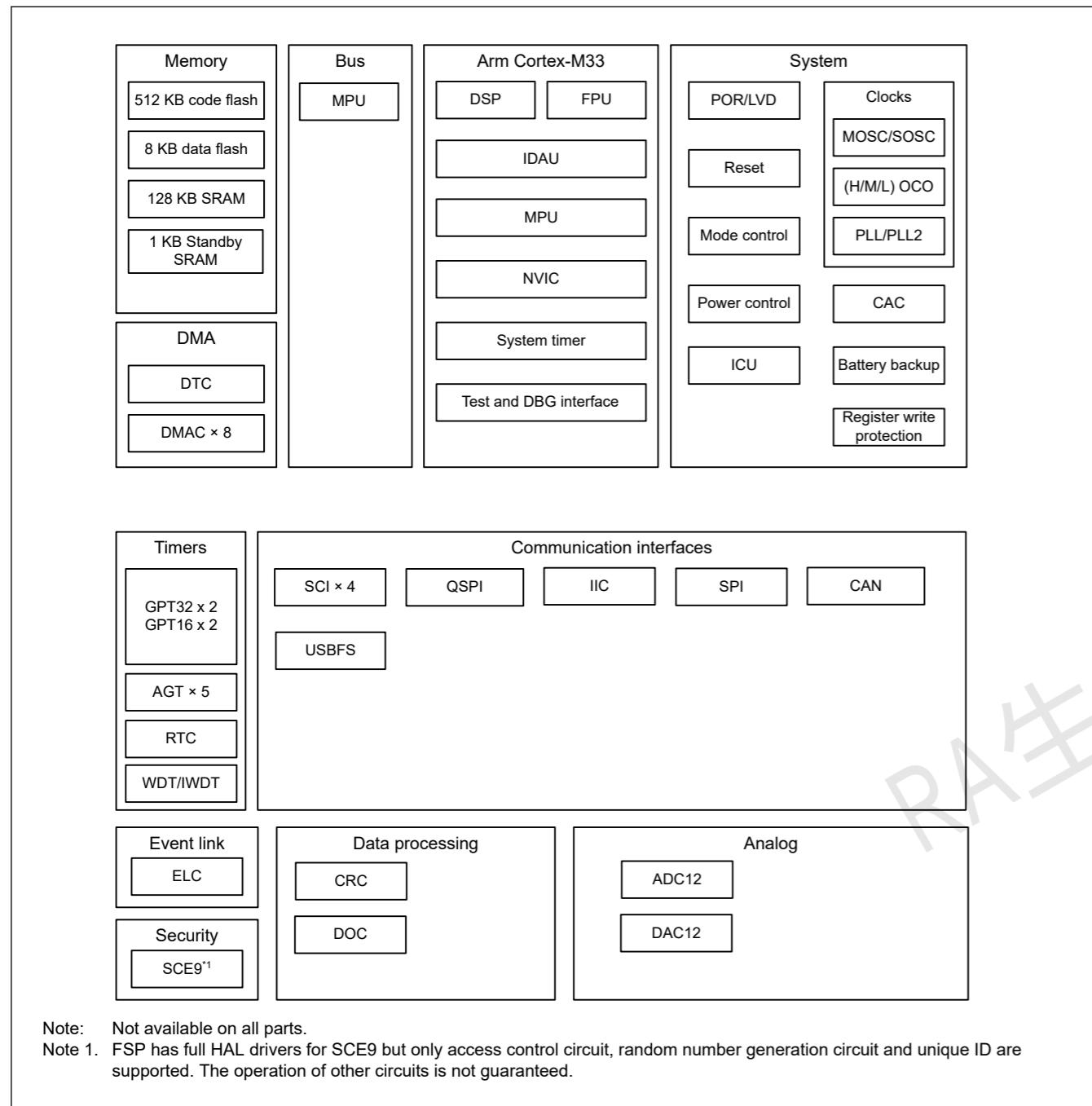


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。

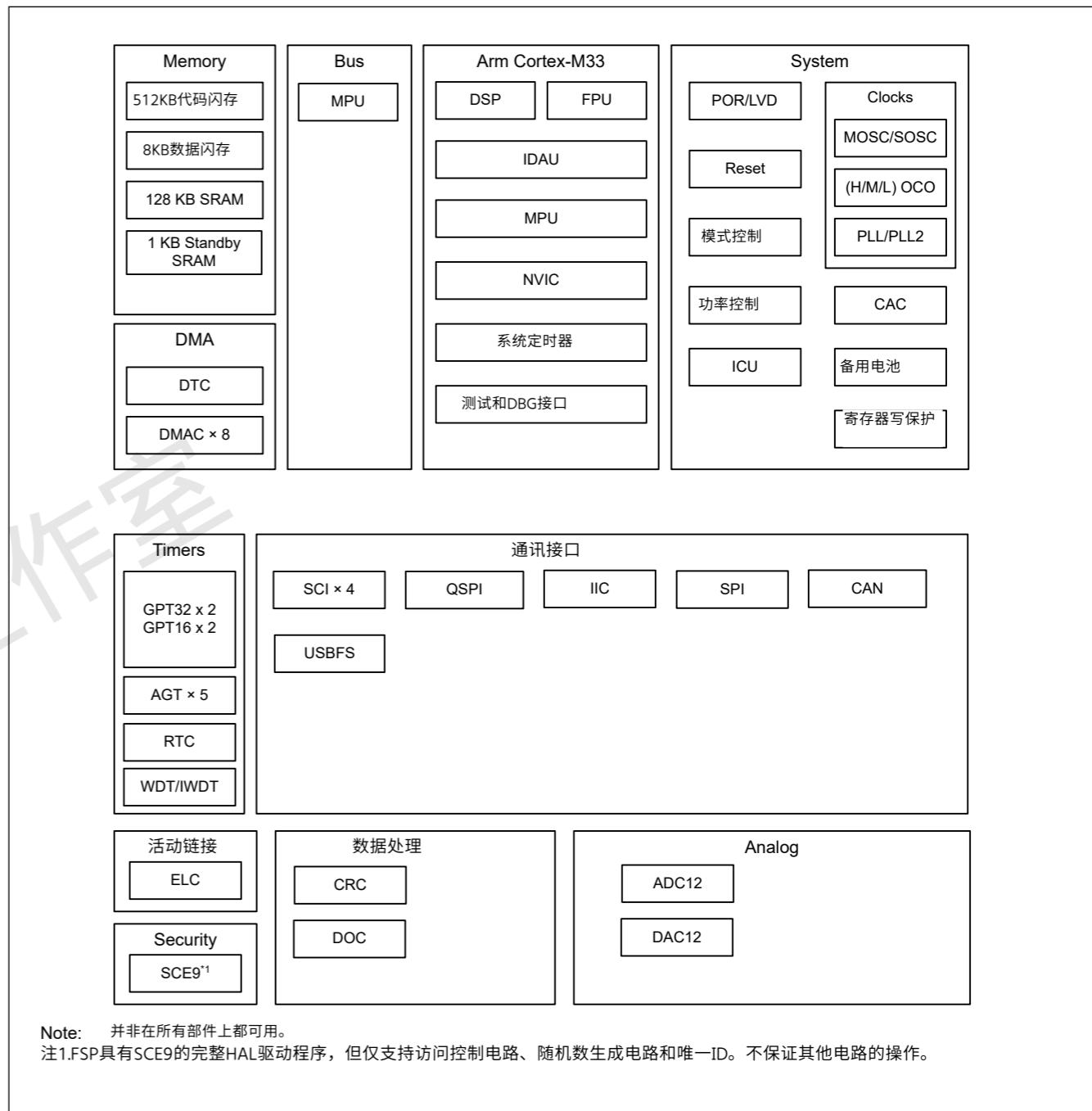


Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.11显示了产品列表。

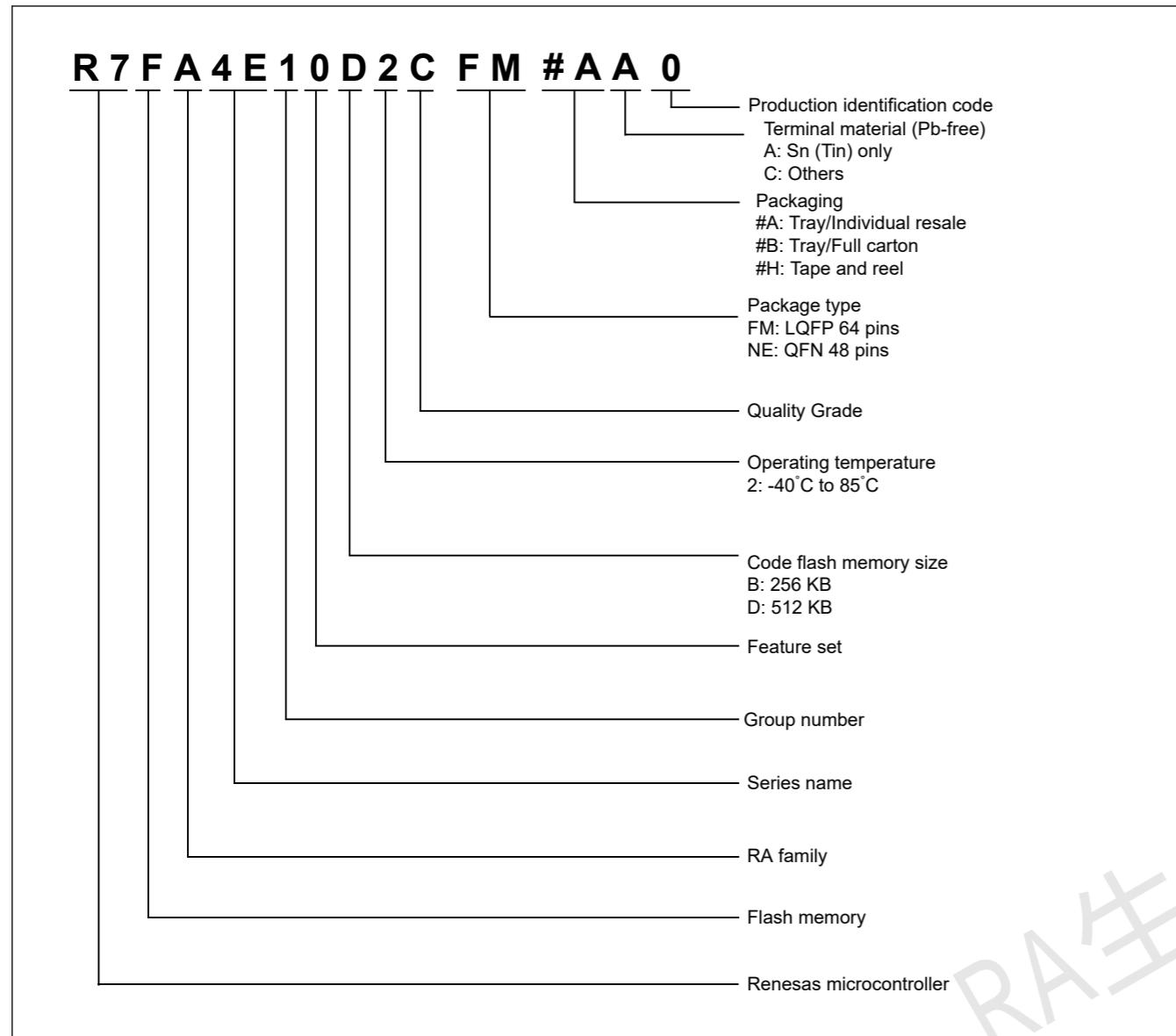


Figure 1.2 Part numbering scheme

Table 1.11 Product list

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---------------------|--------------|------------|------------|--------|-----------------------|
| R7FA4E10D2CFM | PLQP0064KB-C | 512 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10D2CNE | PWQN0048KC-A | | | | |
| R7FA4E10B2CFM | PLQP0064KB-C | 256 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10B2CNE | PWQN0048KC-A | | | | |

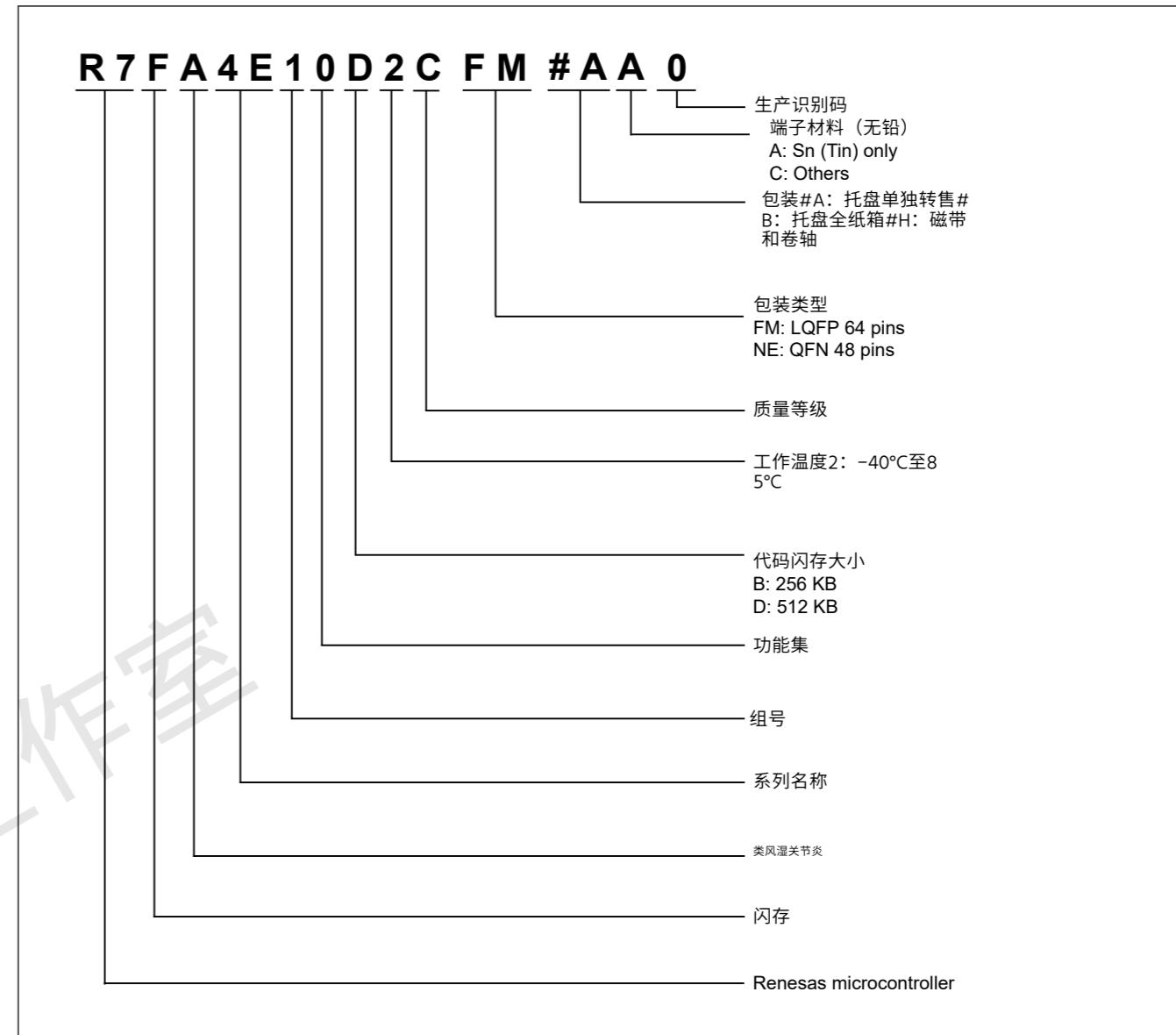


Figure 1.2 零件编号方案

Table 1.11 产品列表

| 产品部件号 | 包装代码 | 代码闪存 | 数据闪存 | SRAM | 工作温度 |
|---------------|--------------|--------|------|--------|--------------|
| R7FA4E10D2CFM | PLQP0064KB-C | 512 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10D2CNE | PWQN0048KC-A | | | | |
| R7FA4E10B2CFM | PLQP0064KB-C | 256 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10B2CNE | PWQN0048KC-A | | | | |

1.4 Function Comparison

Table 1.12 Function Comparison

| Parts number | R7FA4E10D2CFM | R7FA4E10D2CNE | R7FA4E10B2CFM | R7FA4E10B2CNE |
|-------------------|---------------------|--|---------------|---------------|
| Pin count | 64 | 48 | | |
| Package | LQFP | QFN | | |
| Code flash memory | | 512KB 256KB | | |
| Data flash memory | | 8 KB | | |
| SRAM | | 128 KB | | |
| | Parity | 64 KB | | |
| Standby SRAM | | 1 KB | | |
| DMA | DTC | Yes | | |
| | DMAC | 8 | | |
| System | CPU clock | 100 MHz (max.) | | |
| | CPU clock sources | MOSC, SOSC, HOCO, MOCO, LOCO, PLL | | |
| | CAC | Yes | | |
| | WDT/IWDT | Yes | | |
| | Backup register | 128 B | | |
| Communication | SCI ^{*1} | 4 | | |
| | IIC | 1 | | |
| | SPI | 1 | | |
| | CAN | 1 | | |
| | USBFS | Yes | | |
| | QSPI | Yes | No | |
| Timers | GPT32 ^{*1} | 2 | | |
| | GPT16 ^{*1} | 2 | | |
| | AGT ^{*1} | 5 | | |
| | RTC | Yes | | |
| Analog | ADC12 | 9 | | 7 |
| | DAC12 | 1 | | |
| Data processing | CRC | Yes | | |
| | DOC | Yes | | |
| Event control | ELC | Yes | | |
| Security | | SCE9 ^{*2} , TrustZone, and Lifecycle management | | |

Note 1. Available pins depend on the Pin count, about details see [section 1.7. Pin Lists](#).

Note 2. FSP has full HAL drivers for SCE9 but only access control circuit, random number generation circuit and unique ID are supported.
The operation of other circuits is not guaranteed.

1.4 功能比较

Table 1.12 功能比较

| 零件编号 | R7FA4E10D2CFM | R7FA4E10B2CFM | R7FA4E10D2CNE | R7FA4E10B2CNE |
|-----------------|---------------------|---------------------------------------|---------------|---------------|
| 针数 | 64 | 48 | | |
| Package | LQFP | QFN | | |
| 代码闪存 | | 512KB 256KB | | |
| 数据闪存 | | 8 KB | | |
| SRAM | | 128 KB | | |
| | Parity | 64 KB | | |
| Standby SRAM | | 1 KB | | |
| DMA | DTC | Yes | | |
| | DMAC | 8 | | |
| System | 中央处理器时钟 | 100 MHz (max.) | | |
| | CPU时钟源 | MOSC, SOSC, HOCO, MOCO, LOCO, PLL | | |
| | CAC | Yes | | |
| | WDT/IWDT | Yes | | |
| | 备份寄存器 | 128 B | | |
| Communication | SCI ^{*1} | 4 | | |
| | IIC | 1 | | |
| | SPI | 1 | | |
| | CAN | 1 | | |
| | USBFS | Yes | | |
| | QSPI | Yes | No | |
| Timers | GPT32 ^{*1} | 2 | | |
| | GPT16 ^{*1} | 2 | | |
| | AGT ^{*1} | 5 | | |
| | RTC | Yes | | |
| Analog | ADC12 | 9 | | 7 |
| | DAC12 | 1 | | |
| Data processing | CRC | Yes | | |
| | DOC | Yes | | |
| 事件控制 | ELC | Yes | | |
| Security | | SCE9 ^{*2} , TrustZone和生命周期管理 | | |

注1.可用管脚取决于管脚数，详情见1.7节。引脚列表。

注2.FSP具有SCE9的完整HAL驱动程序，但仅支持访问控制电路、随机数生成电路和唯一ID。
不保证其他电路的操作。

1.5 Pin Functions

Table 1.13 Pin functions (1 of 3)

| Function | Signal | I/O | Description |
|------------------------|---------------------------------------|--------|--|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- μ F capacitor. The capacitor should be placed close to the pin. |
| | VCL | I/O | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VBATT | Input | Battery Backup power pin |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCOUT | Output | |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition or release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| On-chip emulator | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | SWO | Output | |
| | SWDIO | I/O | |
| | SWCLK | Input | |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQn | Input | Maskable interrupt request pins |
| | IRQn-DS | Input | Maskable interrupt request pins that can also be used in Deep Software Standby mode |
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pins |
| | GTIOCnA, GTIOCnB | I/O | Input capture, output compare, or PWM output pins |
| AGT | AGTEEn | Input | External event input enable signals |
| | AGTION | I/O | External event input and pulse output pins |
| | AGTOn | Output | Pulse output pins |
| | AGTOAn | Output | Output compare match A output pins |
| | AGTOBn | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock |
| | RTClCn | Input | Time capture event input pins |

1.5 引脚功能

Table 1.13 引脚功能(1of3)

| Function | Signal | I/O | Description |
|------------------|---------------------------------------|--------|---|
| 电源 | VCC | Input | 电源引脚。将其连接到系统电源。通过一个0.1 μ F电容将此引脚连接到VSS。电容应靠近引脚放置。 |
| | VCL | I/O | 通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。 |
| | VBATT | Input | 电池备用电源引脚 |
| | VSS | Input | 接地引脚。将其连接到系统电源(OV)。 |
| Clock | XTAL | Output | 晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。 |
| | EXTAL | Input | |
| | XCIN | Input | 副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。 |
| | XCOUT | Output | |
| | CLKOUT | Output | 时钟输出引脚 |
| 操作模式控制 | MD | Input | 用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。 |
| 系统控制 | RES | Input | 复位信号输入引脚。当该信号变低时，MCU进入复位状态。 |
| CAC | CACREF | Input | 测量参考时钟输入引脚 |
| On-chip emulator | TMS | I/O | 片上仿真器或边界扫描引脚 |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | SWO | Output | |
| | SWDIO | I/O | |
| | SWCLK | Input | |
| Interrupt | NMI | Input | 不可屏蔽中断请求引脚 |
| | IRQn | Input | 可屏蔽中断请求引脚 |
| | IRQn-DS | Input | 可屏蔽中断请求引脚，也可用于Deep Software Standby模式 |
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | 外部触发输入引脚 |
| | GTIOCnA, GTIOCnB | I/O | 输入捕捉、输出比较或PWM输出引脚 |
| AGT | AGTEEn | Input | 外部事件输入使能信号 |
| | AGTION | I/O | 外部事件输入和脉冲输出引脚 |
| | AGTOn | Output | 脉冲输出引脚 |
| | AGTOAn | Output | 输出比较匹配A输出引脚 |
| | AGTOBn | Output | 输出比较匹配B输出引脚 |
| RTC | RTCOUT | Output | 用于1Hz或64Hz时钟的输出引脚 |
| | RTClCn | Input | 时间捕捉事件输入引脚 |

Table 1.13 Pin functions (2 of 3)

| Function | Signal | I/O | Description |
|----------|------------------------------------|--------|---|
| SCI | SCKn | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXDn | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXDn | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTS _n _RTS _n | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low. |
| | CTS _n | Input | Input for the start of transmission. |
| | SCLn | I/O | Input/output pins for the IIC clock (simple IIC mode) |
| | SDAn | I/O | Input/output pins for the IIC data (simple IIC mode) |
| | SCKn | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISOn | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSIn | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| IIC | SCLn | I/O | Input/output pins for the clock |
| | SDAn | I/O | Input/output pins for data |
| SPI | RSPCKA | I/O | Clock input/output pin |
| | MOSIA | I/O | Input or output pins for data output from the master |
| | MISOA | I/O | Input or output pins for data output from the slave |
| | SSLA0 | I/O | Input or output pin for slave selection |
| | SSLA1 to SSLA3 | Output | Output pins for slave selection |
| CAN | CRXn | Input | Receive data |
| | CTXn | Output | Transmit data |
| USBFS | VCC_USB | Input | Power supply pin |
| | VSS_USB | Input | Ground pin |
| | USB_DP | I/O | D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus. |
| | USB_DM | I/O | D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus. |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller. |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA-DS | Input | Overcurrent pins for USBFS that can also be used in Deep Software Standby mode. Connect the external overcurrent detection signals to these pins. |
| QSPI | QSPCLK | Output | QSPI clock output pin |
| | QSSL | Output | QSPI slave output pin |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |

Table 1.13 引脚功能 (2个, 共3个)

| Function | Signal | I/O | Description |
|----------|------------------------------------|--------|---|
| SCI | SCKn | I/O | 时钟输入输出引脚 (时钟同步模式) |
| | RXDn | Input | 接收数据的输入引脚 (异步模式时钟同步模式) |
| | TXDn | Output | 传输数据的输出引脚 (异步模式时钟同步模式) |
| | CTS _n _RTS _n | I/O | 输入输出引脚用于控制发送和接收的开始 (异步模式时钟同步模式)，低电平有效。 |
| | CTS _n | Input | 开始传输的输入。 |
| | SCLn | I/O | IIC时钟的输入输出引脚 (简单IIC模式) |
| | SDAn | I/O | IIC数据的输入输出引脚 (简单IIC模式) |
| | SCKn | I/O | 时钟输入输出引脚 (简单SPI模式) |
| | MISOn | I/O | 用于从机传输数据的输入输出引脚 (简单SPI模式) |
| | MOSIn | I/O | 输入输出引脚用于主数据传输 (简单SPI模式) |
| IIC | SCLn | I/O | 时钟的输入输出引脚 |
| | SDAn | I/O | 数据输入输出引脚 |
| SPI | RSPCKA | I/O | 时钟输入输出引脚 |
| | MOSIA | I/O | 用于从主机输出数据的输入或输出引脚 |
| | MISOA | I/O | 从机数据输出的输入或输出引脚 |
| | SSLA0 | I/O | 从机选择的输入或输出引脚 |
| | SSLA1 to SSLA3 | Output | 从机选择的输出引脚 |
| CAN | CRXn | Input | 接收数据 |
| | CTXn | Output | 传输数据 |
| USBFS | VCC_USB | Input | 电源引脚 |
| | VSS_USB | Input | 接地引脚 |
| | USB_DP | I/O | USB片上收发器的D+引脚。将此引脚连接到USB总线的D+引脚。 |
| | USB_DM | I/O | USB片上收发器的Dpin。将此引脚连接到USB总线的Dpin。 |
| | USB_VBUS | Input | USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测VBUS引脚状态 (连接或断开)。 |
| | USB_VBUSEN | Output | VBUS(5V)为外部供电芯片供电使能信号 |
| | USB_OVRCURA-DS | Input | 也可在DeepSoftware中使用的USBFS过流引脚 待机模式。 将外部过电流检测信号连接到这些引脚。 |
| QSPI | QSPCLK | Output | QSPI时钟输出引脚 |
| | QSSL | Output | QSPI从机输出引脚 |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |

Table 1.13 Pin functions (3 of 3)

| Function | Signal | I/O | Description |
|---------------------|---------------|------------|--|
| Analog power supply | AVCC0 | Input | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin. |
| | AVSS0 | Input | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin. |
| | VREFH | Input | Analog reference voltage supply pin for the D/A Converter. Connect this pin to AVCC0 when not using the D/A Converter. |
| | VREFL | Input | Analog reference ground pin for the D/A Converter. Connect this pin to AVSS0 when not using the D/A Converter. |
| | VREFH0 | Input | Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12. |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12. |
| ADC12 | ANmn | Input | Input pins for the analog signals to be processed by the A/D converter. (m: ADC unit number, n: pin number) |
| | ADTRGm | Input | Input pins for the external trigger signals that start the A/D conversion, active-low. |
| DAC12 | DAn | Output | Output pins for the analog signals processed by the D/A converter. |
| I/O ports | Pmn | I/O | General-purpose input/output pins (m: port number, n: pin number) |
| | P200 | Input | General-purpose input pin |

Table 1.13 引脚功能 (3个中的3个)

| Function | Signal | I/O | Description |
|-----------------|---------------|------------|--|
| 模拟电源 | AVCC0 | Input | 模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。 |
| | AVSS0 | Input | 模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。 |
| | VREFH | Input | 数模转换器的模拟参考电压电源引脚。不使用DA转换器时，将此引脚连接到AVCC0。 |
| | VREFL | Input | DA转换器的模拟参考接地引脚。不使用DA转换器时，将此引脚连接到AVSS0。 |
| | VREFH0 | Input | ADC12的模拟参考电压电源引脚。不使用ADC12时，将此引脚连接到AVCC0。 |
| | VREFL0 | Input | ADC12的模拟参考接地引脚。将此引脚连接到不使用ADC12时为AVSS0。 |
| ADC12 | ANmn | Input | AD转换器要处理的模拟信号的输入引脚。（m: ADC单元编号, n: 引脚编号） |
| | ADTRGm | Input | 用于启动AD转换的外部触发信号的输入引脚，低电平有效。 |
| DAC12 | DAn | Output | 由数模转换器处理的模拟信号的输出引脚。 |
| I/O ports | Pmn | I/O | 通用输入输出引脚（m: 端口号, n: 引脚号） |
| | P200 | Input | 通用输入引脚 |

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

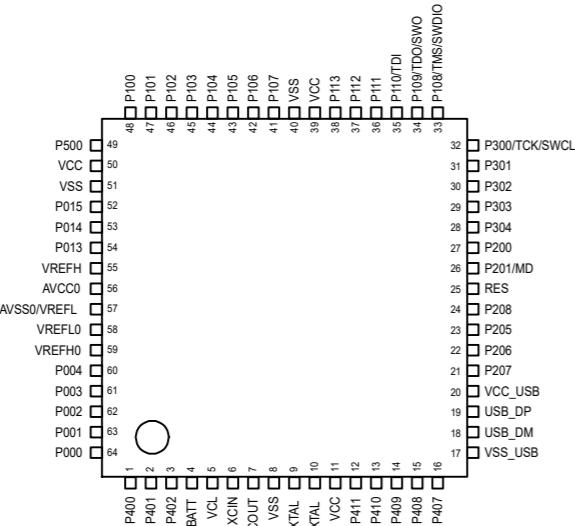


Figure 1.3 Pin assignment for LQFP 64-pin

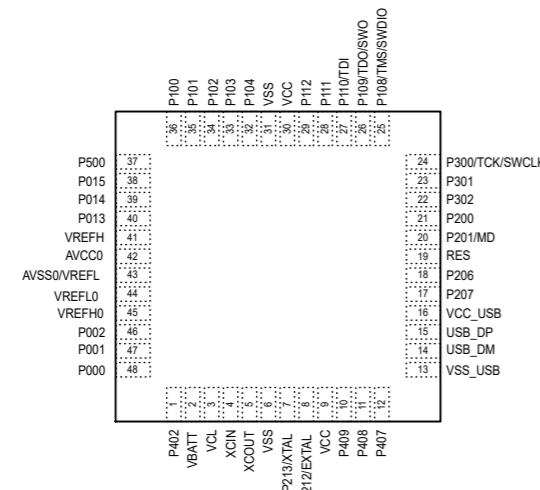


Figure 1.4 Pin assignment for QFN 48-pin

1.6 引脚分配

下图从顶视图显示了引脚分配。

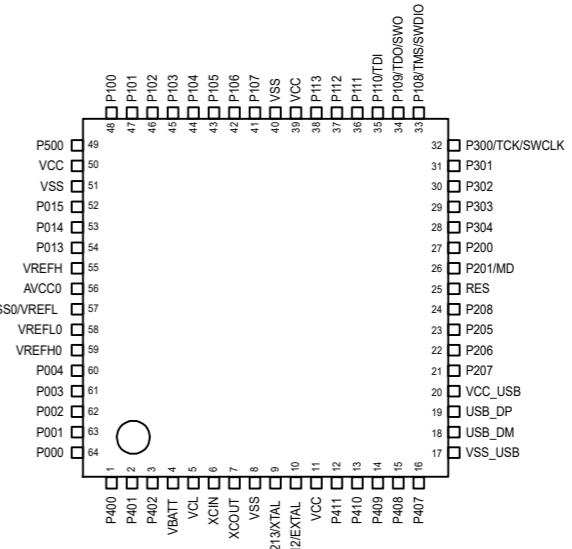


Figure 1.3 LQFP64引脚的引脚分配

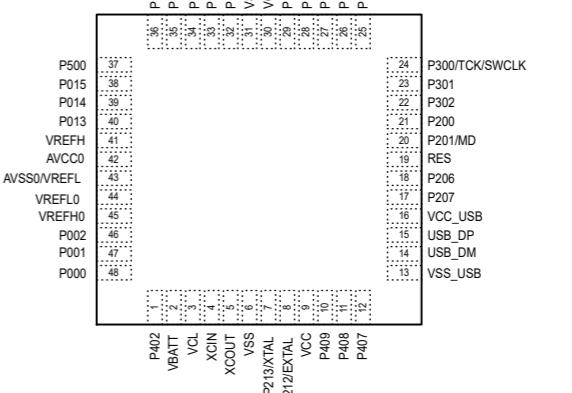


Figure 1.4 QFN48引脚的引脚分配

1.7 Pin Lists

Table 1.14 Pin list (1 of 2)

| LQFP64 QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|-----------------|--|----------------|---------------|---------------------------------|--|------------------------------------|
| 1 | — | P400 | IRQ0 | SCK4/SCL0_A | AGTIO1 | — |
| 2 | — | P401 | IRQ5-DS | CTS4_RTS4/SS4/SDA0_A/CTX0 | GTETRGA | — |
| 3 | 1 | CACREF | P402 | IRQ4-DS | CTS4/CRX0 | AGTIO0/AGTIO1/AGTIO2/AGTIO3/RTCIC0 |
| 4 | 2 | VBATT | — | — | — | — |
| 5 | 3 | VCL | — | — | — | — |
| 6 | 4 | XCIN | — | — | — | — |
| 7 | 5 | XCOUT | — | — | — | — |
| 8 | 6 | VSS | — | — | — | — |
| 9 | 7 | XTAL | P213 | IRQ2 | GTETRGC/AGTEE2 | — |
| 10 | 8 | EXTAL | P212 | IRQ3 | GTETRGD/AGTEE1 | — |
| 11 | 9 | VCC | — | — | — | — |
| 12 | — | P411 | IRQ4 | TXD0/MOSI0/SDA0/CTS3_RTS3/SS3 | AGTOA1 | — |
| 13 | — | P410 | IRQ5 | RXD0/MISO0/SCL0/SCK3 | AGTOB1 | — |
| 14 | 10 | P409 | IRQ6 | TXD3/MOSI3/SDA3 | AGTOA2 | — |
| 15 | 11 | P408 | IRQ7 | CTS4/RXD3/MISO3/SCL3/SCL0_B | AGTOB2 | — |
| 16 | 12 | P407 | — | CTS4_RTS4/SS4/SDA0_B/USB_VBUS | AGTIO0/RTCOUT | ADTRG0 |
| 17 | 13 | VSS_USB | — | — | — | — |
| 18 | 14 | USB_DM | — | — | — | — |
| 19 | 15 | USB_DP | — | — | — | — |
| 20 | 16 | VCC_USB | — | — | — | — |
| 21 | 17 | P207 | — | TXD4/MOSI4/SDA4/QSSL | — | — |
| 22 | 18 | P206 | IRQ0-DS | RXD4/MISO4/SCL4/CTS9/USB_VBUSEN | — | — |
| 23 | — | CLKOUT | P205 | IRQ1-DS | TXD4/MOSI4/SDA4/CTS9_RTS9/SS9/USB_OVRCURA-DS | GTIOC4A/AGTO1 |
| 24 | — | P208 | — | QIO3 | — | — |
| 25 | 19 | RES | — | — | — | — |
| 26 | 20 | MD | P201 | — | — | — |
| 27 | 21 | — | P200 | NMI | — | — |
| 28 | — | P304 | IRQ9 | — | AGTEE2 | — |
| 29 | — | P303 | — | CTS9 | — | — |
| 30 | 22 | — | P302 | IRQ5 | SSLA3 | GTIOC4A |
| 31 | 23 | — | P301 | IRQ6 | CTS9_RTS9/SS9/SSLA2 | GTIOC4B/AGTIO0 |
| 32 | 24 | TCK/SWCLK | P300 | — | SSLA1 | — |
| 33 | 25 | TMS/SWDIO | P108 | — | CTS9_RTS9/SS9/SSLA0 | AGTOA3 |
| 34 | 26 | TDO/SWO/CLKOUT | P109 | — | TXD9/MOSI9/SDA9/MOSIA | GTIOC1A/AGTOB3 |
| 35 | 27 | TDI | P110 | IRQ3 | RXD9/MISO9/SCL9/MISOA | GTIOC1B/AGTEE3 |
| 36 | 28 | — | P111 | IRQ4 | SCK9/RSPCKA | AGTOA5 |
| 37 | 29 | — | P112 | — | SSLA0/QSSL | AGTOB5 |
| 38 | — | P113 | — | — | GTIOC2A/AGTEE5 | — |
| 39 | 30 | VCC | — | — | — | — |
| 40 | 31 | VSS | — | — | — | — |
| 41 | — | P107 | — | — | AGTOA0 | — |
| 42 | — | P106 | — | — | AGTOB0 | — |
| 43 | — | P105 | IRQ0 | — | GTETRGA/GTIOC1A/AGTO2 | — |
| 44 | 32 | — | P104 | IRQ1 | QIO2 | GTETRGB/GTIOC1B/AGTEE2 |
| 45 | 33 | — | P103 | — | CTS0_RTS0/SS0/CTX0/QIO3 | GTIOC2A/AGTIO2 |
| 46 | 34 | — | P102 | — | SCK0/CRX0/QIO0 | GTIOC2B/AGTO0 |
| 47 | 35 | — | P101 | IRQ1 | TXD0/MOSI0/SDA0/QIO1 | GTETRGB/GTIOC5A/AGTEE0 |

1.7 引脚列表

Table 1.14 引脚列表 (1个, 共2个)

| LQFP64 QFN48 | 电源、系统、时钟、调试、CAC | I/O ports | 前段。打断 | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|-----------------|-----------------|----------------|---------|---------------------------------|--|------------------------------------|
| 1 | — | P400 | IRQ0 | SCK4/SCL0_A | AGTIO1 | — |
| 2 | — | P401 | IRQ5-DS | CTS4_RTS4/SS4/SDA0_A/CTX0 | GTETRGA | — |
| 3 | 1 | CACREF | P402 | IRQ4-DS | CTS4/CRX0 | AGTIO0/AGTIO1/AGTIO2/AGTIO3/RTCIC0 |
| 4 | 2 | VBATT | — | — | — | — |
| 5 | 3 | VCL | — | — | — | — |
| 6 | 4 | XCIN | — | — | — | — |
| 7 | 5 | XCOUT | — | — | — | — |
| 8 | 6 | VSS | — | — | — | — |
| 9 | 7 | XTAL | P213 | IRQ2 | — | GTETRGC/AGTEE2 |
| 10 | 8 | EXTAL | P212 | IRQ3 | — | GTETRGD/AGTEE1 |
| 11 | 9 | VCC | — | — | — | — |
| 12 | — | P411 | IRQ4 | TXD0/MOSI0/SDA0/CTS3_RTS3/SS3 | AGTOA1 | — |
| 13 | — | P410 | IRQ5 | RXD0/MISO0/SCL0/SCK3 | AGTOB1 | — |
| 14 | 10 | P409 | IRQ6 | TXD3/MOSI3/SDA3 | AGTOA2 | — |
| 15 | 11 | P408 | IRQ7 | CTS4/RXD3/MISO3/SCL3/SCL0_B | AGTOB2 | — |
| 16 | 12 | P407 | — | CTS4_RTS4/SS4/SDA0_B/USB_VBUS | AGTIO0/RTCOUT | ADTRG0 |
| 17 | 13 | VSS_USB | — | — | — | — |
| 18 | 14 | USB_DM | — | — | — | — |
| 19 | 15 | USB_DP | — | — | — | — |
| 20 | 16 | VCC_USB | — | — | — | — |
| 21 | 17 | P207 | — | TXD4/MOSI4/SDA4/QSSL | — | — |
| 22 | 18 | P206 | IRQ0-DS | RXD4/MISO4/SCL4/CTS9/USB_VBUSEN | — | — |
| 23 | — | CLKOUT | P205 | IRQ1-DS | TXD4/MOSI4/SDA4/CTS9_RTS9/SS9/USB_OVRCURA-DS | GTIOC4A/AGTO1 |
| 24 | — | P208 | — | QIO3 | — | — |
| 25 | 19 | RES | — | — | — | — |
| 26 | 20 | MD | P201 | — | — | — |
| 27 | 21 | — | P200 | NMI | — | — |
| 28 | — | P304 | IRQ9 | — | AGTEE2 | — |
| 29 | — | P303 | — | CTS9 | — | — |
| 30 | 22 | — | P302 | IRQ5 | SSLA3 | GTIOC4A |
| 31 | 23 | — | P301 | IRQ6 | CTS9_RTS9/SS9/SSLA2 | GTIOC4B/AGTIO0 |
| 32 | 24 | TCK/SWCLK | P300 | — | SSLA1 | — |
| 33 | 25 | TMS/SWDIO | P108 | — | CTS9_RTS9/SS9/SSLA0 | AGTOA3 |
| 34 | 26 | TDO/SWO/CLKOUT | P109 | — | TXD9/MOSI9/SDA9/MOSIA | GTIOC1A/AGTOB3 |
| 35 | 27 | TDI | P110 | IRQ3 | RXD9/MISO9/SCL9/MISOA | GTIOC1B/AGTEE3 |
| 36 | 28 | — | P111 | IRQ4 | SCK9/RSPCKA | AGTOA5 |
| 37 | 29 | — | P112 | — | SSLA0/QSSL | AGTOB5 |
| 38 | — | P113 | — | — | GTIOC2A/AGTEE5 | — |
| 39 | 30 | VCC | — | — | — | — |
| 40 | 31 | VSS | — | — | — | — |
| 41 | — | P107 | — | — | AGTOA0 | — |
| 42 | — | P106 | — | — | AGTOB0 | — |
| 43 | — | P105 | IRQ0 | — | GTETRGA/GTIOC1A/AGTO2 | — |
| 44 | 32 | — | P104 | IRQ1 | QIO2 | GTETRGB/GTIOC1B/AGTEE2 |
| 45 | 33 | — | P103 | — | CTS0_RTS0/SS0/CTX0/QIO3 | GTIOC2A/AGTIO2 |
| 46 | 34 | — | P102 | — | SCK0/CRX0/QIO0 | GTIOC2B/AGTO0 |
| 47 | 35 | — | P101 | IRQ1 | TXD0/MOSI0/SDA0/QIO1 | GTETRGB/GTIOC5A/AGTEE0 |

Table 1.14 Pin list (2 of 2)

| LQFP64 QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|-----------------|--|--------------|---------------|----------------------------|------------------------|------------------------|
| 48 | 36 | — | P100 | IRQ2 | RXD0/MISO0/SCL0/QSPCLK | GTETRGA/GTIOC5B/AGTIO0 |
| 49 | 37 | CACREF | P500 | — | USB_VBUSEN/QSPCLK | AGTOA0 |
| 50 | — | VCC | — | — | — | AN016 |
| 51 | — | VSS | — | — | — | — |
| 52 | 38 | — | P015 | IRQ13 | — | AN013 |
| 53 | 39 | — | P014 | — | — | AN012/DA0 |
| 54 | 40 | — | P013 | — | — | AN011 |
| 55 | 41 | VREFH | — | — | — | — |
| 56 | 42 | AVCC0 | — | — | — | — |
| 57 | 43 | AVSS0/VREFL | — | — | — | — |
| 58 | 44 | VREFL0 | — | — | — | — |
| 59 | 45 | VREFH0 | — | — | — | — |
| 60 | — | — | P004 | IRQ9-DS | — | AN004 |
| 61 | — | — | P003 | — | — | AN003 |
| 62 | 46 | — | P002 | IRQ8-DS | — | AN002 |
| 63 | 47 | — | P001 | IRQ7-DS | — | AN001 |
| 64 | 48 | — | P000 | IRQ6-DS | — | AN000 |

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E, and _F. The suffix can be ignored when assigning functionality.

Table 1.14 引脚列表 (2个中的2个)

| LQFP64 QFN48 | 电源、系统、时钟、调试、CAC | I/O ports | 前任。打断 | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|-----------------|-----------------|-------------|-------|----------------------------|------------------------|------------------------|
| 48 | 36 | — | P100 | IRQ2 | RXD0/MISO0/SCL0/QSPCLK | GTETRGA/GTIOC5B/AGTIO0 |
| 49 | 37 | CACREF | P500 | — | USB_VBUSEN/QSPCLK | AGTOA0 |
| 50 | — | VCC | — | — | — | AN016 |
| 51 | — | VSS | — | — | — | — |
| 52 | 38 | — | P015 | IRQ13 | — | AN013 |
| 53 | 39 | — | P014 | — | — | AN012/DA0 |
| 54 | 40 | — | P013 | — | — | AN011 |
| 55 | 41 | VREFH | — | — | — | — |
| 56 | 42 | AVCC0 | — | — | — | — |
| 57 | 43 | AVSS0/VREFL | — | — | — | — |
| 58 | 44 | VREFL0 | — | — | — | — |
| 59 | 45 | VREFH0 | — | — | — | — |
| 60 | — | — | P004 | IRQ9-DS | — | AN004 |
| 61 | — | — | P003 | — | — | AN003 |
| 62 | 46 | — | P002 | IRQ8-DS | — | AN002 |
| 63 | 47 | — | P001 | IRQ7-DS | — | AN001 |
| 64 | 48 | — | P000 | IRQ6-DS | — | AN000 |

Note: 几个引脚名称添加了_A、_B、_C、_D、_E和_F的后缀。分配功能时可以忽略后缀。

2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC = AVCC0 = VCC_USB = VBATT = 2.7$ to 3.6 V
- $2.7 \leq VREFH0/VREFH \leq AVCC0$
- $VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0$ V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

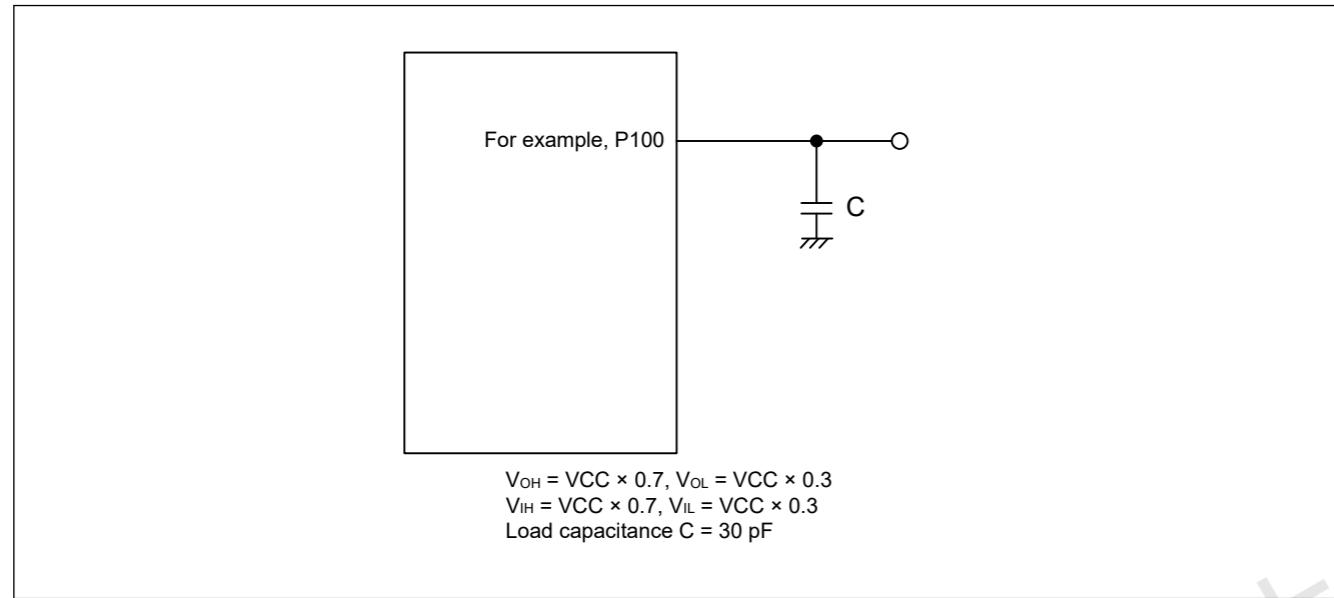


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

| Parameter | Symbol | Value | Unit |
|--|----------------------|----------------------------------|------|
| Power supply voltage | VCC, VCC_USB^{*2} | -0.3 to +4.0 | V |
| VBATT power supply voltage | VBATT | -0.3 to +4.0 | V |
| Input voltage (except for 5 V-tolerant ports ^{*1}) | V_{in} | -0.3 to $VCC + 0.3$ | V |
| Input voltage (5 V-tolerant ports ^{*1}) | V_{in} | -0.3 to + $VCC + 4.0$ (max. 5.8) | V |
| Reference power supply voltage | $VREFH/VREFH0$ | -0.3 to $VCC + 0.3$ | V |
| Analog power supply voltage | $AVCC0^{*2}$ | -0.3 to +4.0 | V |
| Analog input voltage | V_{AN} | -0.3 to $AVCC0 + 0.3$ | V |
| Operating temperature ^{*3 *4} | T_{opr} | -40 to +85 | °C |
| Storage temperature | T_{stg} | -55 to +125 | °C |

Note 1. Ports P205, P206, P400, P401, and P407 to P411 are 5 V tolerant.

Note 2. Connect $AVCC0$ and VCC_USB to VCC .

Note 3. See section 2.2.1. T_j/T_a Definition.

Note 4. Contact a Renesas Electronics sales office for information on derating operation when $T_a = +85^\circ\text{C}$. Derating is the systematic reduction of load for improved reliability.

2. 电气特性

支持的外围功能和引脚因产品名称而异。

除非另有规定，MCU的电气特性在以下条件下定义：

- $VCC = AVCC0 = VCC_USB = VBATT = 2.7$ to 3.6 V
- $2.7 \leq VREFH0/VREFH \leq AVCC0$
- $VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0$ V
- $T_a = T_{opr}$

图2.1显示了时序条件。

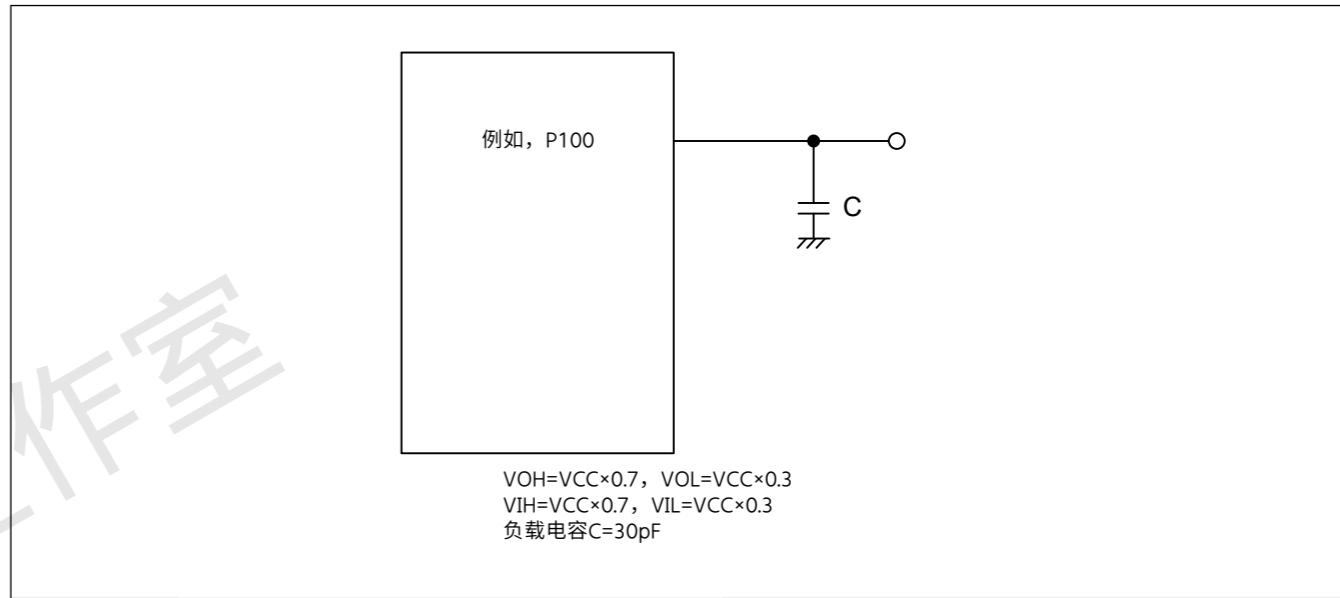


Figure 2.1 输入或输出定时测量条件

所提供的每个外设时序规范的推荐测量条件是为了实现最佳外设操作。确保调整每个引脚的驱动能力以满足您的条件。

2.1 绝对最大额定值

Table 2.1 绝对最大额定值

| Parameter | Symbol | Value | Unit |
|-----------------------|----------------------|----------------------------------|------|
| 电源电压 | VCC, VCC_USB^{*2} | -0.3 to +4.0 | V |
| VBATT电源电压 | VBATT | -0.3 to +4.0 | V |
| 输入电压 (5V容限端口*1除外) | V_{in} | -0.3 to $VCC + 0.3$ | V |
| 输入电压 (5V耐压端口*1) | V_{in} | -0.3 to + $VCC + 4.0$ (max. 5.8) | V |
| 参考电源电压 | $VREFH/VREFH0$ | -0.3 to $VCC + 0.3$ | V |
| 模拟电源电压 | $AVCC0^{*2}$ | -0.3 to +4.0 | V |
| 模拟输入电压 | V_{AN} | -0.3 to $AVCC0 + 0.3$ | V |
| 工作温度 ^{*3 *4} | T_{opr} | -40 to +85 | °C |
| 贮存温度 | T_{stg} | -55 to +125 | °C |

注1. 端口P205、P206、P400、P401和P407至P411可承受5V电压。

注2. 将 $AVCC0$ 和 VCC_USB 连接到 VCC 。

注3. 见第2.2.1节。 T_j/T_a 定义。

注4. 有关在 $T_a=+85^\circ\text{C}$ 时降额操作的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|------------------------------|---------------------|----------------------|-----|-----|-----|------|
| Power supply voltages | VCC | When USB is not used | 2.7 | — | 3.6 | V |
| | | When USB is used | 3.0 | — | 3.6 | V |
| | VSS | — | 0 | — | — | V |
| USB power supply voltages | VCC_USB | — | VCC | — | — | V |
| | VSS_USB | — | 0 | — | — | V |
| VBATT power supply voltage | VBATT | 1.65 ² | — | 3.6 | — | V |
| Analog power supply voltages | AVCC0 ^{*1} | — | VCC | — | — | V |
| | AVSS0 | — | 0 | — | — | V |

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Note 2. Low CL crystal cannot be used below VBATT = 1.8V.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +85°C

| Parameter | Symbol | Typ | Max | Unit | Test conditions |
|----------------------------------|----------------|-----|-----|------|--|
| Permissible junction temperature | T _j | — | 105 | °C | High-speed mode Low-speed mode Subosc-speed mode |

Note: Make sure that T_j = T_a + θ_{ja} × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CCmax} × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------------------|--|-----------------|-----------|---------------------|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL (external clock input), SPI (except RSPCK) | V _{IH} | VCC × 0.8 | — |
| | | | V _{IL} | — | VCC × 0.2 |
| | | IIC (SMBus) | V _{IH} | 2.1 | VCC + 3.6 (max 5.8) |
| | | | V _{IL} | — | 0.8 |

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Table 2.2 推荐工作条件

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|-----------|---------|---------|---------------------|-----|-----|------|
| 电源电压 | VCC | 不使用USB时 | 2.7 | — | 3.6 | V |
| | | 使用USB时 | 3.0 | — | 3.6 | V |
| VSS | VCC_USB | — | 0 | — | — | V |
| | | VSS_USB | — | 0 | — | V |
| VBATT电源电压 | VBATT | — | 1.65 ² | — | 3.6 | V |
| | | 模拟电源电压 | AVCC0 ^{*1} | — | VCC | V |
| AVSS0 | AVSS0 | — | 0 | — | — | V |

注1. 将AVCC0连接到VCC。不使用AD转换器和DA转换器时，不要离开AVCC0、VREFHVREFH0、AVSS0和VREFLVREFL0引脚打开。将AVCC0和VREFHVREFH0引脚连接到VCC，以及AVSS0和VREFLVREFL0引脚分别连接到VSS。

注2. 低于VBATT=1.8V时不能使用低CL晶振。

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics

条件：工作温度(T_a) -40至+85°C的产品

| Parameter | Symbol | Typ | Max | Unit | 测试条件 |
|-----------|----------------|-----|-----|------|--|
| 允许结温 | T _j | — | 105 | °C | High-speed mode Low-speed mode Subosc-speed mode |

Note: 确保T_j=T_a+θ_{ja}×总功耗(W)，其中总功耗=(VCCVOH)×ΣI_{OH}+V_{OL}×ΣI_{OL}+I_{CCmax}×VCC。

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 IOVIH VIL(1of2)

| Parameter | Symbol | 最小值 | Typ | Max | Unit |
|--------------------|-------------|------------------------------|-----------------|-----------|---------------------|
| 输入电压（施密特触发器输入引脚除外） | 外设功能引脚 | EXTAL (外部时钟输入)，SPI (RSPCK除外) | V _{IH} | VCC × 0.8 | — |
| | | | V _{IL} | — | VCC × 0.2 |
| | IIC (SMBus) | IIC (SMBus) | V _{IH} | 2.1 | VCC + 3.6 (max 5.8) |
| | | | V _{IL} | — | 0.8 |

Table 2.4 I/O V_{IH} , V_{IL} (2 of 2)

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|-------------------------------|-------------------------|--|--|-------------------|------------------------|-----------------------|---|
| Schmitt trigger input voltage | Peripheral function pin | IIC (except for SMBus) | V_{IH} | $VCC \times 0.7$ | — | $VCC + 3.6$ (max 5.8) | V |
| | | | V_{IL} | — | — | $VCC \times 0.3$ | |
| | | | ΔV_T | $VCC \times 0.05$ | — | — | |
| | | 5 V-tolerant ports*1 *5 | V_{IH} | $VCC \times 0.8$ | — | $VCC + 3.6$ (max 5.8) | |
| | | | V_{IL} | — | — | $VCC \times 0.2$ | |
| | | | ΔV_T | $VCC \times 0.05$ | — | — | |
| | | RTCIC0 | When using the Battery Backup Function | V_{IH} | $V_{BATT} \times 0.8$ | — | $V_{BATT} + 0.3$ |
| | | | | V_{IL} | — | — | $V_{BATT} \times 0.2$ |
| | | | | ΔV_T | $V_{BATT} \times 0.05$ | — | — |
| | | | When VCC power supply is selected | V_{IH} | $VCC \times 0.8$ | — | Higher voltage either $VCC + 0.3$ V or $V_{BATT} + 0.3$ V |
| | | | | V_{IL} | — | — | $VCC \times 0.2$ |
| | | | | ΔV_T | $VCC \times 0.05$ | — | — |
| | | When not using the Battery Backup Function | V_{IH} | $VCC \times 0.8$ | — | $VCC + 0.3$ | |
| | | | V_{IL} | — | — | $VCC \times 0.2$ | |
| | | | ΔV_T | $VCC \times 0.05$ | — | — | |
| | | Other input pins*2 | V_{IH} | $VCC \times 0.8$ | — | — | |
| | | | V_{IL} | — | — | $VCC \times 0.2$ | |
| | | | ΔV_T | $VCC \times 0.05$ | — | — | |
| Ports | 5 V-tolerant ports*3 *5 | V_{IH} | $VCC \times 0.8$ | — | $VCC + 3.6$ (max 5.8) | V | |
| | | V_{IL} | — | — | $VCC \times 0.2$ | | |
| | Other input pins*4 | V_{IH} | $VCC \times 0.8$ | — | — | | |
| | | V_{IL} | — | — | $VCC \times 0.2$ | | |

Note 1. RES and peripheral function pins associated with Ports P205, P206, P400, P401, and P407 to P411 (total 10 pins).

Note 2. All input pins except for the peripheral function pins already described in the table.

Note 3. Ports P205, P206, P400, P401, and P407 to P411 (total 9 pins).

Note 4. All input pins except for the ports already described in the table.

Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

Table 2.4 IOVIH VIL(2of2)

| Parameter | | | 符号最小值 | Typ | Max | Unit |
|------------|-------------------------|-------------------------|------------------|------------------------|-----------------------|-------------------------------------|
| 施密特触发器输入电压 | 外设功能引脚 | IIC (except for SMBus) | V_{IH} | $VCC \times 0.7$ | — | $VCC + 3.6$ (max 5.8) |
| | | | V_{IL} | — | — | $VCC \times 0.3$ |
| | | | ΔV_T | $VCC \times 0.05$ | — | — |
| | | 5 V-tolerant ports*1 *5 | V_{IH} | $VCC \times 0.8$ | — | $VCC + 3.6$ (max 5.8) |
| | | | V_{IL} | — | — | $VCC \times 0.2$ |
| | | | ΔV_T | $VCC \times 0.05$ | — | — |
| | | RTCICO使用时备用电池Function | V_{IH} | $V_{BATT} \times 0.8$ | — | $V_{BATT} + 0.3$ |
| | | | V_{IL} | — | — | $V_{BATT} \times 0.2$ |
| | | | ΔV_T | $V_{BATT} \times 0.05$ | — | — |
| | | 选择VCC电源时 | V_{IH} | $VCC \times 0.8$ | — | 更高的电压 $V_{CC+0.3}$ 或 $V_{BATT+0.3}$ |
| | | | V_{IL} | — | — | $VCC \times 0.2$ |
| | | | ΔV_T | $VCC \times 0.05$ | — | — |
| | | 不使用备用电池时Function | V_{IH} | $VCC \times 0.8$ | — | $VCC + 0.3$ |
| | | | V_{IL} | — | — | $VCC \times 0.2$ |
| | | | ΔV_T | $VCC \times 0.05$ | — | — |
| | | 其他输入引脚*2 | V_{IH} | $VCC \times 0.8$ | — | — |
| | | | V_{IL} | — | — | $VCC \times 0.2$ |
| | | | ΔV_T | $VCC \times 0.05$ | — | — |
| Ports | 5 V-tolerant ports*3 *5 | V_{IH} | $VCC \times 0.8$ | — | $VCC + 3.6$ (max 5.8) | V |
| | | V_{IL} | — | — | $VCC \times 0.2$ | |
| | 其他输入引脚*4 | V_{IH} | $VCC \times 0.8$ | — | — | |
| | | V_{IL} | — | — | $VCC \times 0.2$ | |

注1.与端口P205、P206、P400、P401和P407至P411相关的RES和外围功能引脚（共10个引脚）。

注2.除表中已描述的外围功能引脚外的所有输入引脚。

注3.端口P205、P206、P400、P401、P407～P411（共9针）。注4.除表中已描述的端口外的所有输入引脚。

注5.当VCC小于2.7V时，5V容限端口的输入电压应小于3.6V，否则可能发生击穿，因为5V容限端口是电气控制的，以免违反击穿电压。

2.2.3 I/O I_{OH} , I_{OL} Table 2.5 I/O I_{OH} , I_{OL}

| Parameter | | Symbol | Min | Typ | Max | Unit |
|--|---|------------------------------|-----|-----|------|------|
| Permissible output current (average value per pin) | Ports P000 to P004, P013 to P015, P201 | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | Ports P205, P206, P407 to P411 (total 7 pins) | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | Low drive* ¹ | I_{OH} | — | — | -2.0 | mA |
| | Middle drive* ² | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | High drive* ³ | I_{OH} | — | — | -20 | mA |
| | | I_{OL} | — | — | 20 | mA |
| | Other output pins* ⁴ | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | Low drive* ¹ | I_{OH} | — | — | -2.0 | mA |
| | Middle drive* ² | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | High drive* ³ | I_{OH} | — | — | -16 | mA |
| | | I_{OL} | — | — | 16 | mA |
| Permissible output current (max value per pin) | Ports P000 to P004, P013 to P015, P201 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | Ports P205, P206, P407 to P411 (total 7 pins) | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | Low drive* ¹ | I_{OH} | — | — | -4.0 | mA |
| | Middle drive* ² | I_{OH} | — | — | -8.0 | mA |
| | | I_{OL} | — | — | 8.0 | mA |
| | High drive* ³ | I_{OH} | — | — | -40 | mA |
| | | I_{OL} | — | — | 40 | mA |
| | Other output pins* ⁴ | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | Low drive* ¹ | I_{OH} | — | — | -4.0 | mA |
| | Middle drive* ² | I_{OH} | — | — | -8.0 | mA |
| | | I_{OL} | — | — | 8.0 | mA |
| | High drive* ³ | I_{OH} | — | — | -32 | mA |
| | | I_{OL} | — | — | 32 | mA |
| Permissible output current (maxvalue of total of all pins) | Maximum of all output pins | $\Sigma I_{OH} (\text{max})$ | — | — | -80 | mA |
| | | $\Sigma I_{OL} (\text{max})$ | — | — | 80 | mA |

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. Except for P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table.
The average output current indicates the average value of current measured during 100 μs .

2.2.3 我爱我哦

Table 2.5 我爱我哦

| Parameter | | Symbol | 最小值 | 典型值 | 最大值 | 单位 |
|---------------------|-------------------------------|------------------------------|-----|-----|------|----|
| 允许输出电流 (每个引脚的平均值) | 端口P000至P004、P013至P015、P201 | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | 端口P205、P206、P407至P411 (共7个引脚) | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | 低驱动*1 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 中间驱动器*2 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 高速驱动*3 | I_{OH} | — | — | -20 | mA |
| | | I_{OL} | — | — | 20 | mA |
| | 其他输出引脚*4 | I_{OH} | — | — | -2.0 | mA |
| | | I_{OL} | — | — | 2.0 | mA |
| | 低驱动*1 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 中间驱动器*2 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 高速驱动*3 | I_{OH} | — | — | -16 | mA |
| | | I_{OL} | — | — | 16 | mA |
| 允许输出电流 (每个引脚的最大值) | 端口P000至P004、P013至P015、P201 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 端口P205、P206、P407至P411 (共7个引脚) | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 低驱动*1 | I_{OH} | — | — | -8.0 | mA |
| | | I_{OL} | — | — | 8.0 | mA |
| | 中间驱动器*2 | I_{OH} | — | — | -40 | mA |
| | | I_{OL} | — | — | 40 | mA |
| | 高速驱动*3 | I_{OH} | — | — | -32 | mA |
| | | I_{OL} | — | — | 32 | mA |
| | 其他输出引脚*4 | I_{OH} | — | — | -4.0 | mA |
| | | I_{OL} | — | — | 4.0 | mA |
| | 低驱动*1 | I_{OH} | — | — | -8.0 | mA |
| | | I_{OL} | — | — | 8.0 | mA |
| | 中间驱动器*2 | I_{OH} | — | — | -32 | mA |
| | | I_{OL} | — | — | 32 | mA |
| 允许输出电流 (所有引脚总和的最大值) | 所有输出引脚的最大值 | $\Sigma I_{OH} (\text{max})$ | — | — | -80 | mA |
| | | $\Sigma I_{OL} (\text{max})$ | — | — | 80 | mA |

注1.这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注2.这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注3.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注4.P200除外，它是一个输入端口。

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。

平均输出电流表示在100 μs 期间测量的电流平均值。

2.2.4 I/O V_{OH} , V_{OL} , and Other CharacteristicsTable 2.6 I/O V_{OH} , V_{OL} , and other characteristics

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------|---|--------------|-----------|-----|-----|---------------|--|
| Output voltage | IIC | V_{OL} | — | — | 0.4 | V | $I_{OL} = 3.0 \text{ mA}$ |
| | | V_{OL} | — | — | 0.6 | | $I_{OL} = 6.0 \text{ mA}$ |
| | IIC ^{*1} | V_{OL} | — | — | 0.4 | | $I_{OL} = 15.0 \text{ mA (ICFER.FMPE = 1)}$ |
| | | V_{OL} | — | 0.4 | — | | $I_{OL} = 20.0 \text{ mA (ICFER.FMPE = 1)}$ |
| | Ports P205, P206, P407 to P411 (total 7 pins) ^{*2} | V_{OH} | VCC – 1.0 | — | — | | $I_{OH} = -20 \text{ mA}$ VCC = 3.3 V |
| | | V_{OL} | — | — | 1.0 | | $I_{OL} = 20 \text{ mA}$ VCC = 3.3 V |
| | | V_{OH} | VCC – 0.5 | — | — | | $I_{OH} = -1.0 \text{ mA}$ |
| | | V_{OL} | — | — | 0.5 | | $I_{OL} = 1.0 \text{ mA}$ |
| | Other output pins | V_{OH} | VCC – 0.5 | — | — | | |
| | | V_{OL} | — | — | 0.5 | | |
| Input leakage current | RES | $ I_{inl} $ | — | — | 5.0 | μA | $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | Port P200 | | — | — | 1.0 | | $V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$ |
| | 5 V-tolerant ports (off state) | $ I_{tsil} $ | — | — | 5.0 | μA | $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | | | — | — | 1.0 | | $V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$ |
| Input pull-up MOS current | Ports P0 to P5 | I_p | -300 | — | -10 | μA | VCC = 2.7 to 3.6 V $V_{in} = 0 \text{ V}$ |
| Input capacitance | USB_DP, USB_DM, and ports P014, P015, P400, P401 | C_{in} | — | — | 16 | pF | $V_{bias} = 0 \text{ V}$ $V_{amp} = 20 \text{ mV}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$ |
| | Other input pins | | — | — | 8 | | |

Note 1. SCL0_A, SDA0_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register.

The selected driving ability is retained in Deep Software Standby mode.

2.2.4 IOVOH VOL和其他特性

Table 2.6 IOVOH、VOL和其他特性

| Parameter | | | 符号最小值 | 典型最大单元测试条件 |
|-----------|--|--------------------|--------------|---|
| 输出电压 | IIC | V_{OL} | — | — 0.4 V 我OL=3.0毫安 |
| | | V_{OL} | — | — 0.6 V 我OL=6.0毫安 |
| | IIC ^{*1} | V_{OL} | — | — 0.4 V IOL=15.0mA(ICFER.FMPE=1) |
| | | V_{OL} | — | 0.4 — V IOL=20.0mA(ICFER.FMPE=1) |
| | 端口P205、P206、P407至P411 (total 7 pins) ^{*2} | V_{OH} | VCC – 1.0 | — — IOH= 20mAV CC=3.3V |
| | | V_{OL} | — | — 1.0 V 我OL=20毫安VCC=3.3V |
| | | V_{OH} | VCC – 0.5 | — — IOH= 1.0毫安 |
| | | V_{OL} | — | — 0.5 V 我OL=1毫安 |
| | 其他输出引脚 | V_{OH} | VCC – 0.5 | — — |
| | | V_{OL} | — | — 0.5 V |
| 输入漏电流 | RES | $ I_{inl} $ | — | — 5.0 μA $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | Port P200 | | — | — 1.0 $V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$ |
| | 三态漏电流 (关闭状态) | 5 V-tolerant ports | $ I_{tsil} $ | — — 5.0 μA $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | | 其他港口 (港口除外) P200 | | — — 1.0 $V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$ |
| 输入上拉MOS电流 | 端口P0至P5 | I_p | -300 | — -10 μA VCC = 2.7 to 3.6 V $V_{in} = 0 \text{ V}$ |
| 输入电容 | USB_DP、USB_DM和端口 P014, P015, P400, P401 | C_{in} | — | — 16 pF $V_{bias} = 0 \text{ V}$ $V_{amp}=20mVf=1MHzTa=25^\circ\text{C}$ |
| | 其他输入引脚 | | — | — 8 C |

Note 1. SCL0_A, SDA0_A (total 2 pins).

注2.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。

在深度软件待机模式下会保留所选的驾驶能力。

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

| Parameter | | | | | Symbol | Min | Typ | Max | Unit | Test conditions | | | |
|------------------------------|---|--|--|--|------------------|-----|--------------------------|-------------------------|--|-------------------------------|--|--|--|
| Supply current ^{*1} | High-speed mode | Maximum ^{*2 *13} | | | | — | — | 65 | mA | I _{CC} ^{*3} | | | |
| | | CoreMark ^{®*5 *6 *12 *14} | | | | — | 8.1 | — | mA | | | | |
| | | Normal mode | All peripheral clocks enabled, while (1) code executing from flash ^{*4 *12} | | | — | 15.4 | — | mA | | | | |
| | | | All peripheral clocks disabled, while (1) code executing from flash ^{*5 *6 *12 *14} | | | — | 6.1 | — | mA | | | | |
| | | Sleep mode ^{*5 *14} | | | | — | 4.4 ^{*6} *12 | 25 ^{*7} *13 | mA | | | | |
| | | Increase during BGO operation | Data flash P/E | | | — | 6 | — | mA | | | | |
| | | | Code flash P/E | | | — | 8 | — | mA | | | | |
| | | Low-speed mode ^{*5 *10} | | | | — | 0.8 | — | mA | | | | |
| | | Subosc-speed mode ^{*5 *11} | | | | — | 0.7 | — | mA | | | | |
| | | Software Standby mode | SNZCR.RXDREQEN = 1 | | | — | — | 14 | mA | | | | |
| | | | SNZCR.RXDREQEN = 0 | | | — | 0.7 | — | mA | | | | |
| | Deep Software Standby mode | Power supplied to Standby SRAM and USB resume detecting unit | | | | — | 16 | 96 | µA | | | | |
| | | Power not supplied to SRAM or USB resume detecting unit | Power-on reset circuit low power function disabled | | | — | 12 | 27 | µA | | | | |
| | | | Power-on reset circuit low power function enabled | | | — | 5 | 17 | µA | | | | |
| | | Increase when the RTC and AGT are operating | When the low-speed on-chip oscillator (LOCO) is in use | | | — | 4.4 | — | µA | | | | |
| | | | When a crystal oscillator for low clock loads is in use | | | — | 1.0 | — | µA | | | | |
| | | | When a crystal oscillator for standard clock loads is in use | | | — | 1.6 | — | µA | | | | |
| | | RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | — | 0.6 | — | µA | V _{BATT} = 1.8 V, V _{CC} = 0 V | | | | |
| | | | | When a crystal oscillator for standard clock loads is in use | — | 1.2 | — | µA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | | |
| | | | | | — | 1.1 | — | µA | V _{BATT} = 1.8 V, V _{CC} = 0 V | | | | |
| | | | | | — | 1.8 | — | µA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | | |
| | Inrush current on returning from deep software standby mode | | Inrush current ^{*8} | I _{RUSH} | — | 160 | — | mA | | | | | |
| | | | Energy of inrush current ^{*8} | E _{RUSH} | — | 1.0 | — | µC | | | | | |
| Analog power supply current | During 12-bit A/D conversion | | | | AI _{CC} | — | 0.8 | 1.1 | mA | — | | | |
| | During D/A conversion | | Without AMP output | — | | 0.1 | 0.2 | mA | — | | | | |
| | | | With AMP output | — | | 0.6 | 1.1 | mA | — | | | | |
| | Waiting for A/D, D/A conversion | | | | | — | 0.5 | 1.0 | mA | — | | | |
| | ADC12, DAC12 in standby modes ^{*9} | | | | | — | 0.4 | 4.0 | µA | — | | | |

2.2.5 工作和待机电流

Table 2.7 工作和待机电流(1of2)

| Parameter | | | | | Symbol | Min | Typ | Max | 单元 | 测试条件 | | | |
|--------------------|-------------------|--|--|-------------------|------------------|------------------------------|--------------------------|-------------------------|-----|--|--|--|--|
| 供电电流 ^{*1} | High-speed mode | Maximum ^{*2 *13} | | | | — | — | 65 | mA | I _{CC} ^{*3} | | | |
| | | CoreMark ^{®*5 *6 *12 *14} | | | | — | 8.1 | — | mA | | | | |
| | | Normal mode | All peripheral clocks enabled, while (1) code executing from flash ^{*4 *12} | | | — | 15.4 | — | mA | | | | |
| | | | All peripheral clocks disabled, while (1) code executing from flash ^{*5 *6 *12 *14} | | | — | 6.1 | — | mA | | | | |
| | | Sleep mode ^{*5 *14} | | | | — | 4.4 ^{*6} *12 | 25 ^{*7} *13 | mA | | | | |
| | | Increase during BGO operation | Data flash P/E | | | — | 6 | — | mA | | | | |
| | | | Code flash P/E | | | — | 8 | — | mA | | | | |
| | | Low-speed mode ^{*5 *10} | | | | — | 0.8 | — | mA | ICLK = 1 MHz | | | |
| | | Subosc-speed mode ^{*5 *11} | | | | — | 0.7 | — | mA | ICLK = 32.768 kHz | | | |
| | | 软件待机模式 | SNZCR.RXDREQEN = 1 | | | — | — | 14 | mA | | | | |
| | | | SNZCR.RXDREQEN = 0 | | | — | 0.7 | — | mA | | | | |
| | Deep 软件待机模式 | 为备用SRAM和USB恢复检测单元供电 | | | | — | 16 | 96 | µA | | | | |
| | | 未向SRAM或USB恢复检测单元供电 | 上电复位电路低功耗功能禁用 | | | — | 12 | 27 | µA | | | | |
| | | | 上电复位电路低功耗功能启用 | | | — | 5 | 17 | µA | | | | |
| | | | RTC和AGT运行时间增加 | 使用低速片上振荡器(LOCO)时 | | — | 4.4 | — | µA | | | | |
| | | | | 当使用用于低时钟负载的晶体振荡器时 | | — | 1.0 | — | µA | | | | |
| | | | | 当使用标准时钟负载的晶体振荡器时 | | — | 1.6 | — | µA | | | | |
| | | VCC关闭时RTC运行 (具有电池备份功能, 只有RTC和副时钟振荡器运行) | | | | — | 0.6 | — | µA | V _{BATT} = 1.8 V, V _{CC} = 0 V | | | |
| | | | | | | — | 1.2 | — | µA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | |
| | | | | | | — | 1.1 | — | µA | V _{BATT} = 1.8 V, V _{CC} = 0 V | | | |
| | | | | | | — | 1.8 | — | µA | V _{BATT} = 3.3 V, V _{CC} = 0 V | | | |
| | 从深度软件待机模式返回时的浪涌电流 | | | | AI _{CC} | Inrush current ^{*8} | — | 160 | — | mA | | | |
| | | | | | | 浪涌电流能量 ^{*8} | — | 1.0 | — | µC | | | |
| | | | | | | 在12位AD转换期间 | — | 0.8 | 1.1 | mA | | | |
| | | | | | | DA转换期间 | — | 0.1 | 0.2 | mA | | | |
| | | | | | | 无AMP输出 | — | 0.6 | 1.1 | mA | | | |
| | | | | | | 带AMP输出 | — | 0.5 | 1.0 | mA | | | |
| | | | | | | 等待AD, DA转换 | — | 0.4 | 4.0 | µA | | | |
| | | | | | | 待机模式下的ADC12、DAC12*9 | — | — | — | — | | | |

Table 2.7 Operating and standby current (2 of 2)

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|---|-----------------------------------|--|--------------------|------------------------|-----|------|------|------|-----------------|--|--|
| Reference power supply current (VREFH0) | During 12-bit A/D conversion | | | AI _{REFH0} | — | 70 | 120 | μA | — | | |
| | Waiting for 12-bit A/D conversion | | | | — | 0.07 | 0.5 | μA | — | | |
| | ADC12 in standby modes | | | | — | 0.07 | 0.5 | μA | — | | |
| Reference power supply current (VREFH) | During D/A conversion | | Without AMP output | AI _{REFH} | — | 0.1 | 0.4 | mA | — | | |
| | | | With AMP output | | — | 0.1 | 0.4 | mA | — | | |
| | Waiting for D/A conversion | | | | — | 0.07 | 0.8 | μA | — | | |
| USB operating current | Low speed | | USB | I _{CCUSBL} | — | 3.5 | 6.5 | mA | VCC_USB | | |
| | Full speed | | USB | I _{CCUSBFS} | — | 4.0 | 10.0 | mA | VCC_USB | | |
| LDO operating current (per unit) ^{*15} | | | | I _{CCLDO} | — | 0.18 | — | mA | — | | |
| PLL2-LDO operating current | | | | I _{CCPLL2LDO} | — | 0.21 | — | mA | — | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows.

$$I_{CC} \text{ Max.} = 0.53 \times f + 12 \text{ (max. operation in high-speed mode)}$$

$$I_{CC} \text{ Typ.} = 0.05 \times f + 1.85 \text{ (normal operation in high-speed mode, all peripheral clocks disabled)}$$

$$I_{CC} \text{ Typ.} = 0.12 \times f + 0.69 \text{ (low-speed mode)}$$

$$I_{CC} \text{ Max.} = 0.13 \times f + 12 \text{ (sleep mode)}$$

Note 4. This does not include the BGO operation.

Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.563 MHz).

Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).

Note 8. Reference value

Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD20 (12-bit D/A converter module stop bit) are in the module-stop state.

Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).

Note 11. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.

Note 12. PLL output frequency = 100MHz.

Note 13. PLL output frequency = 200MHz.

Note 14. PLL2-LDO disabled.

Note 15. n = 0, 1

Table 2.8 Coremark and normal mode current

| Parameter | | | | Symbol | Typ | Unit | Test conditions |
|------------------------------|------------------------------|--|--|-----------------|-----|--------|---|
| Supply Current ^{*1} | Coremark ^{*2 *3 *4} | | | I _{CC} | 81 | μA/MHz | ICLK = 100MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.56 MHz |
| | Normal mode | All peripheral clocks disabled, cache on, while (1) code executing from flash ^{*2 *3 *4} | | | 60 | | |
| | | All peripheral clocks disabled, cache off, while (1) code executing from flash ^{*2 *3 *4} | | | 118 | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 3. PLL output frequency = 100MHz.

Note 4. PLL2-LDO disabled.

Table 2.7 工作和待机电流(2of2)

| Parameter | | | | Symbol | Min | Typ | Max | 单元测试条件 | |
|------------------|-------------|--|--|------------------------|-----|------|------|--------|--|
| 参考电源电流(VREFH0) | 在12位AD转换期间 | | | AI _{REFH0} | — | 70 | 120 | μA | |
| | 等待12位AD转换 | | | | — | 0.07 | 0.5 | μA | |
| | ADC12处于待机模式 | | | | — | 0.07 | 0.5 | μA | |
| 参考电源电流(VREFH) | DA转换期间 | | | AI _{REFH} | — | 0.1 | 0.4 | mA | |
| | 无AMP输出 | | | | — | 0.1 | 0.4 | mA | |
| | 带AMP输出 | | | | — | 0.07 | 0.8 | μA | |
| 等待DA转换 | | | | | | | | | |
| | USB工作电流 | | | I _{CCUSBL} | — | 3.5 | 6.5 | mA | |
| | 全速 | | | | — | 4.0 | 10.0 | mA | |
| LDO工作电流 (每台) *15 | | | | I _{CCLDO} | — | 0.18 | — | mA | |
| PLL2-LDO工作电流 | | | | I _{CCPLL2LDO} | — | 0.21 | — | mA | |

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。

注2.使用提供给外设功能的时钟测量。这不包括BGO操作。

注3.ICC取决于f(ICLK)，如下所示。

$$I_{CC} \text{ 最大。} = 0.53 \times f + 12 \text{ (高速模式下的最大操作)}$$

$$I_{CC} \text{ 典型。} = 0.05 \times f + 1.85 \text{ (高速模式下正常运行, 所有外设时钟禁用)}$$

$$I_{CC} \text{ Typ.} = 0.12 \times f + 0.69 \text{ (低速模式)}$$

$$I_{CC} \text{ Max.} = 0.13 \times f + 12 \text{ (睡眠模式)}$$

注4.这不包括BGO操作。

注5.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。

注6.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频(1.563MHz)。注7.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频(3.125MHz)。

注8.参考值

注9.当MCU处于软件待机模式或MSTPCRD.MSTPD16 (12位AD转换器0模块停止位) 和 MSTPCRD.MSTPD20 (12位DA转换器模块停止位) 处于模块停止状态。

注10.FCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频 (15.6kHz)。

注11.PCLKA、PCLKB、PCLKC和PCLKD设置为除以64(512Hz)。FCLK与ICLK的频率相同。

注12.PLL输出频率=100MHz。注13.PLL输出频率=200MHz。

注14.PLL2-LDO禁用。

注15.n = 0, 1

Table 2.8 Coremark and normal mode current

| Parameter | | | | Symbol | Typ | Unit | 测试条件 |
|--------------------|------------------------------|----------------------------------|--|-----------------|-----|--------|---|
| 电源电流 ^{*1} | Coremark ^{*2 *3 *4} | | | I _{CC} | 81 | μA/MHz | ICLK = 100MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.56 MHz |
| | 正常模式 | 禁用所有外设时钟，开启缓存，同时(1)从闪存执行代码*2*3*4 | | | 60 | | |
| | | 所有外设时钟禁用，缓存关闭，同时(1)代码从闪存执行*2*3*4 | | | 118 | | |

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。

注2.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。

注3.PLL输出频率=100MHz。

注4.PLL2-LDO禁用。

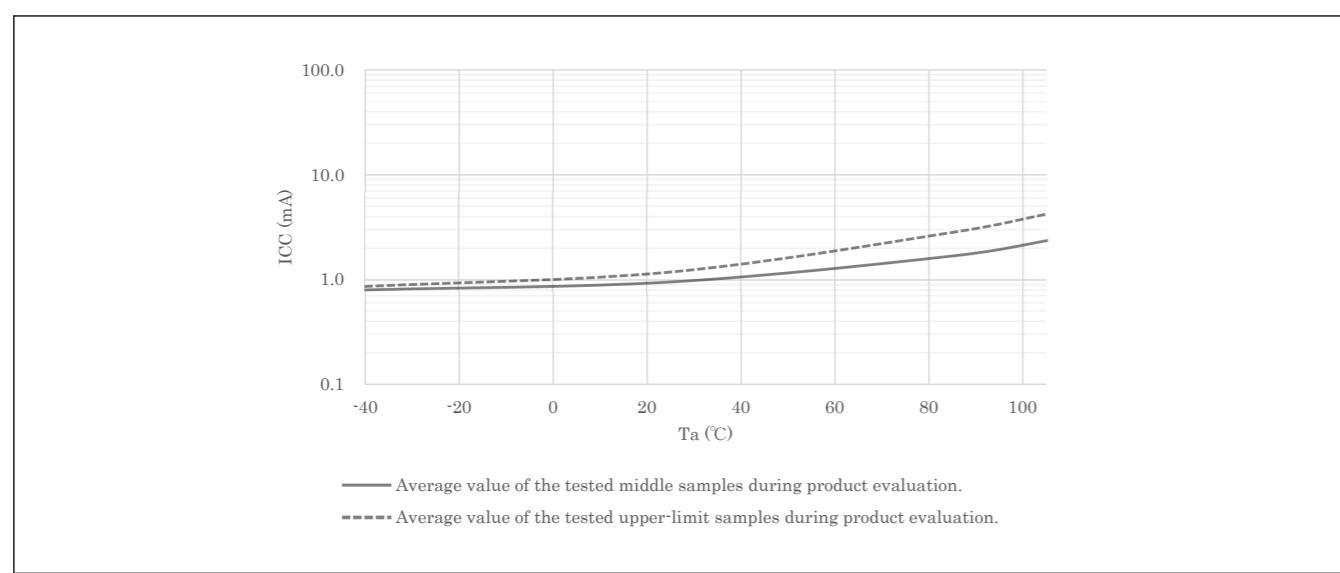


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

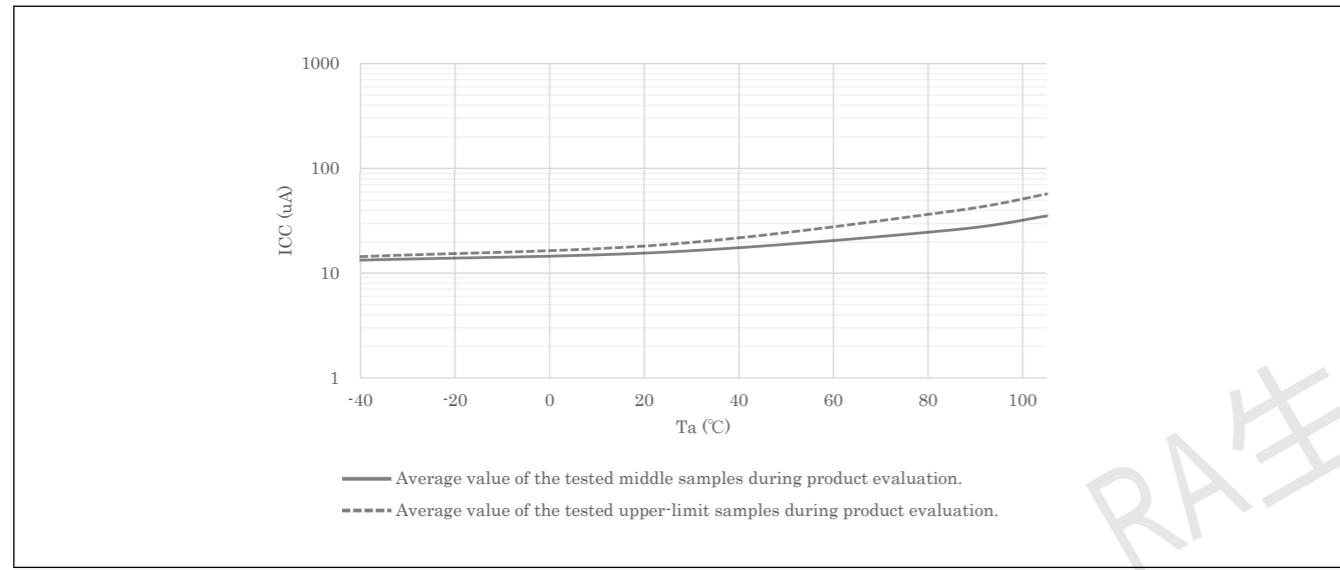
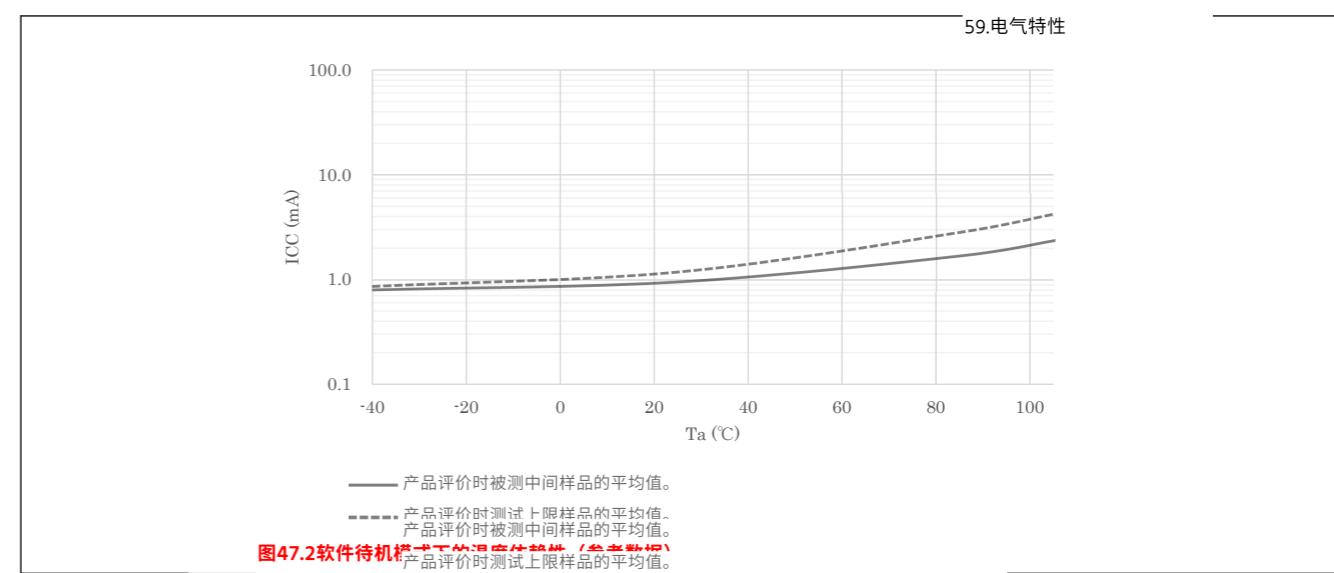
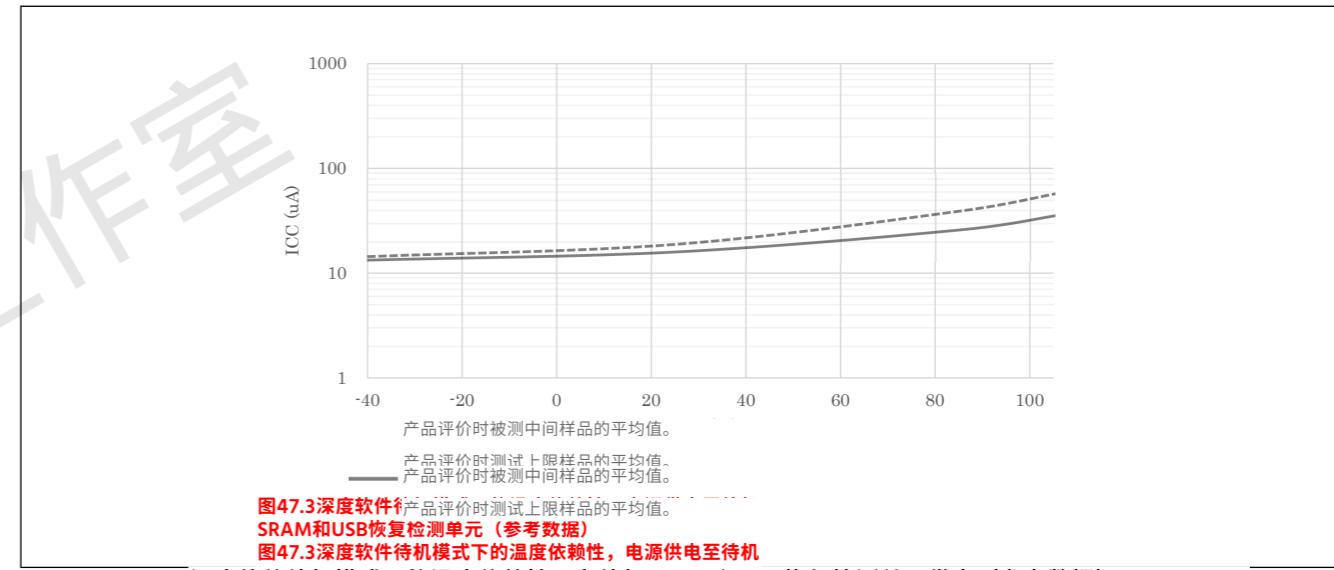


Figure 2.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

Figure 2.2 软件待机模式下的温度依赖性（参考数据）
图47.2软件待机模式下的温度依赖性（参考数据）Figure 2.3 深度软件待机模式下的温度依赖性、为待机SRAM和USB恢复检测单元供电（参考数据）
图47.3深度软件待机模式下的温度依赖性、为待机SRAM和USB恢复检测单元供电（参考数据）

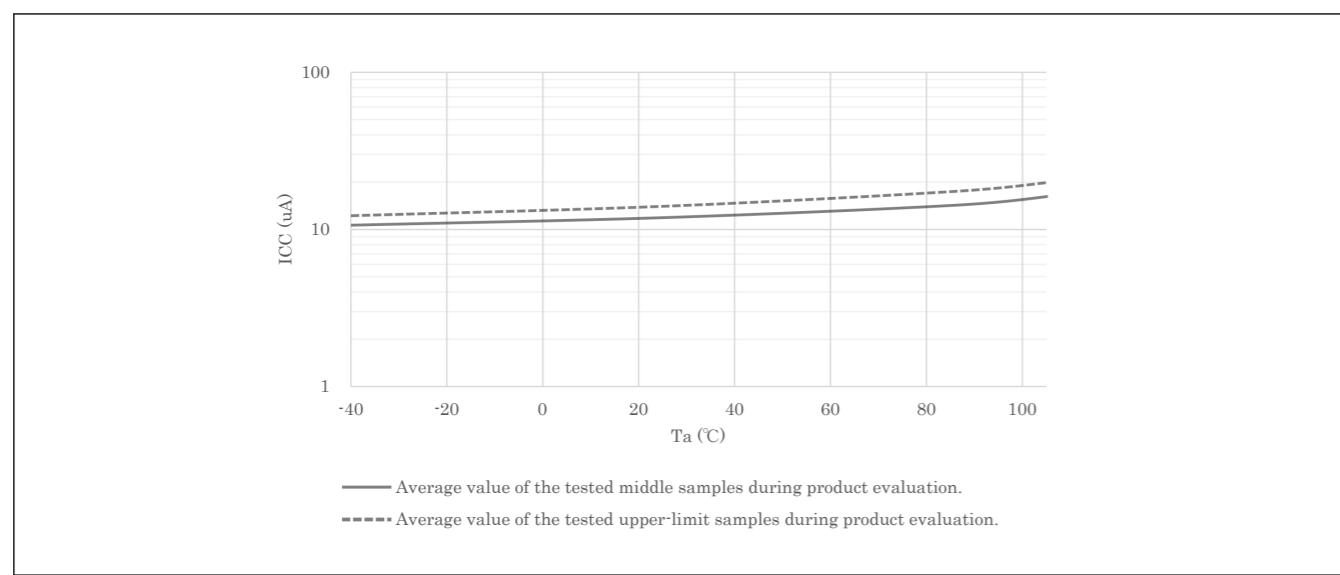


Figure 2.4 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)

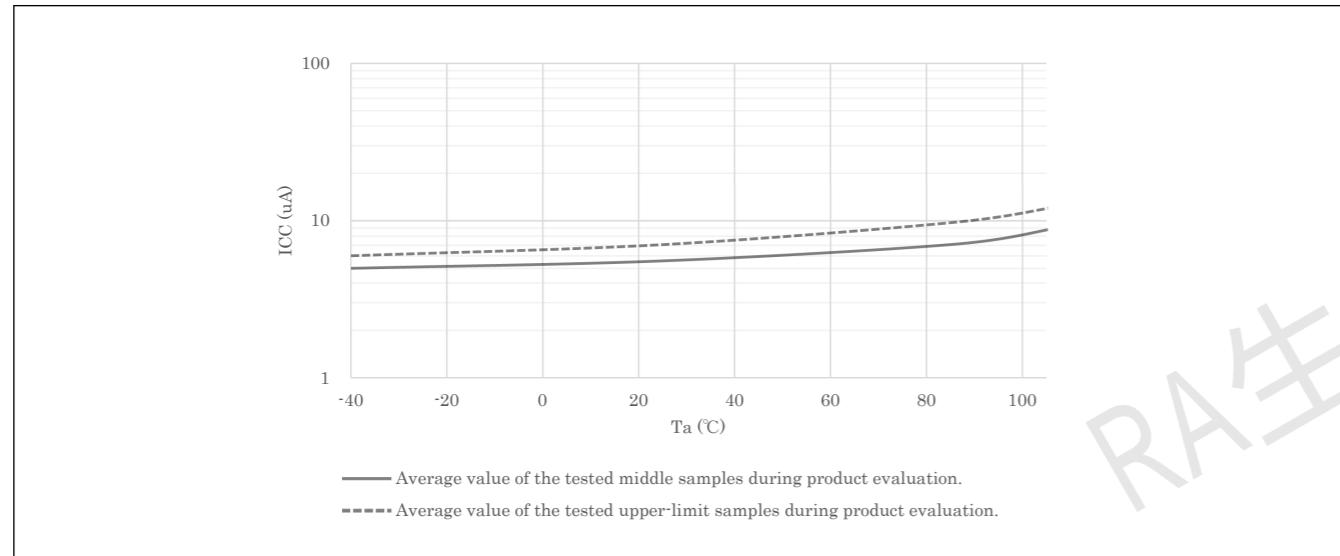


Figure 2.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------|---|--------|--------|-----|-----|------|-----------------|
| VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.0084 | — | 20 | ms/V | — |
| | Voltage monitor 0 reset enabled at startup | | 0.0084 | — | — | | — |
| | SCI/USB boot mode*1 | | 0.0084 | — | 20 | | — |
| VCC falling gradient*2 | | SfVCC | 0.0084 | — | — | ms/V | — |

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Note 2. This applies when VBATT is used.

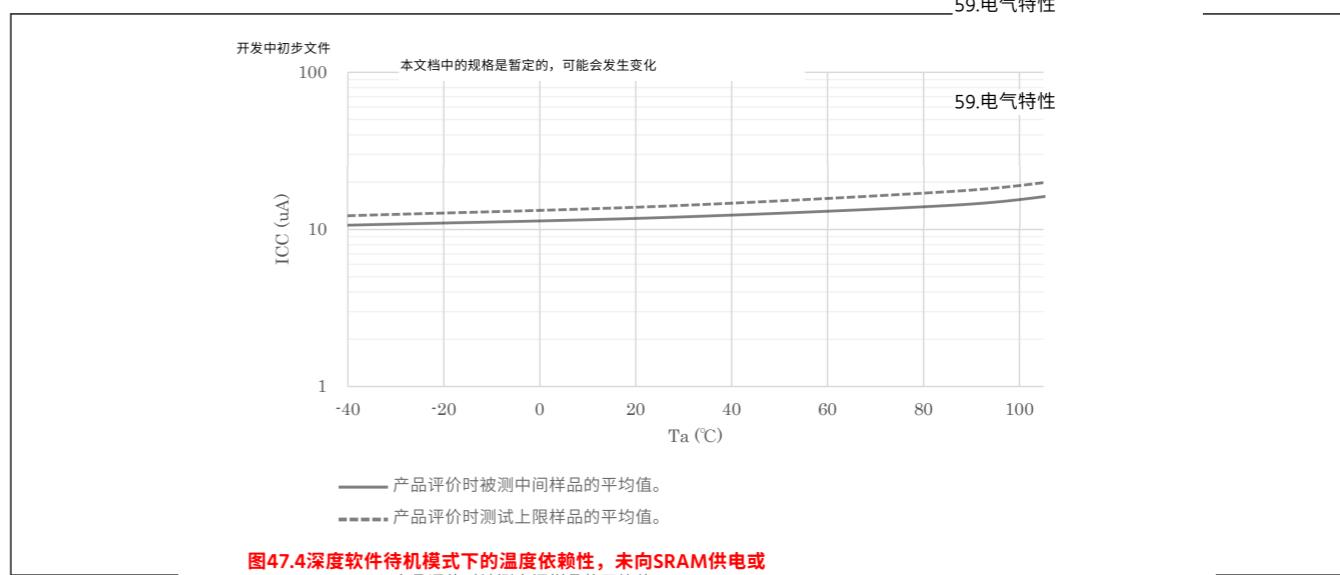


Figure 2.4 深度软件待机模式下，未向SRAM供电或USB恢复检测单元，上电复位电路低功耗功能禁用（参考数据）

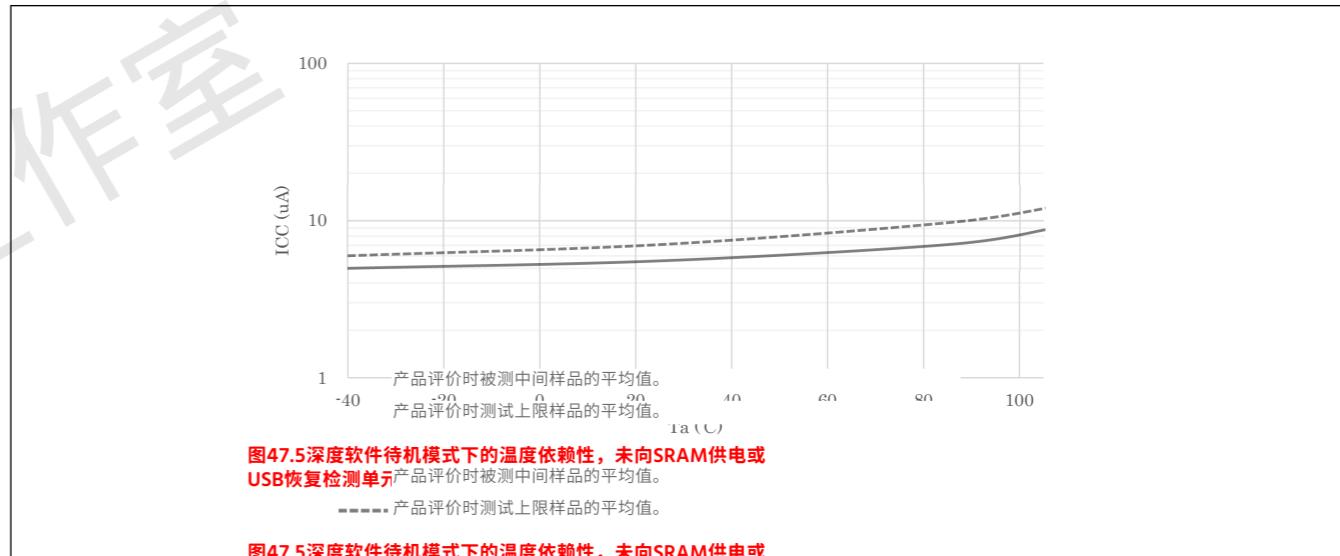


Figure 2.5 深度软件待机模式下的温度依赖性，未向SRAM供电或USB恢复检测单元，上电复位电路低功耗功能启用（参考数据）

2.2.6 VCC上升和下降梯度和纹波频率

Table 2.9 上升和下降梯度特性

| Parameter | | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-----------|---------------|--------|--------|-----|-----|------|------|
| VCC上升梯度 | 启动时禁用电压监视器0复位 | SrVCC | 0.0084 | — | 20 | ms/V | — |
| | 启动时启用电压监视器0复位 | | 0.0084 | — | — | | — |
| | SCI/USB启动模式*1 | | 0.0084 | — | 20 | | — |
| VCC下降梯度*2 | | SfVCC | 0.0084 | — | — | ms/V | — |

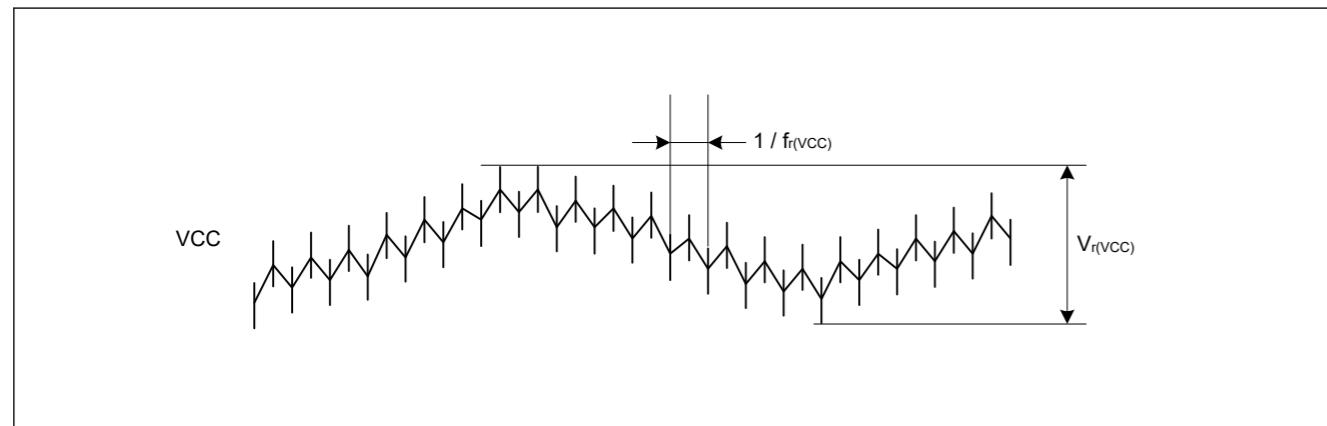
注1.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

注2.这适用于使用VBATT时。

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC $\pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--------------|-----|-----|-----|------|---|
| Allowable ripple frequency | $f_{r(VCC)}$ | — | — | 10 | kHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.2$ |
| | | — | — | 1 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.08$ |
| | | — | — | 10 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$ | 1.0 | — | — | ms/V | When VCC change exceeds VCC $\pm 10\%$ |

**Figure 2.6 Ripple waveform**

2.2.7 Thermal Characteristics

Maximum value of junction temperature (T_j) must not exceed the value of “[section 2.2.1. \$T_j/T_a\$ Definition](#)”.

T_j is calculated by either of the following equations.

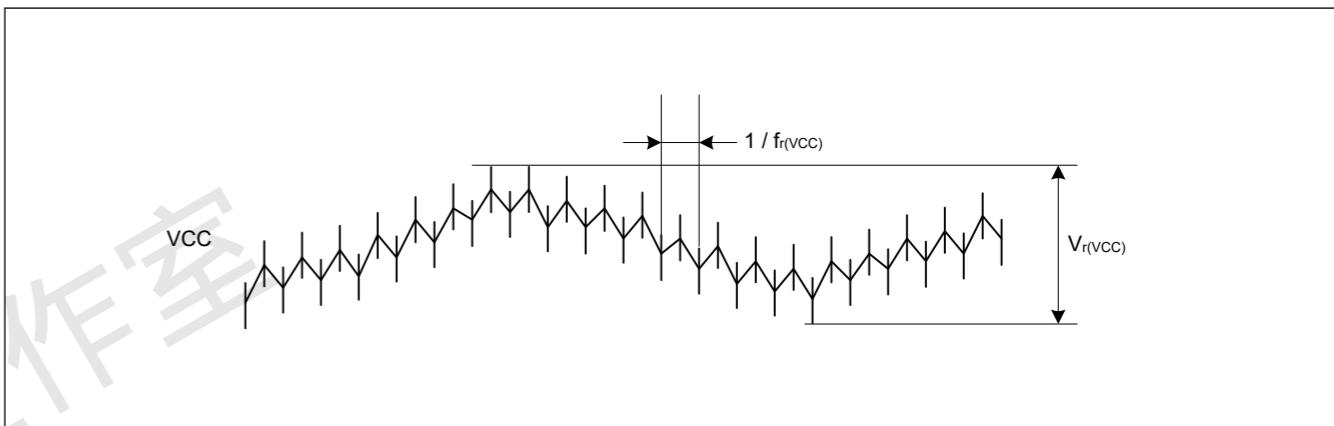
- $T_j = T_a + \theta_{ja} \times \text{Total power consumption}$
- $T_j = T_t + \Psi_{jt} \times \text{Total power consumption}$
 - T_j : Junction Temperature (°C)
 - T_a : Ambient Temperature (°C)
 - T_t : Top Center Case Temperature (°C)
 - θ_{ja} : Thermal Resistance of “Junction”-to-“Ambient” (°C/W)
 - Ψ_{jt} : Thermal Resistance of “Junction”-to-“Top Center Case” (°C/W)
- Total power consumption = Voltage \times (Leakage current + Dynamic current)
- Leakage current of IO = $\Sigma (I_{OL} \times V_{OL}) / \text{Voltage} + \Sigma (|I_{OH}| \times |VCC - V_{OH}|) / \text{Voltage}$
- Dynamic current of IO = $\Sigma IO (C_{in} + C_{load}) \times IO \text{ switching frequency} \times \text{Voltage}$
 - C_{in} : Input capacitance
 - C_{load} : Output capacitance

Regarding θ_{ja} and Ψ_{jt} , refer to [Table 2.11](#).

Table 2.10 上升下降梯度和纹波频率特性

纹波电压必须在VCC上限(3.6V)和下限(2.7V)。当VCC变化超过VCC $\pm 10\%$ 时，必须满足允许的电压变化上升和下降梯度 $dt/dVCC$ 。

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|--------------|--------------|-----|-----|-----|------|---|
| 允许纹波频率 | $f_{r(VCC)}$ | — | — | 10 | kHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.2$ |
| | | — | — | 1 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.08$ |
| | | — | — | 10 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.06$ |
| 允许电压变化上升下降梯度 | $dt/dVCC$ | 1.0 | — | — | ms/V | 当VCC变化超过VCC $\pm 10\%$ |

**Figure 2.6 纹波波形**

2.2.7 热特性

结温 (T_j) 的最大值不得超过“第2.2.1节的值。 T_j/T_a 定义”。

T_j 通过以下任一公式计算。

- $T_j = T_a + \theta_{ja} \times \text{总功耗}$
- $T_j = T_t + \Psi_{jt} \times \text{总功耗}$
 - T_j : 结温(°C)
 - T_a : 环境温度 (°C)
 - T_t : 顶部中心外壳温度(°C)
 - θ_{ja} : “结”到“环境”的热阻(°CW)
 - Ψ_{jt} : “结”到“顶部中心外壳”的热阻(°CW)
- 总功耗=电压 \times (漏电流+动态电流)
- IO漏电流= $\Sigma (I_{OL} \times V_{OL}) / \text{电压} + \Sigma (|I_{OH}| \times |VCC - V_{OH}|) / \text{电压}$
- IO的动态电流= $\Sigma IO (C_{in} + C_{load}) \times IO \text{ 开关频率} \times \text{电压}$
 - C_{in} : 输入电容
 - C负载：输出电容

关于 θ_{ja} 和 Ψ_{jt} ，请参阅表2.11。

Table 2.11 Thermal Resistance

| Parameter | Package | Symbol | Value ^{*1} | Unit | Test conditions |
|--------------------|----------------------------|---------------|---------------------|------|------------------------------|
| Thermal Resistance | 48-pin QFN (PWQN0048KC-A) | θ_{ja} | 23.9 | °C/W | JESD 51-2 and 51-7 compliant |
| | 64-pin LQFP (PLQP0064KB-C) | | 54.6 | | |
| Thermal Resistance | 48-pin QFN (PWQN0048KC-A) | Ψ_{jt} | 0.28 | °C/W | JESD 51-2 and 51-7 compliant |
| | 64-pin LQFP (PLQP0064KB-C) | | 1.90 | | |

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.2.7.1 Calculation guide of I_{CCmax}

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

| Dynamic current/ Leakage current | MCU Domain | Category | Item | Frequency [MHz] | Current [uA/MHz] | Current ^{*1} [mA] |
|-------------------------------------|-----------------------------|----------------------------------|---------------------------|--------------------|---------------------|-------------------------------|
| Leakage current | Analog | LDO and Leak ^{*2} | Ta = 75 °C ^{*3} | — | — | 7.82 |
| | | | Ta = 85 °C ^{*3} | — | — | 9.13 |
| Dynamic current | CPU | Operation with Flash and SRAM | Coremark | 100 | 55.556 | 5.56 |
| | | | GPT16 (2ch) ^{*4} | 100 | 1.788 | 0.18 |
| | | Peripheral Unit | GPT32 (2ch) ^{*4} | 100 | 2.115 | 0.21 |
| | | | POEG (4 Groups) | 50 | 1.361 | 0.07 |
| | | | AGT (6ch) ^{*4} | 50 | 9.228 | 0.46 |
| | | | RTC | 50 | 4.277 | 0.21 |
| | | | WDT | 50 | 0.764 | 0.04 |
| | Communication interfaces | Timer | IWDT | 50 | 0.339 | 0.02 |
| | | | USBFS | 50 | 9.385 | 0.47 |
| | | | SCI (4ch) ^{*4} | 100 | 12.477 | 1.25 |
| | | | IIC | 50 | 1.684 | 0.08 |
| | | | CAN | 50 | 1.898 | 0.09 |
| | | | SPI | 100 | 3.024 | 0.30 |
| | | | QSPI | 100 | 2.051 | 0.21 |
| | Analog | ADC12 | 100 | 2.287 | 0.23 | |
| | | DAC12 | 100 | 0.435 | 0.05 | |
| | Event link | ELC | 50 | 0.865 | 0.04 | |
| | Security | SCE9 | 100 | 218.100 | 21.81 | |
| | Data processing | CRC | 100 | 0.600 | 0.06 | |
| | | DOC | 100 | 0.388 | 0.04 | |
| | System | CAC | 50 | 0.844 | 0.04 | |
| | DMA | DMAC | 100 | 4.479 | 0.45 | |
| | | DTC | 100 | 4.274 | 0.43 | |

Note 1. The values are guaranteed by design.

Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.

It is selected according to the temperature of Ta.

Note 3. $\Delta(T_j-T_a) = 20$ °C is considered to measure the current.

Note 4. To determine the current consumption per channel, group or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.11 热阻

| Parameter | Package | Symbol | Value ^{*1} | Unit | 测试条件 |
|--------------------|----------------------------|---------------|---------------------|------|-----------------|
| Thermal Resistance | 48-pin QFN (PWQN0048KC-A) | θ_{ja} | 23.9 | °C/W | 符合JESD51-2和51-7 |
| | 64-pin LQFP (PLQP0064KB-C) | | 54.6 | | |
| Thermal Resistance | 48-pin QFN (PWQN0048KC-A) | Ψ_{jt} | 0.28 | °C/W | 符合JESD51-2和51-7 |
| | 64-pin LQFP (PLQP0064KB-C) | | 1.90 | | |

注1. 数值为使用4层板时的参考值。热阻取决于板的层数或尺寸。有关详细信息，请参阅JEDEC标准。

2.2.7.1 ICCmax的计算指南

表2.12显示了每个单元的功耗。

Table 2.12 各单元耗电量

| 动态电流漏电流 | MCU Domain | Category | Item | Frequency [MHz] | Current [uA/MHz] | Current ^{*1} [mA] |
|---------|---------------|-------------------------------|---------------------------|--------------------|---------------------|-------------------------------|
| 漏电流 | Analog | LDO and Leakage ^{*2} | Ta = 75 °C ^{*3} | — | — | 7.82 |
| | | | Ta = 85 °C ^{*3} | — | — | 9.13 |
| 动态电流 | CPU | 操作与 闪存和SRAM | Coremark | 100 | 55.556 | 5.56 |
| | | | GPT16 (2ch) ^{*4} | 100 | 1.788 | 0.18 |
| | | 外围单元 | GPT32 (2ch) ^{*4} | 100 | 2.115 | 0.21 |
| | | | POEG (4 Groups) | 50 | 1.361 | 0.07 |
| | | | AGT (6ch) ^{*4} | 50 | 9.228 | 0.46 |
| | | | RTC | 50 | 4.277 | 0.21 |
| | | | WDT | 50 | 0.764 | 0.04 |
| | 通信接口 | Timer | IWDT | 50 | 0.339 | 0.02 |
| | | | USBFS | 50 | 9.385 | 0.47 |
| | | | SCI (4ch) ^{*4} | 100 | 12.477 | 1.25 |
| | | | IIC | 50 | 1.684 | 0.08 |
| | | | CAN | 50 | 1.898 | 0.09 |
| | | | SPI | 100 | 3.024 | 0.30 |
| | | | QSPI | 100 | 2.051 | 0.21 |
| | Analog | ADC12 | 100 | 2.287 | 0.23 | |
| | | DAC12 | 100 | 0.435 | 0.05 | |
| | 活动链接 | ELC | 50 | 0.865 | 0.04 | |
| | Security | SCE9 | 100 | 218.100 | 21.81 | |
| | 数据处理 | CRC | 100 | 0.600 | 0.06 | |
| | | DOC | 100 | 0.388 | 0.04 | |
| | System | CAC | 50 | 0.844 | 0.04 | |
| | DMA | DMAC | 100 | 4.479 | 0.45 | |
| | | DTC | 100 | 4.274 | 0.43 | |

注1. 数值由设计保证。

注2.LDO和Leak是内部稳压器的电流和MCU的漏电流。

根据Ta的温度选择。

注3. 测量电流时考虑 $\Delta(T_j-T_a)=20$ °C。

注4. 要确定每个通道、组或单元的电流消耗，请将电流[mA]除以通道、组或单元的数量。

Table 2.13 shows the outline of operation for each unit.

Table 2.13 Outline of operation for each unit

| Peripheral | Outline of operation |
|------------|---|
| GPT | Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD. |
| POEG | Only clear module stop bit. |
| AGT | AGT is operating with PCLKB. |
| RTC | RTC is operating with LOCO. |
| WDT | WDT is operating with PCLKB. |
| IWDT | IWDT is operating with IWDTCLK. |
| USBFS | Transfer types is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps). |
| SCI | SCI is transmitting data in clock synchronous mode. |
| IIC | Communication format is set to I2C-bus format. IIC is transmitting data in master mode. |
| CAN | CAN is transmitting and receiving data in self-test mode 1. |
| SPI | SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data. |
| QSPI | QSPI is issuing Fast Read Quad I/O Instruction. |
| ADC12 | Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode. |
| DAC12 | DAC12 is outputting the conversion result while updating the value of data register. |
| ELC | Only clear module stop bit. |
| SCE9 | SCE9 is executing built-in self test. |
| CRC | CRC is generating CRC code using 32-bit CRC32-C polynomial. |
| DOC | DOC is operating in data addition mode. |
| CAC | Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy. |
| DMAC | Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0. |
| DTC | Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0. |

2.2.7.2 Example of T_j calculation

Assumption :

- Package 64-pin LQFP : $\theta_{ja} = 54.6 \text{ }^{\circ}\text{C/W}$
- $T_a = 80 \text{ }^{\circ}\text{C}$
- $I_{CC\max} = 40 \text{ mA}$
- $V_{CC} = 3.5 \text{ V}$ ($V_{CC} = AVCC = VCC_USB$)
- $I_{OH} = 1 \text{ mA}$, $V_{OH} = VCC - 0.5 \text{ V}$, 12 Outputs
- $I_{OL} = 20 \text{ mA}$, $V_{OL} = 1.0 \text{ V}$, 8 Outputs
- $I_{OL} = 1 \text{ mA}$, $V_{OL} = 0.5 \text{ V}$, 12 Outputs
- $C_{in} = 8 \text{ pF}$, 16 pins, Input frequency = 10 MHz

表2.13显示了每个单元的操作概要。

Table 2.13 每个单元的操作概要

| Peripheral | 操作概要 |
|------------|---|
| GPT | 操作模式设置为锯齿波PWM模式。 GPT使用PCLKD运行。 |
| POEG | 只清除模块停止位。 |
| AGT | AGT使用PCLKB运行。 |
| RTC | RTC与LOCO一起运行。 |
| WDT | WDT使用PCLKB运行。 |
| IWDT | IWDT使用IWDTCLK运行。 |
| USBFS | 传输类型设置为批量传输。 USBFS使用全速传输(12Mbps)运行。 |
| SCI | SCI在时钟同步模式下传输数据。 |
| IIC | 通信格式设置为I2C总线格式。 IIC在主机模式下传输数据。 |
| CAN | CAN在自检模式1中发送和接收数据。 |
| SPI | SPI模式设置为SPI操作（4线方法）。 SPI主从模式设置为主模式。 SPI正在传输8位宽度的数据。 |
| QSPI | QSPI正在发出快速读取四线IO指令。 |
| ADC12 | 分辨率设置为12位精度。 数据寄存器设置为AD转换值加法模式。 ADC12在连续扫描模式下转换模拟输入。 |
| DAC12 | DAC12在更新数据寄存器值的同时输出转换结果。 |
| ELC | 只清除模块停止位。 |
| SCE9 | SCE9正在执行内置自检。 |
| CRC | CRC使用32位CRC32-C多项式生成CRC码。 |
| DOC | DOC在数据添加模式下运行。 |
| CAC | 测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。CAC正在测量时钟频率精度。 |
| DMAC | 传输数据的位长设置为32位。 传输模式设置为块传输模式。 DMAC正在将数据从SRAM0传输到SRAM0。 |
| DTC | 传输数据的位长设置为32位。 传输模式设置为块传输模式。 DTC正在将数据从SRAM0传输到SRAM0。 |

2.2.7.2 T_j 计算示例

Assumption :

- Package 64-pin LQFP : $\theta_{ja} = 54.6 \text{ }^{\circ}\text{C/W}$
- $T_a = 80 \text{ }^{\circ}\text{C}$
- $I_{CC\max}=40\text{mA}$
- $V_{CC} = 3.5 \text{ V}$ ($V_{CC} = AVCC = VCC_USB$)
- $I_{OH}=1\text{mA}$, $V_{OH}=VCC-0.5\text{V}$, 12个输出
- $I_{OL}=20\text{mA}$, $V_{OL}=1.0\text{V}$, 8个输出
- $I_{OL}=1\text{mA}$, $V_{OL}=0.5\text{V}$, 12路输出
- $C_{in}=8\text{pF}$, 16个引脚, 输入频率=10MHz

- $C_{load} = 30 \text{ pF}$, 16 pins, Output frequency = 10 MHz

$$\text{Leakage current of IO} = \sum (V_{OL} \times I_{OL}) / \text{Voltage} + \sum ((VCC - V_{OH}) \times I_{OH}) / \text{Voltage}$$

$$\begin{aligned} &= (20 \text{ mA} \times 1 \text{ V}) \times 8 / 3.5 \text{ V} + (1 \text{ mA} \times 0.5 \text{ V}) \times 12 / 3.5 \text{ V} + ((VCC - (VCC - 0.5 \text{ V})) \times 1 \text{ mA}) \times 12 / 3.5 \text{ V} \\ &= 45.7 \text{ mA} + 1.71 \text{ mA} + 1.71 \text{ mA} \\ &= 49.1 \text{ mA} \end{aligned}$$

$$\text{Dynamic current of IO} = \sum IO (C_{in} + C_{load}) \times IO \text{ switching frequency} \times \text{Voltage}$$

$$\begin{aligned} &= ((8 \text{ pF} \times 16) \times 10 \text{ MHz} + (30 \text{ pF} \times 16) \times 10 \text{ MHz}) \times 3.5 \text{ V} \\ &= 21.3 \text{ mA} \end{aligned}$$

$$\text{Total power consumption} = (I_{CCmax} \times \text{Voltage}) + (\text{Leakage current of IO} + \text{Dynamic current of IO}) \times \text{Voltage}$$

$$\begin{aligned} &= (40 \text{ mA} \times 3.5 \text{ V}) + (49.1 \text{ mA} + 21.3 \text{ mA}) \times 3.5 \text{ V} \\ &= 386 \text{ mW (0.386 W)} \end{aligned}$$

$$T_j = Ta + \theta_{ja} \times \text{Total power consumption}$$

$$\begin{aligned} &= 80^\circ\text{C} + 54.6^\circ\text{C/W} \times 0.386\text{W} \\ &= 101.1^\circ\text{C} \end{aligned}$$

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---------------------|---------------------------------|--------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK) | f | — | — | 100 | MHz |
| | Peripheral module clock (PCLKA) | | — | — | 100 | |
| | Peripheral module clock (PCLKB) | | — | — | 50 | |
| | Peripheral module clock (PCLKC) | | —*2 | — | 50 | |
| | Peripheral module clock (PCLKD) | | — | — | 100 | |
| | Flash interface clock (FCLK) | | —*1 | — | 50 | |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.

Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|--------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK) | f | — | — | 1 | MHz |
| | Peripheral module clock (PCLKA) | | — | — | 1 | |
| | Peripheral module clock (PCLKB) | | — | — | 1 | |
| | Peripheral module clock (PCLKC)*2 | | —*2 | — | 1 | |
| | Peripheral module clock (PCLKD) | | — | — | 1 | |
| | Flash interface clock (FCLK)*1 | | — | — | 1 | |

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.

Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

- C负载=30pF, 16引脚, 输出频率=10MHz

$$\text{IO的漏电流} = \sum (V_{OL} \times I_{OL}) / \text{电压} + \sum ((VCC - V_{OH}) \times I_{OH}) / \text{电压}$$

$$\begin{aligned} &= (20 \text{ mA} \times 1 \text{ V}) \times 8 / 3.5 \text{ V} + (1 \text{ mA} \times 0.5 \text{ V}) \times 12 / 3.5 \text{ V} + ((VCC - (VCC - 0.5 \text{ V})) \times 1 \text{ mA}) \times 12 / 3.5 \text{ V} \\ &= 45.7 \text{ mA} + 1.71 \text{ mA} + 1.71 \text{ mA} \\ &= 49.1 \text{ mA} \end{aligned}$$

$$\text{IO的动态电流} = \sum IO (C_{in} + C_{load}) \times IO \text{ 开关频率} \times \text{电压}$$

$$\begin{aligned} &= ((8 \text{ pF} \times 16) \times 10 \text{ MHz} + (30 \text{ pF} \times 16) \times 10 \text{ MHz}) \times 3.5 \text{ V} \\ &= 21.3 \text{ mA} \end{aligned}$$

$$\text{总功耗} = (I_{CCmax} \times \text{电压}) + (\text{IO漏电流} + \text{IO动态电流}) \times \text{电压}$$

$$\begin{aligned} &= (40 \text{ mA} \times 3.5 \text{ V}) + (49.1 \text{ mA} + 21.3 \text{ mA}) \times 3.5 \text{ V} \\ &= 386 \text{ mW (0.386 W)} \end{aligned}$$

$$T_j = Ta + \theta_{ja} \times \text{总功耗}$$

$$\begin{aligned} &= 80^\circ\text{C} + 54.6^\circ\text{C/W} \times 0.386\text{W} \\ &= 101.1^\circ\text{C} \end{aligned}$$

2.3 交流特性

2.3.1 频率

Table 2.14 高速模式下的运行频率值

| Parameter | | Symbol | Min | Typ | Max | Unit |
|-----------|---------------|--------|-----|-----|-----|------|
| 运行频率 | 系统时钟(ICLK) | f | — | — | 100 | MHz |
| | 外设模块时钟(PCLKA) | | — | — | 100 | |
| | 外设模块时钟(PCLKB) | | — | — | 50 | |
| | 外设模块时钟(PCLKC) | | —*2 | — | 50 | |
| | 外设模块时钟(PCLKD) | | — | — | 100 | |
| | 闪存接口时钟(FCLK) | | —*1 | — | 50 | |

注1.在对闪存进行编程或擦除时, FCLK必须以至少4MHz的频率运行。

注2.使用ADC12时, PCLKC频率必须至少为1MHz。

Table 2.15 低速模式下的运行频率值

| Parameter | | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
| 运行频率 | 系统时钟(ICLK) | f | — | — | 1 | MHz |
| | 外设模块时钟(PCLKA) | | — | — | 1 | |
| | 外设模块时钟(PCLKB) | | — | — | 1 | |
| | 外围模块时钟(PCLKC)*2 | | —*2 | — | 1 | |
| | 外设模块时钟(PCLKD) | | — | — | 1 | |
| | 闪存接口时钟(FCLK)*1 | | — | — | 1 | |

注1.在低速模式下禁止对闪存进行编程或擦除。

注2.使用ADC12时, PCLKC频率必须设置为至少1MHz。

Table 2.16 Operation frequency value in Subosc-speed mode

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|--------|------|-----|------|------|
| Operation frequency | System clock (ICLK) | f | 29.4 | — | 36.1 | kHz |
| | Peripheral module clock (PCLKA) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKB) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKC)*2 | | — | — | 36.1 | |
| | Peripheral module clock (PCLKD) | | — | — | 36.1 | |
| | Flash interface clock (FCLK)*1 | | 29.4 | — | 36.1 | |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.

Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.17 Clock timing except for sub-clock oscillator (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--|------------------------|---------------------|----------|---------|-------|--|--------------------------------|--|
| EXTAL external clock input cycle time | t _{EXcyc} | 41.66 | — | — | ns | Figure 2.7 | | |
| EXTAL external clock input high pulse width | t _{EXH} | 15.83 | — | — | ns | | | |
| EXTAL external clock input low pulse width | t _{EXL} | 15.83 | — | — | ns | | | |
| EXTAL external clock rise time | t _{Exr} | — | — | 5.0 | ns | | | |
| EXTAL external clock fall time | t _{Exf} | — | — | 5.0 | ns | | | |
| Main clock oscillator frequency | f _{MAIN} | 8 | — | 24 | MHz | | | |
| Main clock oscillation stabilization wait time (crystal)*1 | t _{MAINOSCWT} | — | — | —*1 | ms | Figure 2.8 | | |
| LOCO clock oscillation frequency | f _{LOCO} | 29.4912 | 32.768 | 36.0448 | kHz | | | |
| LOCO clock oscillation stabilization wait time | t _{LOCOWT} | — | — | 60.4 | μs | | | |
| ILOCO clock oscillation frequency | f _{ILOCO} | 13.5 | 15 | 16.5 | kHz | | | |
| MOCO clock oscillation frequency | F _{MOCO} | 6.8 | 8 | 9.2 | MHz | | | |
| MOCO clock oscillation stabilization wait time | t _{MOCOWT} | — | — | 15.0 | μs | | | |
| HOCO clock oscillator oscillation frequency | Without FLL | f _{HOCO16} | 15.78 | 16 | 16.22 | MHz | $-20 \leq T_a \leq 85^\circ C$ | |
| | | f _{HOCO18} | 17.75 | 18 | 18.25 | | | |
| | | f _{HOCO20} | 19.72 | 20 | 20.28 | | | |
| | | f _{HOCO16} | 15.71 | 16 | 16.29 | | | |
| | | f _{HOCO18} | 17.68 | 18 | 18.32 | | | |
| | | f _{HOCO20} | 19.64 | 20 | 20.36 | | | |
| HOCO clock oscillation stabilization wait time*2 | t _{HOCOWT} | — | — | 64.7 | μs | $-40 \leq T_a \leq -20^\circ C$ Sub-clock frequency accuracy is ± 50 ppm. | | |
| HOCO period jitter | — | — | ± 85 | — | ps | | | |
| FLL stabilization wait time | t _{FLLWT} | — | — | 1.8 | ms | | | |
| PLL clock frequency | f _{PLL} | 100 | — | 200 | MHz | | | |
| PLL2 clock frequency | f _{PLL2} | 120 | — | 240 | MHz | | | |
| PLL/PLL2 clock oscillation stabilization wait time | t _{PLLWT} | — | — | 174.9 | μs | | | |

Table 2.16 Subosc-speed模式下的运行频率值

| Parameter | | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|------|-----|------|------|
| 运行频率 | 系统时钟(ICLK) | f | 29.4 | — | 36.1 | kHz |
| | 外设模块时钟(PCLKA) | | — | — | 36.1 | |
| | 外设模块时钟(PCLKB) | | — | — | 36.1 | |
| | 外围模块时钟(PCLKC)*2 | | — | — | 36.1 | |
| | 外设模块时钟(PCLKD) | | — | — | 36.1 | |
| | 闪存接口时钟(FCLK)*1 | | 29.4 | — | 36.1 | |

注1.在Subosc速度模式下，编程或擦除闪存被禁用。

注2.不能使用ADC12。

2.3.2 时钟时序

Table 2.17 除副时钟振荡器外的时钟时序（2个中的1个）

| Parameter | | Symbol | Min | Typ | Max | Unit | 测试条件 | |
|--------------------|------------------------|---------------------|----------|---------|-------|--|--------------------------------|--|
| EXTAL外部时钟输入周期时间 | t _{EXcyc} | 41.66 | — | — | ns | Figure 2.7 | | |
| EXTAL外部时钟输入高脉冲宽度 | t _{EXH} | 15.83 | — | — | ns | | | |
| EXTAL外部时钟输入低脉冲宽度 | t _{EXL} | 15.83 | — | — | ns | | | |
| EXTAL外部时钟上升时间 | t _{Exr} | — | — | 5.0 | ns | | | |
| EXTAL外部时钟下降时间 | t _{Exf} | — | — | 5.0 | ns | | | |
| 主时钟振荡器频率 | f _{MAIN} | 8 | — | 24 | MHz | | | |
| 主时钟振荡稳定等待时间（晶体）*1 | t _{MAINOSCWT} | — | — | —*1 | ms | Figure 2.8 | | |
| LOCO时钟振荡频率 | f _{LOCO} | 29.4912 | 32.768 | 36.0448 | kHz | | | |
| LOCO时钟振荡稳定等待时间 | t _{LOCOWT} | — | — | 60.4 | μs | | | |
| ILOCO时钟振荡频率 | f _{ILOCO} | 13.5 | 15 | 16.5 | kHz | | | |
| MOCO时钟振荡频率 | F _{MOCO} | 6.8 | 8 | 9.2 | MHz | | | |
| MOCO时钟振荡稳定等待时间 | t _{MOCOWT} | — | — | 15.0 | μs | | | |
| HOCO时钟振荡器振荡频率 | Without FLL | f _{HOCO16} | 15.78 | 16 | 16.22 | MHz | $-20 \leq T_a \leq 85^\circ C$ | |
| | | f _{HOCO18} | 17.75 | 18 | 18.25 | | | |
| | | f _{HOCO20} | 19.72 | 20 | 20.28 | | | |
| | | f _{HOCO16} | 15.71 | 16 | 16.29 | | | |
| | | f _{HOCO18} | 17.68 | 18 | 18.32 | | | |
| | | f _{HOCO20} | 19.64 | 20 | 20.36 | | | |
| HOCO时钟振荡稳定等待时间*2 | t _{HOCOWT} | — | — | 64.7 | μs | $-40 \leq T_a \leq -20^\circ C$ Sub-clock frequency accuracy is ± 50 ppm. | | |
| HOCO周期抖动 | — | — | ± 85 | — | ps | | | |
| FLL稳定等待时间 | t _{FLLWT} | — | — | 1.8 | ms | | | |
| 锁相环时钟频率 | f _{PLL} | 100 | — | 200 | MHz | | | |
| PLL2时钟频率 | f _{PLL2} | 120 | — | 240 | MHz | | | |
| PLL/PLL2时钟振荡稳定等待时间 | t _{PLLWT} | — | — | 174.9 | μs | | | |

Table 2.17 Clock timing except for sub-clock oscillator (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------|---------------------------------|-----|-----------|-----------|------|-----------------|
| PLL/PLL2 period jitter | $f_{PLL}, f_{PLL2} \geq 120MHz$ | — | — | ± 100 | — | ps |
| | $f_{PLL}, f_{PLL2} < 120MHz$ | — | — | ± 120 | — | ps |
| PLL/PLL2 long term jitter | — | — | ± 300 | — | ps | Term: 1μs, 10μs |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.

After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.18 Clock timing for the sub-clock oscillator

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|----------------|-----|--------|---------|------|-----------------|
| Sub-clock frequency | f_{SUB} | — | 32.768 | — | kHz | — |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | *1 | s | Figure 2.11 |

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.

After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

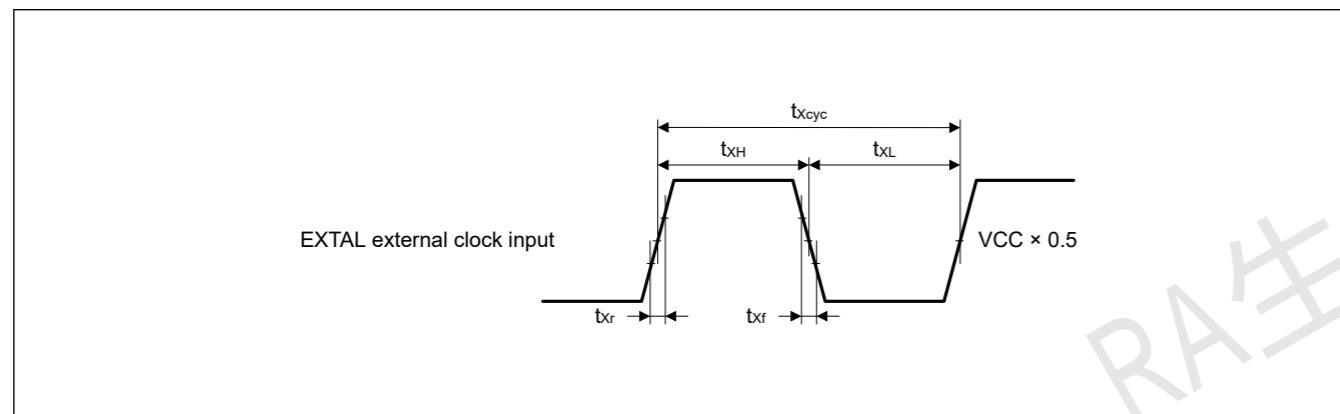


Figure 2.7 EXTAL external clock input timing

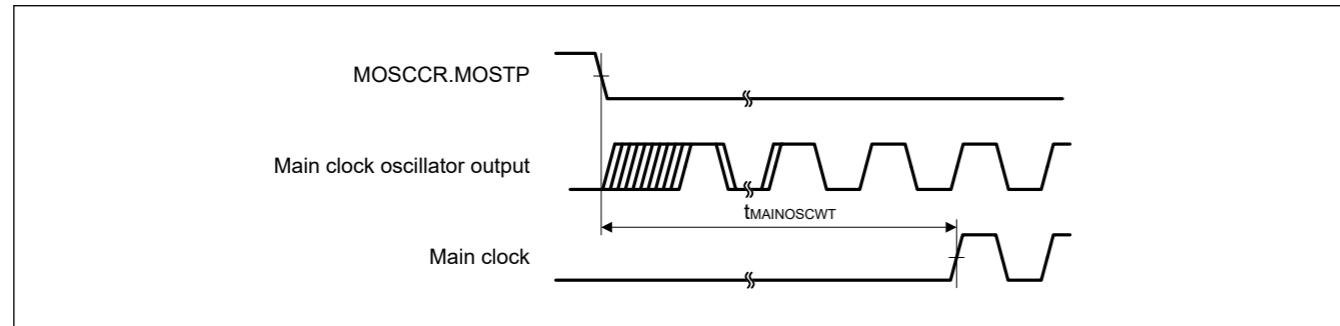


Figure 2.8 Main clock oscillation start timing

Table 2.17 除副时钟振荡器外的时钟时序(2of2)

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-------------|---------------------------------|-----|-----------|-----------|------|-----------------|
| PLLPLL2周期抖动 | $f_{PLL}, f_{PLL2} \geq 120MHz$ | — | — | ± 100 | — | ps |
| | $f_{PLL}, f_{PLL2} < 120MHz$ | — | — | ± 120 | — | ps |
| PLLPLL2长期抖动 | — | — | ± 300 | — | ps | Term: 1μs, 10μs |

注1.设置主时钟振荡器时,请向振荡器制造商索取振荡评估,并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后,读取OSCSF.MOSCSF标志以确认其为1,然后开始使用主时钟振荡器。

注2.这是从复位状态释放到HOCO振荡频率(f_{HOCO})达到保证工作范围的时间。

Table 2.18 副时钟振荡器的时钟时序

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|---------------------|----------------|-----|--------|---------|------|-------------|
| Sub-clock frequency | f_{SUB} | — | 32.768 | — | kHz | — |
| 副时钟振荡稳定等待时间 | $t_{SUBOSCWT}$ | — | — | *1 | s | Figure 2.11 |

注1.设置副时钟振荡器时,请咨询振荡器制造商进行振荡评估,并将结果作为推荐的振荡稳定时间。更改SOSCCR.SOSTP位的设置以启动副时钟操作后,只有在副时钟振荡稳定时间过去并留有足够余量后才开始使用副时钟振荡器。建议使用两倍于显示值的值。

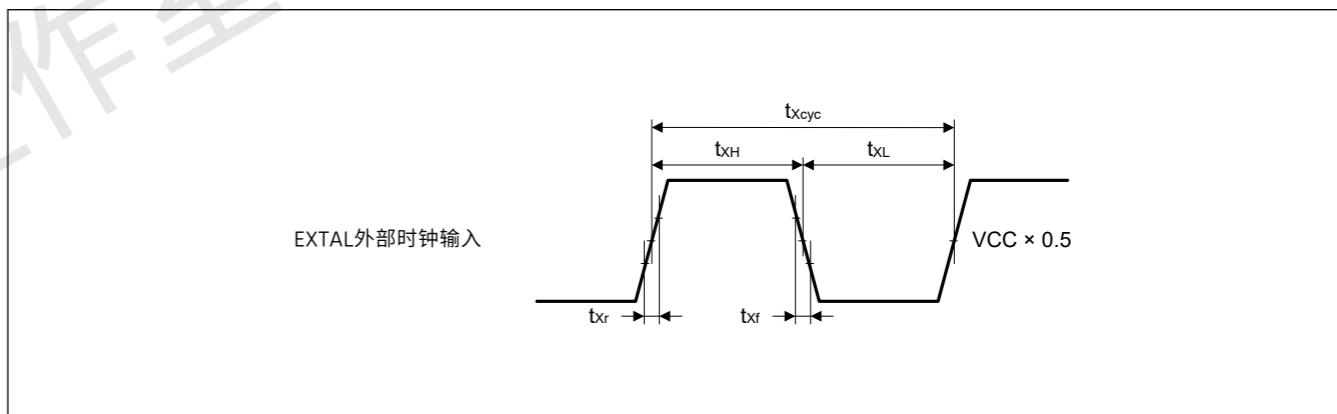


Figure 2.7 EXTAL外部时钟输入时序

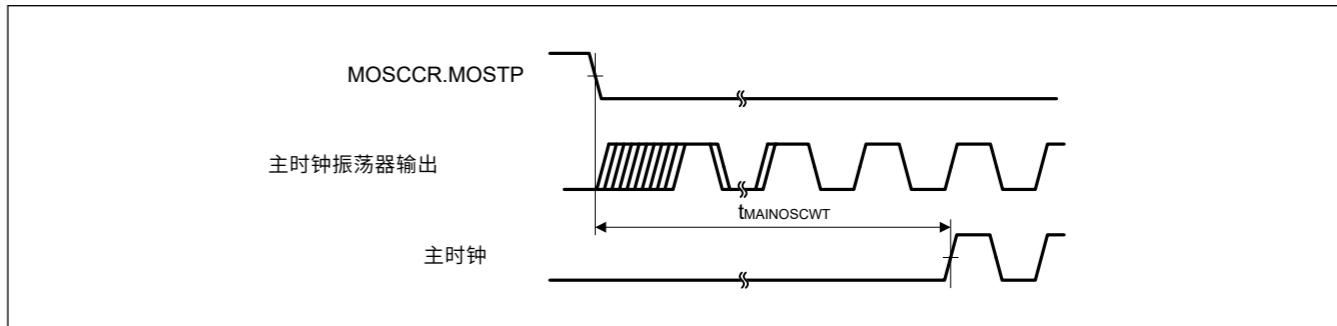


Figure 2.8 主时钟振荡开始时序

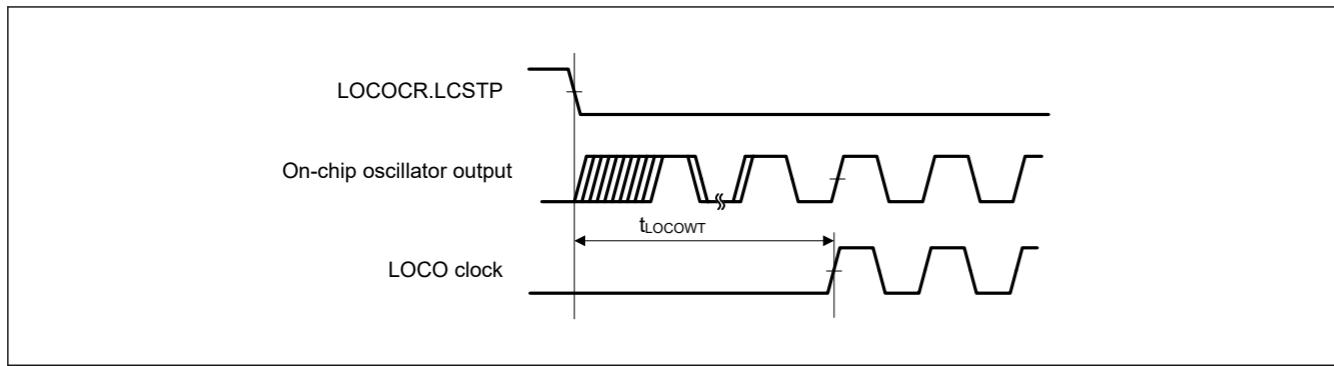


Figure 2.9 LOCO clock oscillation start timing

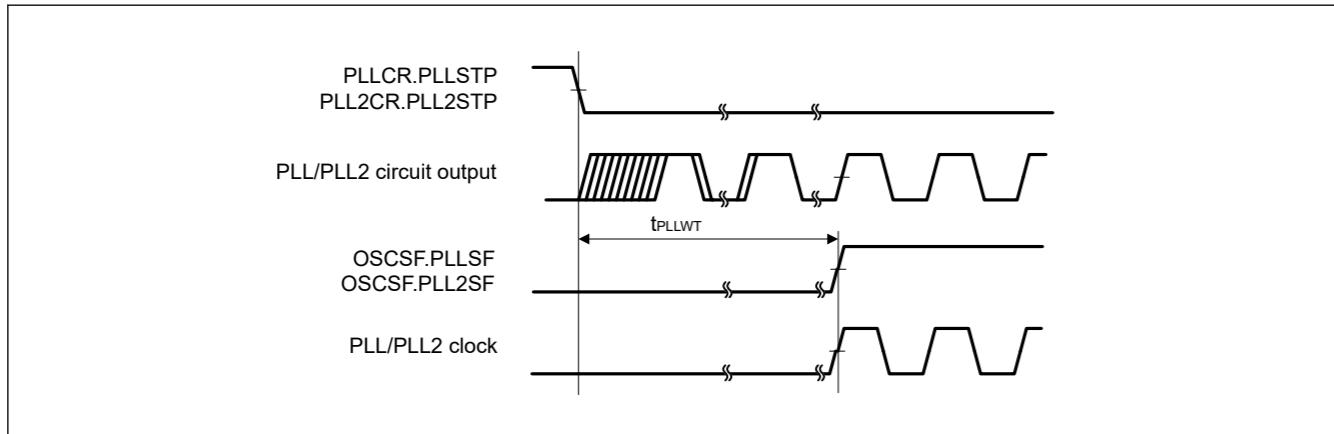


Figure 2.10 PLL/PLL2 clock oscillation start timing

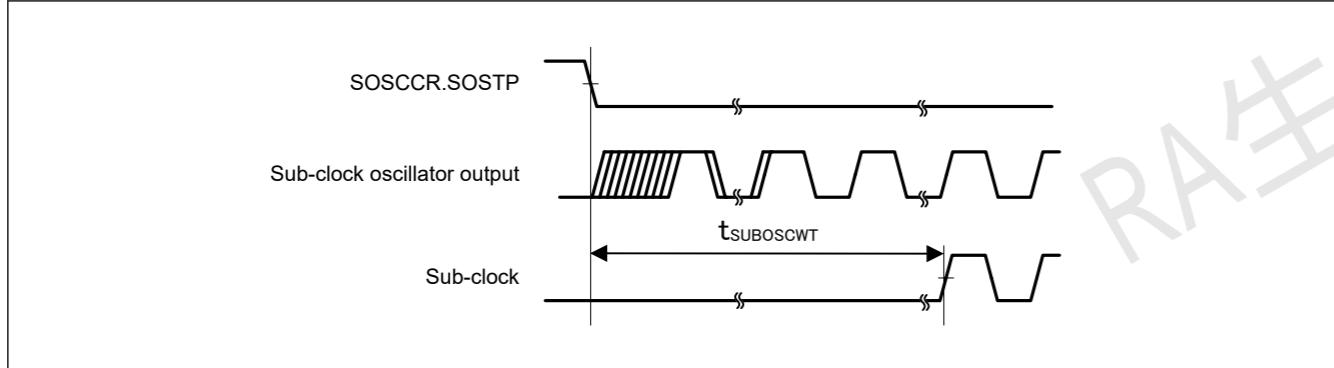


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.19 Reset timing (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------------|--|--------|-----|------|------|------|-----------------------------|
| RES pulse width | Power-on | tRESWP | 0.7 | — | — | ms | Figure 2.12 |
| | Deep Software Standby mode | tRESWD | 0.6 | — | — | ms | Figure 2.13 |
| | Software Standby mode, Subosc-speed mode | tRESWS | 0.3 | — | — | ms | |
| | All other | tRESW | 200 | — | — | μs | |
| Wait time after RES cancellation | | tRESWT | — | 37.3 | 41.2 | μs | Figure 2.12 |

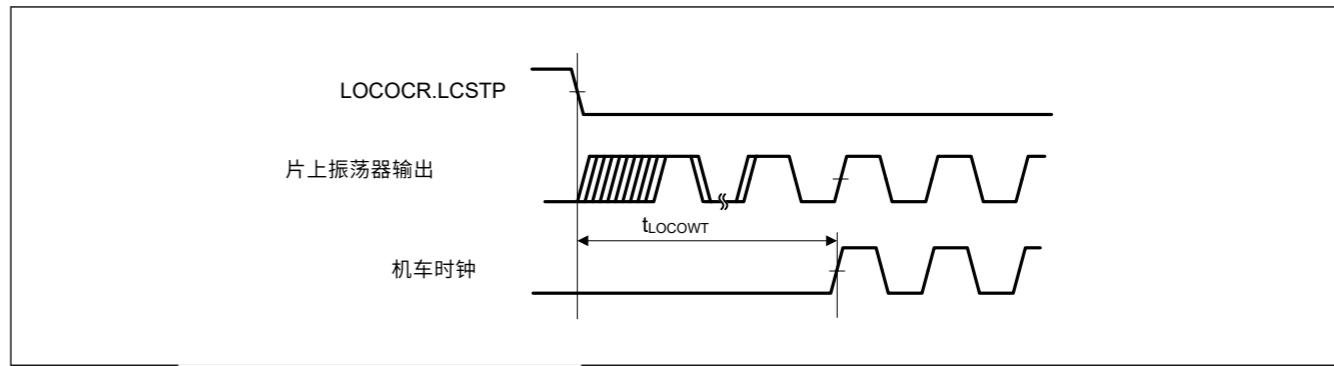


Figure 2.9 LOCO时钟振荡开始时序

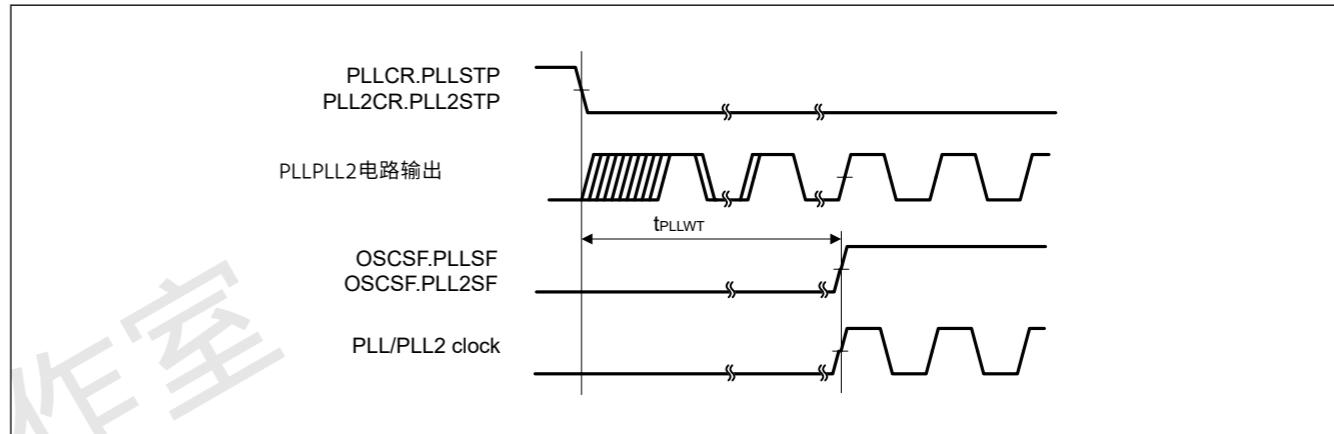


Figure 2.10 PLLPLL2时钟振荡开始时序

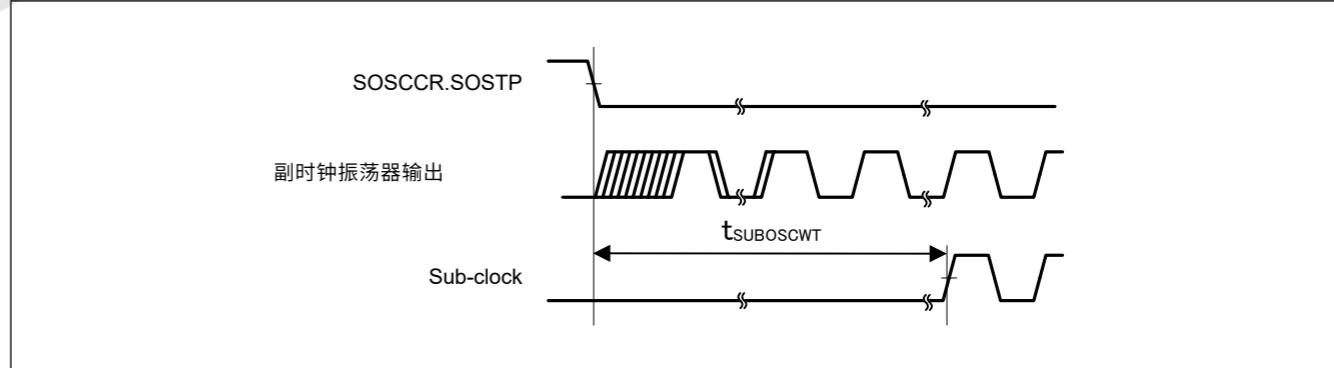


Figure 2.11 副时钟振荡开始时序

2.3.3 重置时间

Table 2.19 重置时间(1 of 2)

| Parameter | | 符号 | 最小值 | 典型值 | Max | 单元测试条件 |
|-------------|--------------------|--------|-----|------|------|--------------------------------|
| RES脉冲宽度 | Power-on | tRESWP | 0.7 | — | — | ms Figure 2.12 |
| | 深度软件待机模式 | tRESWD | 0.6 | — | — | ms Figure 2.13 |
| | 软件待机模式, Subosc速度模式 | tRESWS | 0.3 | — | — | ms |
| | 所有其他 | tRESW | 200 | — | — | μs |
| RES取消后的等待时间 | | tRESWT | — | 37.3 | 41.2 | μs Figure 2.12 |

Table 2.19 Reset timing (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--------|-----|-----|-------|------|-----------------|
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, TrustZone error reset) | tRESW2 | — | 324 | 397.7 | μs | — |

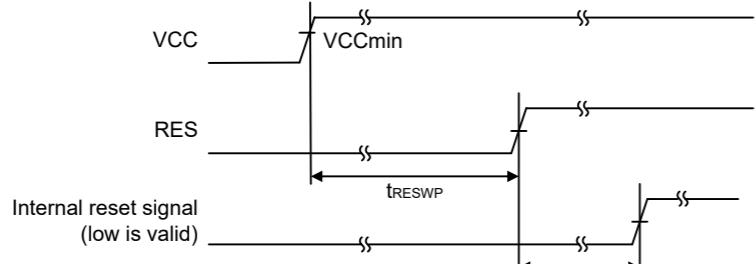


Figure 2.12 RES pin input timing under the condition that VCC exceeds VPOR voltage threshold

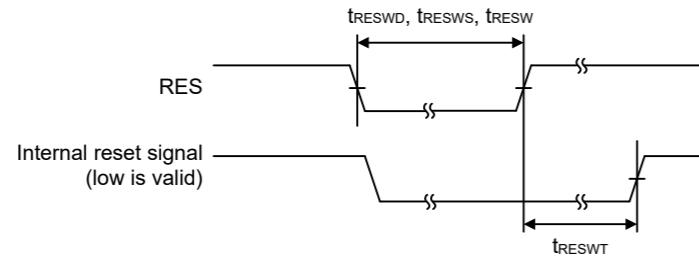


Figure 2.13 Reset input timing

2.3.4 Wakeup Timing

Table 2.20 Timing of recovery from low power modes (1 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--|---|-----------------------|-----|------|-----------------|
| Recovery time from Software Standby mode ^{*1} | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator ^{*2} | tSBYMC ^{*13} | — | 2.1 | 2.4 ms |
| | | System clock source is PLL with main clock oscillator ^{*3} | tSBYPC ^{*13} | — | 2.2 | 2.6 ms |
| | External clock input to main clock oscillator | System clock source is main clock oscillator ^{*4} | tSBYEX ^{*13} | — | 45 | 125 μs |
| | | System clock source is PLL with main clock oscillator ^{*5} | tSBYPE ^{*13} | — | 170 | 255 μs |
| | | System clock source is sub-clock oscillator ^{*6 *11} | tSBYSC ^{*13} | — | 0.7 | 0.8 ms |
| | | System clock source is LOCO ^{*7 *11} | tSBYLO ^{*13} | — | 0.7 | 0.9 ms |
| | | System clock source is HOCO clock oscillator ^{*8} | tSBYHO ^{*13} | — | 55 | 130 μs |
| | | System clock source is PLL with HOCO ^{*9} | tSBYPH ^{*13} | — | 175 | 265 μs |
| | | System clock source is MOCO clock oscillator ^{*10} | tSBYMO ^{*13} | — | 35 | 65 μs |
| | | Figure 2.14 The division ratio of all oscillators is 1. | | | | |

Table 2.19 重置时间 (2之2)

| Parameter | 符号 | 最小值 | 典型值 | Max | 单元测试条件 |
|---|--------|-----|-----|-------|--------|
| 内部复位取消后的等待时间 (IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、总线主控MPU错误复位、TrustZone错误复位) | tRESW2 | — | 324 | 397.7 | μs |

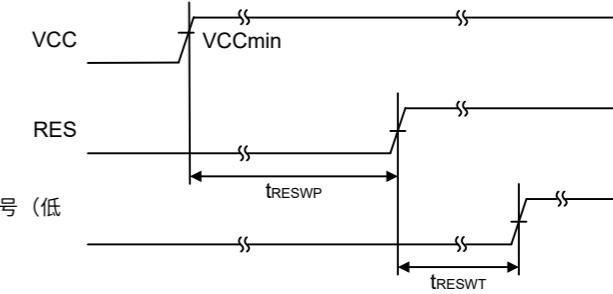


Figure 2.12 VCC超过VPOR电压阈值条件下的RES引脚输入时序

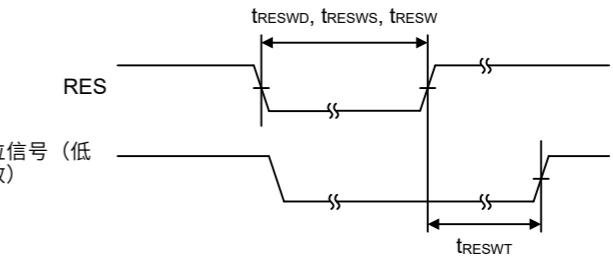


Figure 2.13 复位输入时序

2.3.4 唤醒时间

Table 2.20 从低功耗模式恢复的时间 (2个中的1个)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------|-----------------------------|---------------------------------|-----------------------|-----|------|-----------------|
| 恢复时间从软件待机模式*1 | 连接到主时钟振荡器的晶体谐振器 | 系统时钟源为主时钟振荡器*2 | tSBYMC ^{*13} | — | 2.1 | 2.4 ms |
| | | 系统时钟源为带主时钟振荡器的PLL ^{*3} | tSBYPC ^{*13} | — | 2.2 | 2.6 ms |
| | 主时钟振荡器的外部时钟输入 | 系统时钟源为主时钟振荡器*4 | tSBYEX ^{*13} | — | 45 | 125 μs |
| | | 系统时钟源为带主时钟振荡器的PLL ^{*5} | tSBYPE ^{*13} | — | 170 | 255 μs |
| | | 系统时钟源为副时钟振荡器*6*11 | tSBYSC ^{*13} | — | 0.7 | 0.8 ms |
| | | 系统时钟源为LOCO*7*11 | tSBYLO ^{*13} | — | 0.7 | 0.9 ms |
| | | 系统时钟源为HOCO时钟振荡器*8 | tSBYHO ^{*13} | — | 55 | 130 μs |
| | | 系统时钟源是带有HOCO*9的PLL | tSBYPH ^{*13} | — | 175 | 265 μs |
| | | 系统时钟源为MOCO时钟振荡器*10 | tSBYMO ^{*13} | — | 35 | 65 μs |
| | Figure 2.14 所有振荡器的分频比为1。 | | | | | |

Table 2.20 Timing of recovery from low power modes (2 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---|---------------------|-----|-------------------|-------------------|------------------|-----------------|
| Recovery time from Deep Software Standby mode | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E | t _{DSBY} | — | 0.38 | 0.54 | ms | Figure 2.15 |
| | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19 | t _{DSBY} | — | 0.55 | 0.73 | ms | |
| Wait time after cancellation of Deep Software Standby mode | | t _{DSBYWT} | 56 | — | 57 | t _{cyc} | |
| Recovery time from Software Standby mode to Snooze mode | High-speed mode when system clock source is HOCO (20 MHz) | t _{SNZ} | — | 35 ^{*12} | 70 ^{*12} | μs | Figure 2.16 |
| | High-speed mode when system clock source is MOCO (8 MHz) | t _{SNZ} | — | 11 ^{*12} | 14 ^{*12} | μs | |

- Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:

$$\text{Total recovery time} = \text{recovery time for an oscillator as the system clock source} + \text{the longest tSBYOSCW} \text{ in the active oscillators} - \text{tSBYOSCW} \text{ for the system clock} + 2 \text{ LOCO cycles (when LOCO is operating)} + \text{Subosc is oscillating and MSTPC0 = 0 (CAC module stop))}$$
- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWT) is set to 0x05) and the greatest value of the internal clock division setting is 1.
- Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWT) is set to 0x05) and the greatest value of the internal clock division setting is 4.
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWT) is set to 0x00) and the greatest value of the internal clock division setting is 1.
- Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWT) is set to 0x00) and the greatest value of the internal clock division setting is 4.
- Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
- Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
- Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
- Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
- Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
- Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
- Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 μs (typical), 48 μs (maximum).
- Note 13. The recovery time can be calculated with the equation of tSBYOSCW + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

| Wakeup time | TYP | | MAX | | Unit |
|--------------------|-----------------------------|--|-----------------------------|--|------|
| | t _{SBYOSCW} | t _{SBYSEQ} | t _{SBYOSCW} | t _{SBYSEQ} | |
| t _{SBYMC} | (MSTS[7:0]*32 + 3) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{MAIN} | (MSTS[7:0]*32 + 14) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{MAIN} | μs |
| t _{SBYPC} | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYEX} | 10 | 35 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | 62 | 62 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | μs |
| t _{SBYPE} | 135 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 192 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYSC} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{SUB} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{SUB} | μs |
| t _{SBYLO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{LOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{LOCO} | μs |
| t _{SBYHO} | 20 | 35 + 18 / f _{ICLK} + 4n / f _{HOCO} | 67 | 62 + 18 / f _{ICLK} + 4n / f _{HOCO} | μs |
| t _{SBYPH} | 140 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 202 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYMO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{MOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{MOCO} | μs |

Table 2.20 从低功耗模式恢复的时间 (2个中的2个)

| Parameter | | Symbol | Min | Typ | Max | 单元 | 测试条件 |
|------------------|---|---------------------|-----|-------------------|-------------------|------------------|-------------|
| 恢复时间从深度软件待机模式 | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E | t _{DSBY} | — | 0.38 | 0.54 | ms | Figure 2.15 |
| | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19 | t _{DSBY} | — | 0.55 | 0.73 | ms | |
| 取消深度软件待机模式后的等待时间 | | t _{DSBYWT} | 56 | — | 57 | t _{cyc} | |
| 恢复时间从软件待机模式到贪睡模式 | 系统时钟源为高速模式 HOCO (20 MHz) | t _{SNZ} | — | 35 ^{*12} | 70 ^{*12} | μs | Figure 2.16 |
| | 系统时钟源为高速模式 MOCO (8 MHz) | t _{SNZ} | — | 11 ^{*12} | 14 ^{*12} | μs | |

注1. 恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=一个振荡器作为系统时钟源的恢复时间+系统时钟有效振荡器中的最长tSBYOSCW+2个LOCO周期（当LOCO正在运行）+Subosc正在振荡且MSTPC0=0（CA C模块停止）

注2. 当晶振频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWT）设置为0x05）且内部时钟分频设置的最大值为1时。

注3. 当PLL的频率为200MHz（主时钟振荡器等待控制寄存器（MOSCWT）设置为0x05）且内部时钟分频设置的最大值为4时。

注4. 当外部时钟频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWT）设置为0x00）且内部时钟分频设置的最大值为1时。

注5. 当PLL的频率为200MHz（主时钟振荡器等待控制寄存器（MOSCWT）设置为0x00）且内部时钟分频设置的最大值为4时。

注6. 副时钟振荡器频率为32.768KHz，内部时钟分频设置的最大值为1。

注7. LOCO频率为32.768kHz，内部时钟分频设置的最大值为1。

注8. HOCO频率为20MHz，内部时钟分频设置最大值为1。注9. PLL频率为200MHz，内部时钟分频设置最大值为4。注10. MOCO频率为8MHz，内部时钟分频设置的最大值为1。

注11. 在Subosc速度模式下，副时钟振荡器或LOCO在软件待机模式下继续振荡。

注12. 当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：16μs（典型值）、48μs（最大值）。

注13. 恢复时间可以用tSBYOSCW+tSBYSEQ等式计算。并且它们可以通过以下值和等式确定。对于n，从内部时钟分频设置中选择最大值。

| 唤醒时间 | 典型值 | | MAX | | Unit |
|--------------------|-----------------------------|--|-----------------------------|--|------|
| | t _{SBYOSCW} | t _{SBYSEQ} | t _{SBYOSCW} | t _{SBYSEQ} | |
| t _{SBYMC} | (MSTS[7:0]*32 + 3) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{MAIN} | (MSTS[7:0]*32 + 14) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{MAIN} | μs |
| t _{SBYPC} | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYEX} | 10 | 35 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | 62 | 62 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | μs |
| t _{SBYPE} | 135 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 192 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYSC} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{SUB} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{SUB} | μs |
| t _{SBYLO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{LOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{LOCO} | μs |
| t _{SBYHO} | 20 | 35 + 18 / f _{ICLK} + 4n / f _{HOCO} | 67 | 62 + 18 / f _{ICLK} + 4n / f _{HOCO} | μs |
| t _{SBYPH} | 140 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 202 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYMO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{MOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{MOCO} | μs |

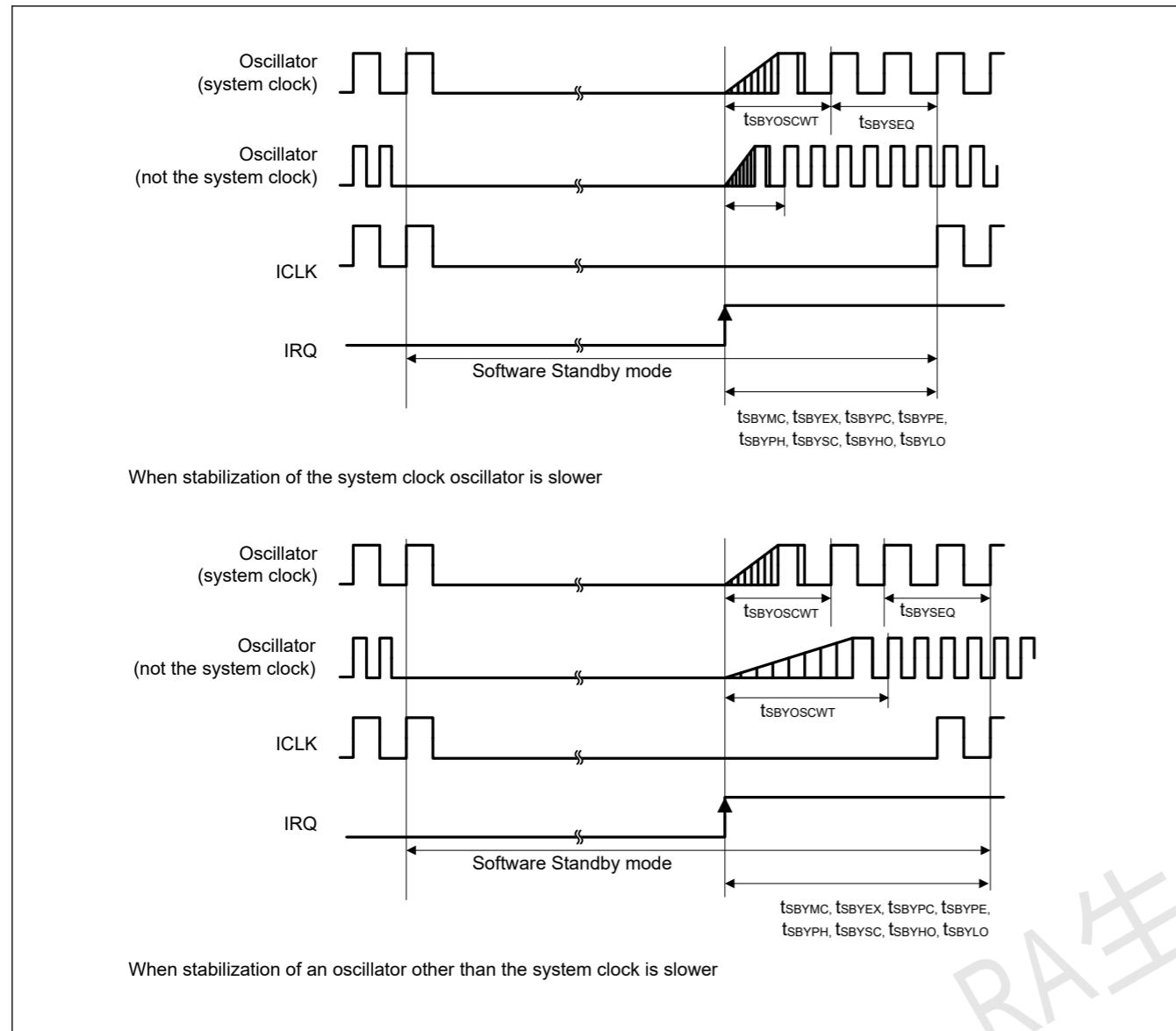


Figure 2.14 Software Standby mode cancellation timing

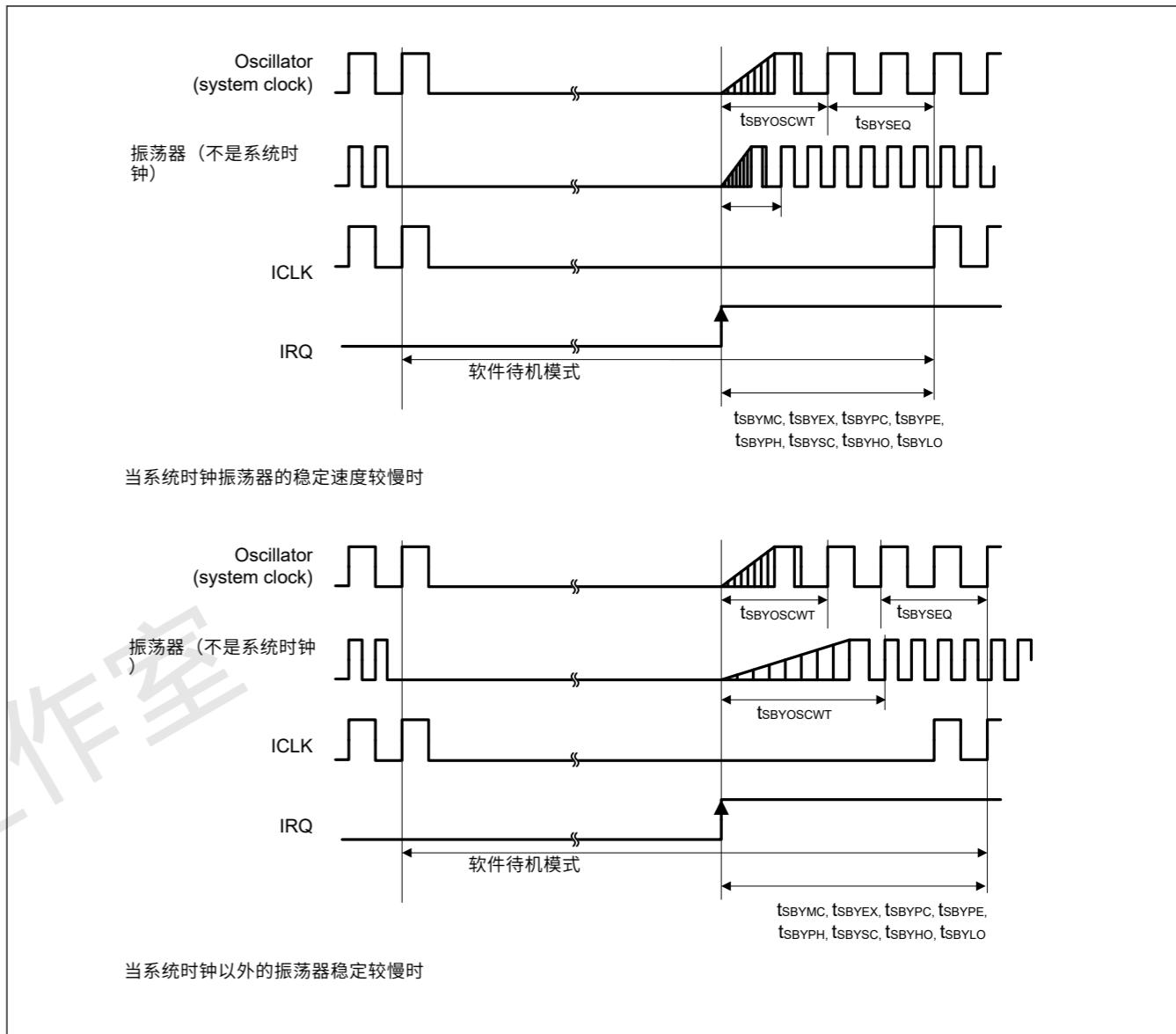


Figure 2.14 软件待机模式取消时序

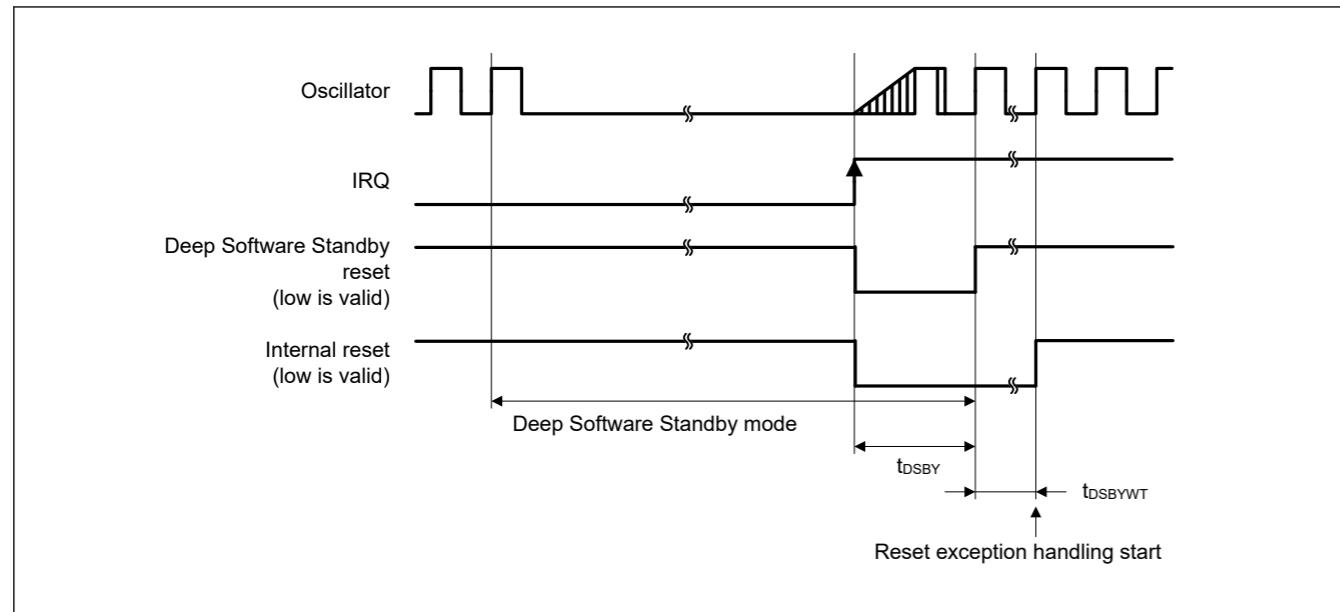


Figure 2.15 Deep Software Standby mode cancellation timing

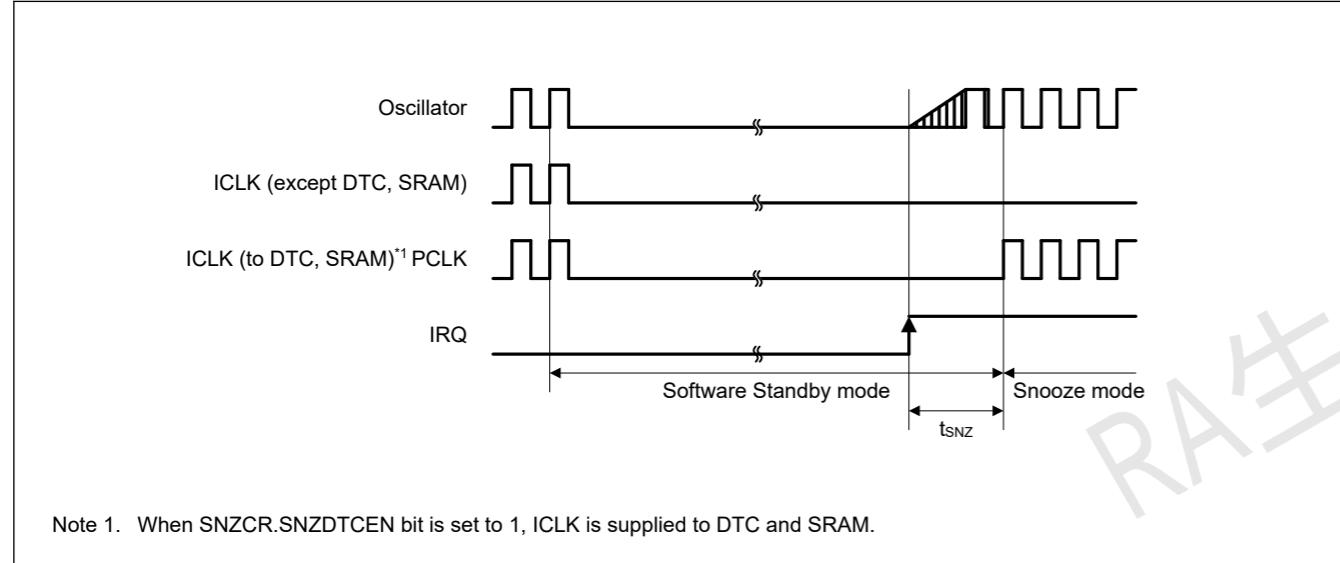


Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.21 NMI and IRQ noise filter

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|-----------------|-------------------|--|-----|-----|------|-----------------------------|---------------------------------|
| NMI pulse width | t _{NMIW} | 200 | — | — | ns | NMI digital filter disabled | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2 ^{*1} | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | NMI digital filter enabled | t _{NMICK} × 3 ≤ 200 ns |
| | | t _{NMICK} × 3.5 ^{*2} | — | — | | | t _{NMICK} × 3 > 200 ns |
| IRQ pulse width | t _{IRQW} | 200 | — | — | ns | IRQ digital filter disabled | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2 ^{*1} | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | IRQ digital filter enabled | t _{IRQCK} × 3 ≤ 200 ns |
| | | t _{IRQCK} × 3.5 ^{*3} | — | — | | | t _{IRQCK} × 3 > 200 ns |

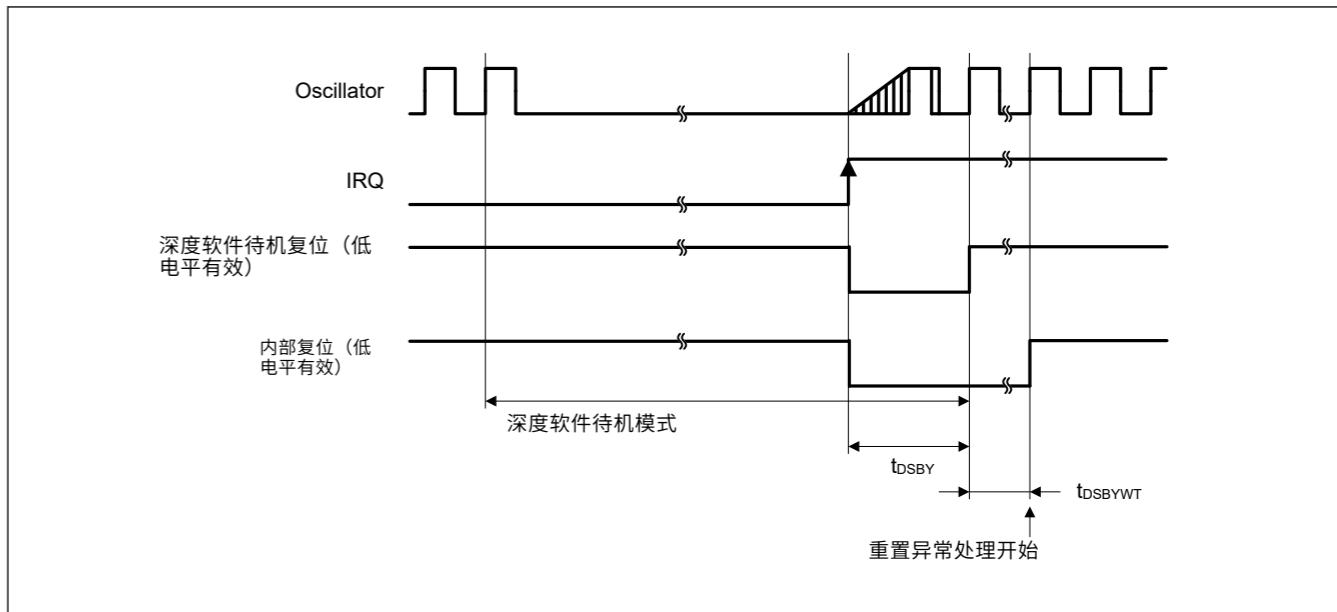


Figure 2.15 深度软件待机模式取消时序

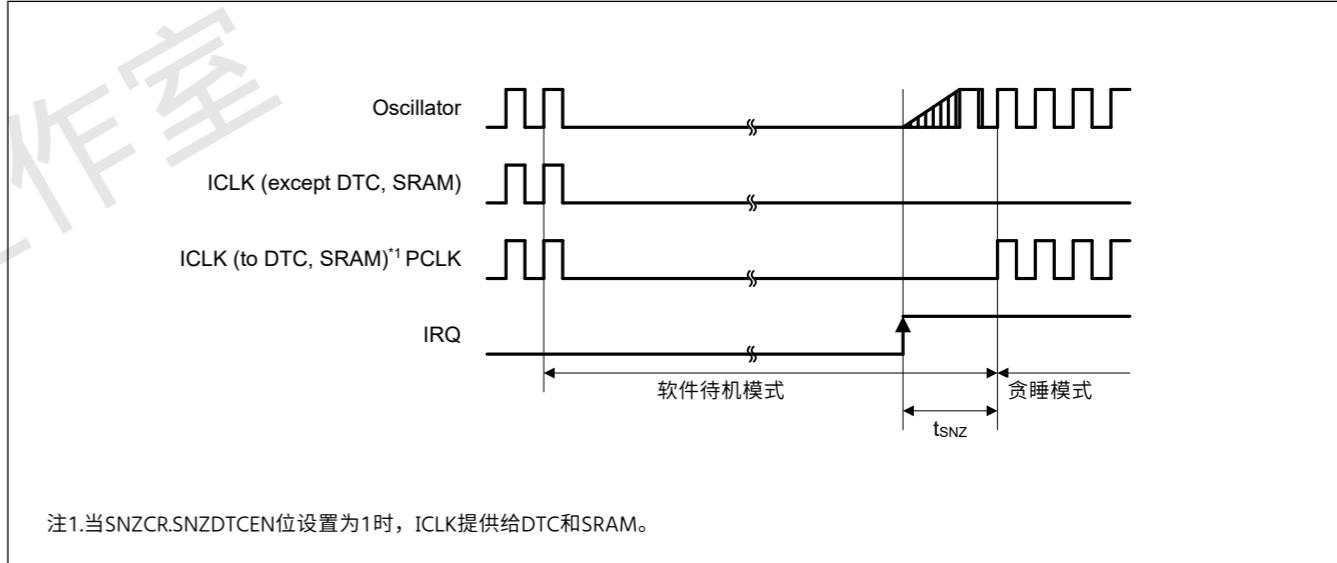


Figure 2.16 从软件待机模式到贪睡模式的恢复时间

2.3.5 NMI和IRQ噪声滤波器

Table 2.21 NMI和IRQ噪声滤波器

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 | |
|-----------|-------------------|--|-----|-----|------|------------|---------------------------------|
| NMI脉冲宽度 | t _{NMIW} | 200 | — | — | ns | NMI数字滤波器禁用 | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2 ^{*1} | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | 启用NMI数字滤波器 | t _{NMICK} × 3 ≤ 200 ns |
| | | t _{NMICK} × 3.5 ^{*2} | — | — | | | t _{NMICK} × 3 > 200 ns |
| IRQ脉冲宽度 | t _{IRQW} | 200 | — | — | ns | IRQ数字滤波器禁用 | t _{Pcyc} × 2 ≤ 200 ns |
| | | t _{Pcyc} × 2 ^{*1} | — | — | | | t _{Pcyc} × 2 > 200 ns |
| | | 200 | — | — | | 启用IRQ数字滤波器 | t _{IRQCK} × 3 ≤ 200 ns |
| | | t _{IRQCK} × 3.5 ^{*3} | — | — | | | t _{IRQCK} × 3 > 200 ns |

- Note: 200 ns minimum in Software Standby mode.
 Note: If the clock source is switched, add 4 clock cycles of the switched source.
 Note 1. t_{Pcyc} indicates the PCLKB cycle.
 Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
 Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

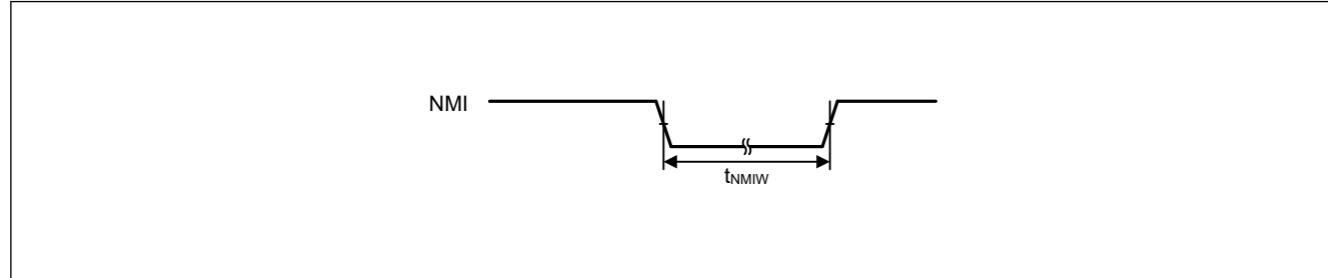


Figure 2.17 NMI interrupt input timing

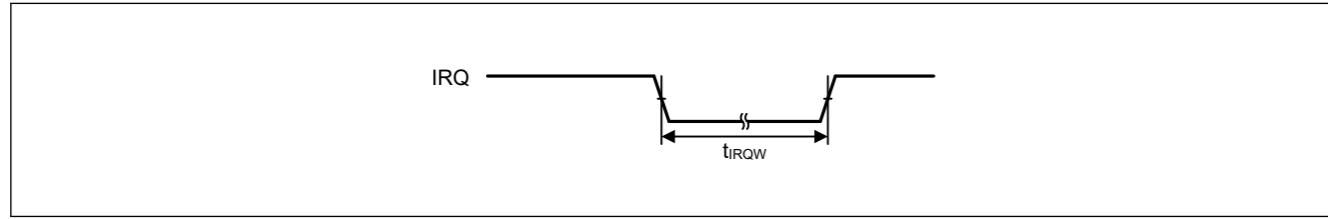


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT32 Conditions:

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:

Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|-----------|--|------------------------|------|-----|-------------|-----------------------------|
| I/O ports | Input data pulse width | t_{PRW} | 1.5 | — | t_{Pcyc} | Figure 2.19 |
| POEG | POEG input trigger pulse width | t_{POEW} | 3 | — | t_{Pcyc} | Figure 2.20 |
| GPT | Input capture pulse width (Single edge) | t_{GTICW} | 1.5 | — | t_{PDcyc} | Figure 2.21 |
| | | | 2.5 | — | | |
| | GTIOCxY output skew (x = 1, 2, Y = A or B) Middle drive buffer | t_{GTISK}^* | — | 4 | ns | Figure 2.22 |
| | | | — | 4 | | |
| | GTIOCxY output skew (x = 4, 5, Y = A or B) Middle drive buffer | t_{GTISK}^* | — | 4 | | |
| | | | — | 4 | | |
| | GTIOCxY output skew (x = 1, 2, 4, 5, Y = A or B) Middle drive buffer | t_{GTISK}^* | — | 6 | | |
| | | | — | 6 | | |
| AGT | AGTIO, AGTEE input cycle | t_{ACYC}^* | 100 | — | ns | Figure 2.23 |
| | AGTIO, AGTEE input high width, low width | t_{ACKWH}, t_{ACKWL} | 40 | — | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | t_{ACYC2} | 62.5 | — | ns | |
| ADC12 | ADC12 trigger input pulse width | t_{TRGW} | 1.5 | — | t_{Pcyc} | Figure 2.24 |

Note: t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle.

Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.

Note 2. Constraints on input cycle:

When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

- Note: 软件待机模式下最少200ns。
 Note: 如果时钟源切换，则增加切换源的4个时钟周期。
 注1.tPcyc表示PCLKB周期。
 注2.tNMICK表示NMI数字滤波器采样时钟的周期。注3.tIRQCK表示IRQi数字滤波器采样时钟的周期。

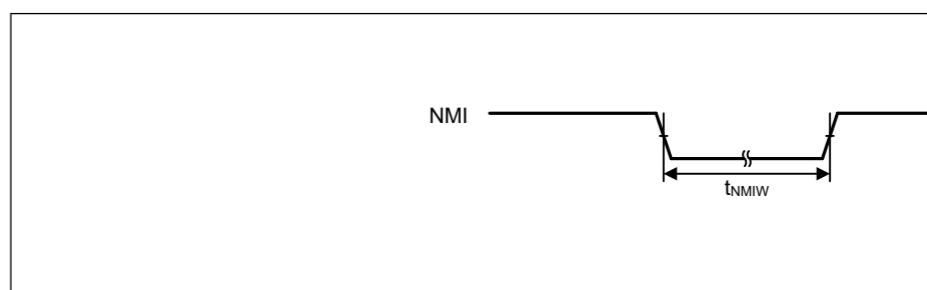


Figure 2.17 NMI中断输入时序

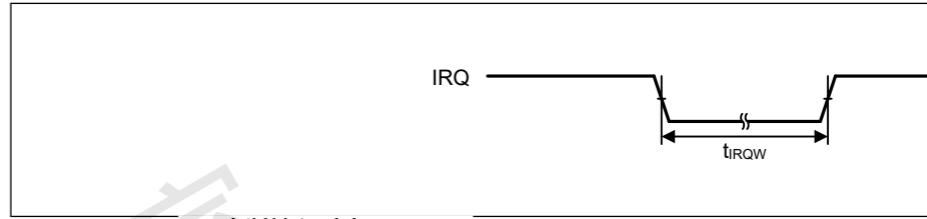


Figure 2.18 IRQ中断输入时序

2.3.6 IO端口、POEG、GPT、AGT和ADC12触发时序

Table 2.22 IO端口、POEG、GPT、AGT和ADC12触发时序

GPT32 Conditions:

在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:

在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter | | Symbol | Min | Max | Unit | 测试条件 |
|-----------|---|------------------------|------|-----|-------------|-----------------------------|
| I/O ports | 输入数据脉冲宽度 | t_{PRW} | 1.5 | — | t_{Pcyc} | Figure 2.19 |
| POEG | POEG输入触发脉冲宽度 | t_{POEW} | 3 | — | t_{Pcyc} | Figure 2.20 |
| GPT | 输入捕捉脉冲宽度 (单边) | t_{GTICW} | 1.5 | — | t_{PDcyc} | Figure 2.21 |
| | | | 2.5 | — | | |
| | GTIOCxY输出偏移 (x = 1, 2, Y = A或B) 中间驱动缓冲器 | t_{GTISK}^* | — | 4 | ns | Figure 2.22 |
| | | | — | 4 | | |
| | GTIOCxY输出偏移 (x = 4, 5, Y = A或B) 中间驱动缓冲器 | t_{GTISK}^* | — | 4 | | |
| | | | — | 4 | | |
| | GTIOCxY输出偏移 (x = 1, 2, 4, 5, Y = A或B) 中间驱动缓冲器 | t_{GTISK}^* | — | 6 | | |
| | | | — | 6 | | |
| AGT | AGTIO, AGTEE输入周期 | t_{ACYC}^* | 100 | — | ns | Figure 2.23 |
| | AGTIO, AGTEE输入高宽、低宽 | t_{ACKWH}, t_{ACKWL} | 40 | — | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB输出周期 | t_{ACYC2} | 62.5 | — | ns | |
| ADC12 | ADC12触发输入脉冲宽度 | t_{TRGW} | 1.5 | — | t_{Pcyc} | Figure 2.24 |

Note: t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle.

注1.当使用相同的驱动器IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。

注2.输入周期的限制：

不切换源时钟时： $t_{Pcyc} \times 2 < t_{ACYC}$ 应满足。切换源时钟时： $t_{Pcyc} \times 6 < t_{ACYC}$ 应满足。

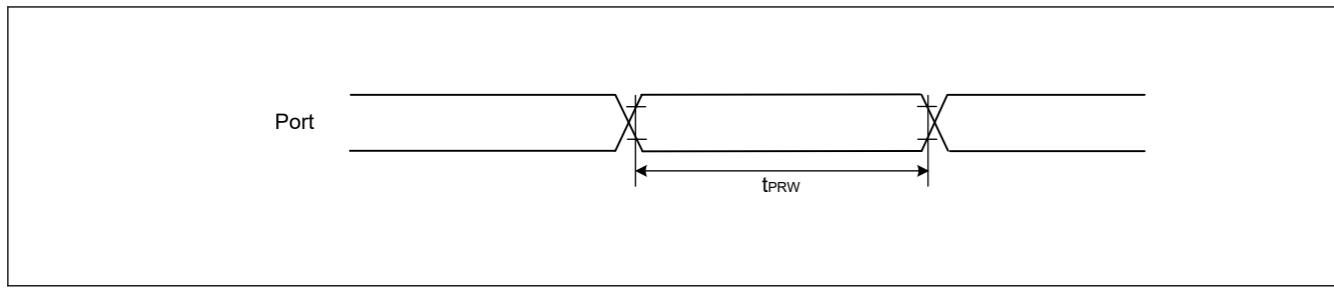


Figure 2.19 I/O ports input timing

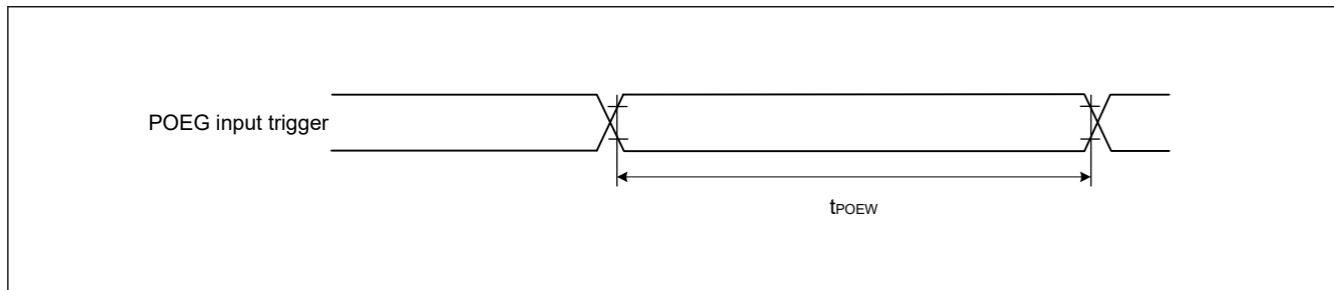


Figure 2.20 POEG input trigger timing

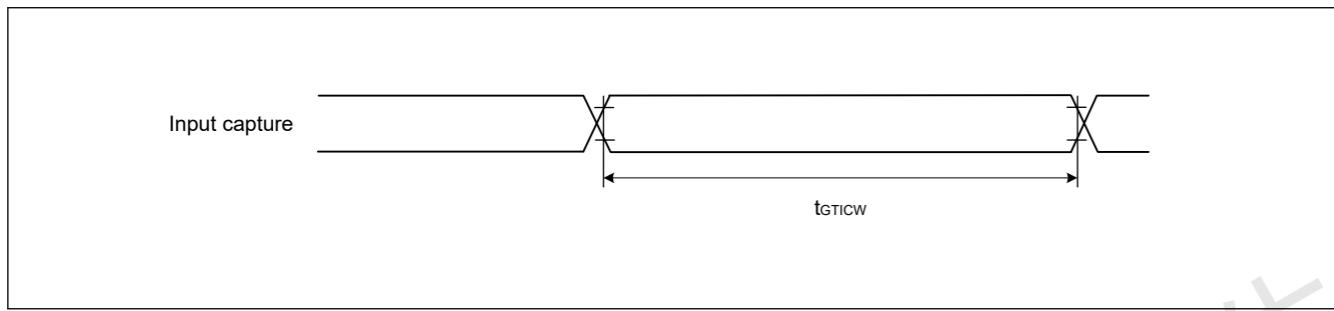


Figure 2.21 GPT input capture timing

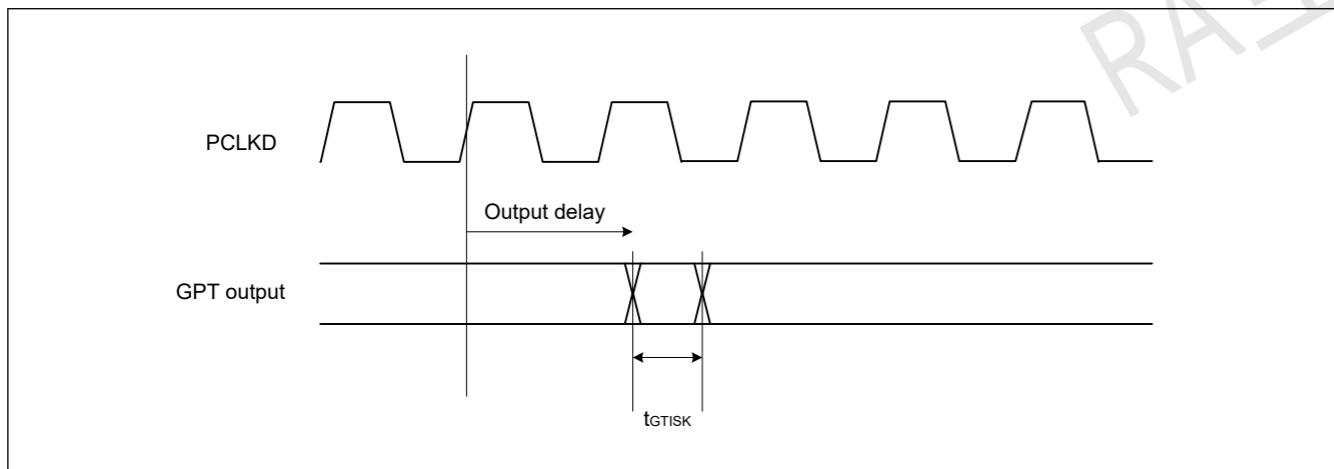


Figure 2.22 GPT output delay skew

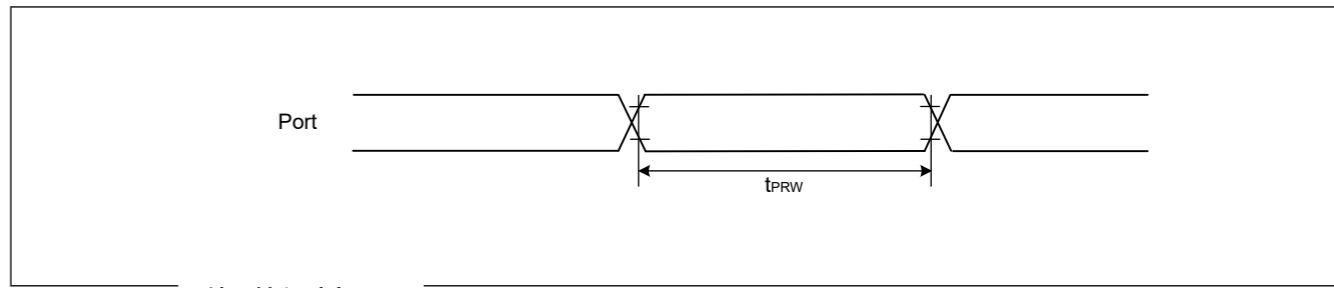


Figure 2.19 IO端口输入时序

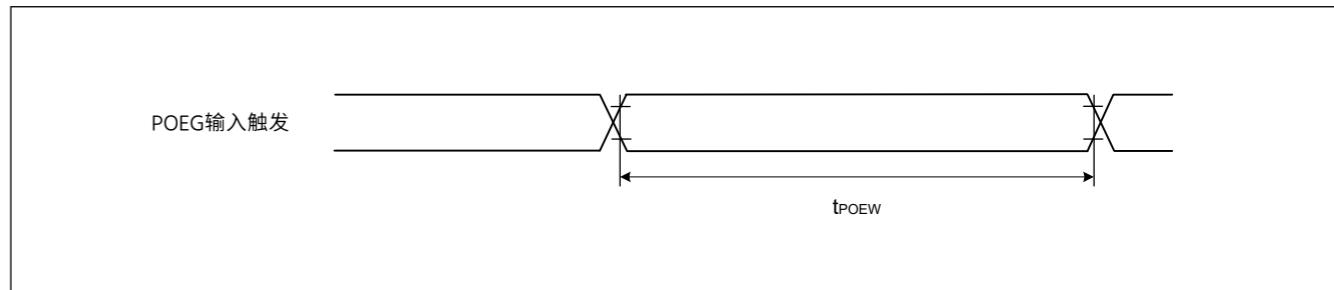


Figure 2.20 POEG输入触发时序

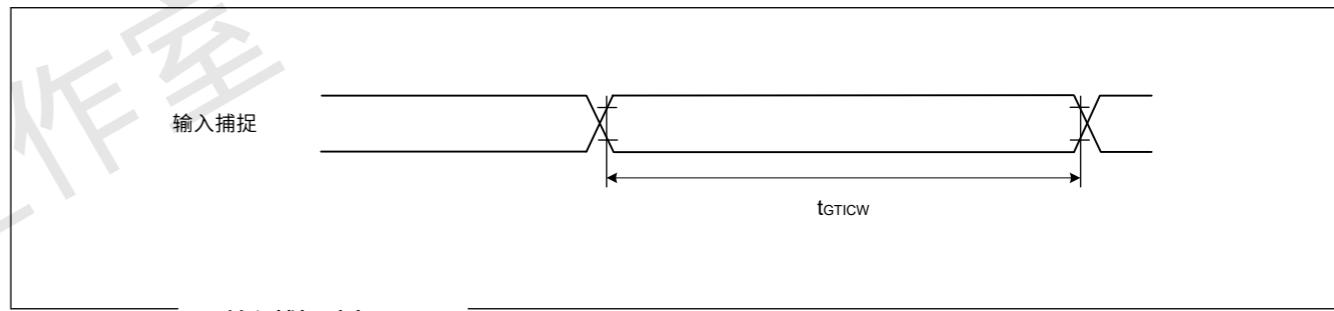


Figure 2.21 GPT输入捕捉时序

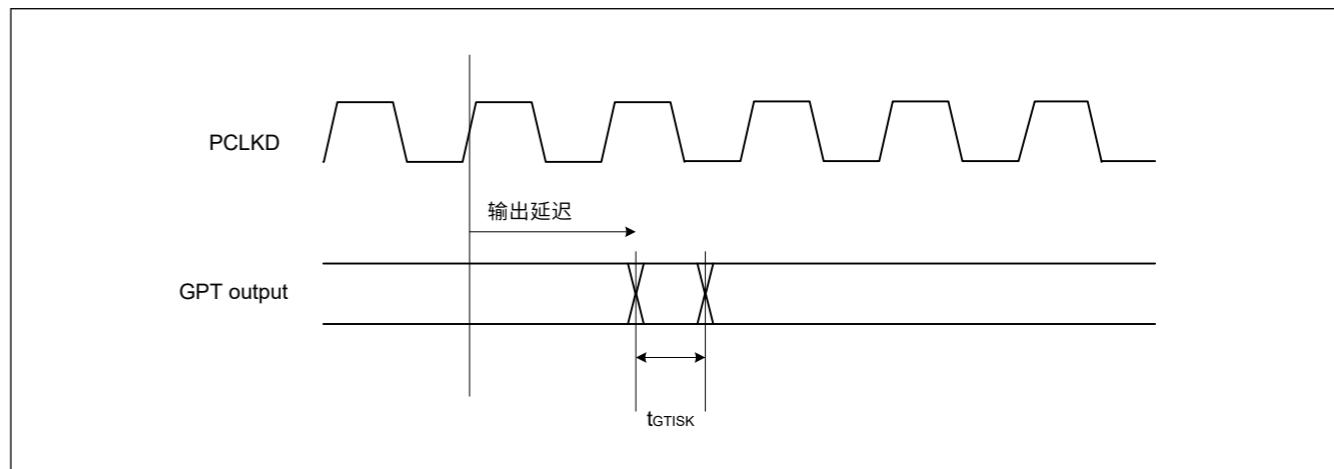


Figure 2.22 GPT输出延迟偏差

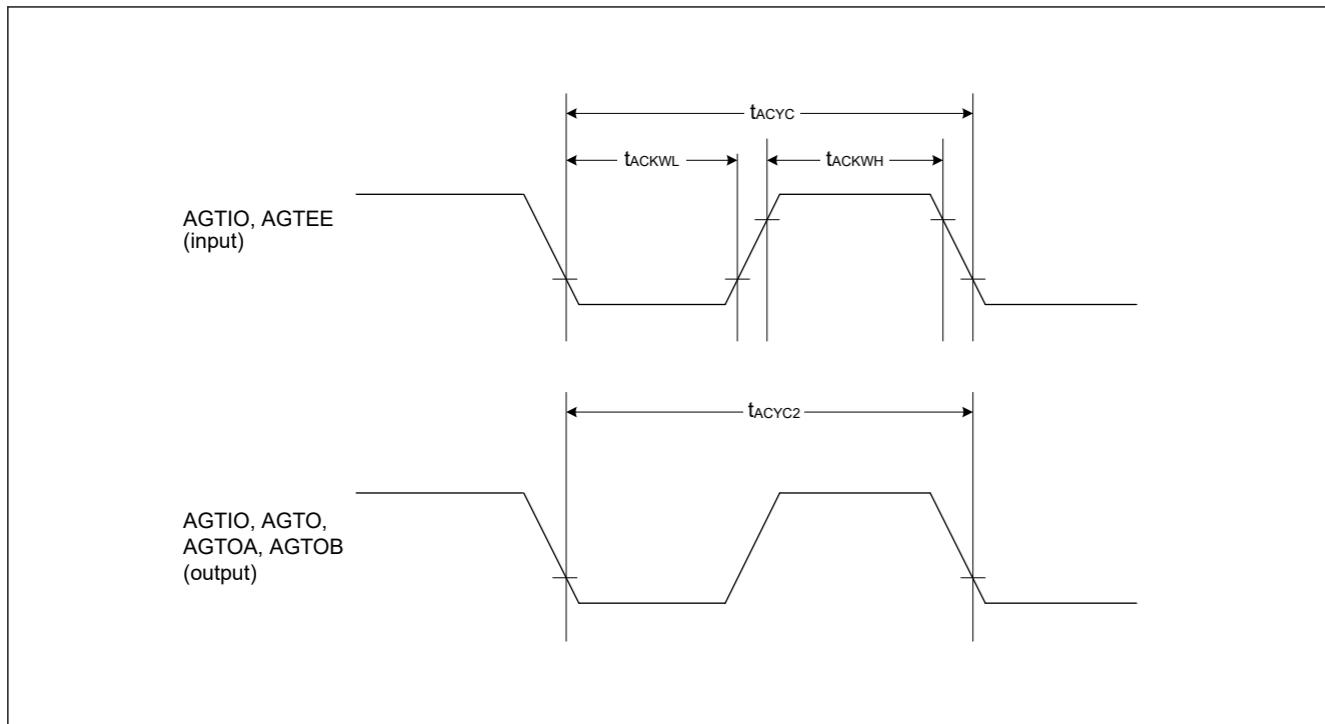


Figure 2.23 AGT input/output timing

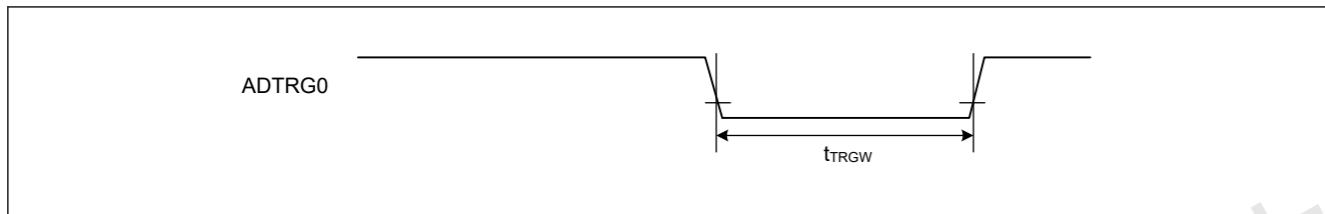


Figure 2.24 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.23 CAC timing

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------|--------------------------|---|---------------------|---|-----|-----|------|-----------------|
| CAC | CACREF input pulse width | t _{PBcyc} ≤ t _{cac} ^{*1} | t _{CACREF} | 4.5 × t _{cac} + 3 × t _{PBcyc} | — | — | ns | — |
| | | t _{PBcyc} > t _{cac} ^{*1} | | 5 × t _{cac} + 6.5 × t _{PBcyc} | — | — | ns | |

Note: t_{PBcyc}: PCLKB cycle.

Note 1. t_{cac}: CAC count clock source cycle.

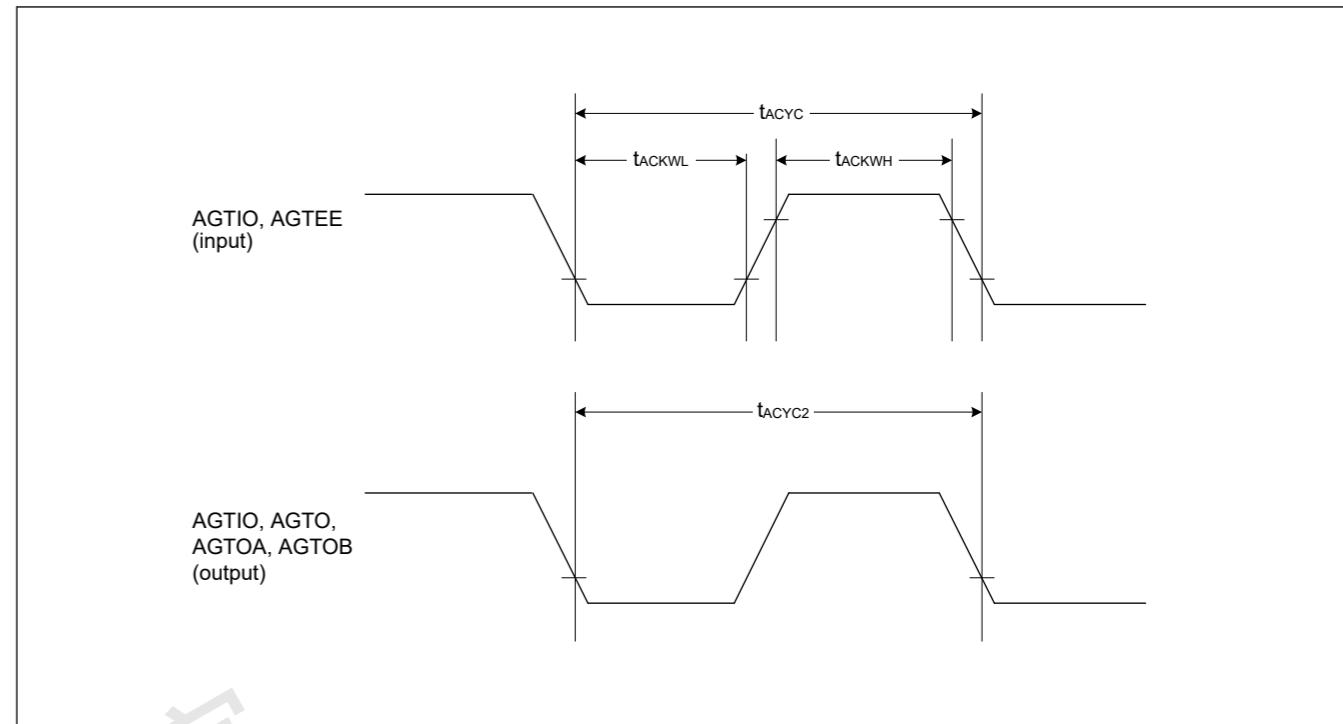


Figure 2.23 AGT input/output timing

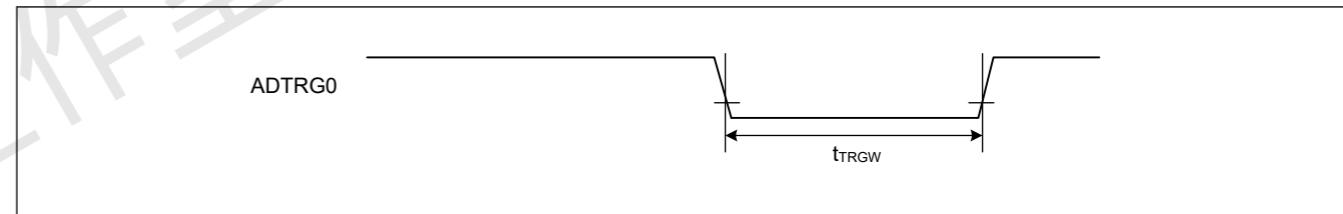


Figure 2.24 ADC12触发输入时序

2.3.7 CAC时序

Table 2.23 CAC计时

| Parameter | | | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-----------|--------------|---|---------------------|---|-----|-----|------|------|
| CAC | CACREF输入脉冲宽度 | t _{PBcyc} ≤ t _{cac} ^{*1} | t _{CACREF} | 4.5 × t _{cac} + 3 × t _{PBcyc} | — | — | ns | — |
| | | t _{PBcyc} > t _{cac} ^{*1} | | 5 × t _{cac} + 6.5 × t _{PBcyc} | — | — | ns | |

Note: t_{PBcyc}: PCLKB cycle.

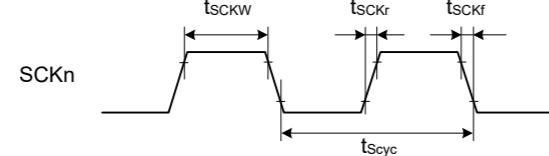
注1.t_{cac}: CAC计数时钟源周期。

2.3.8 SCI Timing

Table 2.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|-------------------------|--|-------------------|-------------------|---|-----|-------------------|-----------------|
| SCI | Input clock cycle | Asynchronous | t _{Scyc} | 4 | — | t _{Pcyc} | Figure 2.25 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Input clock rise time | | t _{SCKr} | — | 5 | ns | |
| | Input clock fall time | | t _{SCKf} | — | 5 | ns | |
| | Output clock cycle | Asynchronous | t _{Scyc} | 6 (other than SCI1, SCI2) 8 (SCI1, SCI2) | — | t _{Pcyc} | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Output clock rise time | | t _{SCKr} | — | 5 | ns | |
| | Output clock fall time | | t _{SCKf} | — | 5 | ns | |
| Transmit data delay | Clock synchronous master mode (internal clock) | t _{TXD} | — | 5 | ns | Figure 2.26 | Figure 2.26 |
| | Clock synchronous slave mode (external clock) | t _{TXD} | — | 25 | ns | | |
| Receive data setup time | Clock synchronous master mode (internal clock) | t _{RXS} | 15 | — | ns | | |
| | Clock synchronous slave mode (external clock) | t _{RXS} | 5 | — | ns | | |
| Receive data hold time | Clock synchronous | t _{RXH} | 5 | — | ns | | |

Note: t_{Pcyc}: PCLKA cycle.

Note: n = 0, 3, 4, 9

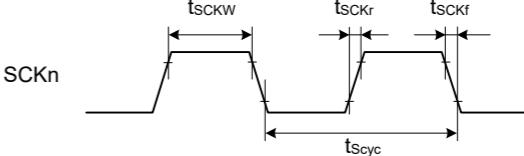
Figure 2.25 SCK clock input/output timing

2.3.8 SCI时序

Table 2.24 SCI时序 (1)

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | | 符号最小值 | | 最大单位 | 测试条件 |
|-----------|------------------------|-------------------|---|-------------------|-------------------------------|
| SCI输入时钟周期 | Asynchronous | t _{Scyc} | 4 | — | t _{Pcyc} Figure 2.25 |
| | 时钟同步 | | 6 | — | |
| 输入时钟脉冲宽度 | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} |
| 输入时钟上升时间 | | t _{SCKr} | — | 5 | ns |
| 输入时钟下降时间 | | t _{SCKf} | — | 5 | ns |
| 输出时钟周期 | Asynchronous | t _{Scyc} | 6 (other than SCI1, SCI2) 8 (SCI1, SCI2) | t _{Pcyc} | |
| 时钟同步 | | 4 | — | | |
| 输出时钟脉冲宽度 | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} |
| 输出时钟上升时间 | | t _{SCKr} | — | 5 | ns |
| 输出时钟下降时间 | | t _{SCKf} | — | 5 | ns |
| 传输数据延迟 | 时钟同步主模式 (内部时钟) | t _{TXD} | — | 5 | ns Figure 2.26 |
| | 时钟同步从机模式 (外部时钟) | t _{TXD} | — | 25 | ns |
| | 接收数据建立时间时钟同步主模式 (内部时钟) | t _{RXS} | 15 | — | ns |
| | 时钟同步从机模式 (外部时钟) | t _{RXS} | 5 | — | ns |
| 接收数据保持时间 | | t _{RXH} | 5 | — | ns |

Note: t_{Pcyc}: PCLKA cycle.

Note: n = 0, 3, 4, 9

Figure 2.25 SCK时钟输入输出时序

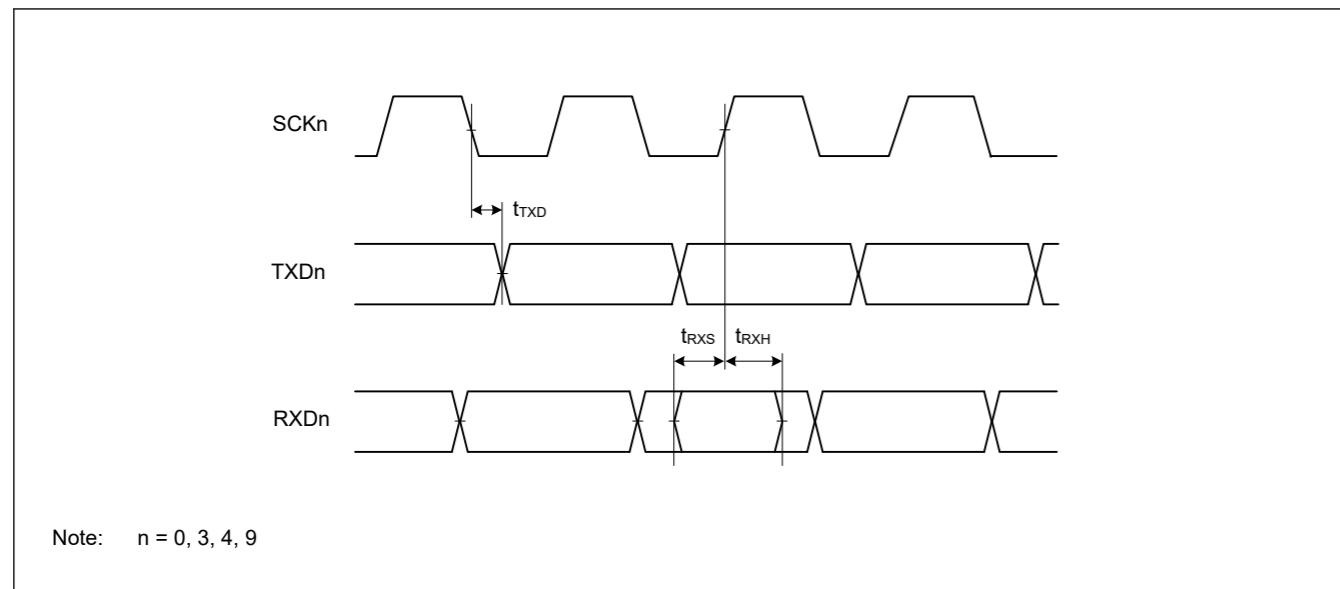


Figure 2.26 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|------------|---------------------------------|------------------------|-----|--------------------------|-------------|-----------------|
| Simple SPI | SCK clock cycle output (master) | t_{SPcyc} | 4 | 65536 | t_{Pcyc} | Figure 2.27 |
| | SCK clock cycle input (slave) | | 6 | 65536 | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock rise and fall time | t_{SPCKr}, t_{SPCKf} | — | 5 | ns | |
| | Data input setup time | t_{SU} | 15 | — | ns | |
| | master | | 5 | — | ns | |
| | slave | | — | — | ns | |
| | Data input hold time | t_H | 5 | — | ns | |
| | SS input setup time | t_{LEAD} | 1 | — | t_{SPcyc} | |
| | SS input hold time | t_{LAG} | 1 | — | t_{SPcyc} | |
| | Data output delay | t_{OD} | — | 5 | ns | |
| | master | | — | 25 | ns | |
| | slave | | — | — | ns | |
| | Data output hold time | t_{OH} | -5 | — | ns | |
| | Data rise and fall time | t_{Dr}, t_{Df} | — | 5 | ns | |
| | SS input rise and fall time | t_{SSLr}, t_{SSLf} | — | 5 | ns | |
| | Slave access time | t_{SA} | — | $3 \times t_{Pcyc} + 25$ | ns | Figure 2.31 |
| | Slave output release time | t_{REL} | — | $3 \times t_{Pcyc} + 25$ | ns | |

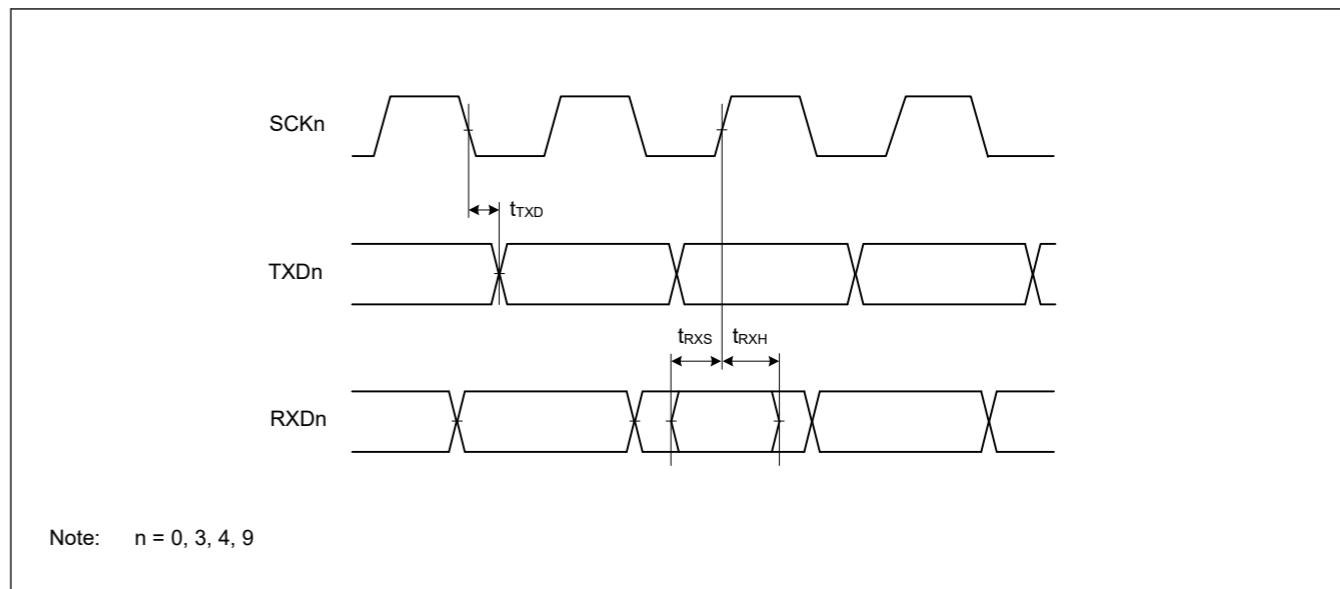
Note: t_{Pcyc} : PCLKA cycle.

Figure 2.26 时钟同步模式下的SCI输入输出时序

Table 2.25 SCI时序 (2)

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|-----------|---------------|------------------------|-----|--------------------------|-------------|
| 简单的SPI | SCK时钟周期输出（主机） | t_{SPcyc} | 4 | 65536 | t_{Pcyc} |
| | SCK时钟周期输入（从机） | | 6 | 65536 | |
| | SCK时钟高脉冲宽度 | t_{SPCKWH} | 0.4 | 0.6 | t_{SPcyc} |
| | SCK时钟低脉冲宽度 | t_{SPCKWL} | 0.4 | 0.6 | t_{SPcyc} |
| | SCK时钟上升和下降时间 | t_{SPCKr}, t_{SPCKf} | — | 5 | ns |
| | 数据输入建立时间 | t_{SU} | 15 | — | ns |
| | master | | 5 | — | ns |
| | slave | | — | — | ns |
| | 数据输入保持时间 | t_H | 5 | — | ns |
| | SS输入建立时间 | t_{LEAD} | 1 | — | t_{SPcyc} |
| | SS输入保持时间 | t_{LAG} | 1 | — | t_{SPcyc} |
| | 数据输出延迟 | t_{OD} | — | 5 | ns |
| | master | | — | 25 | ns |
| | slave | | — | — | ns |
| | 数据输出保持时间 | t_{OH} | -5 | — | ns |
| | 数据上升和下降时间 | t_{Dr}, t_{Df} | — | 5 | ns |
| | SS输入上升和下降时间 | t_{SSLr}, t_{SSLf} | — | 5 | ns |
| | 从站访问时间 | t_{SA} | — | $3 \times t_{Pcyc} + 25$ | ns |
| | 从机输出释放时间 | t_{REL} | — | $3 \times t_{Pcyc} + 25$ | ns |

Note: t_{Pcyc} : PCLKA cycle.

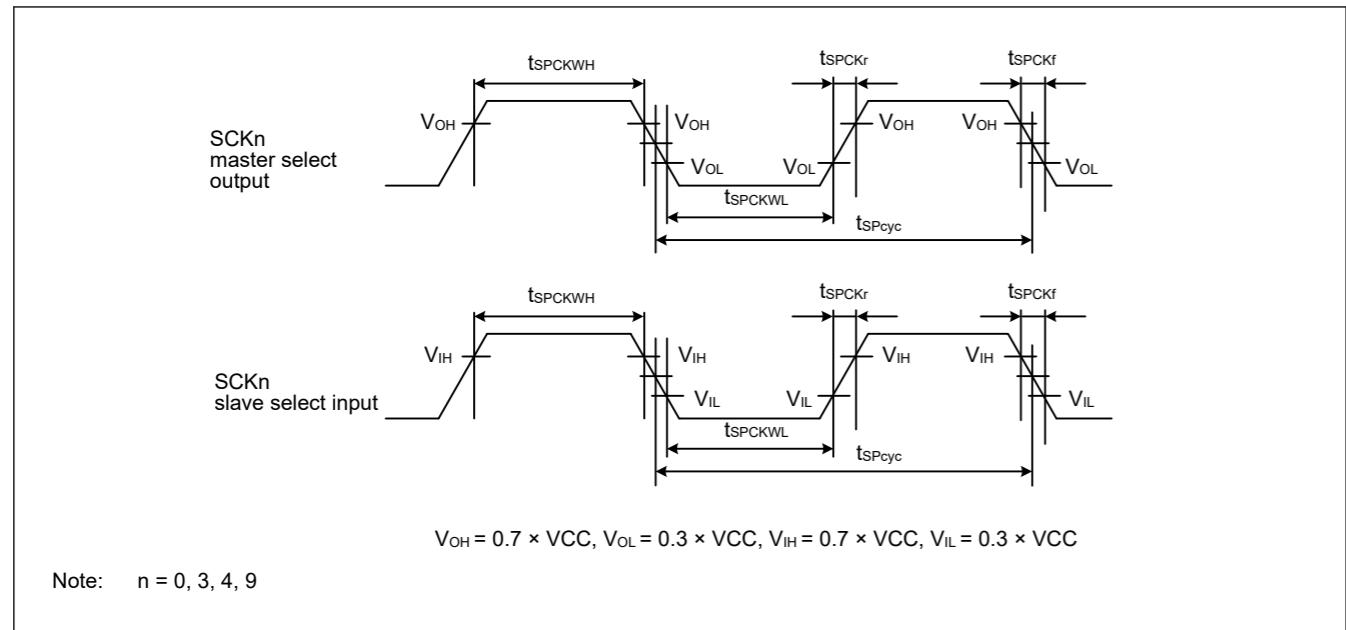


Figure 2.27 SCI simple SPI mode clock timing

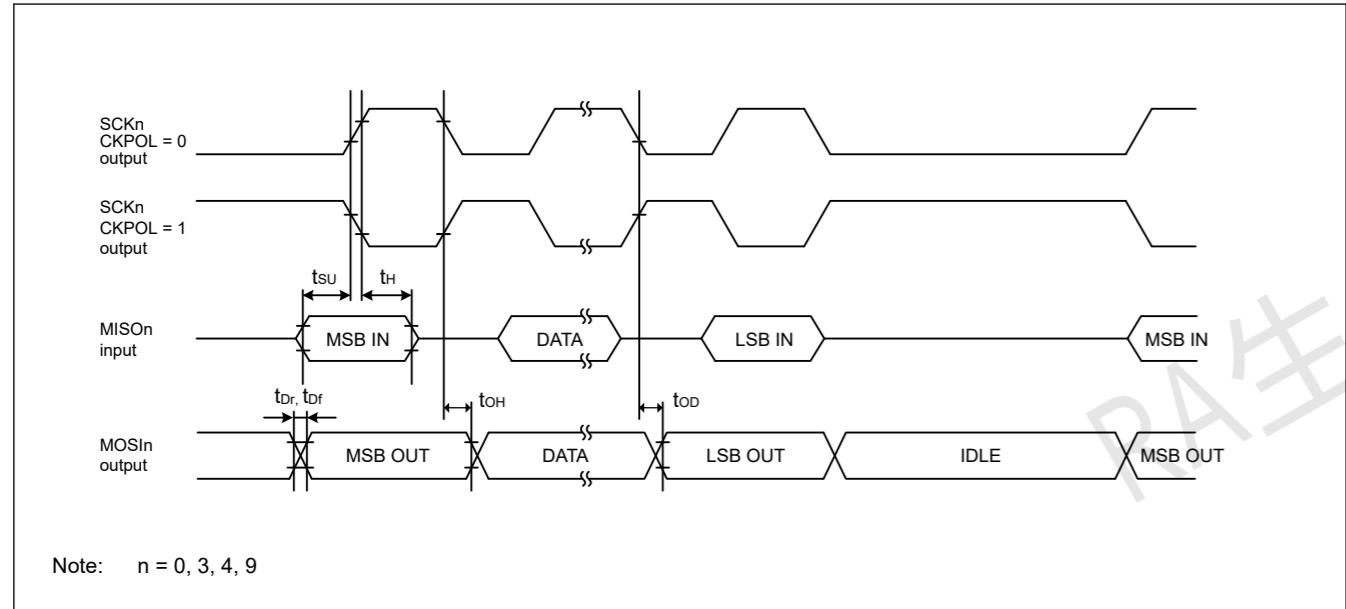


Figure 2.28 SCI simple SPI mode timing for master when CKPH = 1

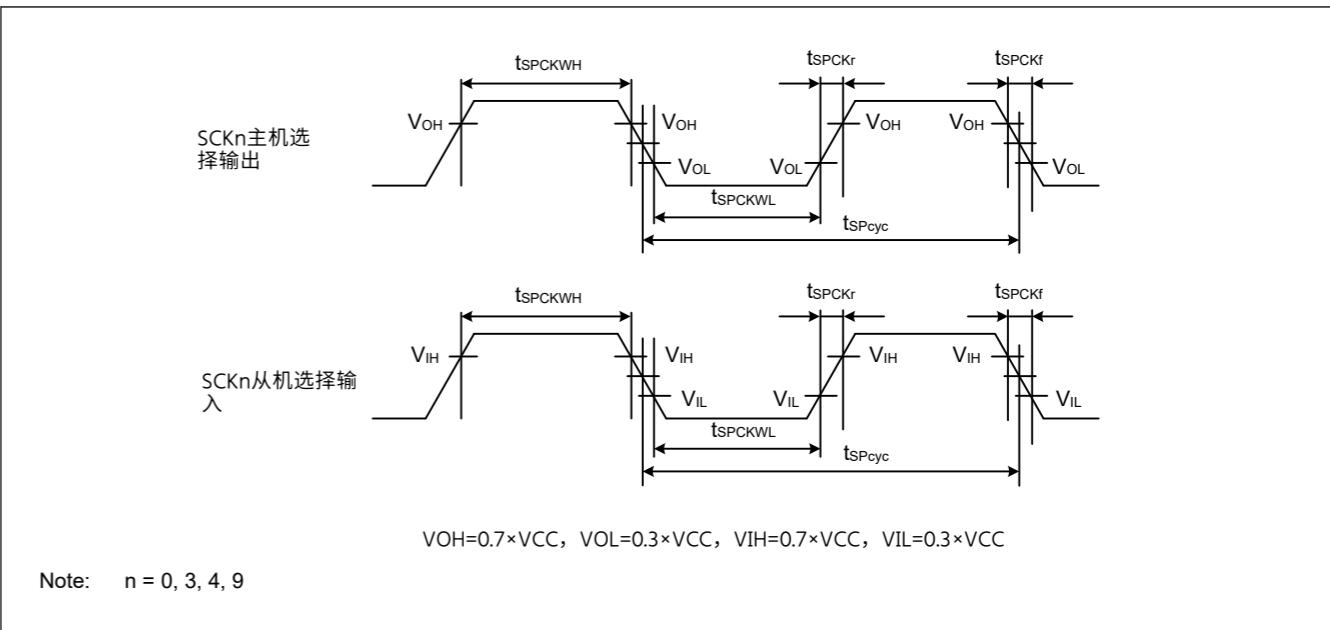


Figure 2.27 SCI简单SPI模式时钟时序

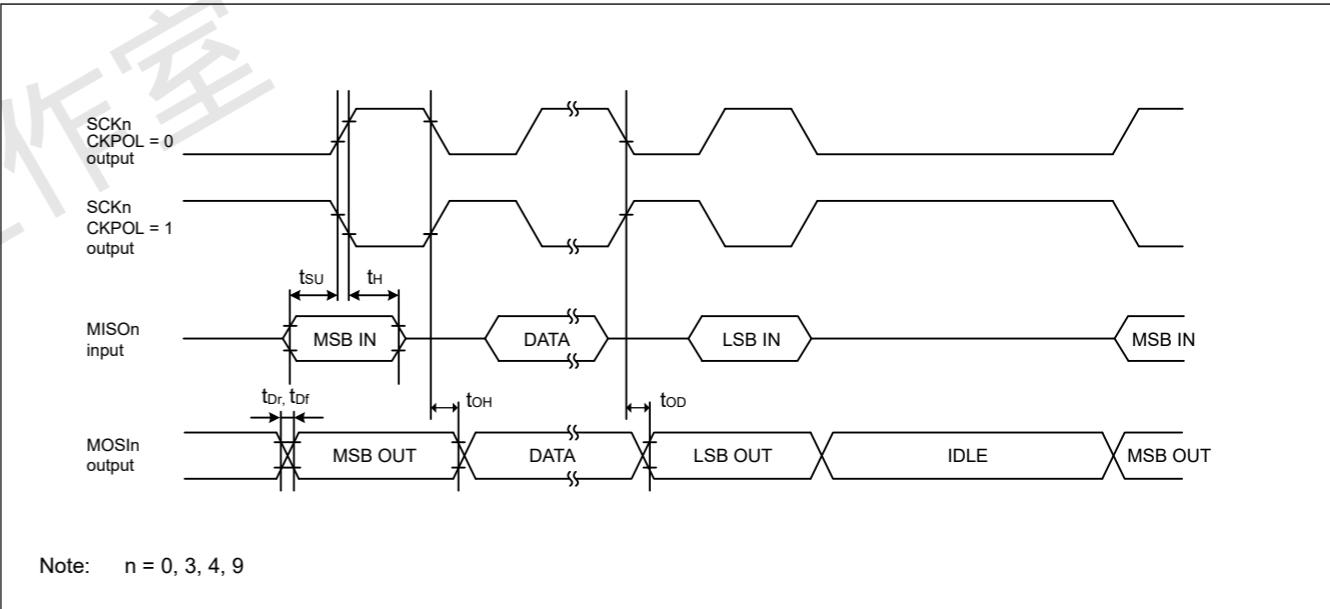


Figure 2.28 CKPH=1时主机的SCI简单SPI模式时序

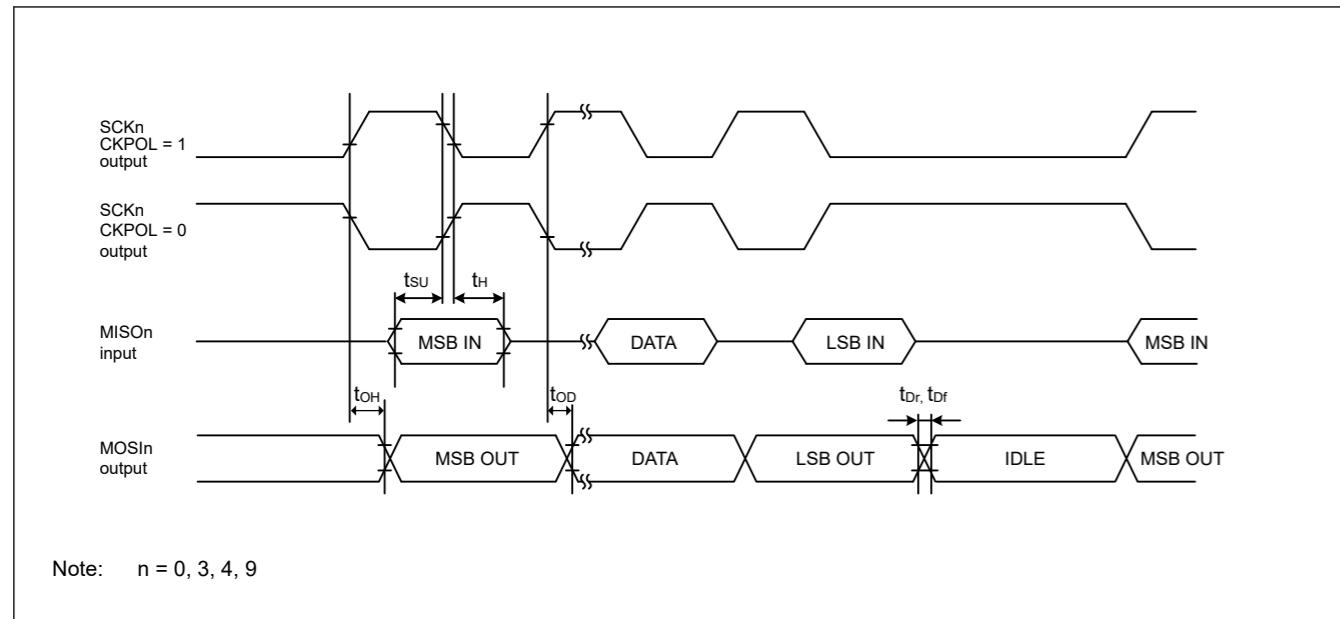


Figure 2.29 SCI simple SPI mode timing for master when CKPH = 0

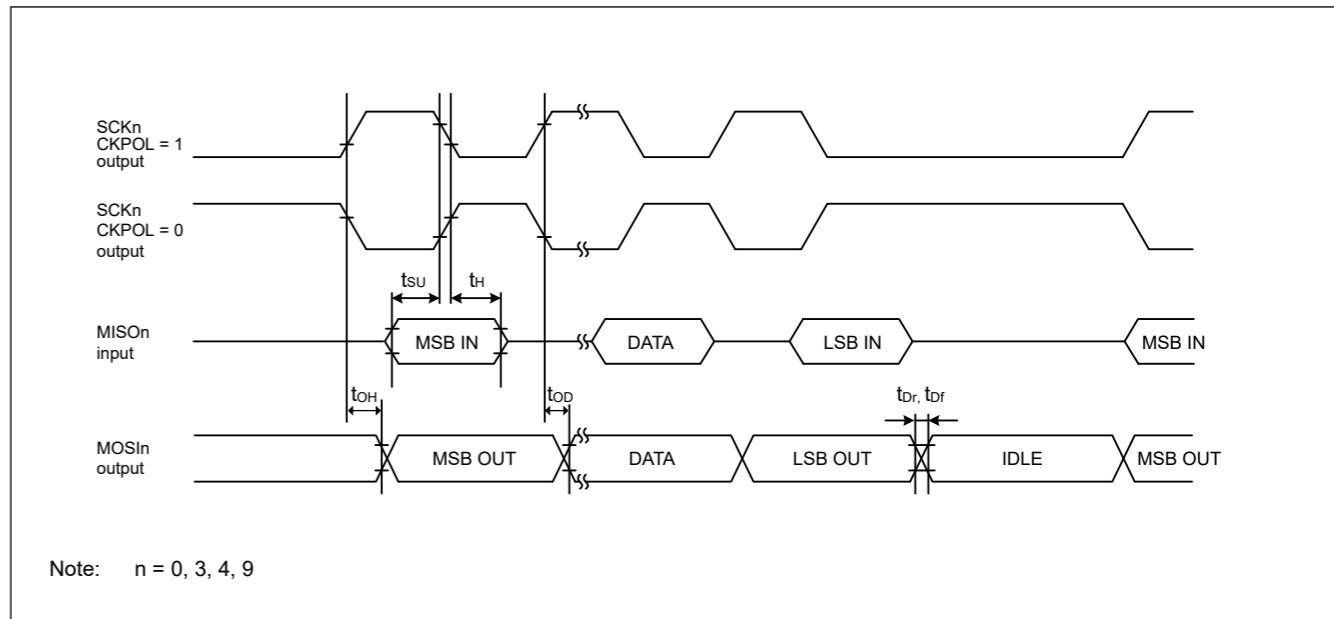


Figure 2.29 CKPH=0时主机的SCI简单SPI模式时序

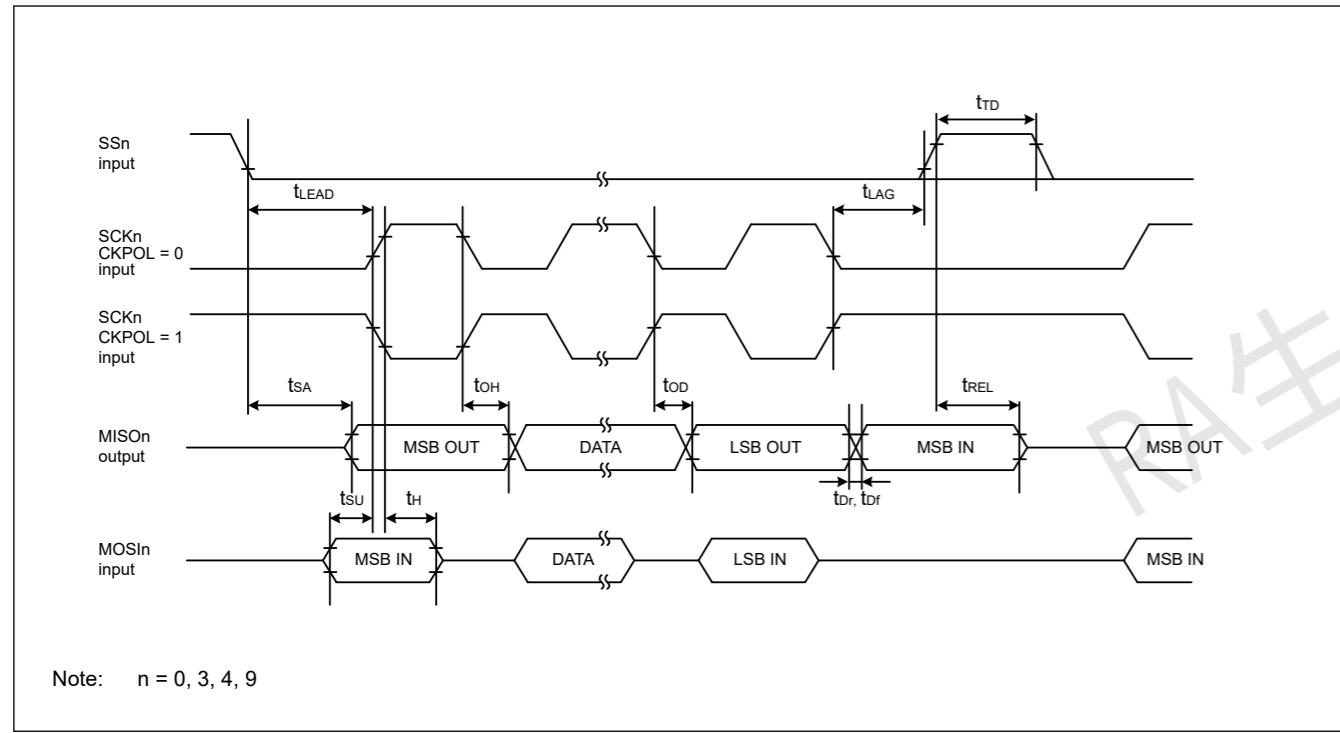


Figure 2.30 SCI simple SPI mode timing for slave when CKPH = 1

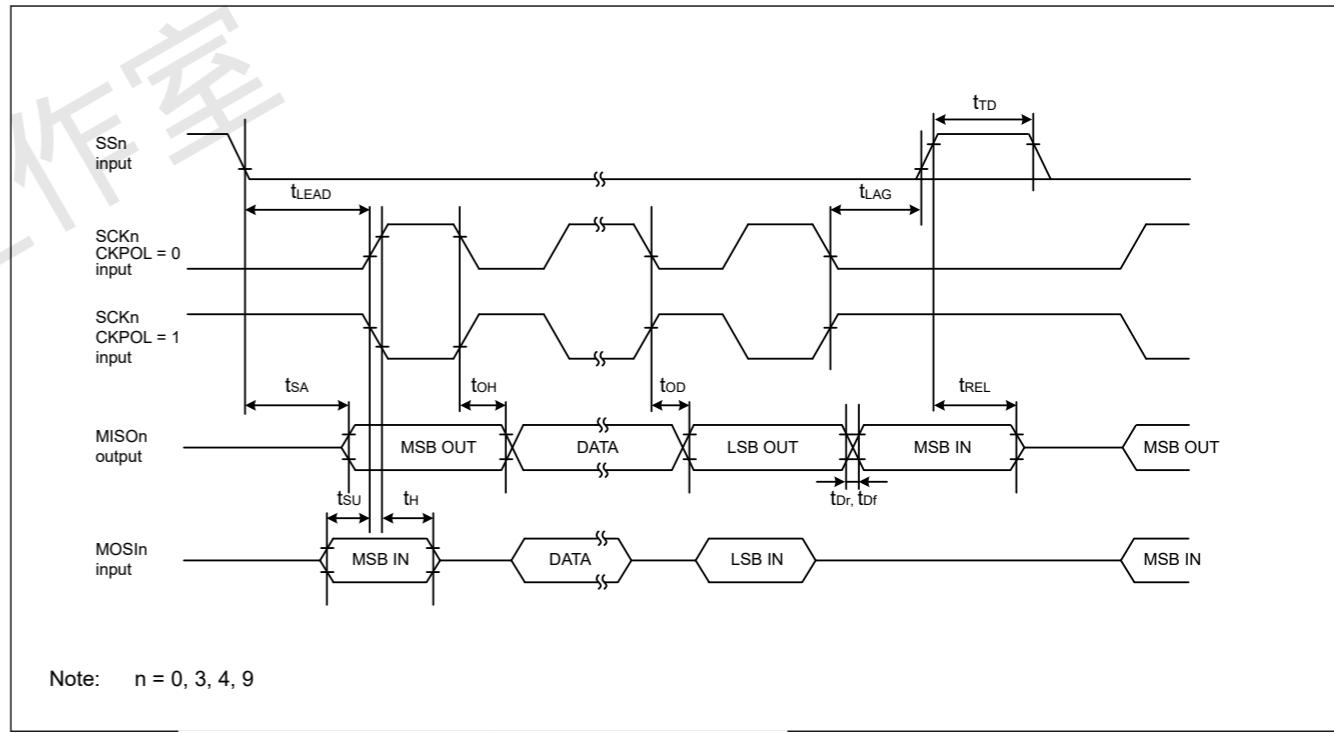


Figure 2.30 CKPH=1时从机的SCI简单SPI模式时序

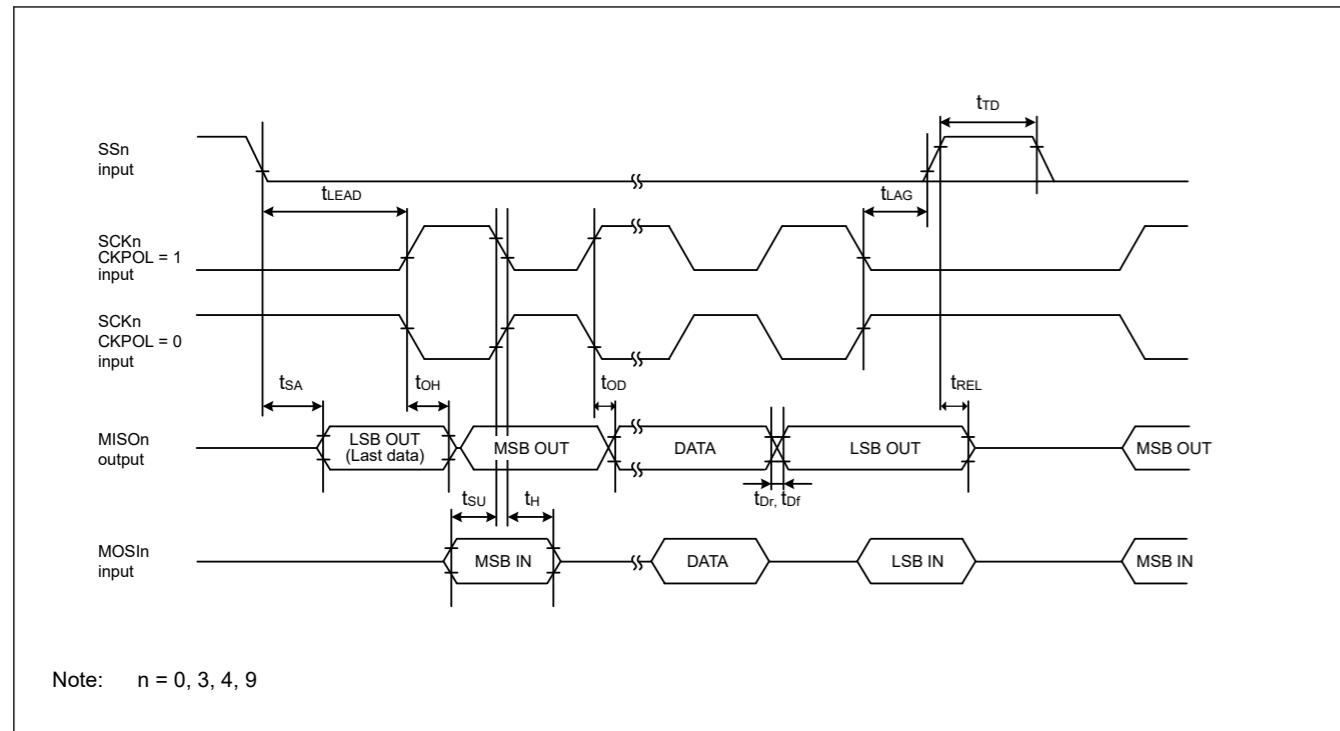


Figure 2.31 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|-------------------------------|------------------------------------|------------------------------|-----|-------------------------|-----------------|
| Simple IIC (Standard mode) | SDA input rise time | t _{Sr} | — | 1000 | ns |
| | SDA input fall time | t _{Sf} | — | 300 | ns |
| | SDA input spike pulse removal time | t _{SP} | 0 | 4 × t _{IICcyc} | ns |
| | Data input setup time | t _{SDAS} | 250 | — | ns |
| | Data input hold time | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 400 | pF |
| Simple IIC (Fast mode) | SDA input rise time | t _{Sr} | — | 300 | ns |
| | SDA input fall time | t _{Sf} | — | 300 | ns |
| | SDA input spike pulse removal time | t _{SP} | 0 | 4 × t _{IICcyc} | ns |
| | Data input setup time | t _{SDAS} | 100 | — | ns |
| | Data input hold time | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 400 | pF |

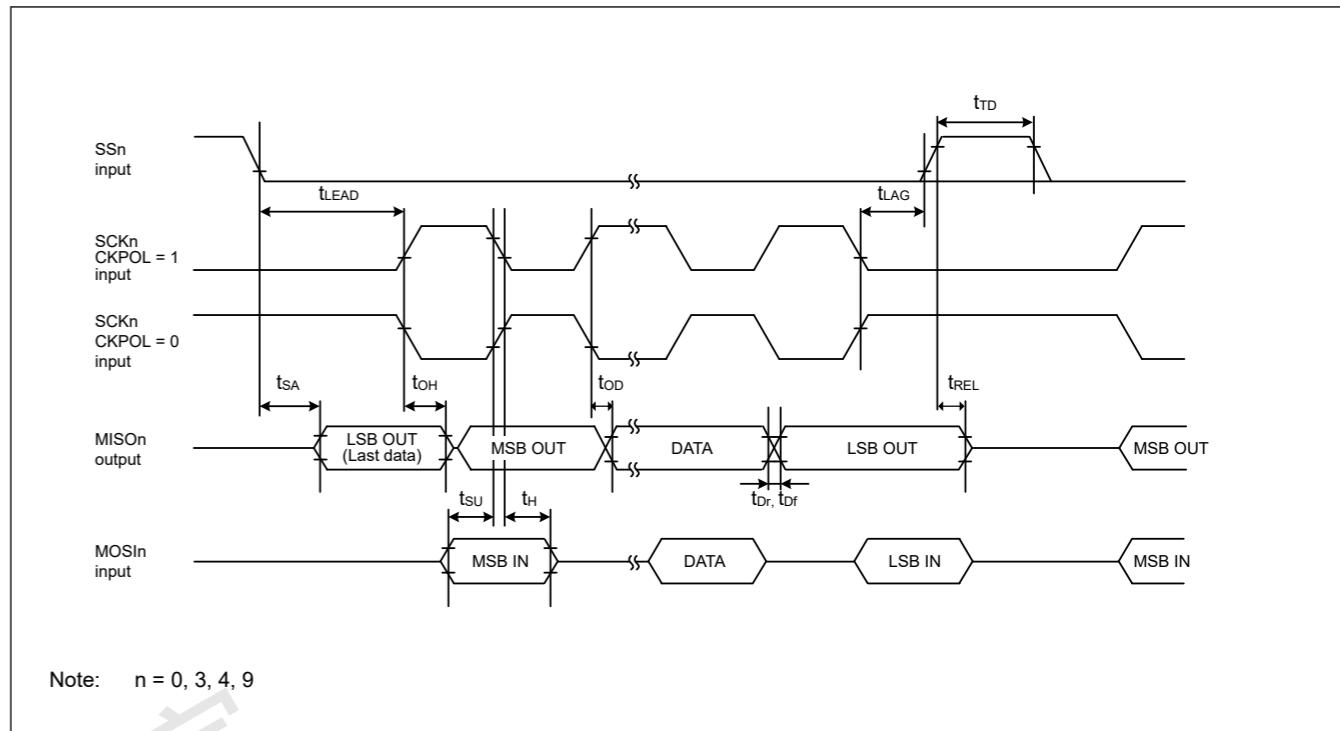
Note: t_{IICcyc}: IIC internal reference clock (IIC ϕ) cycle.Note 1. C_b indicates the total capacity of the bus line.

Figure 2.31 CKPH=0时从机的SCI简单SPI模式时序

Table 2.26 SCI时序 (3)

条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|-------------------------------|--------------------------|------------------------------|-----|-------------------------|------|
| Simple IIC (Standard mode) | SDA输入上升时间 | t _{Sr} | — | 1000 | ns |
| | SDA输入下降时间 | t _{Sf} | — | 300 | ns |
| | SDA输入尖峰脉冲去除时间 | t _{SP} | 0 | 4 × t _{IICcyc} | ns |
| | 数据输入建立时间 | t _{SDAS} | 250 | — | ns |
| | 数据输入保持时间 | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 400 | pF |
| Simple IIC (Fast mode) | SDA输入上升时间 | t _{Sr} | — | 300 | ns |
| | SDA输入下降时间 | t _{Sf} | — | 300 | ns |
| | SDA输入尖峰脉冲去除时间 | t _{SP} | 0 | 4 × t _{IICcyc} | ns |
| | 数据输入建立时间 | t _{SDAS} | 100 | — | ns |
| | 数据输入保持时间 | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 400 | pF |

Note: t_{IICcyc}: IIC内部参考时钟(IIC ϕ)周期。注1.C_b表示公交线路的总容量。

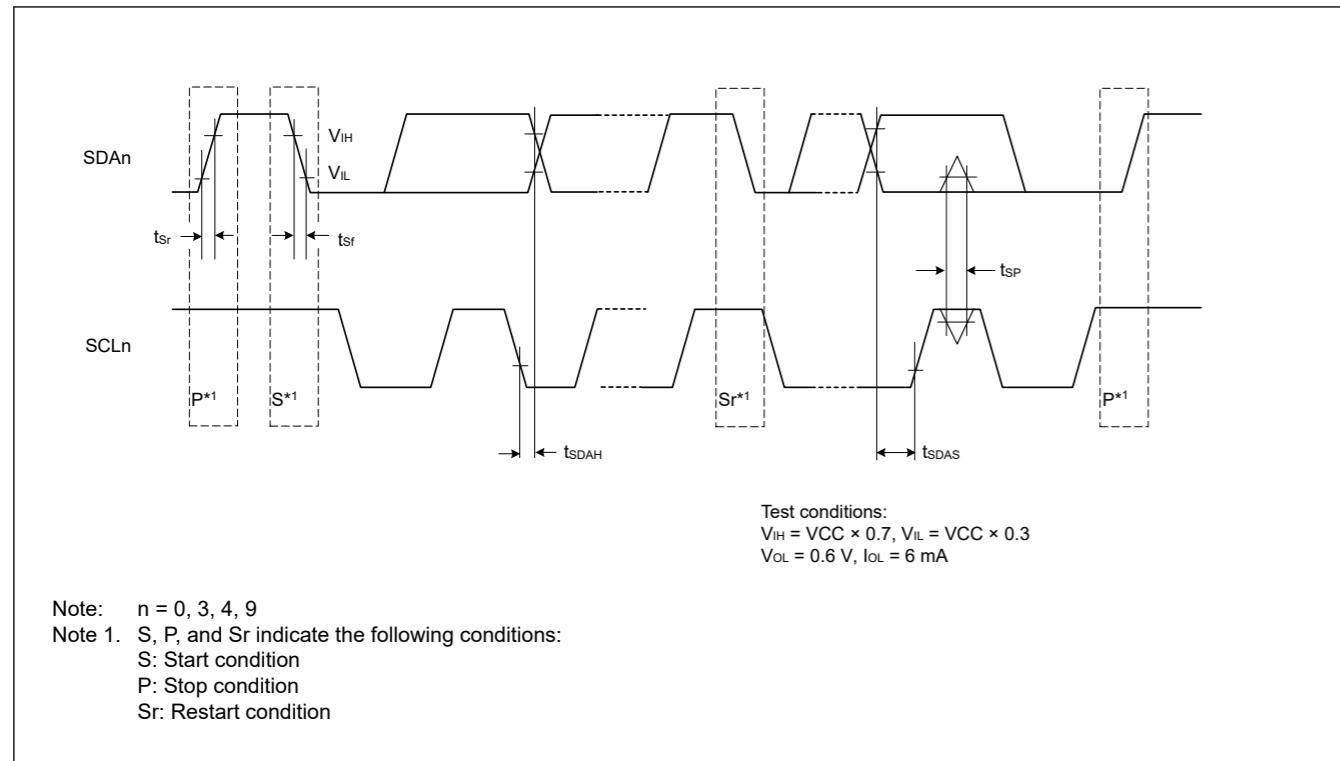


Figure 2.32 SCI simple IIC mode timing

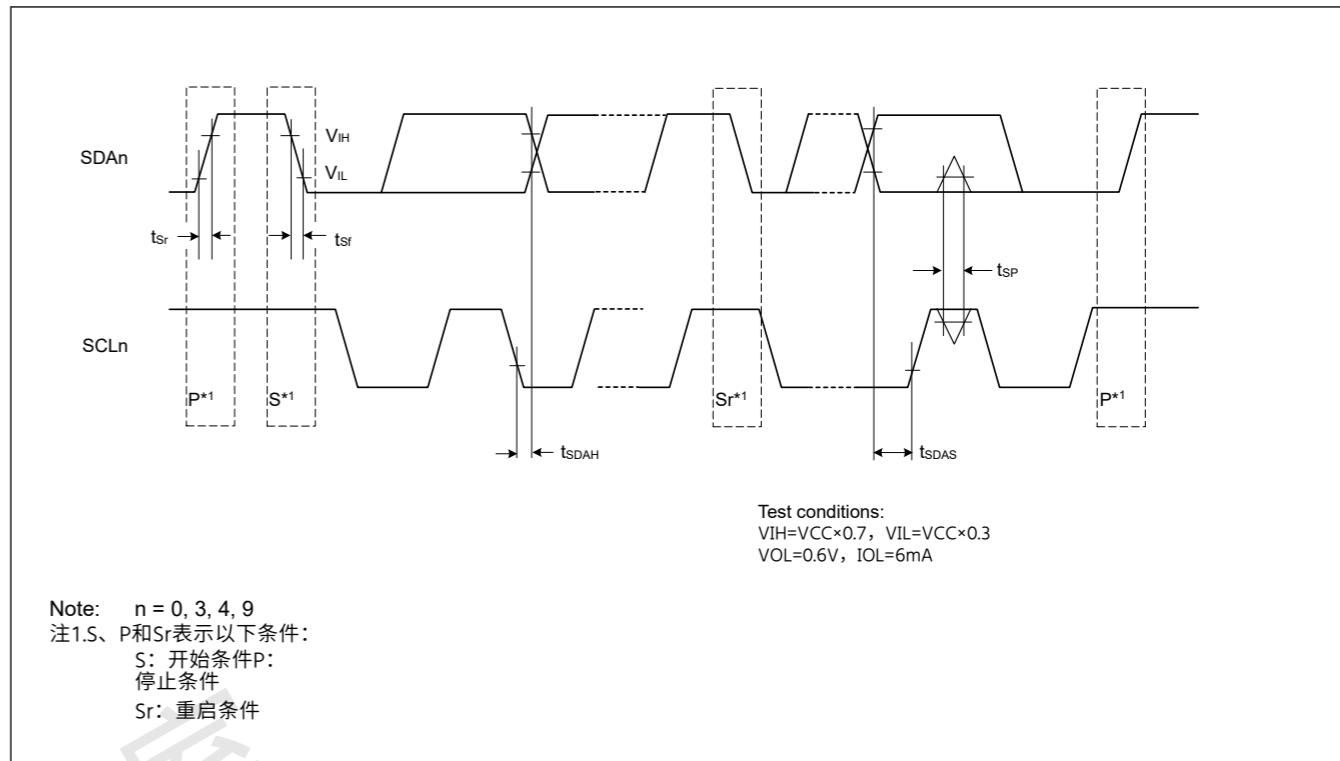


Figure 2.32 SCI简单IIC模式时序

2.3.9 SPI Timing

Table 2.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|----------------------------------|---|---|---|---|------|-----------------------------|
| SPI | RSPCK clock cycle | Master | t _{SPcyc} | 2 | 4096 | Figure 2.33 |
| | | Slave | | 4 | 4096 | |
| RSPCK clock high pulse width | Master | t _{SPCKWH} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | Figure 2.33 |
| | | | | 0.4 | 0.6 | |
| RSPCK clock low pulse width | Master | t _{SPCKWL} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | Figure 2.33 |
| | | | | 0.4 | 0.6 | |
| RSPCK clock rise and fall time | Master | t _{SPCKr} , t _{SPCKf} | — | 5 | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | — | 1 | μs | |
| Data input setup time | Master | t _{SU} | 4 | — | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | 5 | — | ns | |
| Data input hold time | Master (PCLKA division ratio set to 1/2) | t _{HF} | 0 | — | ns | Figure 2.34 to Figure 2.39 |
| | Master (PCLKA division ratio set to a value other than 1/2) | t _H | t _{SPcyc} | — | ns | |
| | Slave | t _H | 20 | — | ns | |
| SSL setup time | Master | t _{LEAD} | $N \times t_{SPcyc} - 10^{*1}$ | $N \times t_{SPcyc} + 100^{*1}$ | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | $4 \times t_{SPcyc}$ | — | ns | |
| SSL hold time | Master | t _{LAG} | $N \times t_{SPcyc} - 10^{*2}$ | $N \times t_{SPcyc} + 100^{*2}$ | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | $4 \times t_{SPcyc}$ | — | ns | |
| Data output delay | Master | t _{OD1} | — | 6.3 | ns | Figure 2.34 to Figure 2.39 |
| | | | — | 6.3 | | |
| | Slave | t _{OD} | — | 20 | | |
| Data output hold time | Master | t _{OH} | 0 | — | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | 0 | — | | |
| Successive transmission delay | Master | t _{TD} | $t_{SPcyc} + 2 \times t_{SPcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{SPcyc}$ | ns | Figure 2.34 to Figure 2.39 |
| | Slave | | $4 \times t_{SPcyc}$ | — | | |
| MOSI and MISO rise and fall time | Output | t _{DR} , t _{DF} | — | 5 | ns | Figure 2.34 to Figure 2.39 |
| | Input | | — | 1 | μs | |
| SSL rise and fall time | Output | t _{SSLr} , t _{SSLf} | — | 5 | ns | Figure 2.34 to Figure 2.39 |
| | Input | | — | 1 | μs | |
| Slave access time | | t _{SA} | — | 25 | ns | Figure 2.38 and Figure 2.39 |
| Slave output release time | | t _{REL} | — | 25 | | |

2.3.9 SPI时序

Table 2.27 SPI时序

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | | Symbol | Min | Max | Unit | 测试条件 | | |
|------------------|------------------------|---|---|---|------|-------------|-------------------|--|
| SPI | RSPCK时钟周期 | Master | t _{SPcyc} | 2 | 4096 | Figure 2.33 | | |
| | | Slave | | 4 | 4096 | | | |
| RSPCK时钟高脉冲宽度 | Master | t _{SPCKWH} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | Figure 2.33 | | |
| | | | | 0.4 | 0.6 | | | |
| RSPCK时钟低脉冲宽度 | Master | t _{SPCKWL} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | Figure 2.33 | | |
| | | | | 0.4 | 0.6 | | | |
| RSPCK时钟上升和下降时间 | Master | t _{SPCKr} , t _{SPCKf} | — | 5 | ns | 图2.34至图2.39 | | |
| | | | — | 1 | μs | | | |
| 数据输入建立时间 | Master | t _{SU} | 4 | — | ns | 图2.34至图2.39 | | |
| | Slave | | 5 | — | ns | | | |
| 数据输入保持时间 | 主控 (PCLKA分频比设置为12) | t _{HF} | 0 | — | ns | 图2.34至图2.39 | | |
| | 主控 (PCLKA分频比设置为12以外的值) | t _H | t _{SPcyc} | — | ns | | | |
| | Slave | t _H | 20 | — | ns | | | |
| SSL设置时间 | Master | t _{LEAD} | $N \times t_{SPcyc} - 10^{*1}$ | $N \times t_{SPcyc} + 100^{*1}$ | ns | 图2.34至图2.39 | | |
| | Slave | | $4 \times t_{SPcyc}$ | — | ns | | | |
| SSL保持时间 | Master | t _{LAG} | $N \times t_{SPcyc} - 10^{*2}$ | $N \times t_{SPcyc} + 100^{*2}$ | ns | 图2.34至图2.39 | | |
| | Slave | | $4 \times t_{SPcyc}$ | — | ns | | | |
| 数据输出延迟 | Master | t _{OD1} | — | 6.3 | ns | 图2.34至图2.39 | | |
| | | | — | 6.3 | | | | |
| | Slave | t _{OD} | — | 20 | | | | |
| 数据输出保持时间 | Master | t _{OH} | 0 | — | ns | 图2.34至图2.39 | | |
| | Slave | | 0 | — | | | | |
| 连续传输延迟 | Master | t _{TD} | $t_{SPcyc} + 2 \times t_{SPcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{SPcyc}$ | ns | 图2.34至图2.39 | | |
| | Slave | | $4 \times t_{SPcyc}$ | — | | | | |
| MOSI和MISO上升和下降时间 | Output | t _{DR} , t _{DF} | — | 5 | ns | 图2.34至图2.39 | | |
| | Input | | — | 1 | μs | | | |
| SSL上升和下降时间 | Output | t _{SSLr} , t _{SSLf} | — | 5 | ns | 图2.34至图2.39 | | |
| | Input | | — | 1 | μs | | | |
| 从站访问时间 | | | t _{SA} | — | 25 | ns | 图2.38和Figure 2.39 | |
| 从机输出释放时间 | | | t _{REL} | — | 25 | | | |

Note: t_{Pcyc} : PCLKA cycle.

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.

Note 1. N is set to an integer from 1 to 8 by the SPCKD register.

Note 2. N is set to an integer from 1 to 8 by the SSLND register.

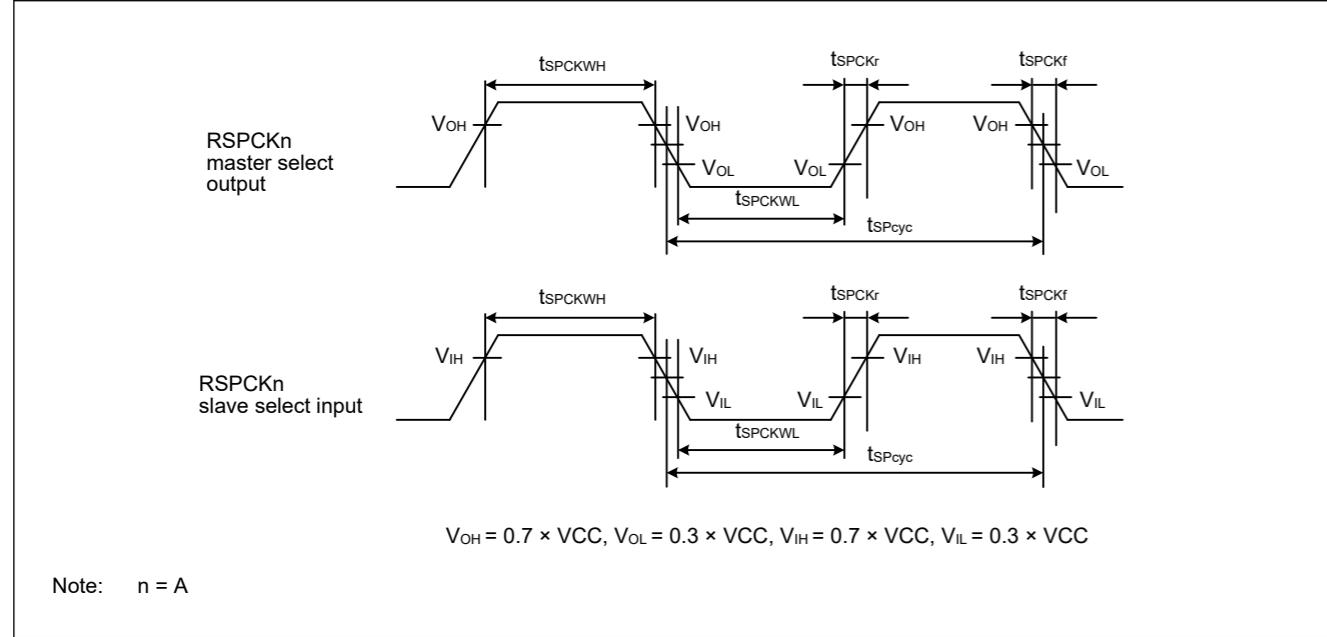


Figure 2.33 SPI clock timing

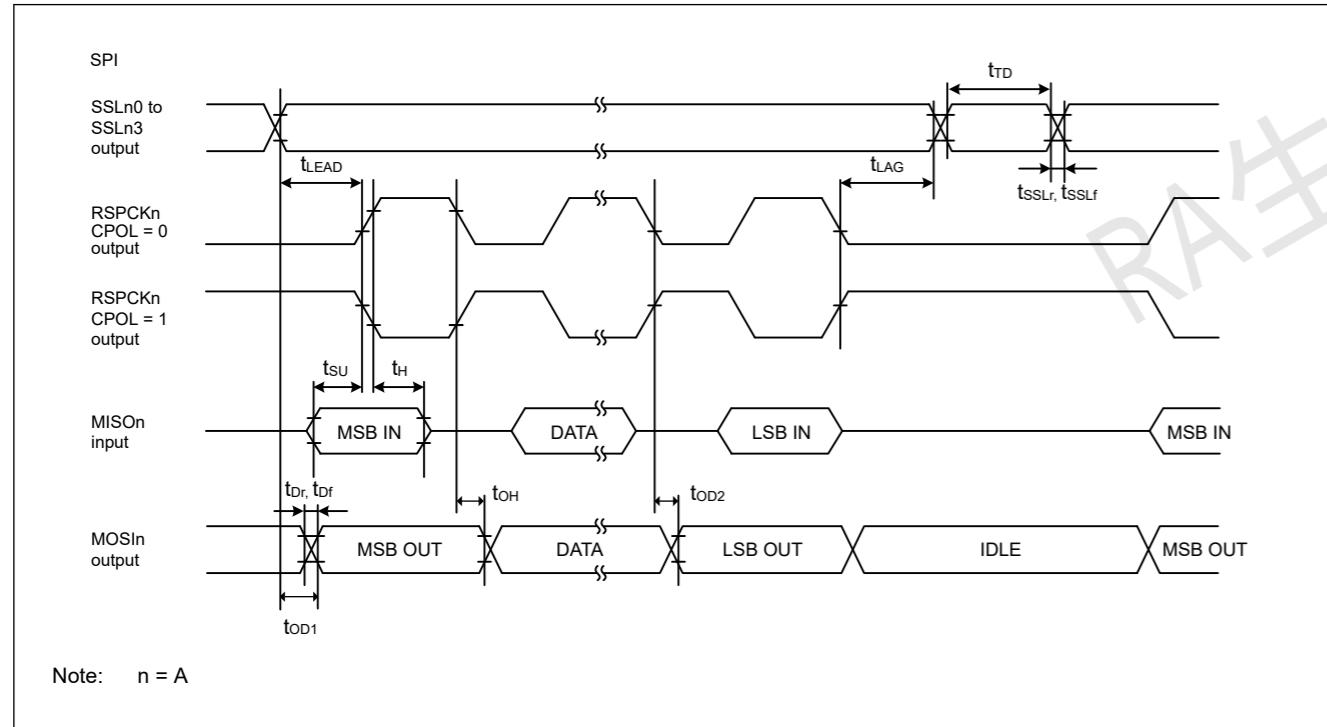


Figure 2.34 SPI timing for master when CPHA = 0

Note: t_{Pcyc} : PCLKA cycle.

Note: 必须使用名称后附有字母的引脚，例如“_A”、“_B”，以表示组成员身份。对于SPI接口，测量每组的电气特性的交流部分。

注1.N由SPCKD寄存器设置为1到8的整数。注2.N由SSLND寄存器设置为1到8的整数。

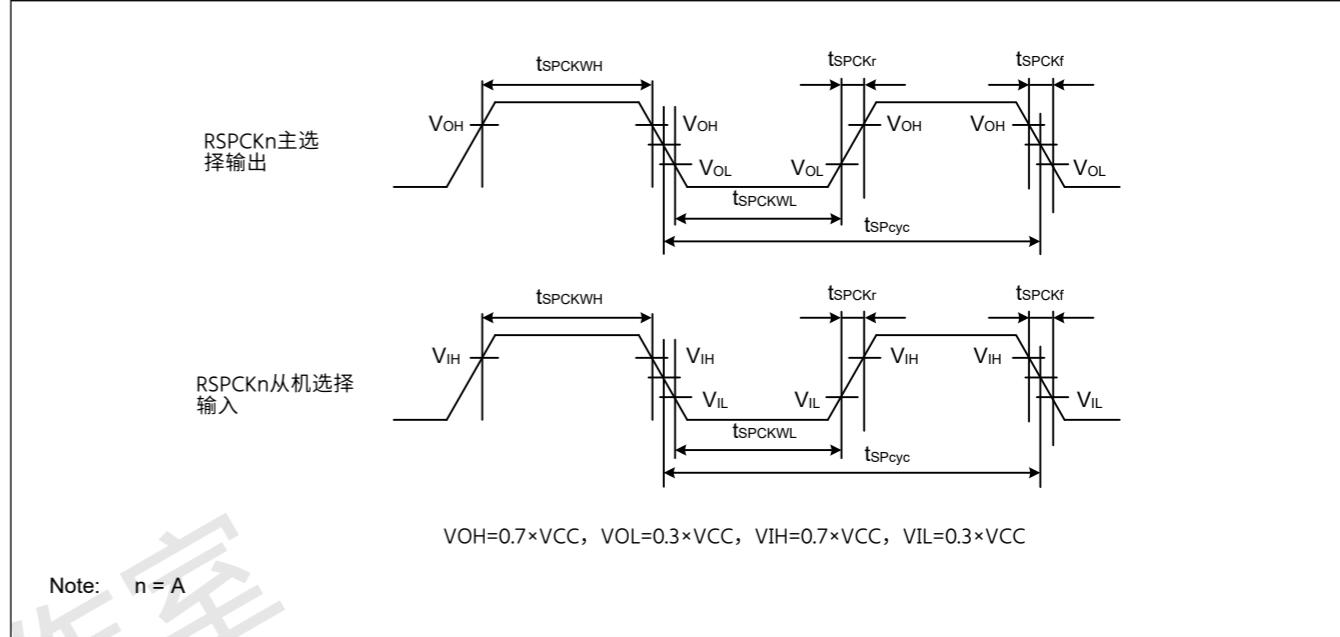


Figure 2.33 SPI时钟时序

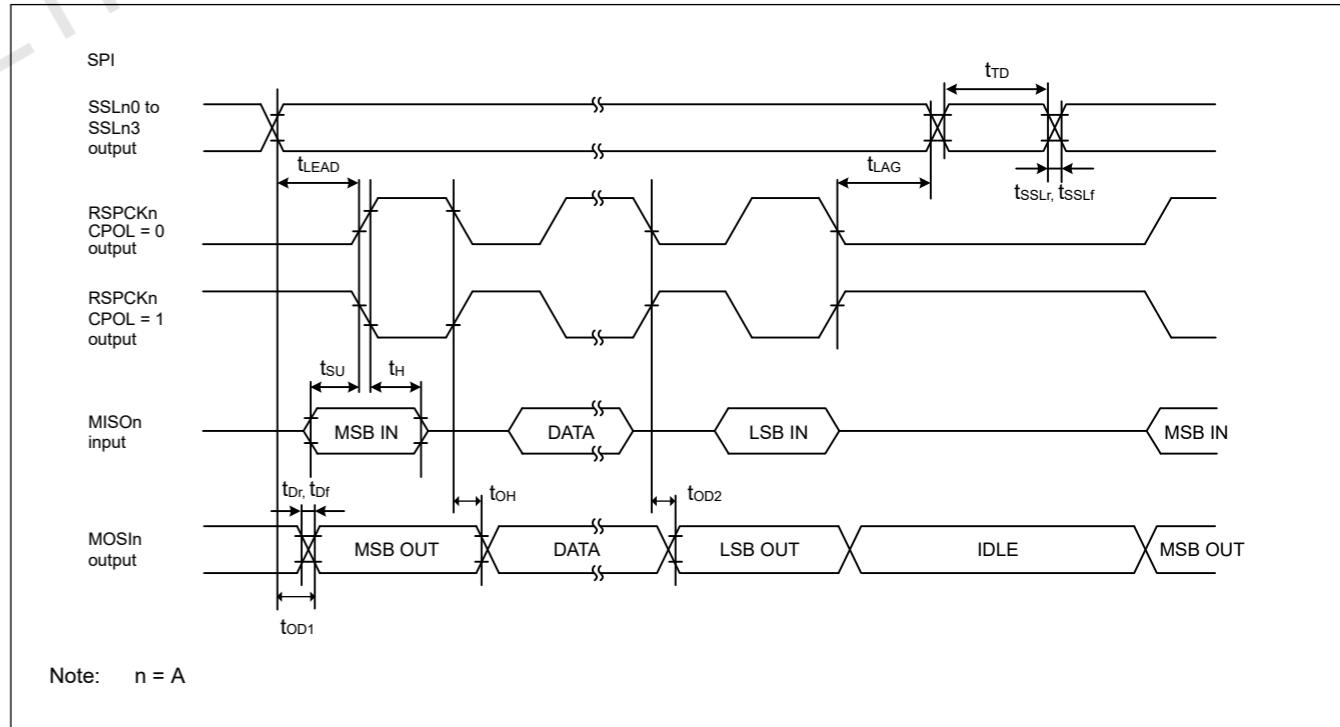


Figure 2.34 CPHA=0时主机的SPI时序

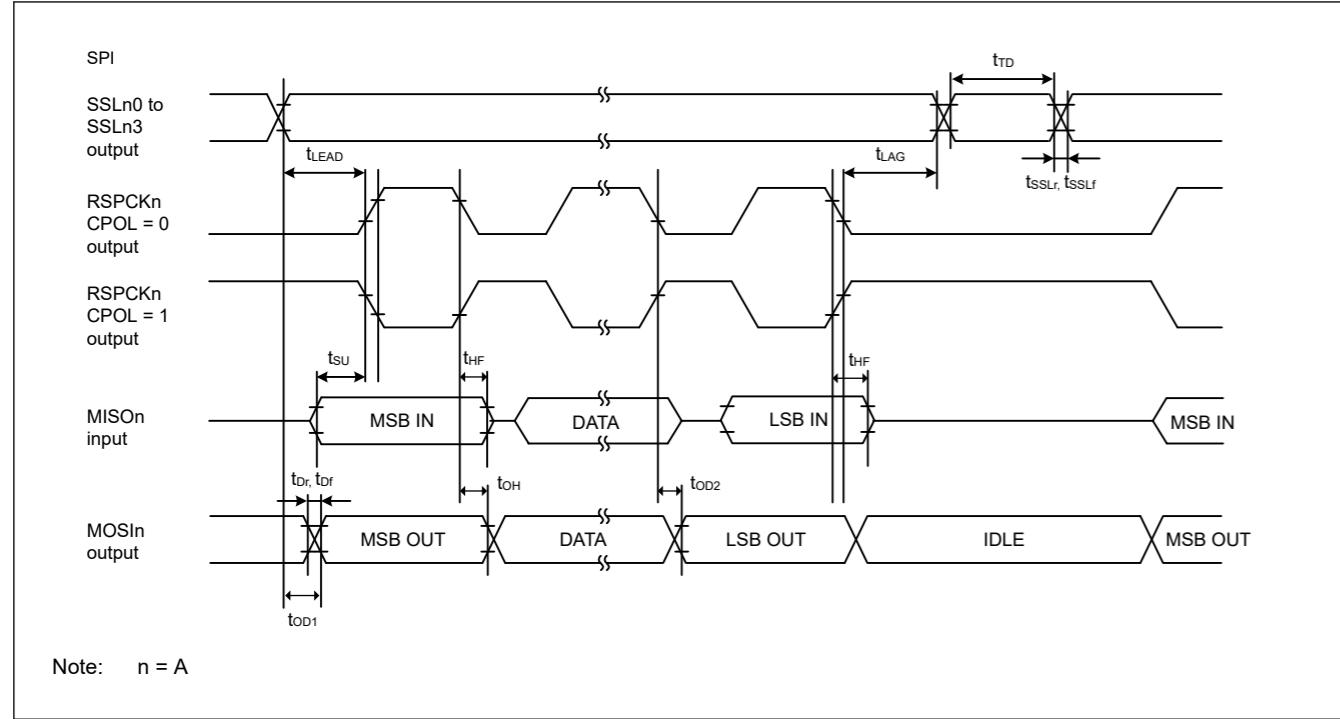


Figure 2.35 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

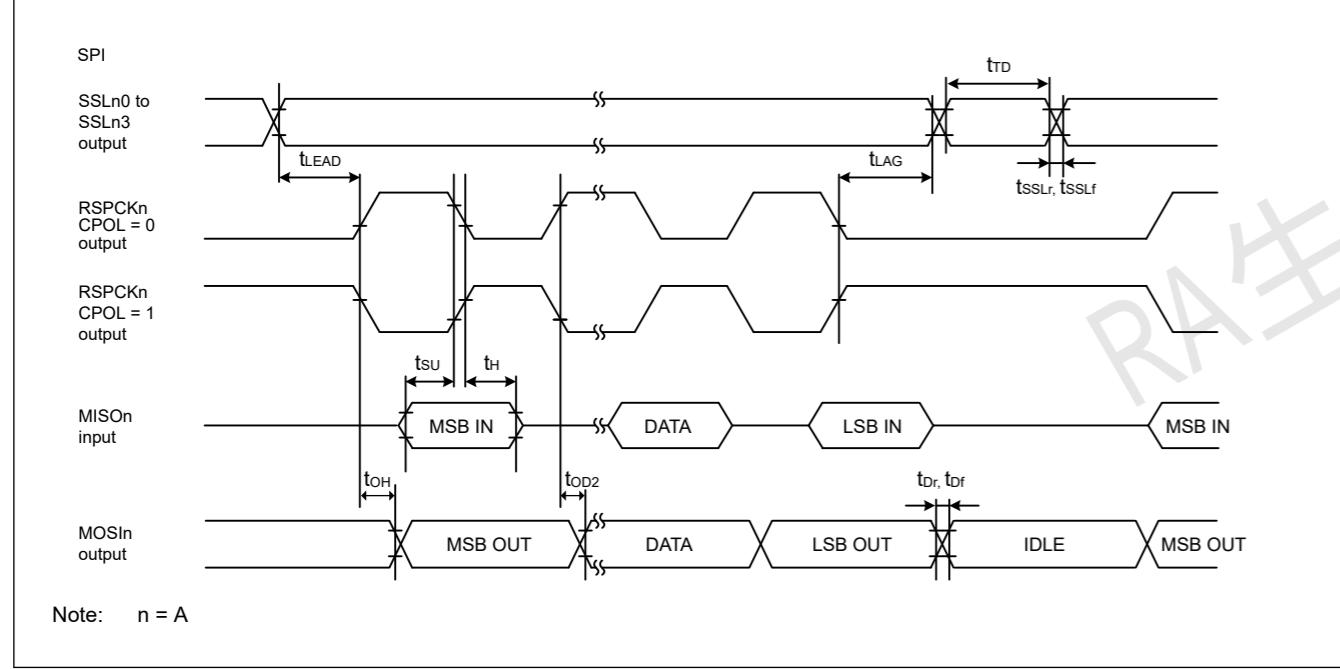


Figure 2.36 SPI timing for master when CPHA = 1

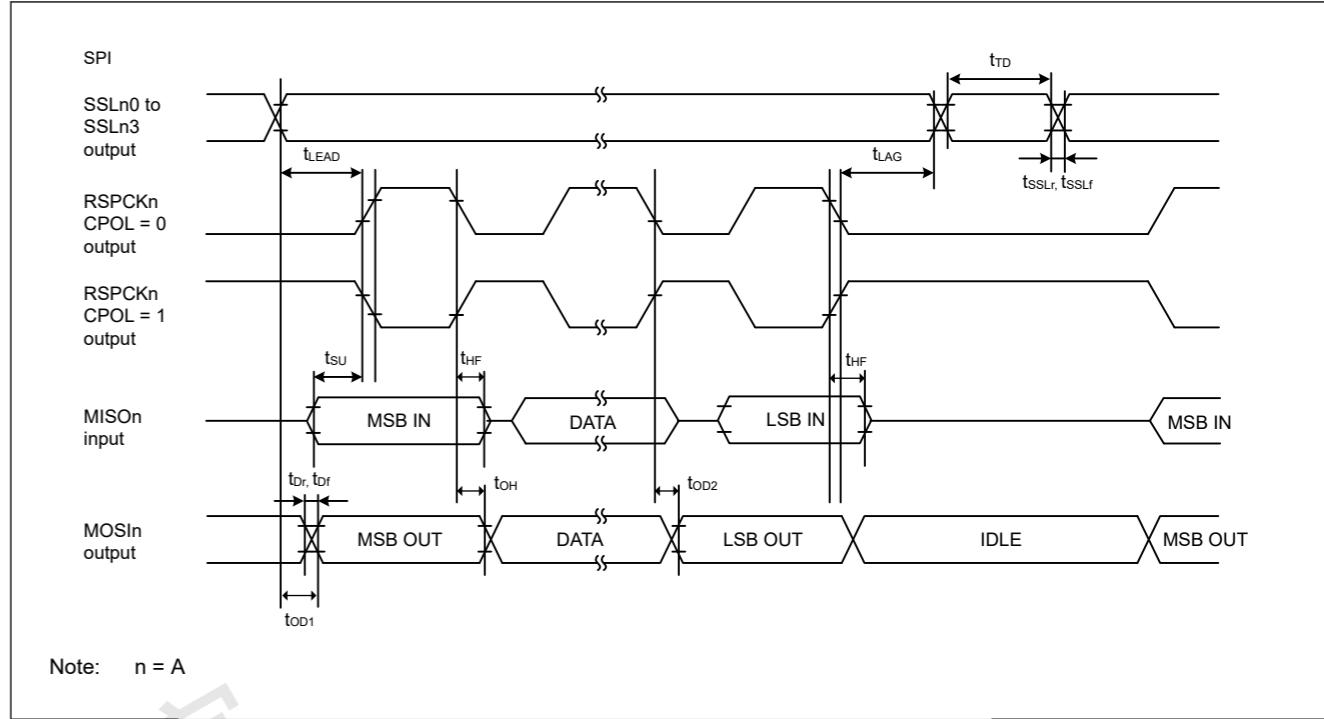


Figure 2.35 当CPHA=0且比特率设置为PCLKA2时主设备的SPI时序

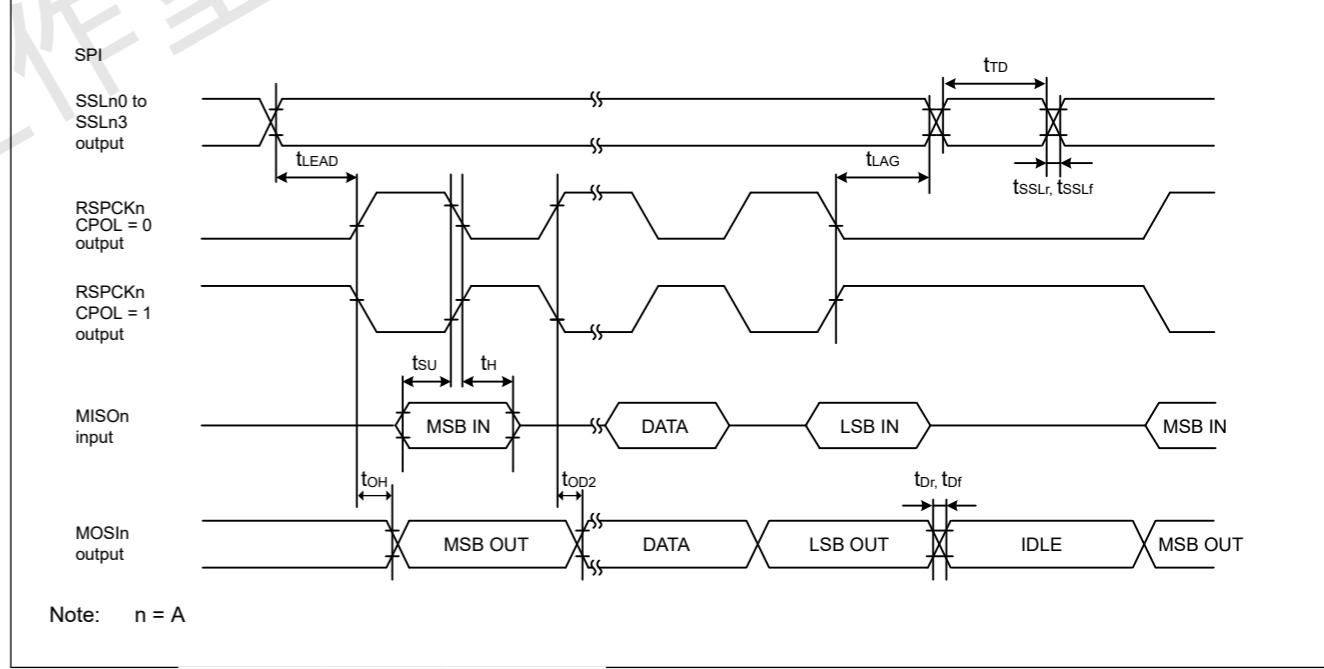


Figure 2.36 CPHA=1时主机的SPI时序

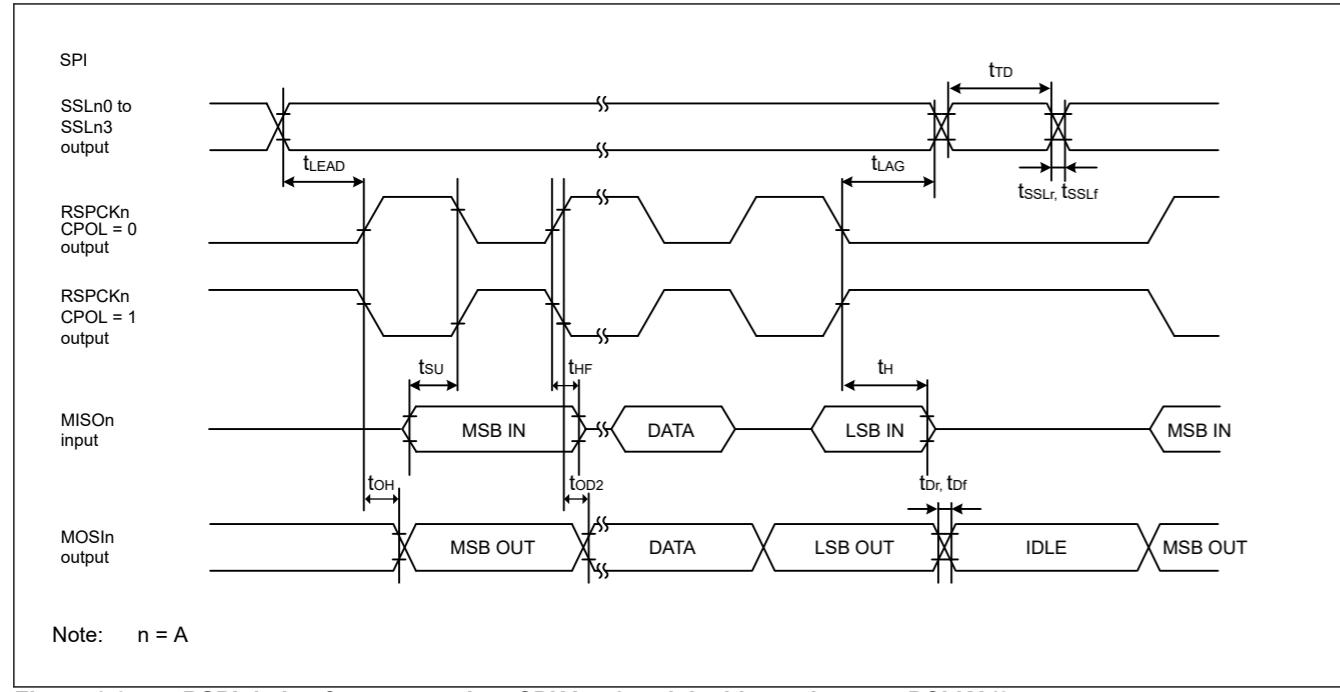


Figure 2.37 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

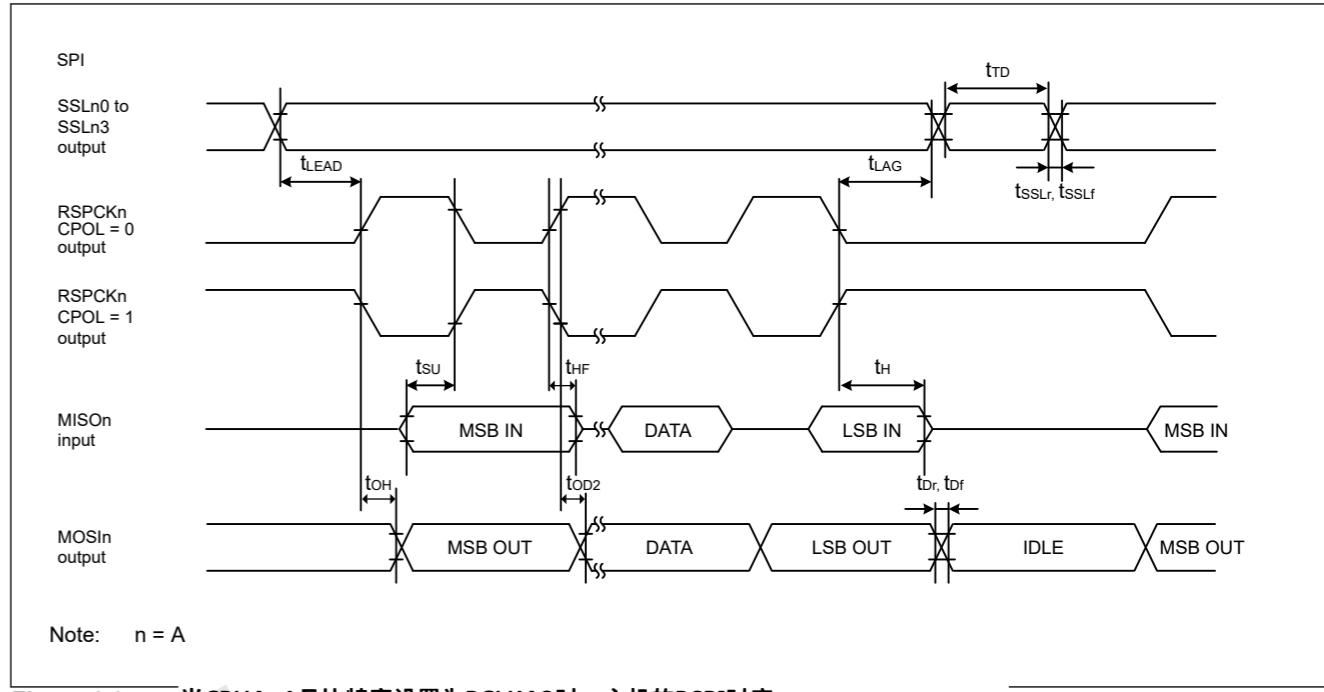


Figure 2.37 当CPHA=1且比特率设置为PCLKA2时，主机的RSPI时序

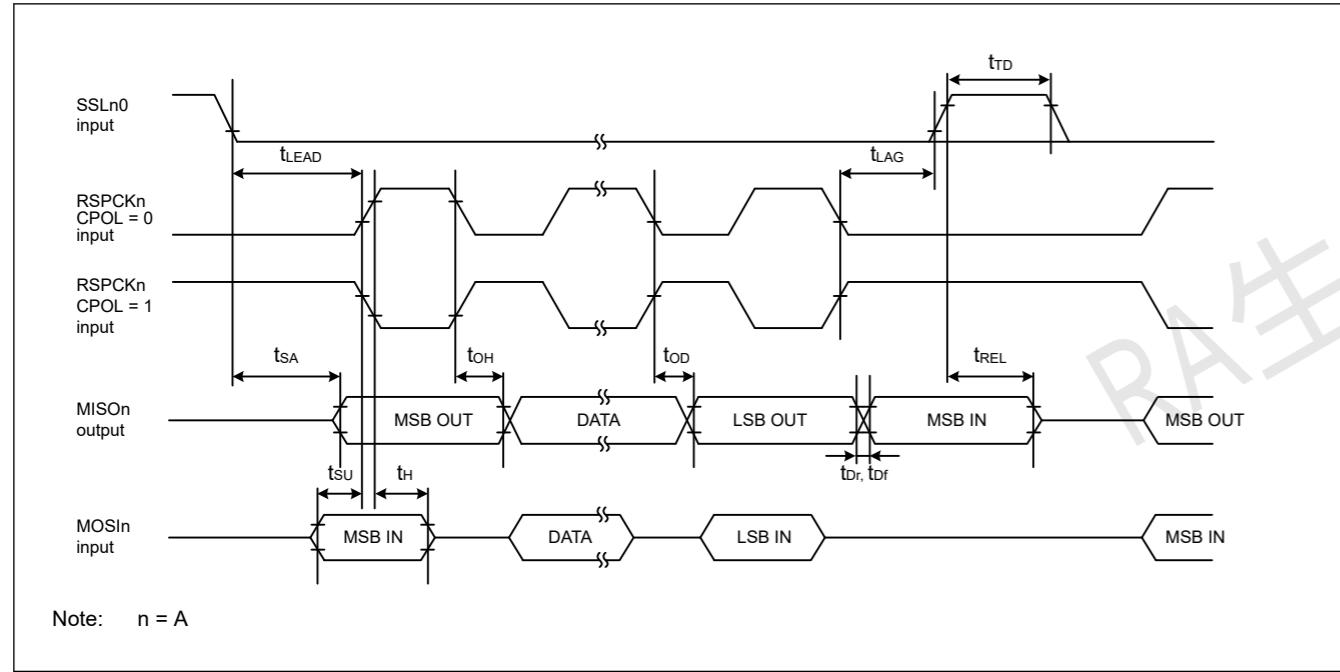


Figure 2.38 SPI timing for slave when CPHA = 0

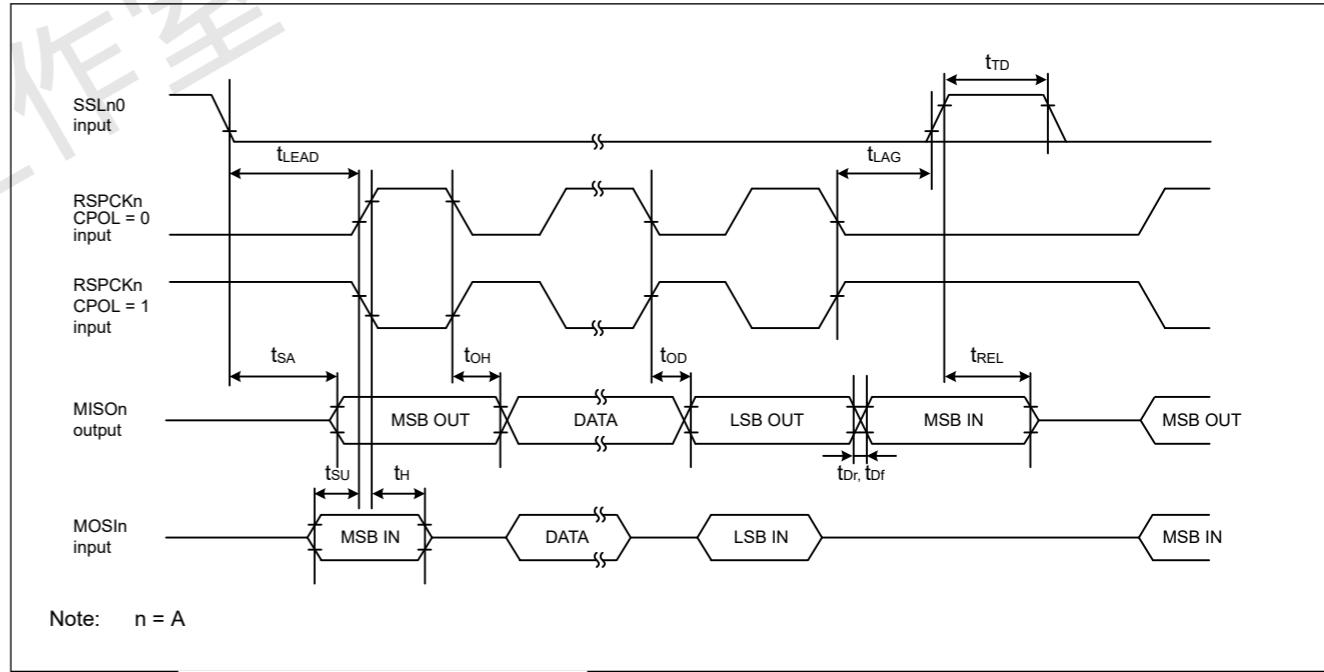


Figure 2.38 CPHA=0时从机的SPI时序

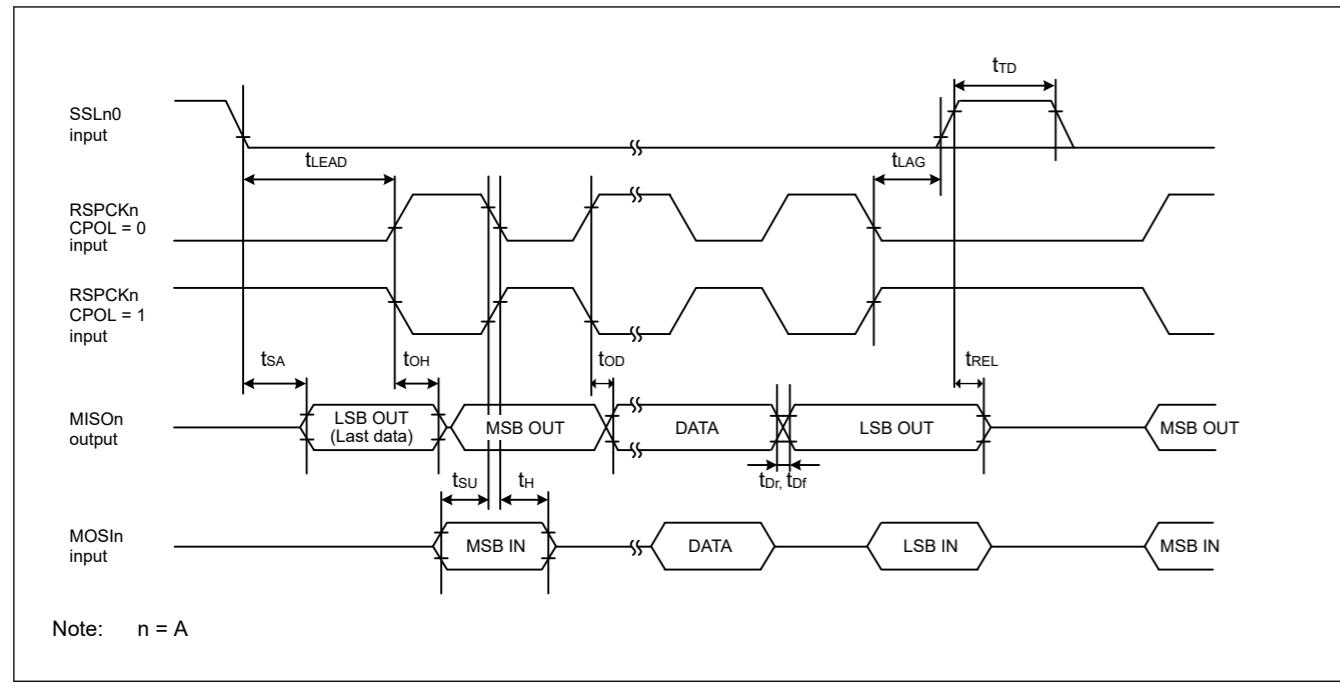


Figure 2.39 SPI timing for slave when CPHA = 1

2.3.10 QSPI Timing

Table 2.28 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|-----------|-------------------------------|--------------------|--|--|--------------------|
| QSPI | QSPCK clock cycle | t _{QScyc} | 2 | 48 | t _{Pcyc} |
| | QSPCK clock high pulse width | t _{QSWH} | t _{QScyc} × 0.4 | — | ns |
| | QSPCK clock low pulse width | t _{QSWL} | t _{QScyc} × 0.4 | — | ns |
| | Data input setup time | t _{Su} | 10 | — | ns |
| | Data input hold time | t _{IH} | 0 | — | ns |
| | QSSL setup time | t _{LEAD} | (N + 0.5) × t _{QScyc} - 5 ^{*1} | (N + 0.5) × t _{QScyc} + 100 ^{*1} | ns |
| | QSSL hold time | t _{LAG} | (N + 0.5) × t _{QScyc} - 5 ^{*2} | (N + 0.5) × t _{QScyc} + 100 ^{*2} | ns |
| | Data output delay | t _{OD} | — | 4 | ns |
| | Data output hold time | t _{OH} | -3.3 | — | ns |
| | Successive transmission delay | t _{TD} | 1 | 16 | t _{QScyc} |

Note: t_{Pcyc}: PCLKA cycle.

Note 1. N is set to 0 or 1 in SFMSLD.

Note 2. N is set to 0 or 1 in SFMSHD.

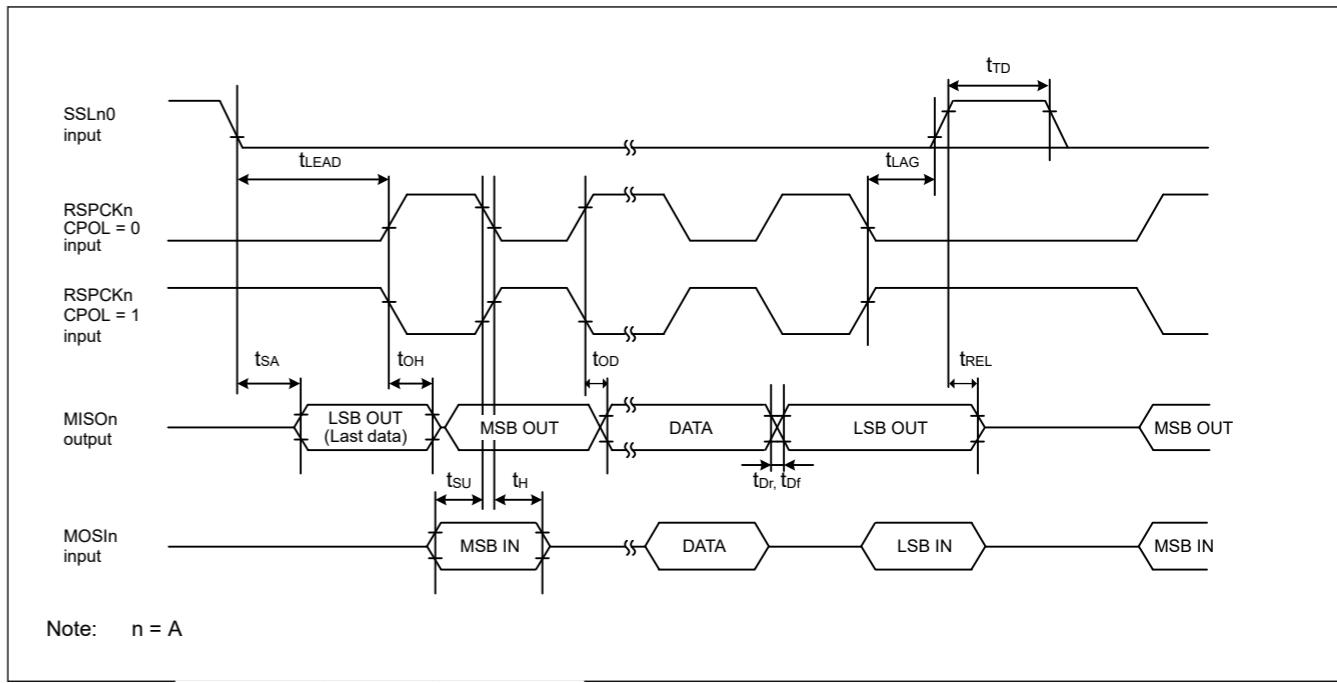


Figure 2.39 CPHA=1时从机的SPI时序

2.3.10 QSPI Timing

Table 2.28 QSPI timing

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|-----------|--------------|--------------------|--|--|--------------------|
| QSPI | QSPCK时钟周期 | t _{QScyc} | 2 | 48 | t _{Pcyc} |
| | QSPCK时钟高脉冲宽度 | t _{QSWH} | t _{QScyc} × 0.4 | — | ns |
| | QSPCK时钟低脉冲宽度 | t _{QSWL} | t _{QScyc} × 0.4 | — | ns |
| | 数据输入建立时间 | t _{Su} | 10 | — | ns |
| | 数据输入保持时间 | t _{IH} | 0 | — | ns |
| | QSSL设置时间 | t _{LEAD} | (N + 0.5) × t _{QScyc} - 5 ^{*1} | (N + 0.5) × t _{QScyc} + 100 ^{*1} | ns |
| | QSSL保持时间 | t _{LAG} | (N + 0.5) × t _{QScyc} - 5 ^{*2} | (N + 0.5) × t _{QScyc} + 100 ^{*2} | ns |
| | 数据输出延迟 | t _{OD} | — | 4 | ns |
| | 数据输出保持时间 | t _{OH} | -3.3 | — | ns |
| | 连续传输延迟 | t _{TD} | 1 | 16 | t _{QScyc} |

Note: t_{Pcyc}: PCLKA cycle.

注1.在SFMSLD中N设置为0或1。注2.在

SFMSHD中N设置为0或1。

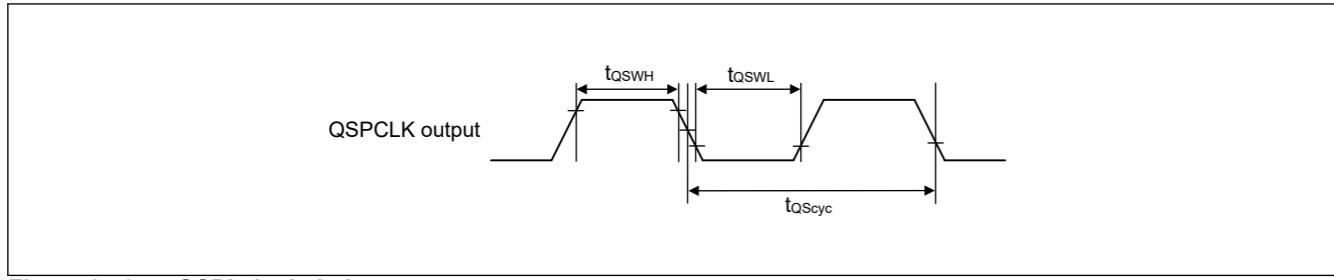


Figure 2.40 QSPI clock timing

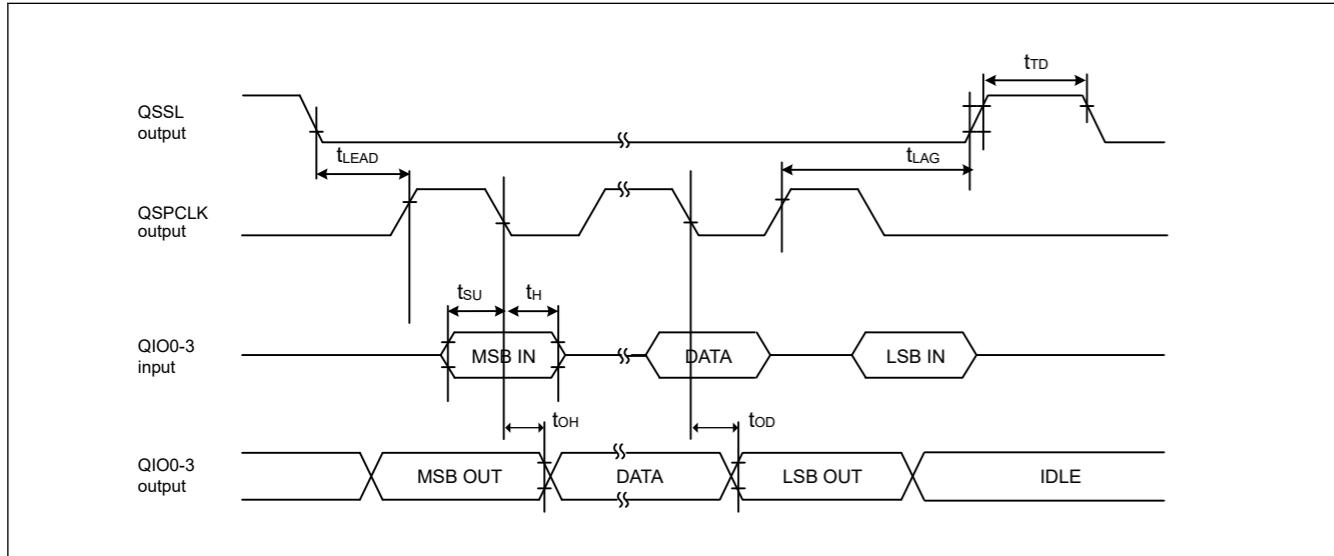


Figure 2.41 Transmit and receive timing

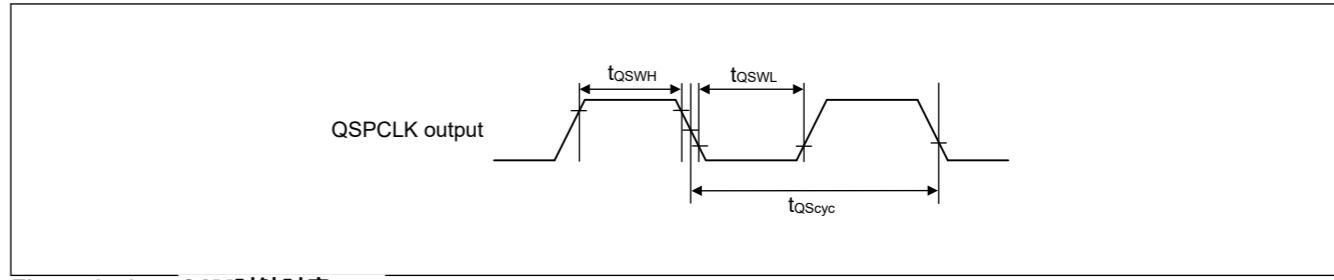


Figure 2.40 QSPI时钟时序

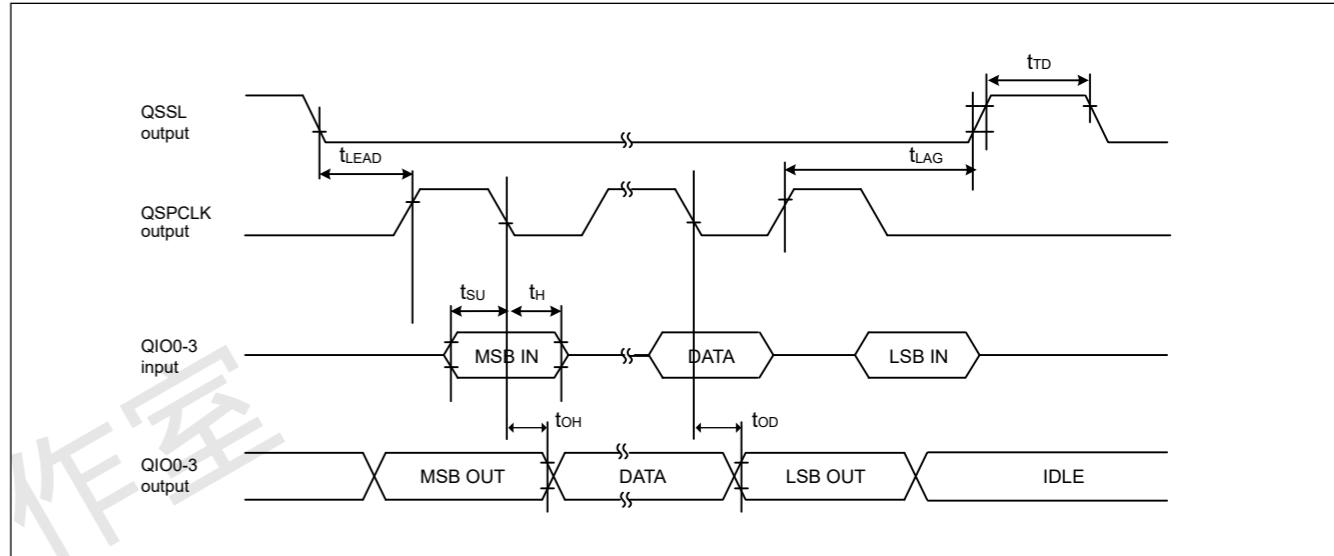


Figure 2.41 发送和接收时序

2.3.11 IIC Timing

Table 2.29 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A.

(3) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|--|--|------------------------------|---|-----------------------------|-----------------|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | t _{SCL} | 6 (12) × t _{IICcyc} + 1300 | — | ns |
| | SCL input high pulse width | t _{SCLH} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | SCL input low pulse width | t _{SCLL} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | SCL, SDA rise time | t _{sr} | — | 1000 | ns |
| | SCL, SDA fall time | t _{sf} | — | 300 | ns |
| | SCL, SDA input spike pulse removal time | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns |
| | SDA input bus free time when wakeup function is disabled | t _{BUF} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | SDA input bus free time when wakeup function is enabled | t _{BUF} | 3 (6) × t _{IICcyc} + 4 × t _{Pcyc} + 300 | — | ns |
| | START condition input hold time when wakeup function is disabled | t _{STAH} | t _{IICcyc} + 300 | — | ns |
| | START condition input hold time when wakeup function is enabled | t _{STAH} | 1 (5) × t _{IICcyc} + t _{Pcyc} + 300 | — | ns |
| | Repeated START condition input setup time | t _{STAS} | 1000 | — | ns |
| | STOP condition input setup time | t _{STOS} | 1000 | — | ns |
| | Data input setup time | t _{SDAS} | t _{IICcyc} + 50 | — | ns |
| | Data input hold time | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*2} | — | 400 | pF |

Figure 2.42

2.3.11 IIC Timing

Table 2.29 IIC时序(1)(1of2)

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A。(3)使用名称后附有字母的图钉，例如“_A”或“_B”，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|--|--------------------------|------------------------------|---|-----------------------------|------|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL输入周期时间 | t _{SCL} | 6 (12) × t _{IICcyc} + 1300 | — | ns |
| | SCL输入高脉冲宽度 | t _{SCLH} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | SCL输入低脉冲宽度 | t _{SCLL} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | SCL、SDA上升时间 | t _{sr} | — | 1000 | ns |
| | SCL、SDA下降时间 | t _{sf} | — | 300 | ns |
| | SCL、SDA输入尖峰脉冲去除时间 | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns |
| | 禁用唤醒功能时的SDA输入总线空闲时间 | t _{BUF} | 3 (6) × t _{IICcyc} + 300 | — | ns |
| | 唤醒功能启用时SDA输入总线空闲时间 | t _{BUF} | 3 (6) × t _{IICcyc} + 4 × t _{Pcyc} + 300 | — | ns |
| | 禁用唤醒功能时的START条件输入保持时间 | t _{STAH} | t _{IICcyc} + 300 | — | ns |
| | 启用唤醒功能时的START条件输入保持时间 | t _{STAH} | 1 (5) × t _{IICcyc} + t _{Pcyc} + 300 | — | ns |
| | 重复启动条件输入建立时间 | t _{STAS} | 1000 | — | ns |
| | STOP条件输入建立时间 | t _{STOS} | 1000 | — | ns |
| | 数据输入建立时间 | t _{SDAS} | t _{IICcyc} + 50 | — | ns |
| | 数据输入保持时间 | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*2} | — | 400 | pF |

Figure 2.42

Table 2.29 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B.
 (2) The following pins do not require setting: SCL0_A, SDA0_A.
 (3) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|--------------------|--|------------|--|--------------------------|-----------------|
| IIC (Fast mode) | SCL input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 600$ | — | ns |
| | SCL input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | SCL input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | SCL, SDA rise time | t_{Sr} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns |
| | SCL, SDA fall time | t_{Sf} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | — | ns |
| | START condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 300$ | — | ns |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1(5) \times t_{IICcyc} + t_{Pcyc} + 300$ | — | ns |
| | Repeated START condition input setup time | t_{STAS} | 300 | — | ns |
| | STOP condition input setup time | t_{STOS} | 300 | — | ns |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns |
| | Data input hold time | t_{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Note 1. Only supported for SCL0_A and SDA0_A.

Note 2. C_b indicates the total capacity of the bus line.

Table 2.29 IIC时序(1)(2of2)

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A。(3)使用名称后附有字母的图钉，例如“_A”或“_B”，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|--------------------|--------------------------|------------|--|--------------------------|------|
| IIC (Fast mode) | SCL输入周期时间 | t_{SCL} | $6(12) \times t_{IICcyc} + 600$ | — | ns |
| | SCL输入高脉冲宽度 | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | SCL输入低脉冲宽度 | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | SCL、SDA上升时间 | t_{Sr} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns |
| | SCL、SDA下降时间 | t_{Sf} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns |
| | SCL、SDA输入尖峰脉冲去除时间 | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns |
| | 禁用唤醒功能时的SDA输入总线空闲时间 | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns |
| | 唤醒功能启用时SDA输入总线空闲时间 | t_{BUF} | $3(6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | — | ns |
| | 禁用唤醒功能时的START条件输入保持时间 | t_{STAH} | $t_{IICcyc} + 300$ | — | ns |
| | 启用唤醒功能时的START条件输入保持时间 | t_{STAH} | $1(5) \times t_{IICcyc} + t_{Pcyc} + 300$ | — | ns |
| | 重复启动条件输入建立时间 | t_{STAS} | 300 | — | ns |
| | STOP条件输入建立时间 | t_{STOS} | 300 | — | ns |
| | 数据输入建立时间 | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns |
| | 数据输入保持时间 | t_{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF |

Note: t_{IICcyc} : IIC内部参考时钟(IIC ϕ)周期, t_{Pcyc} : PCLKB周期。

Note: 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。

Note: 必须使用名称后附有字母的引脚，例如“_A”、“_B”，以表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

注1.仅支持SCL0_A和SDA0_A。

注2.Cb表示公交线路的总容量。

Table 2.30 IIC timing (2)

Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---------------------------------------|--|------------------------------|---|-----------------------------|-----------------|
| IIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | t _{SCL} | 6 (12) × t _{IICcyc} + 240 | — | ns |
| | SCL input high pulse width | t _{SCLH} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | SCL input low pulse width | t _{SCLL} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | SCL, SDA rise time | t _{SR} | — | 120 | ns |
| | SCL, SDA fall time | t _{SF} | 20 × (external pullup voltage/ 5.5V) | 120 | ns |
| | SCL, SDA input spike pulse removal time | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns |
| | SDA input bus free time when wakeup function is disabled | t _{BUF} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | SDA input bus free time when wakeup function is enabled | t _{BUF} | 3 (6) × t _{IICcyc} + 4 × t _{Pcyc} + 120 | — | ns |
| | Start condition input hold time when wakeup function is disabled | t _{STAH} | t _{IICcyc} + 120 | — | ns |
| | START condition input hold time when wakeup function is enabled | t _{STAH} | 1 (5) × t _{IICcyc} + t _{Pcyc} + 120 | — | ns |
| | Restart condition input setup time | t _{STAS} | 120 | — | ns |
| | Stop condition input setup time | t _{STOS} | 120 | — | ns |
| | Data input setup time | t _{SDAS} | t _{IICcyc} + 30 | — | ns |
| | Data input hold time | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 550 | pF |

Note: t_{IICcyc}: IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc}: PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.

Table 2.30 IIC timing (2)

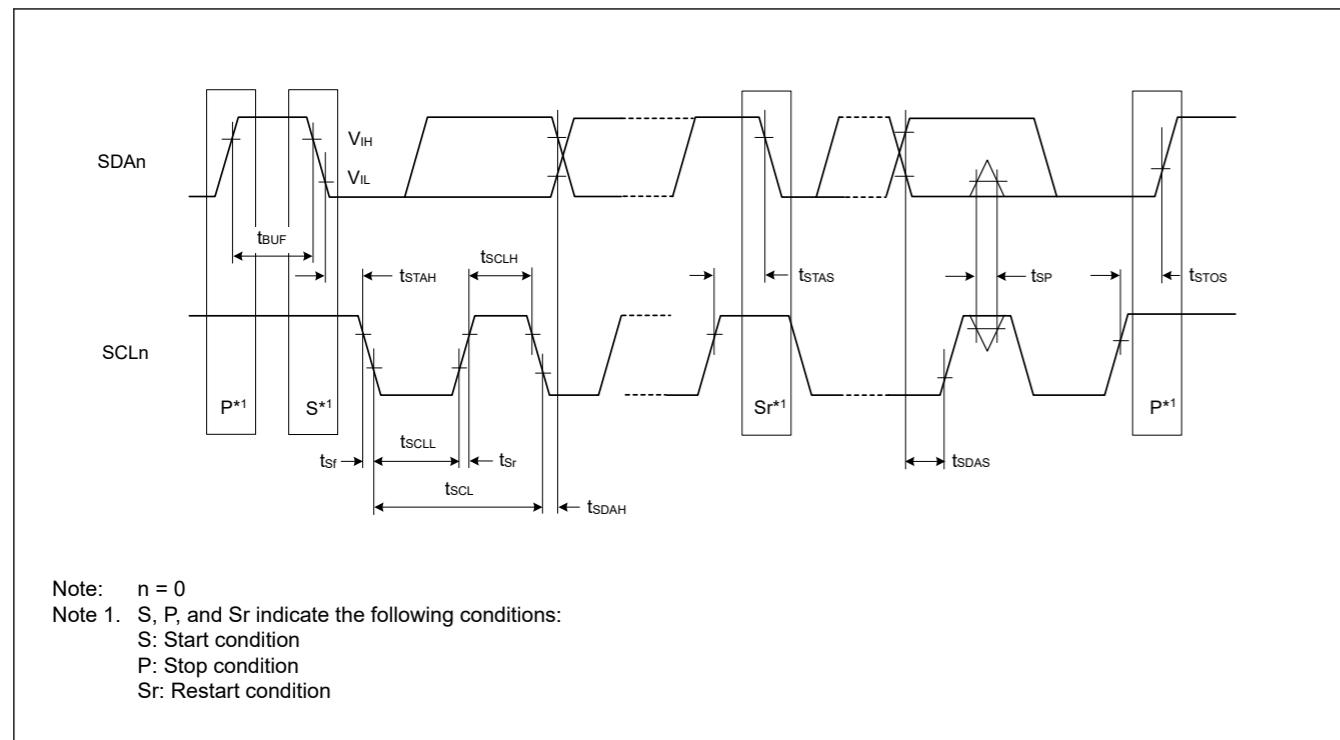
PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

| Parameter | Symbol | Min | Max | Unit | 测试条件 |
|---------------------------------------|--------------------------|------------------------------|---|-----------------------------|------|
| IIC (Fast-mode+) ICFER.FMPE = 1 | SCL输入周期时间 | t _{SCL} | 6 (12) × t _{IICcyc} + 240 | — | ns |
| | SCL输入高脉冲宽度 | t _{SCLH} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | SCL输入低脉冲宽度 | t _{SCLL} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | SCL、SDA上升时间 | t _{SR} | — | 120 | ns |
| | SCL、SDA下降时间 | t _{SF} | 20 × (external pullup voltage/ 5.5V) | 120 | ns |
| | SCL、SDA输入尖峰脉冲去除时间 | t _{SP} | 0 | 1 (4) × t _{IICcyc} | ns |
| | 禁用唤醒功能时的SDA输入总线空闲时间 | t _{BUF} | 3 (6) × t _{IICcyc} + 120 | — | ns |
| | 唤醒功能启用时SDA输入总线空闲时间 | t _{BUF} | 3 (6) × t _{IICcyc} + 4 × t _{Pcyc} + 120 | — | ns |
| | 禁用唤醒功能时的启动条件输入保持时间 | t _{STAH} | t _{IICcyc} + 120 | — | ns |
| | 启用唤醒功能时的START条件输入保持时间 | t _{STAH} | 1 (5) × t _{IICcyc} + t _{Pcyc} + 120 | — | ns |
| | 重启条件输入建立时间 | t _{STAS} | 120 | — | ns |
| | 停止条件输入建立时间 | t _{STOS} | 120 | — | ns |
| | 数据输入建立时间 | t _{SDAS} | t _{IICcyc} + 30 | — | ns |
| | 数据输入保持时间 | t _{SDAH} | 0 | — | ns |
| | SCL, SDA capacitive load | C _b ^{*1} | — | 550 | pF |

Note: t_{IICcyc}: IIC内部参考时钟(IIC ϕ)周期, t_{Pcyc}: PCLKB周期。

Note: 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。

注1.C_b表示总线的总容量。

Figure 2.42 I²C bus interface input/output timing

2.4 USB Characteristics

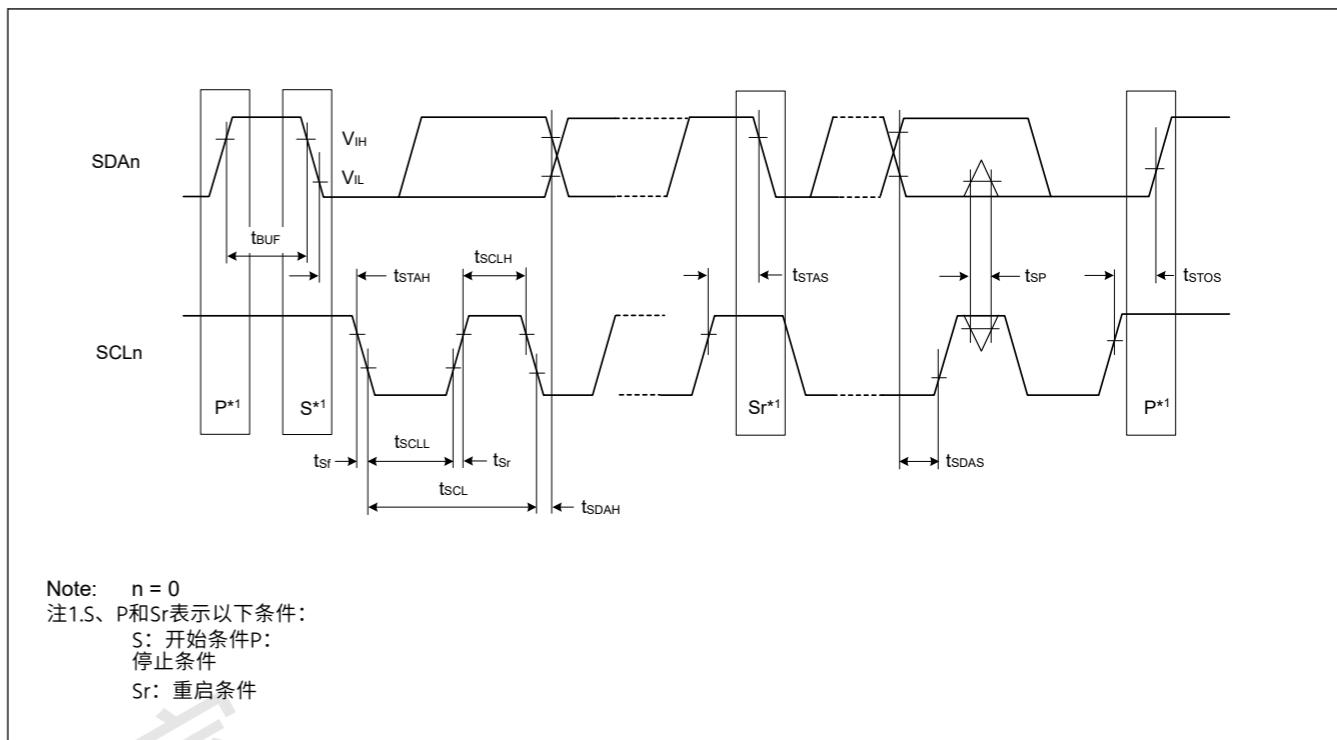
2.4.1 USBFS Timing

Table 2.31 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|--|-----------------------------------|-------|-----|-------|-----------------|
| Input characteristics | Input high voltage | V _{IH} | 2.0 | — | V | — |
| | Input low voltage | V _{IL} | — | 0.8 | V | — |
| | Differential input sensitivity | V _{DI} | 0.2 | — | V | USB_DP - USB_DM |
| | Differential common-mode range | V _{CM} | 0.8 | — | 2.5 | V |
| Output characteristics | Output high voltage | V _{OH} | 2.8 | — | 3.6 | V |
| | Output low voltage | V _{OL} | 0.0 | — | 0.3 | V |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V |
| | Rise time | t _{LR} | 75 | — | 300 | ns |
| | Fall time | t _{LF} | 75 | — | 300 | ns |
| | Rise/fall time ratio | t _{LR} / t _{LF} | 80 | — | 125 | % |
| Pull-up and pull-down characteristics | USB_DP and USB_DM pull-down resistance in host controller mode | R _{pd} | 14.25 | — | 24.80 | kΩ |

Figure 2.43

Figure 2.42 I²C总线接口输入输出时序

2.4 USB特性

2.4.1 USBFS Timing

Table 2.31 仅主机的USBFS低速特性 (USB_DP和USB_DM引脚特性)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-----------|----------------------------|-----------------------------------|-------|-----|-------|------|
| 输入特性 | 输入高压 | V _{IH} | 2.0 | — | — | V |
| | 输入低电压 | V _{IL} | — | — | 0.8 | V |
| | 差分输入灵敏度 | V _{DI} | 0.2 | — | — | V |
| | 差分共模范围 | V _{CM} | 0.8 | — | 2.5 | V |
| 输出特性 | 输出高压 | V _{OH} | 2.8 | — | 3.6 | V |
| | 输出低电压 | V _{OL} | 0.0 | — | 0.3 | V |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V |
| | 上升时间 | t _{LR} | 75 | — | 300 | ns |
| | 秋季时间 | t _{LF} | 75 | — | 300 | ns |
| | 上升下降时间比 | t _{LR} / t _{LF} | 80 | — | 125 | % |
| 上拉和下拉特性 | 主机控制器模式下的USB_DP和USB_DM下拉电阻 | R _{pd} | 14.25 | — | 24.80 | kΩ |

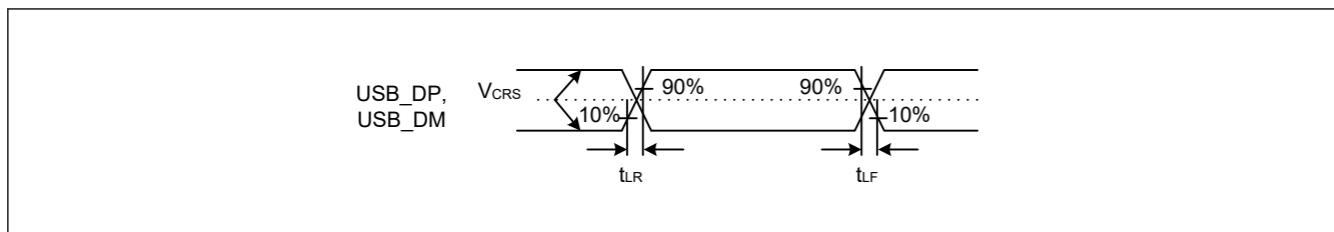


Figure 2.43 USB_DP and USB_DM output timing in low-speed mode

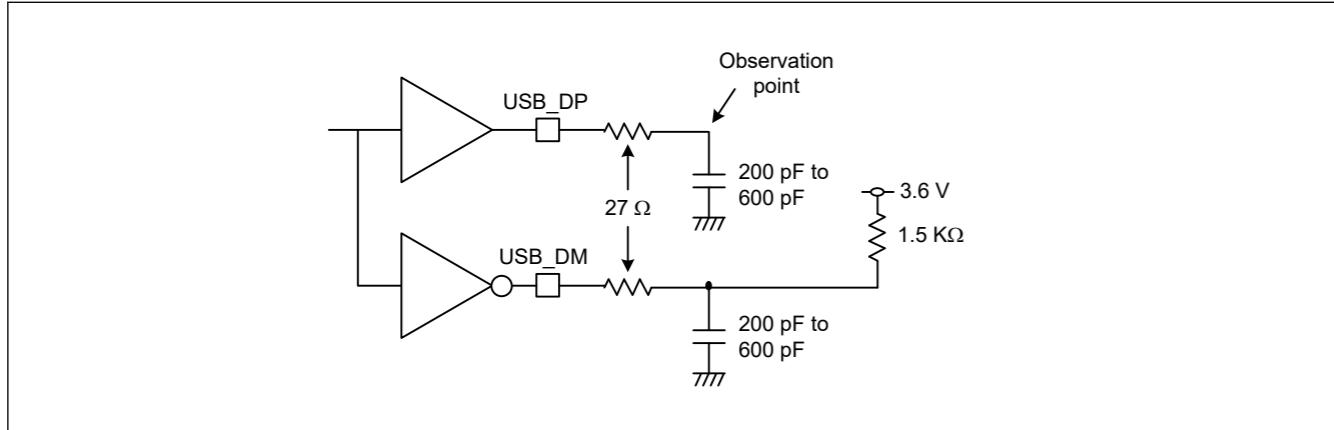


Figure 2.44 Test circuit in low-speed mode

Table 2.32 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|--|-----------------------------------|-------|-----|--------|-----------------|
| Input characteristics | Input high voltage | V _{IH} | 2.0 | — | V | — |
| | Input low voltage | V _{IL} | — | — | 0.8 | V |
| | Differential input sensitivity | V _{DI} | 0.2 | — | V | USB_DP - USB_DM |
| | Differential common-mode range | V _{CM} | 0.8 | — | 2.5 | V |
| Output characteristics | Output high voltage | V _{OH} | 2.8 | — | 3.6 | V |
| | Output low voltage | V _{OL} | 0.0 | — | 0.3 | V |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V |
| | Rise time | t _{LR} | 4 | — | 20 | ns |
| | Fall time | t _{LF} | 4 | — | 20 | ns |
| | Rise/fall time ratio | t _{LR} / t _{LF} | 90 | — | 111.11 | % |
| | Output resistance | Z _{DRV} | 28 | — | 44 | Ω |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | R _{pu} | 0.900 | — | 1.575 | kΩ |
| | | | 1.425 | — | 3.090 | kΩ |
| | USB_DP and USB_DM pull-down resistance in host controller mode | R _{pd} | 14.25 | — | 24.80 | kΩ |

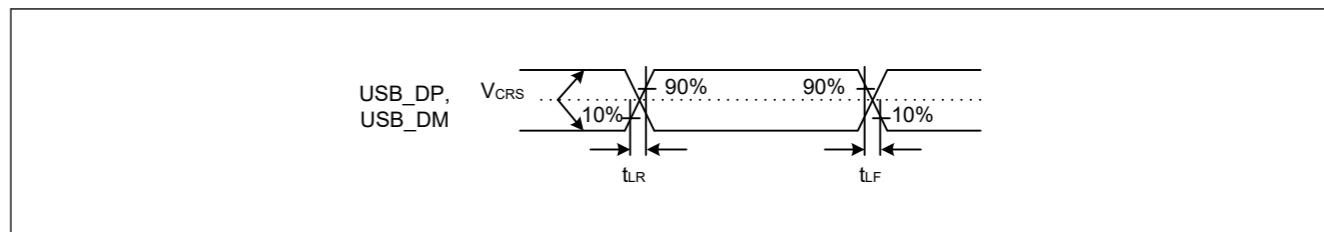


Figure 2.43 低速模式下的USB_DP和USB_DM输出时序

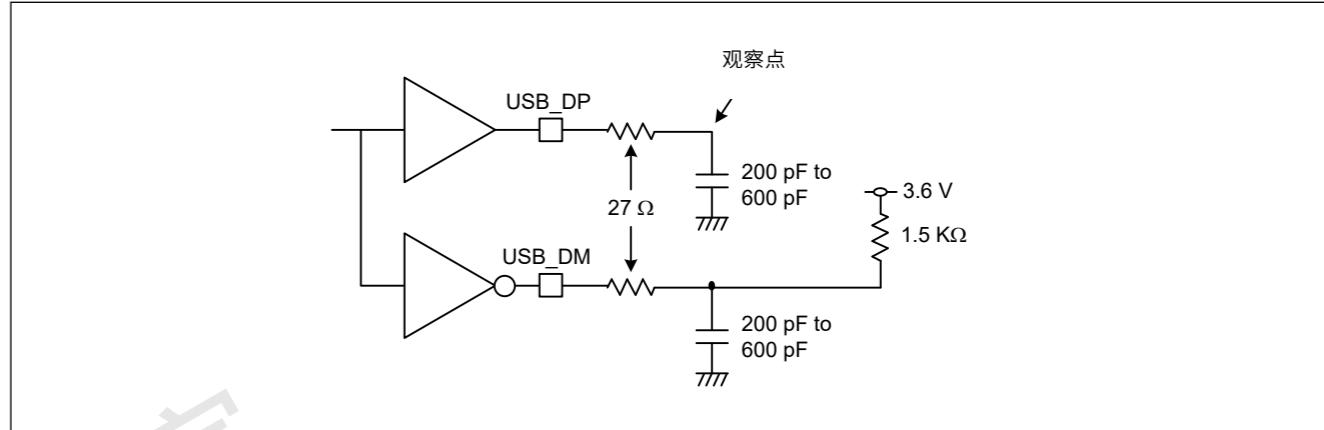


Figure 2.44 低速模式下的测试电路

Table 2.32 USBFS全速特性 (USB_DP和USB_DM引脚特性)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-----------|----------------------------|-----------------------------------|-------|-----|--------|------|
| 输入特性 | 输入高压 | V _{IH} | 2.0 | — | — | V |
| | 输入低电压 | V _{IL} | — | — | 0.8 | V |
| | 差分输入灵敏度 | V _{DI} | 0.2 | — | — | V |
| | 差分共模范围 | V _{CM} | 0.8 | — | 2.5 | V |
| 输出特性 | 输出高压 | V _{OH} | 2.8 | — | 3.6 | V |
| | 输出低电压 | V _{OL} | 0.0 | — | 0.3 | V |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V |
| | 上升时间 | t _{LR} | 4 | — | 20 | ns |
| | 秋季时间 | t _{LF} | 4 | — | 20 | ns |
| | 上升下降时间比 | t _{LR} / t _{LF} | 90 | — | 111.11 | % |
| | 输出电阻 | Z _{DRV} | 28 | — | 44 | Ω |
| 上拉和下拉特性 | 设备控制器模式下的DM上拉电阻 | R _{pu} | 0.900 | — | 1.575 | kΩ |
| | | | 1.425 | — | 3.090 | kΩ |
| | 主机控制器模式下的USB_DP和USB_DM下拉电阻 | R _{pd} | 14.25 | — | 24.80 | kΩ |

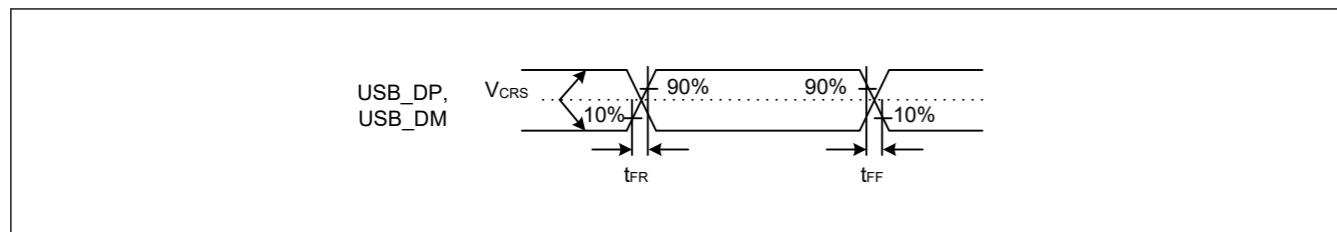


Figure 2.45 USB_DP and USB_DM output timing in full-speed mode

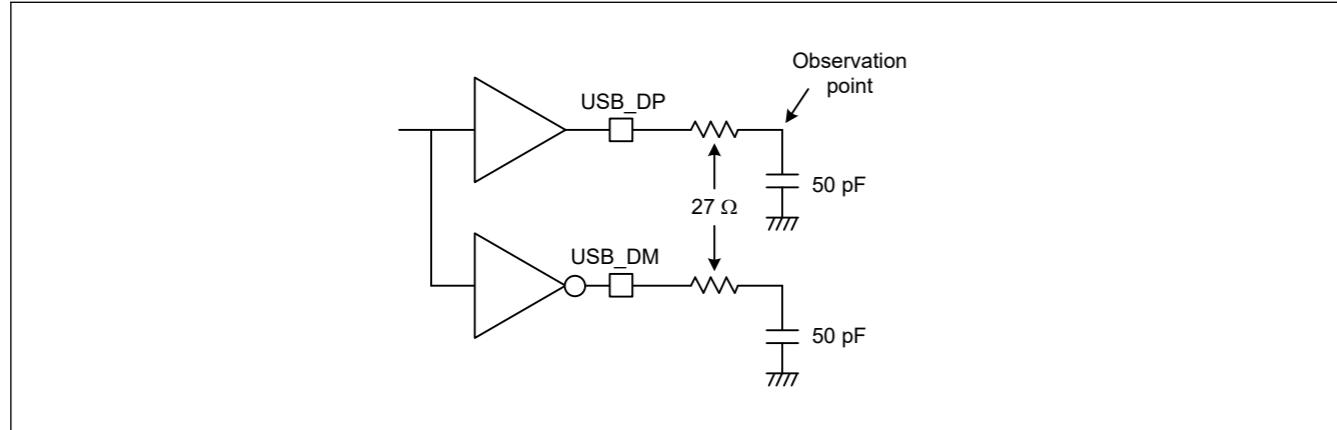


Figure 2.46 Test circuit in full-speed mode

Table 2.33 USBFS characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------------------|----------------------|------|-----|-----|------|-------------------------|
| Battery Charging Specification | I _{DP_SINK} | 25 | — | 175 | μA | — |
| | I _{DM_SINK} | 25 | — | 175 | μA | — |
| | I _{DP_SRC} | 7 | — | 13 | μA | — |
| | V _{DAT_REF} | 0.25 | — | 0.4 | V | — |
| | V _{DP_SRC} | 0.5 | — | 0.7 | V | Outout current = 250 μA |
| | V _{DM_SRC} | 0.5 | — | 0.7 | V | Outout current = 250 μA |

2.5 ADC12 Characteristics

Table 2.34 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----|------|-----|------|-----------------|
| Frequency | 1 | — | 50 | MHz | — |
| Analog input capacitance | — | — | 30 | pF | — |
| Quantization error | — | ±0.5 | — | LSB | — |
| Resolution | — | — | 12 | Bits | — |

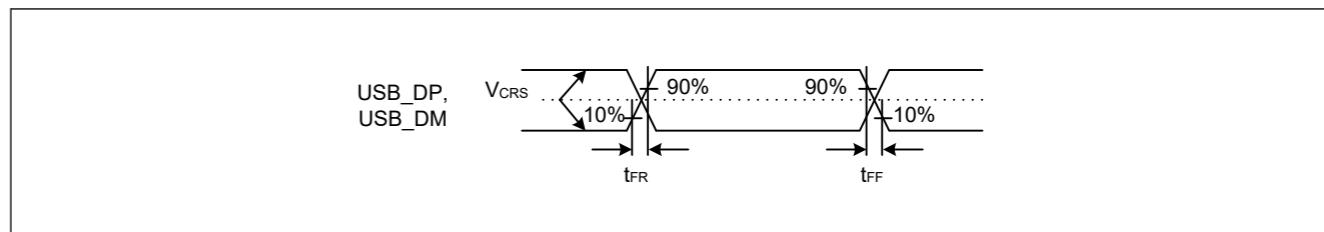


Figure 2.45 全速模式下的USB_DP和USB_DM输出时序

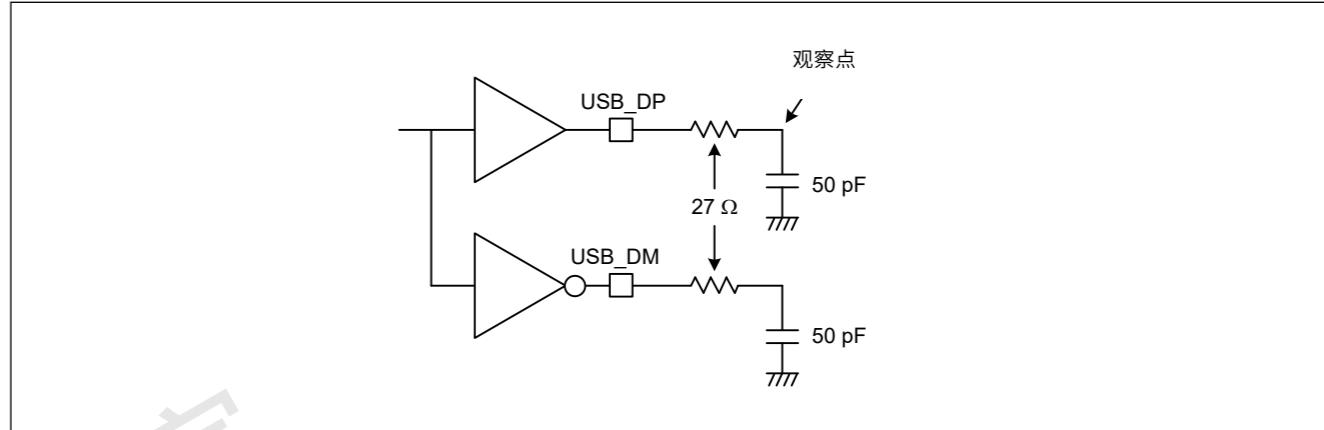


Figure 2.46 全速模式下的测试电路

Table 2.33 USBFS特性 (USB_DP和USB_DM引脚特性)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|--------------------|----------------------|------|-----|-----|------|-------------------------|
| 电池充电 Specification | I _{DP_SINK} | 25 | — | 175 | μA | — |
| | I _{DM_SINK} | 25 | — | 175 | μA | — |
| | I _{DP_SRC} | 7 | — | 13 | μA | — |
| | V _{DAT_REF} | 0.25 | — | 0.4 | V | — |
| | V _{DP_SRC} | 0.5 | — | 0.7 | V | Outout current = 250 μA |
| | V _{DM_SRC} | 0.5 | — | 0.7 | V | Outout current = 250 μA |

2.5 ADC12 Characteristics

Table 2.34 单元0(1of2)的AD转换特性

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | 最大单位 | 测试条件 |
|------------|-----|------|------|------|
| Frequency | 1 | — | 50 | MHz |
| 模拟输入电容 | — | — | 30 | pF |
| 量化误差 | — | ±0.5 | — | LSB |
| Resolution | — | — | 12 | Bits |

Table 2.34 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|--|--|---|---------------------------|------|------|------|--|
| High-precision high-speed channels (AN000 to AN002) | Conversion time ^{*1} (operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.52 (0.26) ^{*2} | — | — | μs | Sampling in 13 states |
| | | Max. = 400 Ω | 0.40 (0.14) ^{*2} | — | — | μs | Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | — | ±1.0 | ±2.5 | LSB | — | |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | — | |
| | Absolute accuracy | — | ±2.0 | ±4.5 | LSB | — | |
| | DNL differential nonlinearity error | — | ±0.5 | ±1.5 | LSB | — | |
| | INL integral nonlinearity error | — | ±1.0 | ±2.5 | LSB | — | |
| High-precision normal-speed channels (AN003, AN004, AN011 to AN013) | Conversion time ^{*1} (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66) ^{*2} | — | — | μs | Sampling in 33 states |
| | | Offset error | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | — | |
| | Absolute accuracy | — | ±2.0 | ±4.5 | LSB | — | |
| | DNL differential nonlinearity error | — | ±0.5 | ±1.5 | LSB | — | |
| | INL integral nonlinearity error | — | ±1.0 | ±2.5 | LSB | — | |
| Normal-precision normal-speed channels (AN016) | Conversion time ^{*1} (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66) ^{*2} | — | — | μs | Sampling in 33 states |
| | | Offset error | — | ±1.0 | ±5.5 | LSB | — |
| | Full-scale error | — | ±1.0 | ±5.5 | LSB | — | |
| | Absolute accuracy | — | ±2.0 | ±7.5 | LSB | — | |
| | DNL differential nonlinearity error | — | ±0.5 | ±4.5 | LSB | — | |
| | INL integral nonlinearity error | — | ±1.0 | ±5.5 | LSB | — | |

Note: These specification values apply when there is no access to the external memory during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.35 A/D internal reference voltage characteristics

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | — |
| Sampling time | 4.15 | — | — | μs | — |

Table 2.34 单元0(2of2)的AD转换特性

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | 最大单位 | 测试条件 |
|--|---|-------------------|---------------------------|------|------|--|
| 高精度高速通道 (AN000 至AN002) | 转换时间 ^{*1} (operation at PCLKC = 50 MHz) | 允许的信号源阻抗Max.= 1kΩ | 0.52 (0.26) ^{*2} | — | — | μs 在13个州进行抽样 |
| | | Max. = 400 Ω | 0.40 (0.14) ^{*2} | — | — | μs 在7种状态下采样 VCC=AVCC0=3.0至3.6V3.0V≤VREF H0≤AVCC0 |
| | 偏移误差 | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | — |
| | 绝对精度 | — | ±2.0 | ±4.5 | LSB | — |
| | DNL微分非线性误差 | — | ±0.5 | ±1.5 | LSB | — |
| 高精度常速通道 (AN003、AN004、AN011至AN013) | 转换时间 ^{*1} (Operation at PCLKC = 50 MHz) | 允许的信号源阻抗Max.= 1kΩ | 0.92 (0.66) ^{*2} | — | — | μs 在33个州进行抽样 |
| | | 偏移误差 | — | ±1.0 | ±2.5 | LSB |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | — |
| | 绝对精度 | — | ±2.0 | ±4.5 | LSB | — |
| | DNL微分非线性误差 | — | ±0.5 | ±1.5 | LSB | — |
| | INL积分非线性误差 | — | ±1.0 | ±2.5 | LSB | — |
| Normal-precision normal-speed channels (AN016) | 转换时间 ^{*1} (Operation at PCLKC = 50 MHz) | 允许的信号源阻抗Max.= 1kΩ | 0.92 (0.66) ^{*2} | — | — | μs 在33个州进行抽样 |
| | | 偏移误差 | — | ±1.0 | ±5.5 | LSB |
| | Full-scale error | — | ±1.0 | ±5.5 | LSB | — |
| | 绝对精度 | — | ±2.0 | ±7.5 | LSB | — |
| | DNL微分非线性误差 | — | ±0.5 | ±4.5 | LSB | — |
| | INL积分非线性误差 | — | ±1.0 | ±5.5 | LSB | — |

Note: 这些规格值适用于在AD转换期间无法访问外部存储器的情况。如果访问发生在D转换，值可能不在指定范围内。

使用12位AD转换器时，不允许将PORT0用作数字输出。

该特性适用于AVCC0、AVSS0、VREFH0、VREFL0和12位AD转换器输入电压稳定时。

注1.转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

注2：括号内的数值表示采样时间。

Table 2.35 AD内部参考电压特性

| Parameter | Min | Typ | Max | Unit | 测试条件 |
|-----------|------|------|------|------|------|
| AD内部参考电压 | 1.13 | 1.18 | 1.23 | V | — |
| 采样时间 | 4.15 | — | — | μs | — |

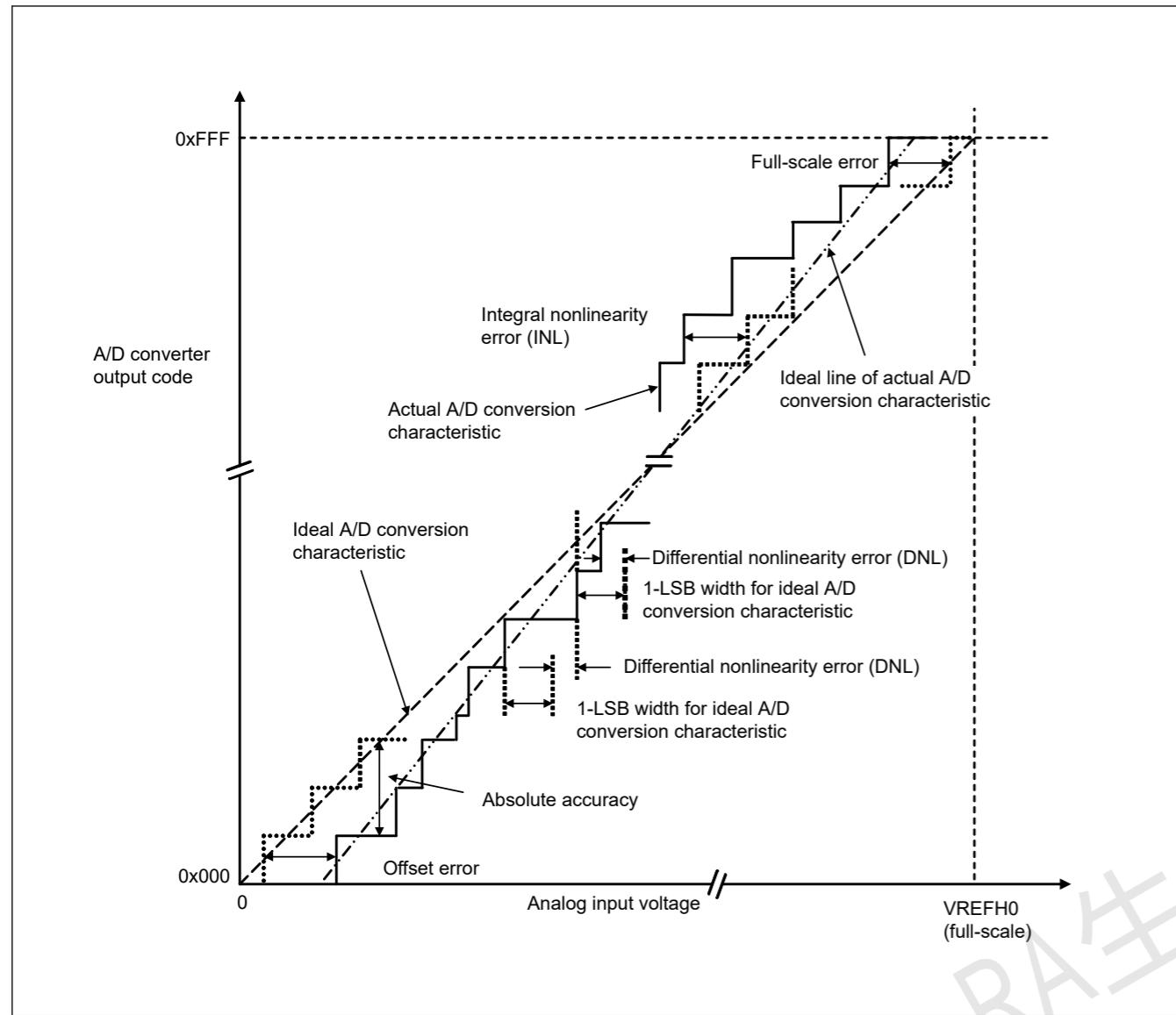


Figure 2.47 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072\text{V}$, then the 1-LSB width becomes 0.75mV , and 0mV , 0.75mV , and 1.5mV are used as the analog input voltages. If the analog input voltage is 6mV , an absolute accuracy of $\pm 5\text{ LSB}$ means that the actual A/D conversion result is in the range of $0x003$ to $0x00D$, though an output code of $0x008$ can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

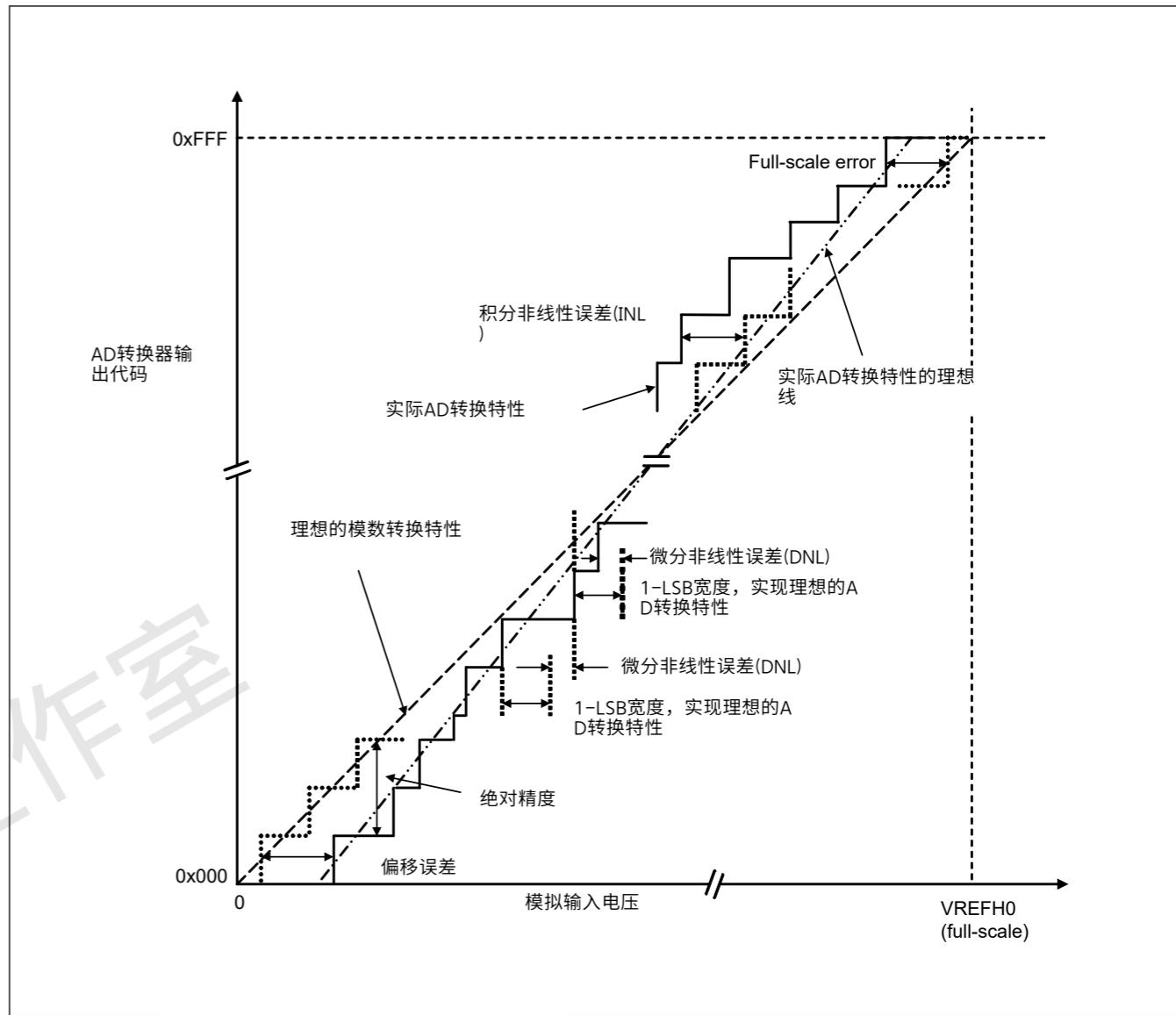


Figure 2.47 ADC12特征项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压可以满足基于理论模数转换特性输出等码的预期。例如，如果使用12位分辨率且参考电压 $V_{REFH0}=3.072\text{V}$ ，则1-LSB宽度变为 0.75mV ，并且使用 0mV 、 0.75mV 和 1.5mV 作为模拟输入电压。如果模拟输入电压为 6mV ， $\pm 5\text{LSB}$ 的绝对精度意味着实际的AD转换结果在 $0x003$ 到 $0x00D$ 的范围内，尽管从理论上的AD转换特性可以预期输出代码为 $0x008$ 。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

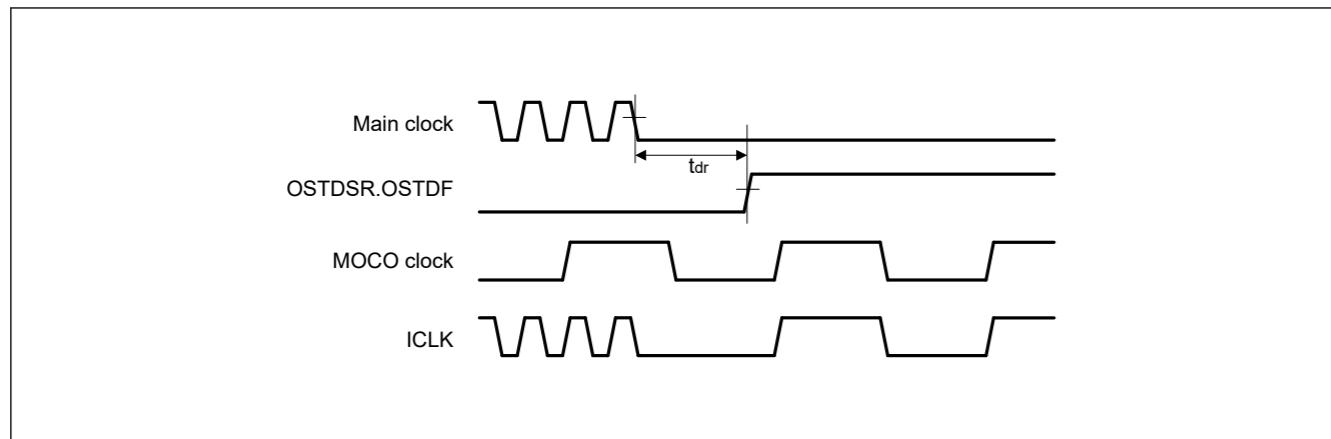
Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics**Table 2.36 D/A conversion characteristics**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----|------|-------------|------|--|
| Resolution | — | — | 12 | Bits | — |
| Without output amplifier | | | | | |
| Absolute accuracy | — | — | ±24 | LSB | Resistive load 2 MΩ |
| INL | — | ±2.0 | ±8.0 | LSB | Resistive load 2 MΩ |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Output impedance | — | 8.5 | — | kΩ | — |
| Conversion time | — | — | 3 | μs | Resistive load 2 MΩ, Capacitive load 20 pF |
| Output voltage range | 0 | — | VREFH | V | — |
| With output amplifier | | | | | |
| INL | — | ±2.0 | ±4.0 | LSB | — |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Conversion time | — | — | 4.0 | μs | — |
| Resistive load | 5 | — | — | kΩ | — |
| Capacitive load | — | — | 50 | pF | — |
| Output voltage range | 0.2 | — | VREFH – 0.2 | V | — |

2.7 OSC Stop Detect Characteristics**Table 2.37 Oscillation stop detection circuit characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------|-----------------|-----|-----|-----|------|-----------------------------|
| Detection time | t _{dr} | — | — | 1 | ms | Figure 2.48 |

**Figure 2.48 Oscillation stop detection timing****偏移误差**

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

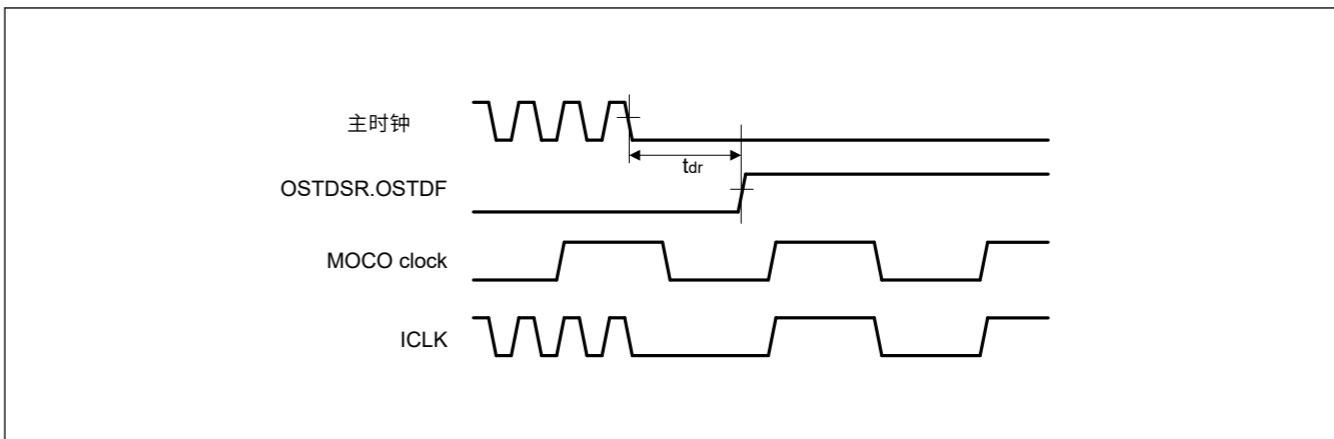
满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

2.6 DAC12 Characteristics**Table 2.36 DA转换特性**

| Parameter | Min | Typ | Max | Unit | 测试条件 |
|-----------------|-----|------|-------------|------|-------------------|
| Resolution | — | — | 12 | Bits | — |
| 无输出放大器 | | | | | |
| 绝对精度 | — | — | ±24 | LSB | 阻性负载2MΩ |
| INL | — | ±2.0 | ±8.0 | LSB | 阻性负载2MΩ |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| 输出阻抗 | — | 8.5 | — | kΩ | — |
| 转换时间 | — | — | 3 | μs | 电阻负载2MΩ, 电容负载20pF |
| 输出电压范围 | 0 | — | VREFH | V | — |
| 带输出放大器 | | | | | |
| INL | — | ±2.0 | ±4.0 | LSB | — |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| 转换时间 | — | — | 4.0 | μs | — |
| 阻性负载 | 5 | — | — | kΩ | — |
| Capacitive load | — | — | 50 | pF | — |
| 输出电压范围 | 0.2 | — | VREFH – 0.2 | V | — |

2.7 OSC停止检测特性**Table 2.37 振荡停止检测电路特性**

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|-----------|-----------------|-----|-----|-----|------|-----------------------------|
| 检测时间 | t _{dr} | — | — | 1 | ms | Figure 2.48 |

**Figure 2.48 振荡停止检测时机**

2.8 POR and LVD Characteristics

Table 2.38 Power-on reset circuit and voltage detection circuit characteristics (1)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|----------------------------------|------------------------------------|------------------|------|------|--|----------------------------------|
| Voltage detection level | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | V _{POR} | 2.5 | 2.6 | 2.7 | V Figure 2.49 |
| | | DPSBYCR.DEEPCUT[1:0] = 11b. | | 1.8 | 2.25 | 2.7 | |
| | Voltage detection circuit (LVDO) | V _{det0_1} | 2.84 | 2.94 | 3.04 | | Figure 2.50 |
| | | V _{det0_2} | 2.77 | 2.87 | 2.97 | | |
| | | V _{det0_3} | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | V _{det1_1} | 2.89 | 2.99 | 3.09 | | Figure 2.51 |
| | | V _{det1_2} | 2.82 | 2.92 | 3.02 | | |
| | | V _{det1_3} | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | V _{det2_1} | 2.89 | 2.99 | 3.09 | | Figure 2.52 |
| | | V _{det2_2} | 2.82 | 2.92 | 3.02 | | |
| | | V _{det2_3} | 2.75 | 2.85 | 2.95 | | |
| Internal reset time | Power-on reset time | t _{POR} | — | 4.5 | — | ms Figure 2.49 | |
| | LVDO reset time | t _{LVDO} | — | 0.51 | — | Figure 2.50 | |
| | LVD1 reset time | t _{LVD1} | — | 0.38 | — | Figure 2.51 | |
| | LVD2 reset time | t _{LVD2} | — | 0.38 | — | Figure 2.52 | |
| Minimum VCC down time*1 | | t _{VOFF} | 200 | — | — | μs Figure 2.49, Figure 2.50 | |
| Response delay | | t _{det} | — | — | 200 | μs Figure 2.50 to Figure 2.52 | |
| LVD operation stabilization time (after LVD is enabled) | | t _{d(E-A)} | — | — | 10 | μs Figure 2.51, Figure 2.52 | |
| Hysteresis width (LVD1 and LVD2) | | V _{LVH} | — | 70 | — | mV | |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

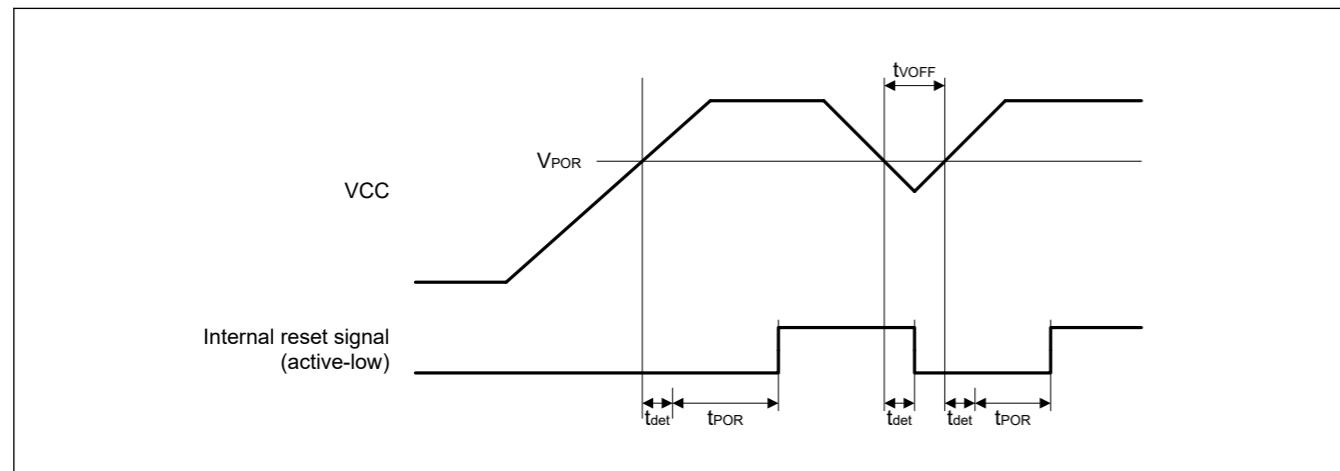


Figure 2.49 Power-on reset timing

2.8 POR和LVD特性

Table 2.38 上电复位电路及电压检测电路特性 (一)

| Parameter | | Symbol | Min | Typ | Max | 单元 | 测试条件 |
|--------------------|----------------------|------------------------------------|------------------|------|------|--|----------------------------------|
| 电压检测电平 | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | V _{POR} | 2.5 | 2.6 | 2.7 | V Figure 2.49 |
| | | DPSBYCR.DEEPCUT[1:0] = 11b. | | 1.8 | 2.25 | 2.7 | |
| | 电压检测电路 (LVDO) | V _{det0_1} | 2.84 | 2.94 | 3.04 | | Figure 2.50 |
| | | V _{det0_2} | 2.77 | 2.87 | 2.97 | | |
| | | V _{det0_3} | 2.70 | 2.80 | 2.90 | | |
| | 电压检测电路 (LVD1) | V _{det1_1} | 2.89 | 2.99 | 3.09 | | Figure 2.51 |
| | | V _{det1_2} | 2.82 | 2.92 | 3.02 | | |
| | | V _{det1_3} | 2.75 | 2.85 | 2.95 | | |
| | 电压检测电路 (LVD2) | V _{det2_1} | 2.89 | 2.99 | 3.09 | | Figure 2.52 |
| | | V _{det2_2} | 2.82 | 2.92 | 3.02 | | |
| | | V _{det2_3} | 2.75 | 2.85 | 2.95 | | |
| 内部复位时间 | 上电复位时间 | t _{POR} | — | 4.5 | — | ms Figure 2.49 | |
| | LVDO复位时间 | t _{LVDO} | — | 0.51 | — | Figure 2.50 | |
| | LVD1复位时间 | t _{LVD1} | — | 0.38 | — | Figure 2.51 | |
| | LVD2复位时间 | t _{LVD2} | — | 0.38 | — | Figure 2.52 | |
| 最小VCC停机时间*1 | | t _{VOFF} | 200 | — | — | μs Figure 2.49, Figure 2.50 | |
| 响应延迟 | | t _{det} | — | — | 200 | μs 图2.50至 Figure 2.52 | |
| LVD操作稳定时间 (启用LVD后) | | t _{d(E-A)} | — | — | 10 | μs Figure 2.51, Figure 2.52 | |
| 迟滞宽度 (LVD1和LVD2) | | V _{LVH} | — | 70 | — | mV | |

注1. 最小VCC停机时间是指VCC低于电压检测电平V_{POR}、V_{det0}、V_{det1}和V_{det2}用于POR和LVD。

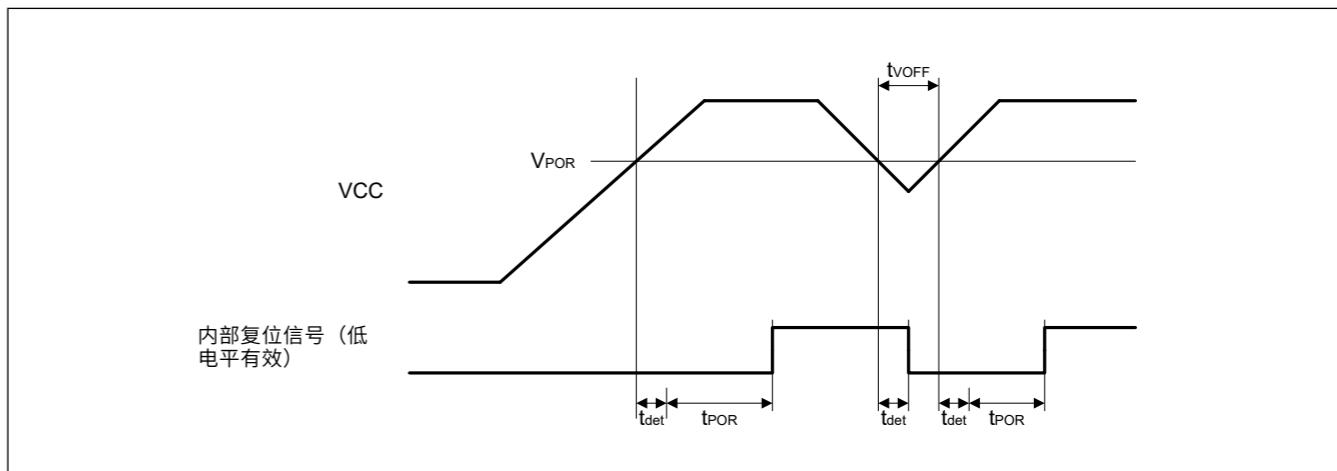
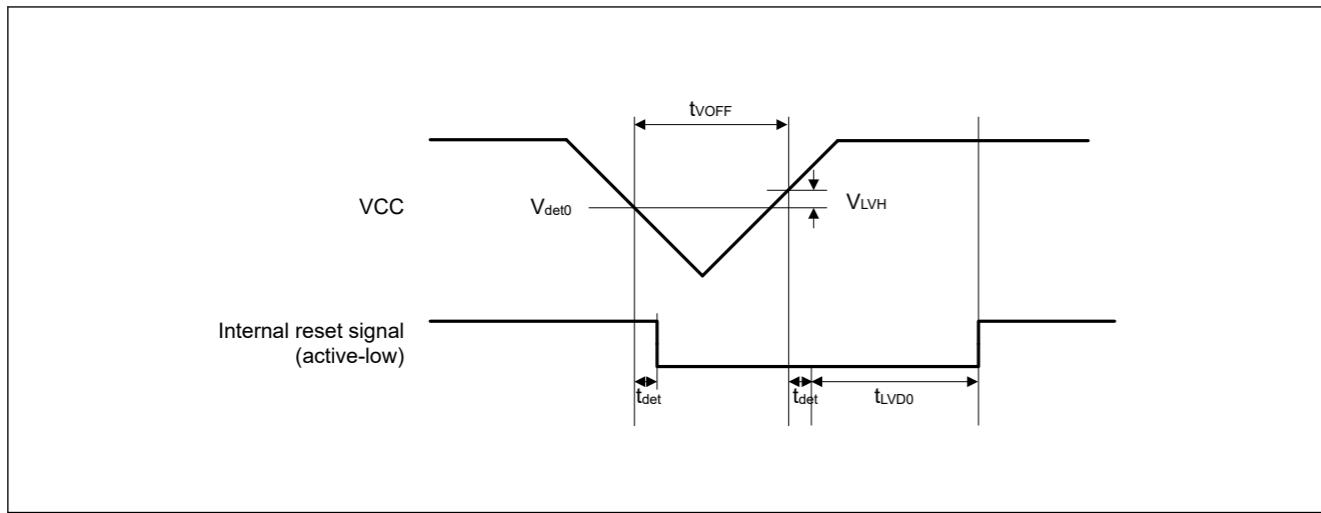
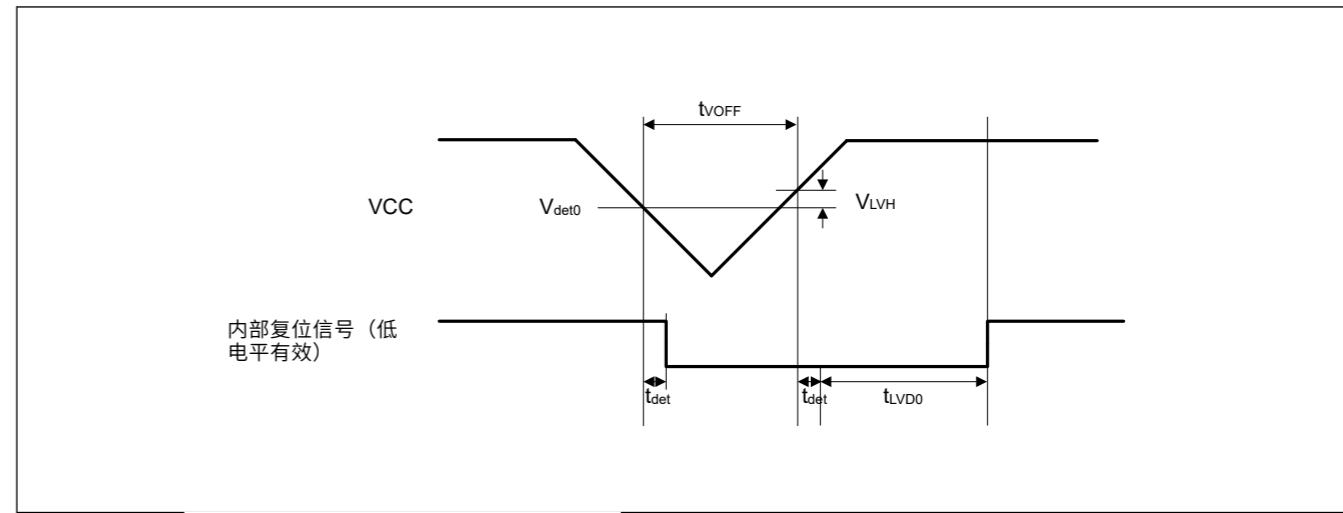
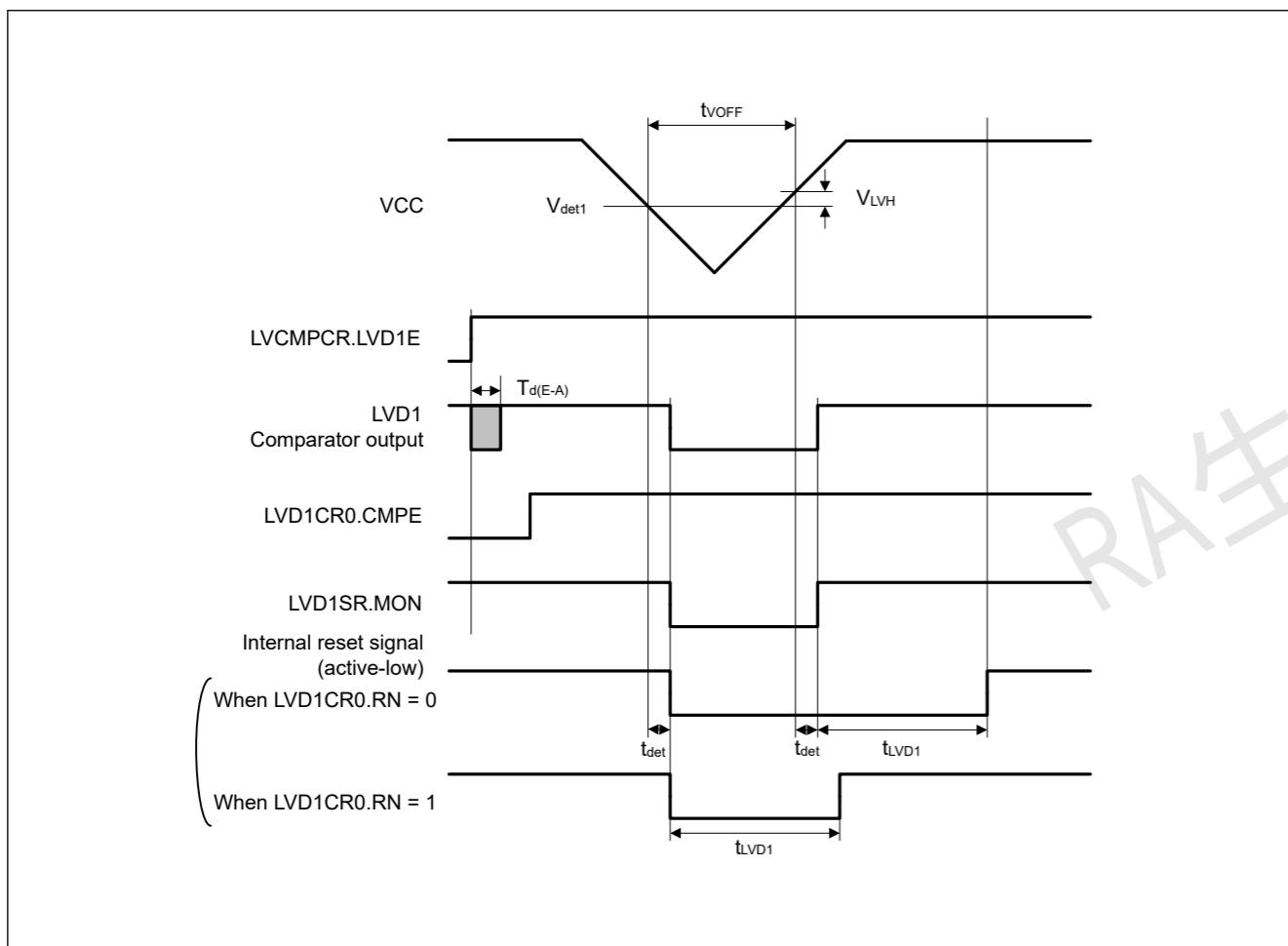
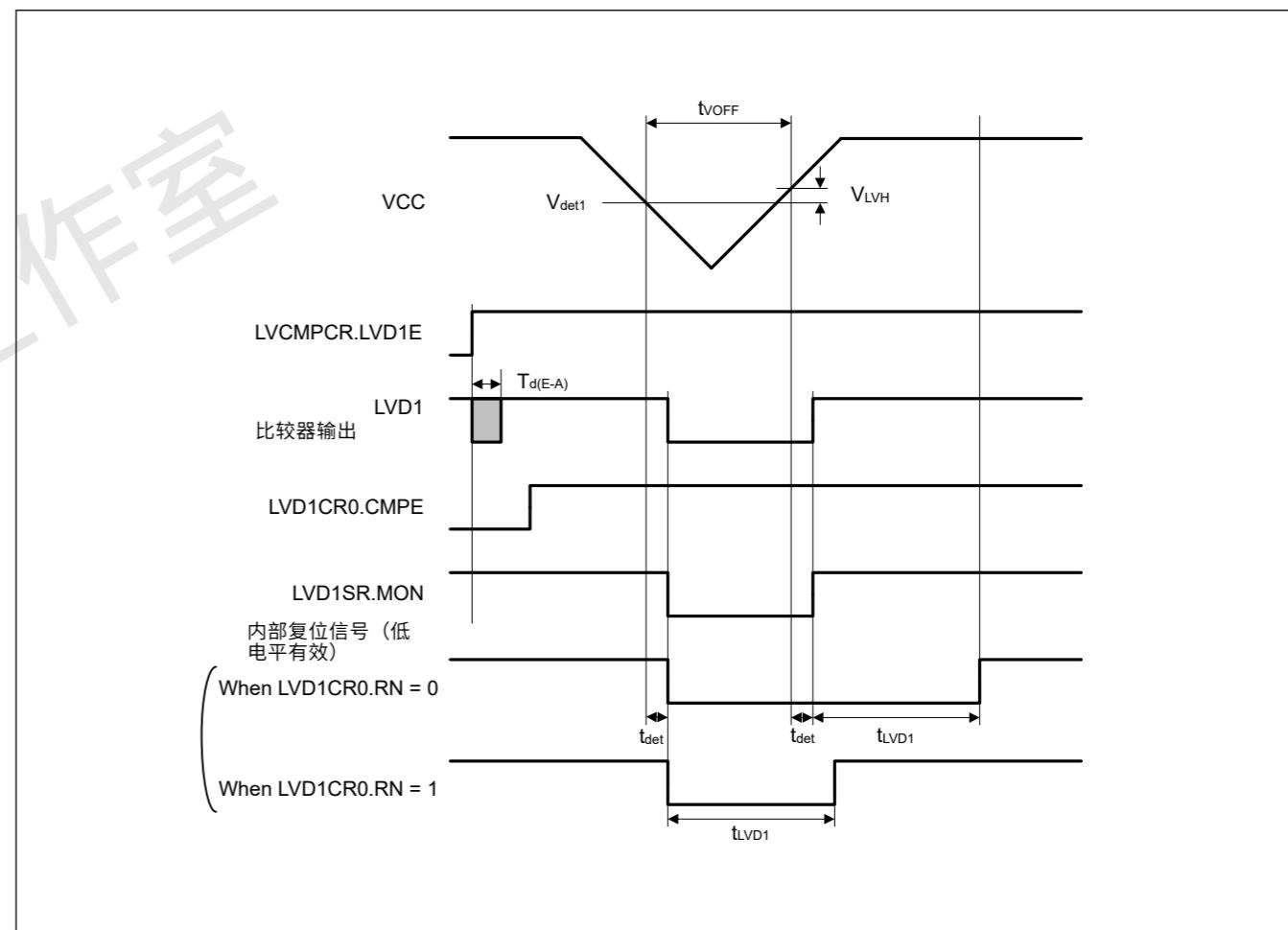
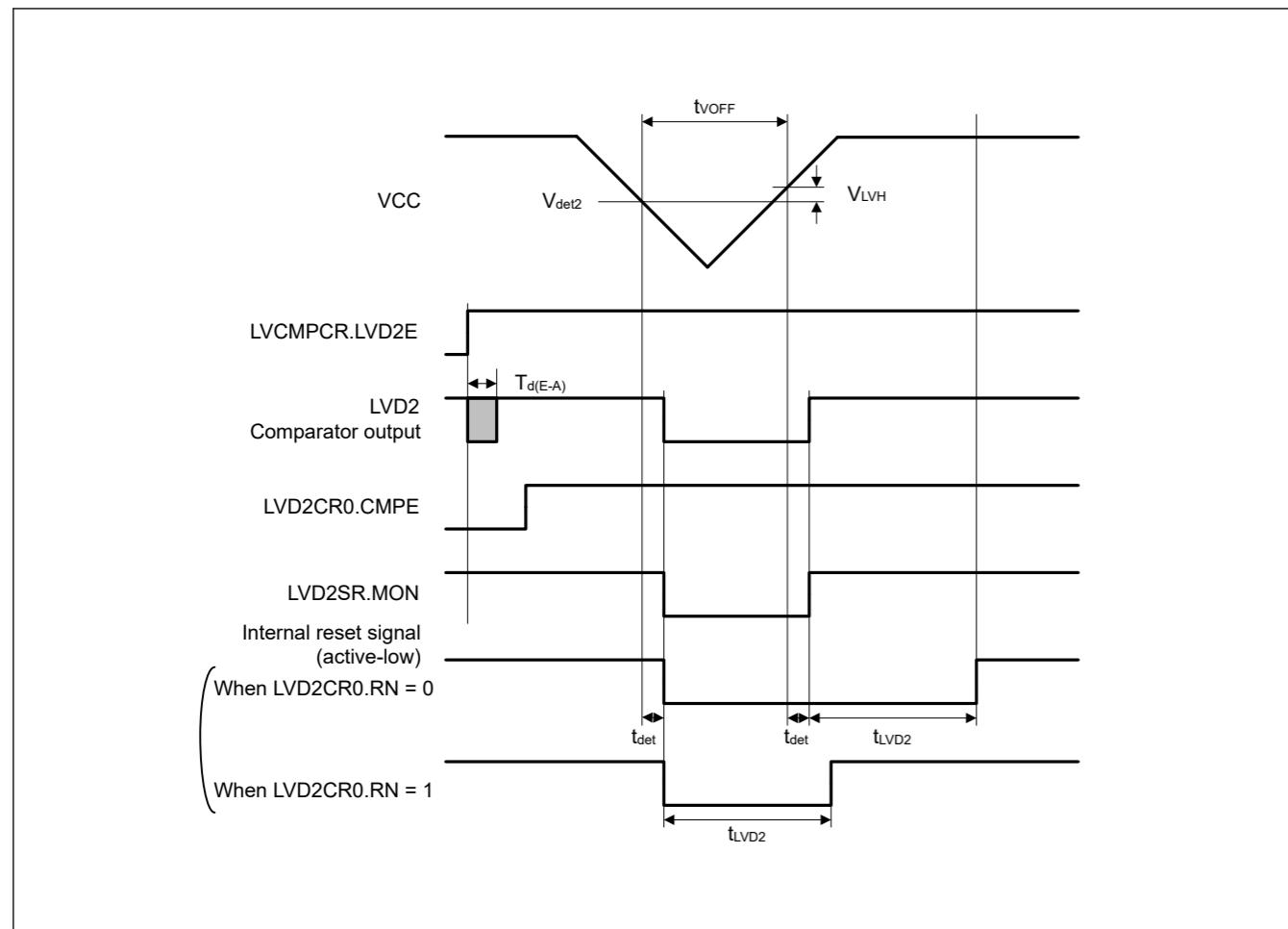


Figure 2.49 上电复位时序

Figure 2.50 Voltage detection circuit timing (V_{det0})Figure 2.50 电压检测电路时序 (V_{det0})Figure 2.51 Voltage detection circuit timing (V_{det1})Figure 2.51 电压检测电路时序 (V_{det1})

Figure 2.52 Voltage detection circuit timing (V_{det2})

2.9 VBATT Characteristics

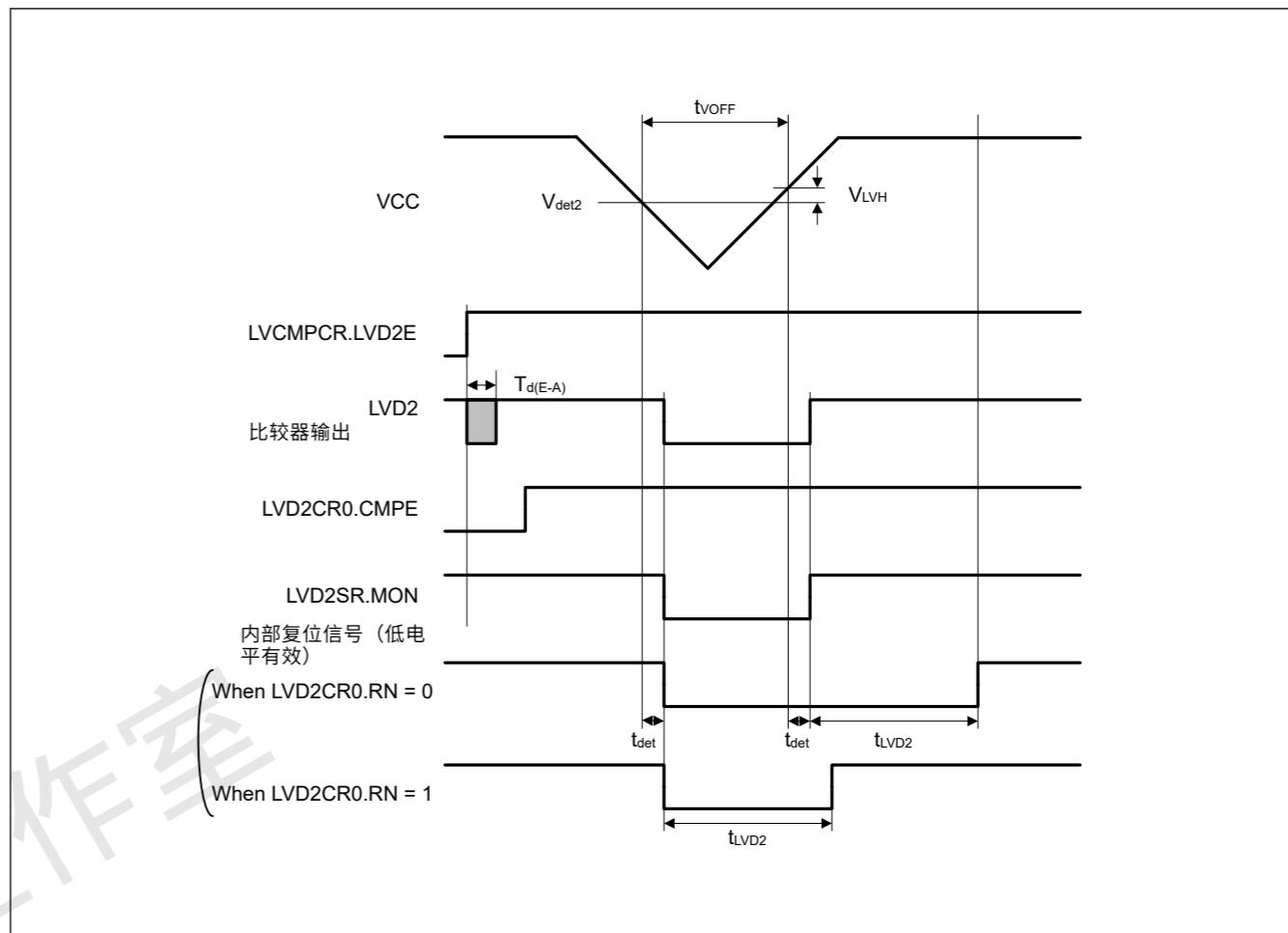
Table 2.39 Battery backup function characteristics

Conditions: $VCC = AVCC0 = VCC_USB = 2.7$ to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, $VBATT = 1.65$ to 3.6 V¹

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|----------------|------|------|------|------|-----------------------------|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.53 |
| Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop | V_{BATTSW} | 2.70 | — | — | V | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | — | — | μs | |
| VBATT low voltage detection level | $V_{battdet}$ | 1.8 | 1.9 | 2.0 | V | Figure 2.54 |
| Minimum VBATT down time | $t_{BATTOFF}$ | 200 | — | — | μs | |
| Response delay | $t_{BATTdet}$ | — | — | 200 | μs | |
| VBATT monitor operation stabilization time (after VBATTMNSEL.R.VBATTMNSEL is changed to 1) | $t_{d(E-A)}$ | — | — | 20 | μs | |
| VBATT current increase (when VBATTMNSEL.R.VBATTMNSEL is 1 compared to the case that VBATTMNSEL.R.VBATTMNSEL is 0) | $I_{VBATTSEL}$ | — | 140 | 350 | nA | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

Note 1. Low CL crystal cannot be used below $VBATT = 1.8$ V.

Figure 2.52 电压检测电路时序 (V_{det2})

2.9 VBATT Characteristics

Table 2.39 电池备份功能特点

Conditions: $VCC = AVCC0 = VCC_USB = 2.7$ to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, $VBATT = 1.65$ to 3.6 V¹

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|---|----------------|------|------|------|------|-----------------------------|
| 切换到备用电池的电压电平 | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.53 |
| VCC压降引起的电源切换下限VBATT电压 | V_{BATTSW} | 2.70 | — | — | V | |
| 启动电源切换的VCC-off周期 | $t_{VOFFBATT}$ | 200 | — | — | μs | |
| VBATT低电压检测电平 | $V_{battdet}$ | 1.8 | 1.9 | 2.0 | V | Figure 2.54 |
| 最短VBATT停机时间 | $t_{BATTOFF}$ | 200 | — | — | μs | |
| 响应延迟 | $t_{BATTdet}$ | — | — | 200 | μs | |
| VBATT监视器运行稳定时间 (VBATTMNSEL.R.VBATTMNSEL变为1后) | $t_{d(E-A)}$ | — | — | 20 | μs | |
| VBATT电流增加 (当与VBATTMNSEL.R.VBATTMNSEL为0的情况相比, VBATTMNSEL.R.VBATTMNSEL为1) | $I_{VBATTSEL}$ | — | 140 | 350 | nA | |

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值($V_{DETBATT}$)的周期。

注1. 低于VBATT=1.8V时不能使用低CL晶振。

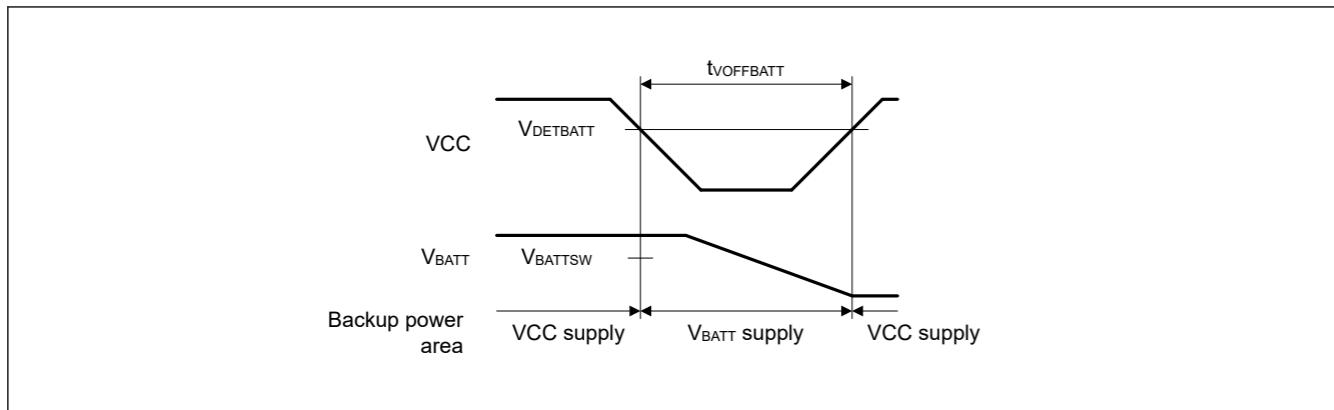


Figure 2.53 Battery backup function characteristics

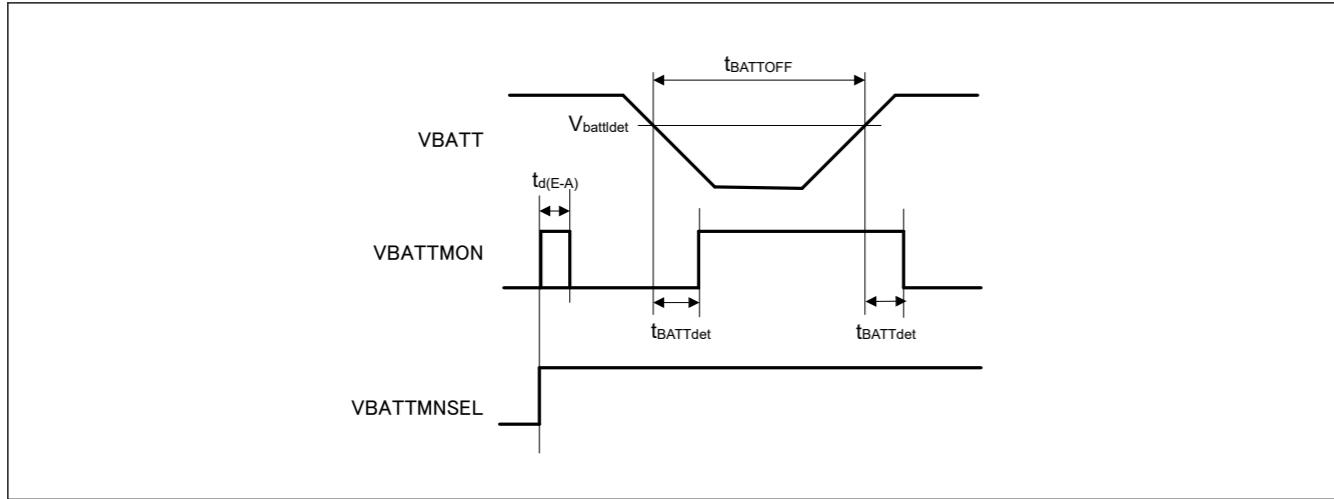


Figure 2.54 Battery backup function characteristics

2.10 Flash Memory Characteristics

2.10.1 Code Flash Memory Characteristics

Table 2.40 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz

Read: FCLK \leq 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz \leq FCLK \leq 50 MHz | | | Unit | Test conditions |
|---|----------|--------------|-------------------|------|----------------------------------|-------------------|------|------|-----------------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| Programming time NPEC \leq 100 times | 128-byte | t_{P128} | — | 0.75 | 13.2 | — | 0.34 | 6.0 | ms |
| | 8-KB | t_{P8K} | — | 49 | 176 | — | 22 | 80 | ms |
| | 32-KB | t_{P32K} | — | 194 | 704 | — | 88 | 320 | ms |
| Programming time NPEC > 100 times | 128-byte | t_{P128} | — | 0.91 | 15.8 | — | 0.41 | 7.2 | ms |
| | 8-KB | t_{P8K} | — | 60 | 212 | — | 27 | 96 | ms |
| | 32-KB | t_{P32K} | — | 234 | 848 | — | 106 | 384 | ms |
| Erasure time NPEC \leq 100 times | 8-KB | t_{E8K} | — | 78 | 216 | — | 43 | 120 | ms |
| | 32-KB | t_{E32K} | — | 283 | 864 | — | 157 | 480 | ms |
| Erasure time NPEC > 100 times | 8-KB | t_{E8K} | — | 94 | 260 | — | 52 | 144 | ms |
| | 32-KB | t_{E32K} | — | 341 | 1040 | — | 189 | 576 | ms |

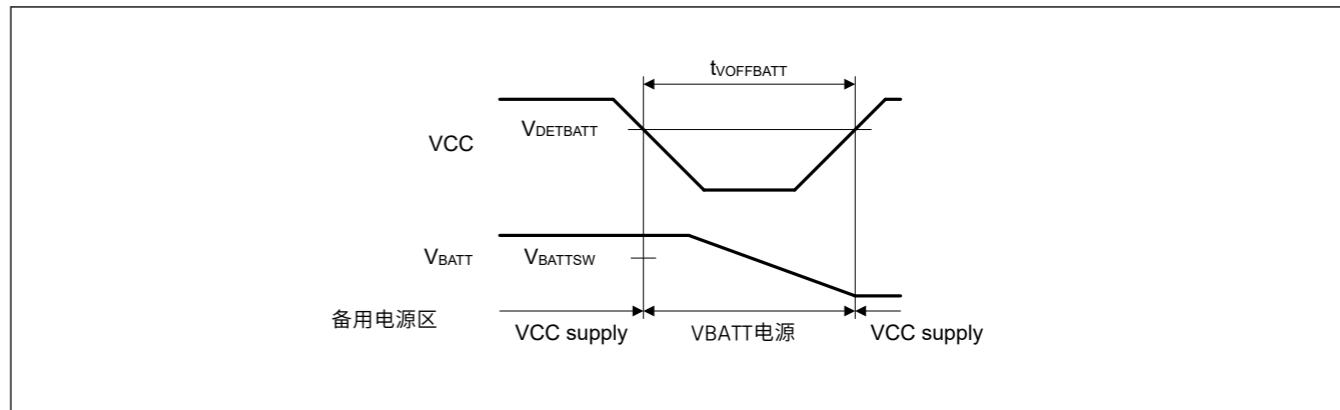


Figure 2.53 电池备份功能特点

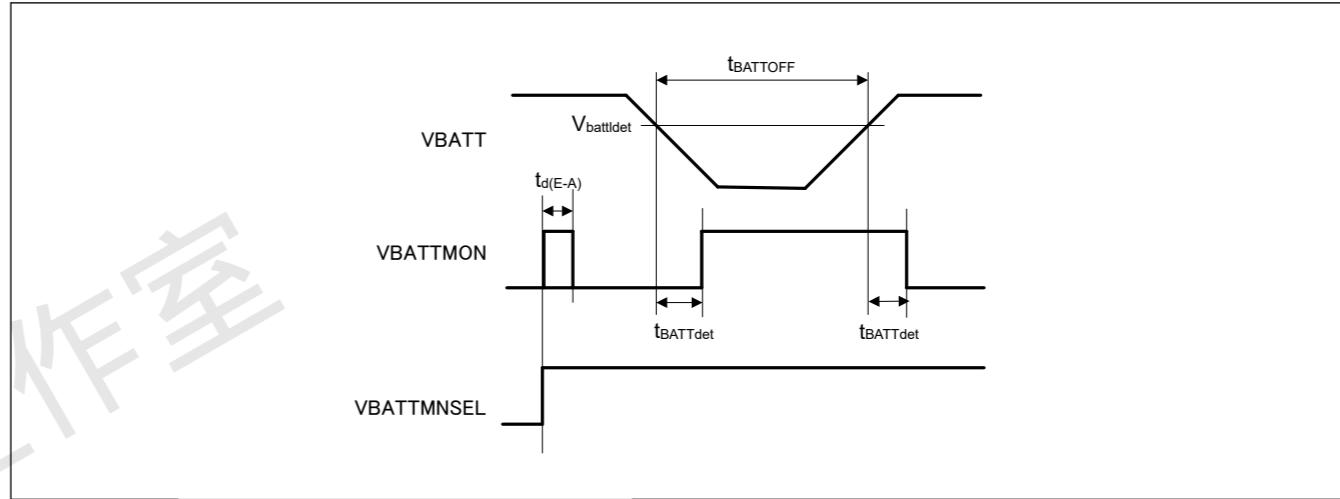


Figure 2.54 电池备份功能特点

2.10 闪存特性

2.10.1 代码闪存特性

Table 2.40 代码闪存特性(1of2)

条件：编程或擦除：FCLK=4至50MHz

读：FCLK \leq 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz \leq FCLK \leq 50 MHz | | | Unit | 测试条件 |
|---------------------------|--------|--------------|-------------------|------|----------------------------------|-------------------|------|------|------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| 编程时间 NPEC \leq 100 次 | 128字节 | t_{P128} | — | 0.75 | 13.2 | — | 0.34 | 6.0 | ms |
| | 8-KB | t_{P8K} | — | 49 | 176 | — | 22 | 80 | ms |
| | 32-KB | t_{P32K} | — | 194 | 704 | — | 88 | 320 | ms |
| 编程时间 NPEC > 100 次 | 128字节 | t_{P128} | — | 0.91 | 15.8 | — | 0.41 | 7.2 | ms |
| | 8-KB | t_{P8K} | — | 60 | 212 | — | 27 | 96 | ms |
| | 32-KB | t_{P32K} | — | 234 | 848 | — | 106 | 384 | ms |
| 擦除时间 NPEC \leq 100 次 | 8-KB | t_{E8K} | — | 78 | 216 | — | 43 | 120 | ms |
| | 32-KB | t_{E32K} | — | 283 | 864 | — | 157 | 480 | ms |
| 擦除时间 NPEC > 100 次 | 8-KB | t_{E8K} | — | 94 | 260 | — | 52 | 144 | ms |
| | 32-KB | t_{E32K} | — | 341 | 1040 | — | 189 | 576 | ms |

Table 2.40 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|--------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|-------|-----------------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| Reprogramming/erasure cycle ^{*4} | N _{PEC} | 10000 ^{*1} | — | — | 10000 ^{*1} | — | — | Times | |
| Suspend delay during programming | t _{SPD} | — | — | 264 | — | — | 120 | μs | |
| Programming resume time | t _{PRT} | — | — | 110 | — | — | 50 | μs | |
| First suspend delay during erasure in suspend priority mode | t _{SESD1} | — | — | 216 | — | — | 120 | μs | |
| Second suspend delay during erasure in suspend priority mode | t _{SESD2} | — | — | 1.7 | — | — | 1.7 | ms | |
| Suspend delay during erasure in erasure priority mode | t _{SEED} | — | — | 1.7 | — | — | 1.7 | ms | |
| First erasing resume time during erasure in suspend priority mode ^{*5} | t _{REST1} | — | — | 1.7 | — | — | 1.7 | ms | |
| Second erasing resume time during erasure in suspend priority mode | t _{REST2} | — | — | 144 | — | — | 80 | μs | |
| Erasing resume time during erasure in erasure priority mode | t _{REET} | — | — | 144 | — | — | 80 | μs | |
| Forced stop command | t _{FD} | — | — | 32 | — | — | 20 | μs | |
| Data hold time ^{*2} | t _{DRP} | 10 ^{*2 *3} | — | — | 10 ^{*2 *3} | — | — | Years | |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Note 6. The reference value at VCC = 3.3V and room temperature.

Table 2.40 代码闪存特性(2of2)

条件：编程或擦除：FCLK=4至50MHz
读：FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | 测试条件 |
|---|--------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|-------|------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| Reprogramming/erasure cycle ^{*4} | N _{PEC} | 10000 ^{*1} | — | — | 10000 ^{*1} | — | — | Times | |
| 编程期间暂停延迟 | t _{SPD} | — | — | 264 | — | — | 120 | μs | |
| 编程恢复时间 | t _{PRT} | — | — | 110 | — | — | 50 | μs | |
| 挂起优先模式下擦除期间的第一个挂起延迟 | t _{SESD1} | — | — | 216 | — | — | 120 | μs | |
| 挂起优先模式下擦除期间的第二挂起延迟 | t _{SESD2} | — | — | 1.7 | — | — | 1.7 | ms | |
| 擦除优先模式下擦除期间的挂起延迟 | t _{SEED} | — | — | 1.7 | — | — | 1.7 | ms | |
| 挂起优先模式擦除期间的第一次擦除恢复时间 ^{*5} | t _{REST1} | — | — | 1.7 | — | — | 1.7 | ms | |
| 挂起优先模式下擦除期间的第二次擦除恢复时间 | t _{REST2} | — | — | 144 | — | — | 80 | μs | |
| 在擦除优先模式下擦除期间擦除恢复时间 | t _{REET} | — | — | 144 | — | — | 80 | μs | |
| 强制停止命令 | t _{FD} | — | — | 32 | — | — | 20 | μs | |
| 数据保持时间 ^{*2} | t _{DRP} | 10 ^{*2 *3} | — | — | 10 ^{*2 *3} | — | — | Years | |

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

注2.这表示在指定范围内执行重新编程时特性的最小值。

注3: 此结果来自可靠性测试。

注4.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次 (n=10 000) 时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。

注6.VCC=3.3V和室温下的参考值。

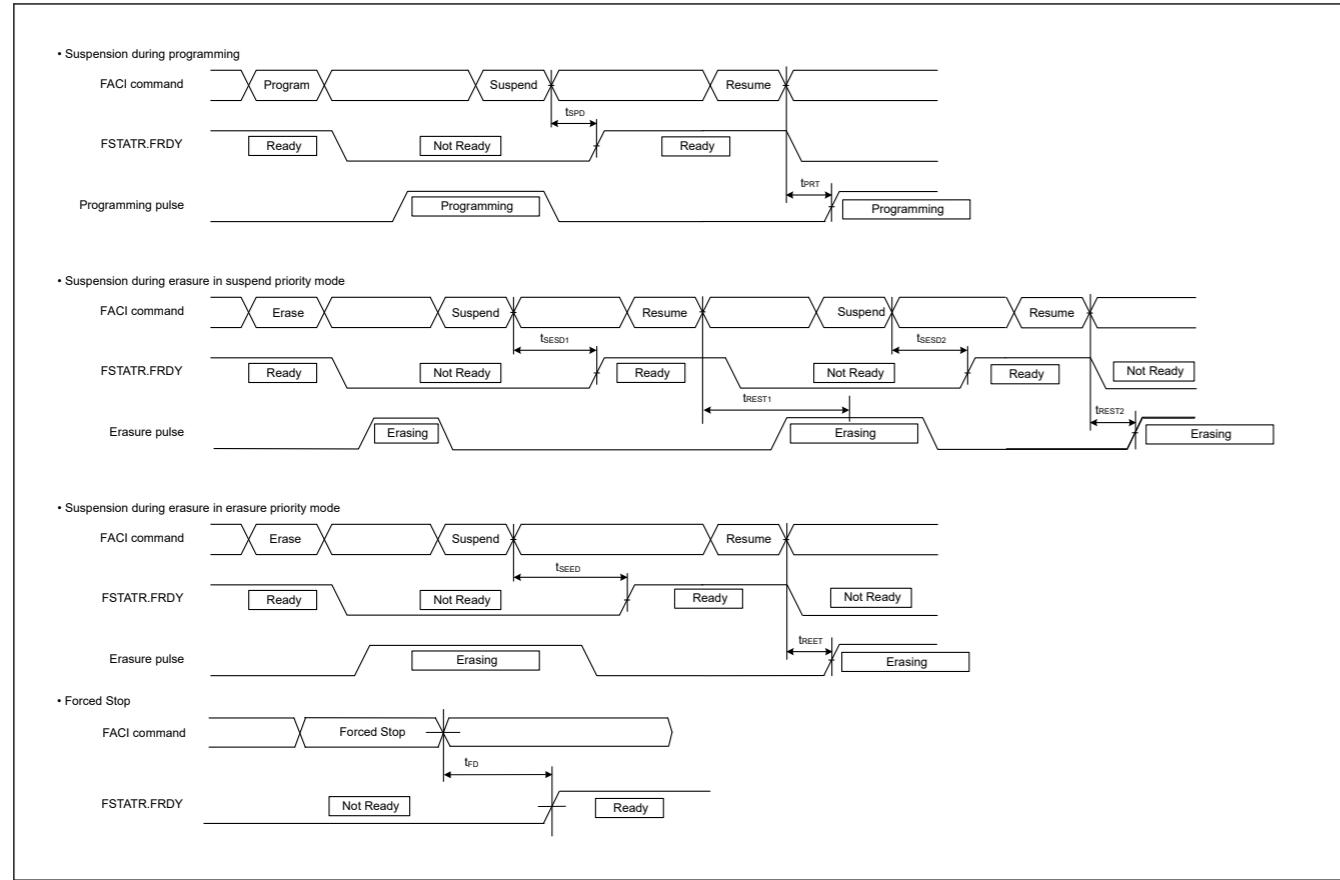


Figure 2.55 Suspension and forced stop timing for flash memory programming and erasure

2.10.2 Data Flash Memory Characteristics

Table 2.41 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz

Read: FCLK \leq 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz \leq FCLK \leq 50 MHz | | | Test conditions |
|---|-------------------|----------------------|-------------------|------|----------------------------------|-------------------|------|-----------------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | |
| Programming time | 4-byte | t _{DP4} | — | 0.36 | 3.8 | — | 0.16 | 1.7 |
| | 8-byte | t _{DP8} | — | 0.38 | 4.0 | — | 0.17 | 1.8 |
| | 16-byte | t _{DP16} | — | 0.42 | 4.5 | — | 0.19 | 2.0 |
| Erasure time | 64-byte | t _{DE64} | — | 3.1 | 18 | — | 1.7 | 10 |
| | 128-byte | t _{DE128} | — | 4.7 | 27 | — | 2.6 | 15 |
| | 256-byte | t _{DE256} | — | 8.9 | 50 | — | 4.9 | 28 |
| Blank check time | 4-byte | t _{DBC4} | — | — | 84 | — | — | 30 |
| Reprogramming/erasure cycle ^{*1} | N _{DPEC} | 125000 ^{*2} | — | — | 125000 ^{*2} | — | — | — |
| Suspend delay during programming | 4-byte | t _{DSPD} | — | — | 264 | — | — | 120 |
| | 8-byte | | — | — | 264 | — | — | 120 |
| | 16-byte | | — | — | 264 | — | — | 120 |
| Programming resume time | | t _{DPRT} | — | — | 110 | — | — | 50 |
| First suspend delay during erasure in suspend priority mode | 64-byte | t _{DSESD1} | — | — | 216 | — | — | 120 |
| | 128-byte | | — | — | 216 | — | — | 120 |
| | 256-byte | | — | — | 216 | — | — | 120 |

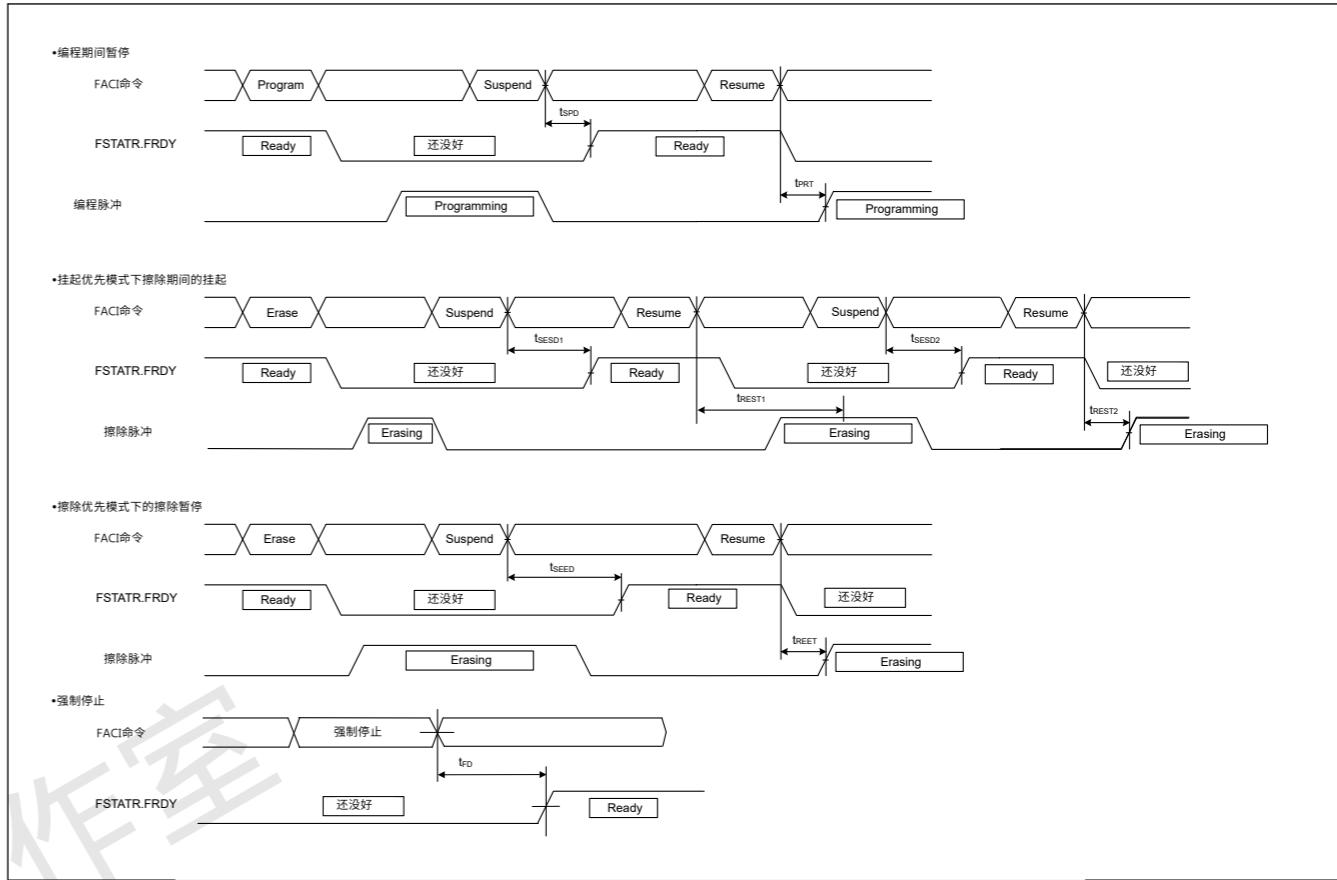


Figure 2.55 闪存编程和擦除的暂停和强制停止时序

2.10.2 数据闪存特性

Table 2.41 数据闪存特性(1of2)

条件：编程或擦除：FCLK=4至50MHz

读：FCLK \leq 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz \leq FCLK \leq 50 MHz | | | 测试条件 |
|---|-------------------|----------------------|------------------|------|----------------------------------|------------------|------|------|
| | | Min | 典型 ^{*6} | 最大值 | Min | 典型 ^{*6} | 最大值 | |
| 编程时间 | 4-byte | t _{DP4} | — | 0.36 | 3.8 | — | 0.16 | 1.7 |
| | 8-byte | t _{DP8} | — | 0.38 | 4.0 | — | 0.17 | 1.8 |
| | 16-byte | t _{DP16} | — | 0.42 | 4.5 | — | 0.19 | 2.0 |
| 擦除时间 | 64-byte | t _{DE64} | — | 3.1 | 18 | — | 1.7 | 10 |
| | 128-byte | t _{DE128} | — | 4.7 | 27 | — | 2.6 | 15 |
| | 256-byte | t _{DE256} | — | 8.9 | 50 | — | 4.9 | 28 |
| 空白检查时间 | 4-byte | t _{DBC4} | — | — | 84 | — | — | 30 |
| Reprogramming/erasure cycle ^{*1} | N _{DPEC} | 125000 ^{*2} | — | — | 125000 ^{*2} | — | — | — |
| 编程期间暂停延迟 | 4-byte | t _{DSPD} | — | — | 264 | — | — | 120 |
| | 8-byte | | — | — | 264 | — | — | 120 |
| | 16-byte | | — | — | 264 | — | — | 120 |
| 编程恢复时间 | | t _{DPRT} | — | — | 110 | — | — | 50 |
| 挂起优先模式下擦除期间的第一个挂起延迟 | 64-byte | t _{DSESD1} | — | — | 216 | — | — | 120 |
| | 128-byte | | — | — | 216 | — | — | 120 |
| | 256-byte | | — | — | 216 | — | — | 120 |

Table 2.41 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|---------|-------------------------------|-------------------|-----|-------------------------------|-------------------|-----|------|-----------------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| Second suspend delay during erasure in suspend priority mode | tDSESD2 | — | — | 300 | — | — | 300 | μs | |
| | | — | — | 390 | — | — | 390 | | |
| | | — | — | 570 | — | — | 570 | | |
| Suspend delay during erasing in erasure priority mode | tDSEED | — | — | 300 | — | — | 300 | μs | |
| | | — | — | 390 | — | — | 390 | | |
| | | — | — | 570 | — | — | 570 | | |
| First erasing resume time during erasure in suspend priority mode ^{*5} | tDREST1 | — | — | 300 | — | — | 300 | μs | |
| Second erasing resume time during erasure in suspend priority mode | tDREST2 | — | — | 126 | — | — | 70 | μs | |
| Erasing resume time during erasure in erasure priority mode | tDREET | — | — | 126 | — | — | 70 | μs | |
| Forced stop command | tFD | — | — | 32 | — | — | 20 | μs | |
| Data hold time ^{*3} | tDRP | 10 ³ ^{*4} | — | — | 10 ³ ^{*4} | — | — | Year | |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 4. This result is obtained from reliability testing.

Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Note 6. The reference value at VCC = 3.3 V and room temperature.

2.10.3 Option Setting Memory Characteristics

Table 2.42 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|------------------|-------------------------------|-------------------|-----|-------------------------------|-------------------|-----|-------|-----------------|
| | | Min | Typ ^{*4} | Max | Min | Typ ^{*4} | Max | | |
| Programming time N _{OPC} ≤ 100 times | t _{OP} | — | 83 | 309 | — | 45 | 162 | ms | |
| Programming time N _{OPC} > 100 times | t _{OP} | — | 100 | 371 | — | 55 | 195 | ms | |
| Reprogramming cycle N _{OPC} | N _{OPC} | 20000 ^{*1} | — | — | 20000 ^{*1} | — | — | Times | |
| Data hold time ^{*2} | t _{DRP} | 10 ² ^{*3} | — | — | 10 ² ^{*3} | — | — | Years | |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reference value at VCC = 3.3 V and room temperature.

2.11 Boundary Scan

Table 2.41 数据闪存特性(2of2)

条件：编程或擦除：FCLK=4至50MHz
读：FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | 测试条件 |
|------------------------------------|------------------|-------------------------------|----------------------|-----|-------------------------------|-----|------|------|------|
| | | Min | 典型 ^{*6} 最大值 | 最小值 | Typ ^{*6} | Max | Unit | | |
| 挂起优先模式下擦除期间的第二挂起延迟 | tDSESD2 | — | — | 300 | — | — | 300 | μs | |
| | | — | — | 390 | — | — | 390 | | |
| | | — | — | 570 | — | — | 570 | | |
| 在擦除优先模式下擦除期间暂停延迟 | tDSEED | — | — | 300 | — | — | 300 | μs | |
| | | — | — | 390 | — | — | 390 | | |
| | | — | — | 570 | — | — | 570 | | |
| 挂起优先模式擦除期间的第一次擦除恢复时间 ^{*5} | tDREST1 | — | — | 300 | — | — | 300 | μs | |
| 挂起优先模式下擦除期间的第二次擦除恢复时间 | tDREST2 | — | — | 126 | — | — | 70 | μs | |
| 在擦除优先模式下擦除期间擦除恢复时间 | tDREET | — | — | 126 | — | — | 70 | μs | |
| 强制停止命令 | t _{FD} | — | — | 32 | — | — | 20 | μs | |
| 数据保持时间 ^{*3} | t _{DRP} | 10 ³ ^{*4} | — | — | 10 ³ ^{*4} | — | — | Year | |

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125 000）时，可以对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

注2.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

注3.这表示在指定范围内执行重新编程时特性的最小值。

注4: 此结果来自可靠性测试。

注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。

注6.VCC=3.3V和室温下的参考值。

2.10.3 选项设置内存特性

Table 2.42 选项设置内存特性

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | 测试条件 |
|----------------------------|------------------|-------------------------------|-------------------|-----|-------------------------------|-------------------|-----|-------|------|
| | | Min | Typ ^{*4} | Max | Min | Typ ^{*4} | Max | | |
| 编程时间N _{OPC} ≤100次 | t _{OP} | — | 83 | 309 | — | 45 | 162 | ms | |
| 编程时间N _{OPC} >100次 | t _{OP} | — | 100 | 371 | — | 55 | 195 | ms | |
| 重编程周期 | N _{OPC} | 20000 ^{*1} | — | — | 20000 ^{*1} | — | — | Times | |
| 数据保持时间 ^{*2} | t _{DRP} | 10 ² ^{*3} | — | — | 10 ² ^{*3} | — | — | Years | |

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

注2.这表示在指定范围内执行重新编程时特性的最小值。

注3: 此结果来自可靠性测试。

注4.VCC=3.3V和室温下的参考值。

2.11 Boundary Scan

2.11 边界扫描

Table 2.43 Boundary scan characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--------------------------------------|--------------|-------------|-----|-----|------|-----------------|--|
| TCK clock cycle time | t_{TCKcyc} | 100 | — | — | ns | Figure 2.56 | |
| TCK clock high pulse width | t_{TCKH} | 45 | — | — | ns | | |
| TCK clock low pulse width | t_{TCKL} | 45 | — | — | ns | | |
| TCK clock rise time | t_{TCKr} | — | — | 5 | ns | | |
| TCK clock fall time | t_{TCKf} | — | — | 5 | ns | | |
| TMS setup time | t_{TMSS} | 20 | — | — | ns | Figure 2.57 | |
| TMS hold time | t_{TMSH} | 20 | — | — | ns | | |
| TDI setup time | t_{TDIS} | 20 | — | — | ns | | |
| TDI hold time | t_{TDIH} | 20 | — | — | ns | | |
| TDO data delay | t_{TDOD} | — | — | 40 | ns | | |
| Boundary scan circuit startup time*1 | T_{BSSTUP} | t_{RESWP} | — | — | — | Figure 2.58 | |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

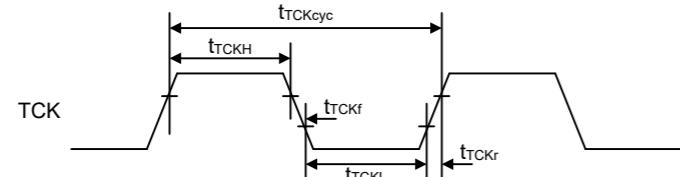


Figure 2.56 Boundary scan TCK timing

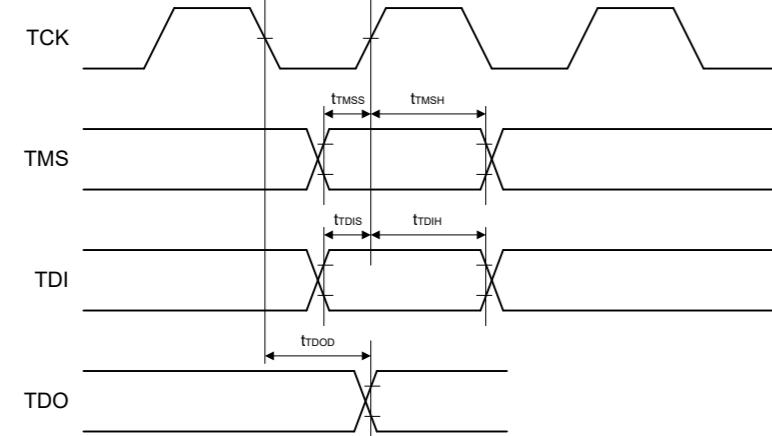


Figure 2.57 Boundary scan input/output timing

Table 2.43 边界扫描特性

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 | |
|--------------|--------------|-------------|-----|-----|------|-------------|--|
| TCK时钟周期时间 | t_{TCKcyc} | 100 | — | — | ns | Figure 2.56 | |
| TCK时钟高脉冲宽度 | t_{TCKH} | 45 | — | — | ns | | |
| TCK时钟低脉冲宽度 | t_{TCKL} | 45 | — | — | ns | | |
| TCK时钟上升时间 | t_{TCKr} | — | — | 5 | ns | | |
| TCK时钟下降时间 | t_{TCKf} | — | — | 5 | ns | | |
| TMS设置时间 | t_{TMSS} | 20 | — | — | ns | Figure 2.57 | |
| TMS保持时间 | t_{TMSH} | 20 | — | — | ns | | |
| TDI建立时间 | t_{TDIS} | 20 | — | — | ns | | |
| TDI保持时间 | t_{TDIH} | 20 | — | — | ns | | |
| TDO数据延迟 | t_{TDOD} | — | — | 40 | ns | | |
| 边界扫描电路启动时间*1 | T_{BSSTUP} | t_{RESWP} | — | — | — | Figure 2.58 | |

注1.在上电复位变为负值之前，边界扫描不起作用。

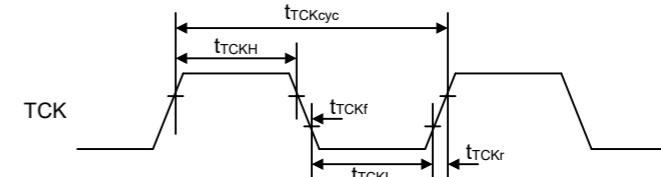


Figure 2.56 边界扫描TCK时序

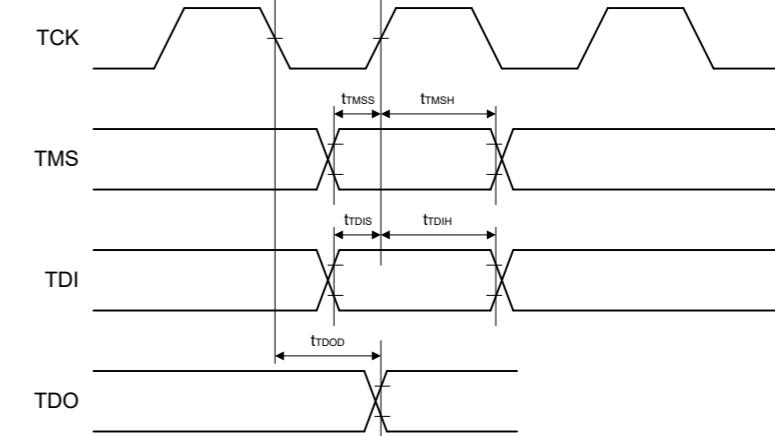


Figure 2.57 边界扫描输入输出时序

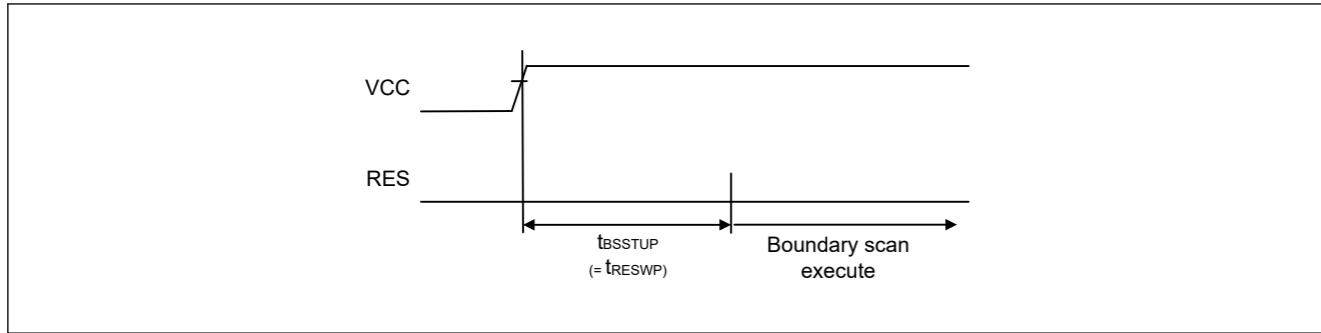


Figure 2.58 Boundary scan circuit startup timing

2.12 Joint Test Action Group (JTAG)

Table 2.44 JTAG

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time | t_{TCKcyc} | 40 | — | — | ns | Figure 2.59 |
| TCK clock high pulse width | t_{TCKH} | 15 | — | — | ns | |
| TCK clock low pulse width | t_{TCKL} | 15 | — | — | ns | |
| TCK clock rise time | t_{TCKr} | — | — | 5 | ns | |
| TCK clock fall time | t_{TCKf} | — | — | 5 | ns | |
| TMS setup time | t_{TMSS} | 8 | — | — | ns | |
| TMS hold time | t_{TMSH} | 8 | — | — | ns | |
| TDI setup time | t_{TDIS} | 8 | — | — | ns | |
| TDI hold time | t_{TDIH} | 8 | — | — | ns | |
| TDO data delay time | t_{TDOD} | — | — | 20 | ns | |

Figure 2.58 Boundary scan circuit startup timing

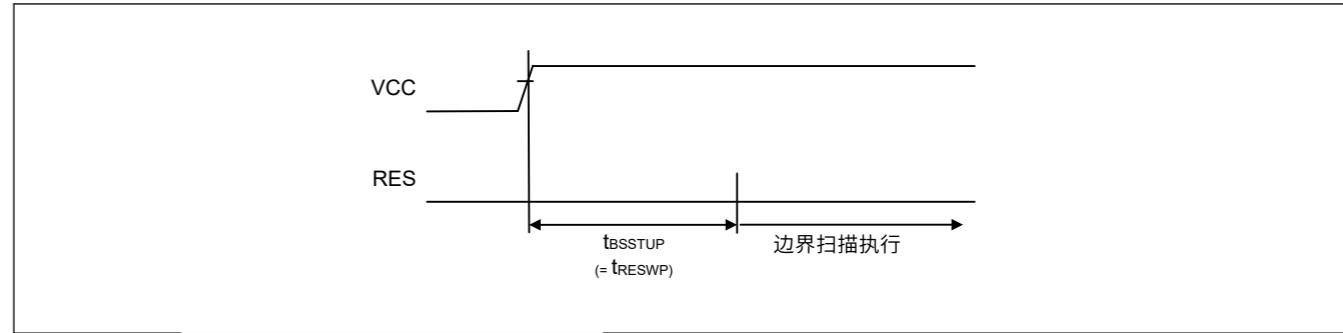


Figure 2.58 边界扫描电路启动时序

2.12 联合测试行动组(JTAG)

Table 2.44 JTAG

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 |
|------------|--------------|-----|-----|-----|------|-------------|
| TCK时钟周期时间 | t_{TCKcyc} | 40 | — | — | ns | Figure 2.59 |
| TCK时钟高脉冲宽度 | t_{TCKH} | 15 | — | — | ns | |
| TCK时钟低脉冲宽度 | t_{TCKL} | 15 | — | — | ns | |
| TCK时钟上升时间 | t_{TCKr} | — | — | 5 | ns | |
| TCK时钟下降时间 | t_{TCKf} | — | — | 5 | ns | |
| TMS设置时间 | t_{TMSS} | 8 | — | — | ns | |
| TMS保持时间 | t_{TMSH} | 8 | — | — | ns | |
| TDI建立时间 | t_{TDIS} | 8 | — | — | ns | |
| TDI保持时间 | t_{TDIH} | 8 | — | — | ns | |
| TDO数据延迟时间 | t_{TDOD} | — | — | 20 | ns | |

Figure 2.58 边界扫描电路启动时序

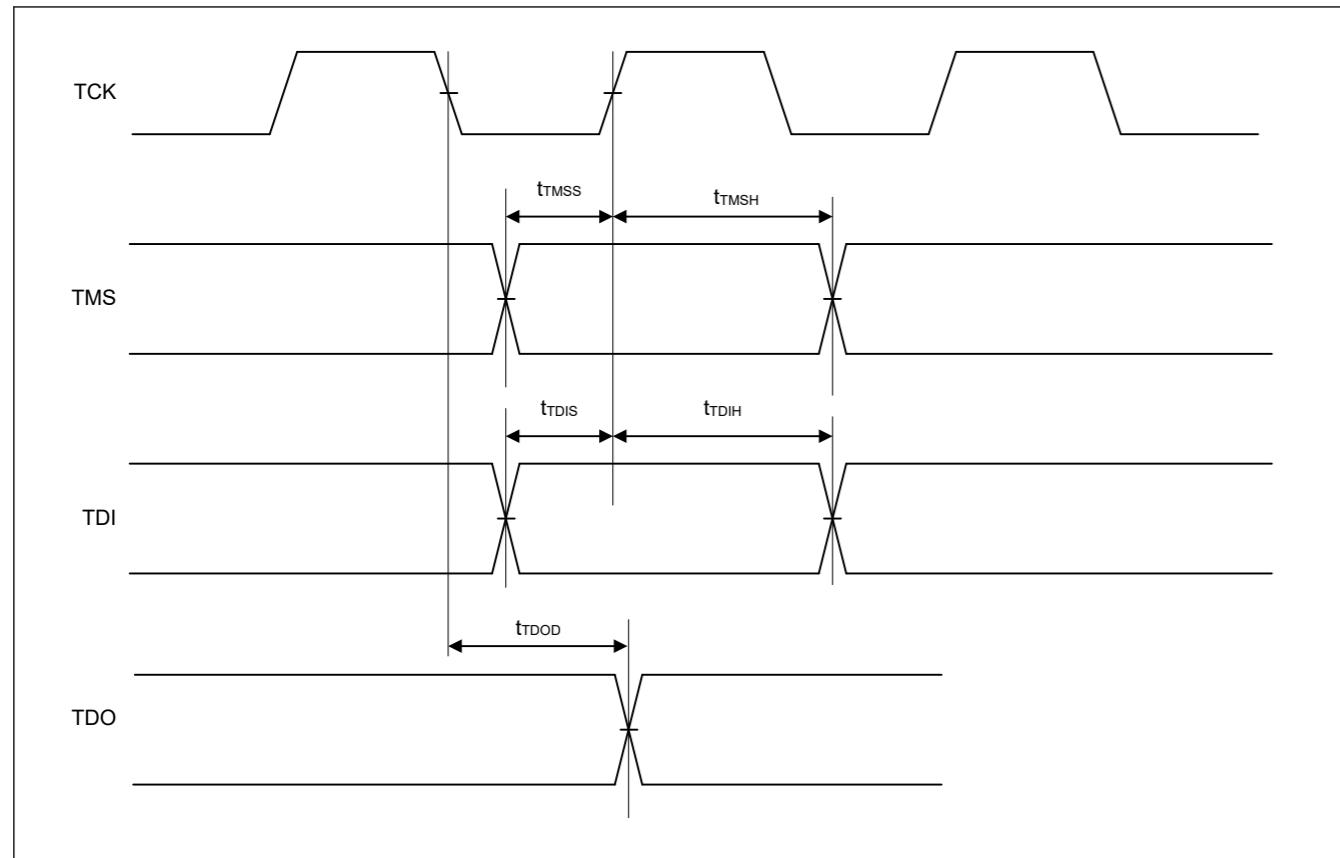


Figure 2.60 JTAG input/output timing

2.13 Serial Wire Debug (SWD)

Table 2.45 SWD

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|------------------------------|----------------------|-----|-----|-----|------|-----------------|--|
| SWCLK clock cycle time | t _{SWCKcyc} | 40 | — | — | ns | Figure 2.61 | |
| SWCLK clock high pulse width | t _{SWCKH} | 15 | — | — | ns | | |
| SWCLK clock low pulse width | t _{SWCKL} | 15 | — | — | ns | | |
| SWCLK clock rise time | t _{SWCKr} | — | — | 5 | ns | | |
| SWCLK clock fall time | t _{SWCKf} | — | — | 5 | ns | Figure 2.62 | |
| SWDIO setup time | t _{SWDS} | 8 | — | — | ns | | |
| SWDIO hold time | t _{SWDH} | 8 | — | — | ns | | |
| SWDIO data delay time | t _{SWDD} | 2 | — | 28 | ns | | |

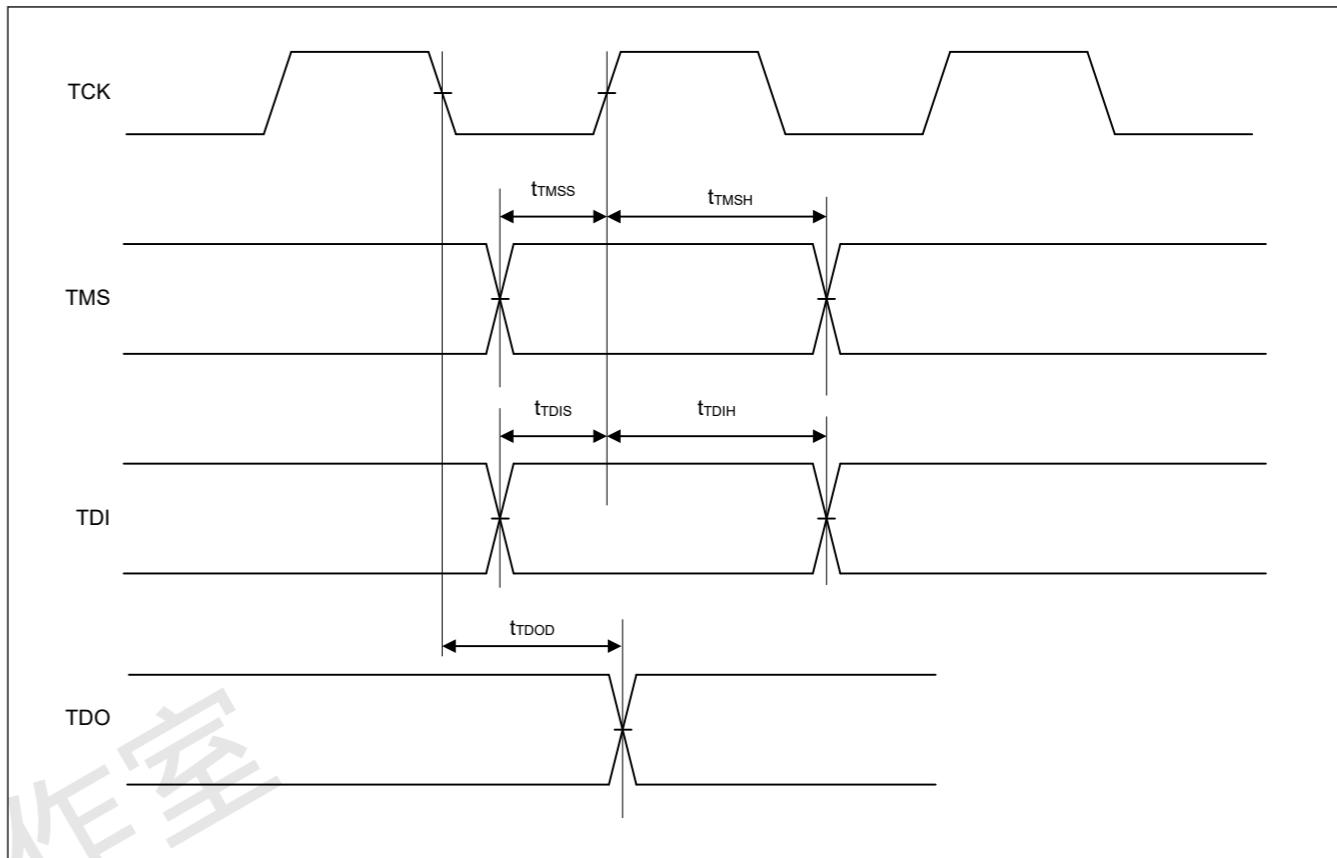


Figure 2.60 JTAG input/output timing

2.13 串行线调试(SWD)

Table 2.45 SWD

| Parameter | Symbol | Min | Typ | Max | Unit | 测试条件 | |
|--------------|----------------------|-----|-----|-----|------|-------------|--|
| SWCLK时钟周期时间 | t _{SWCKcyc} | 40 | — | — | ns | Figure 2.61 | |
| SWCLK时钟高脉冲宽度 | t _{SWCKH} | 15 | — | — | ns | | |
| SWCLK时钟低脉冲宽度 | t _{SWCKL} | 15 | — | — | ns | | |
| SWCLK时钟上升时间 | t _{SWCKr} | — | — | 5 | ns | | |
| SWCLK时钟下降时间 | t _{SWCKf} | — | — | 5 | ns | Figure 2.62 | |
| SWDIO设置时间 | t _{SWDS} | 8 | — | — | ns | | |
| SWDIO保持时间 | t _{SWDH} | 8 | — | — | ns | | |
| SWDIO数据延迟时间 | t _{SWDD} | 2 | — | 28 | ns | | |

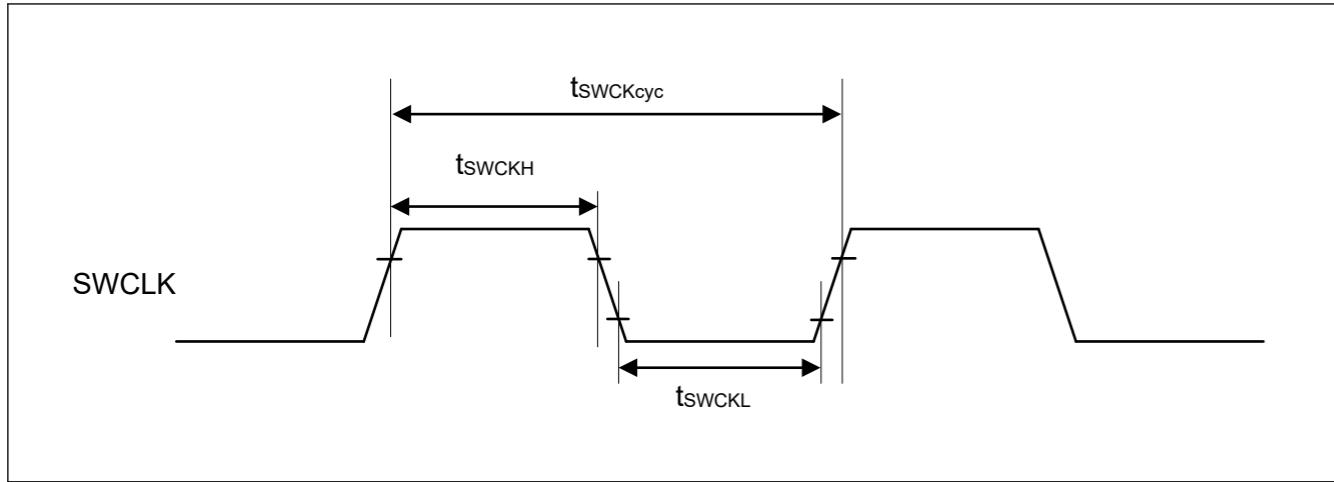


Figure 2.61 SWD SWCLK timing

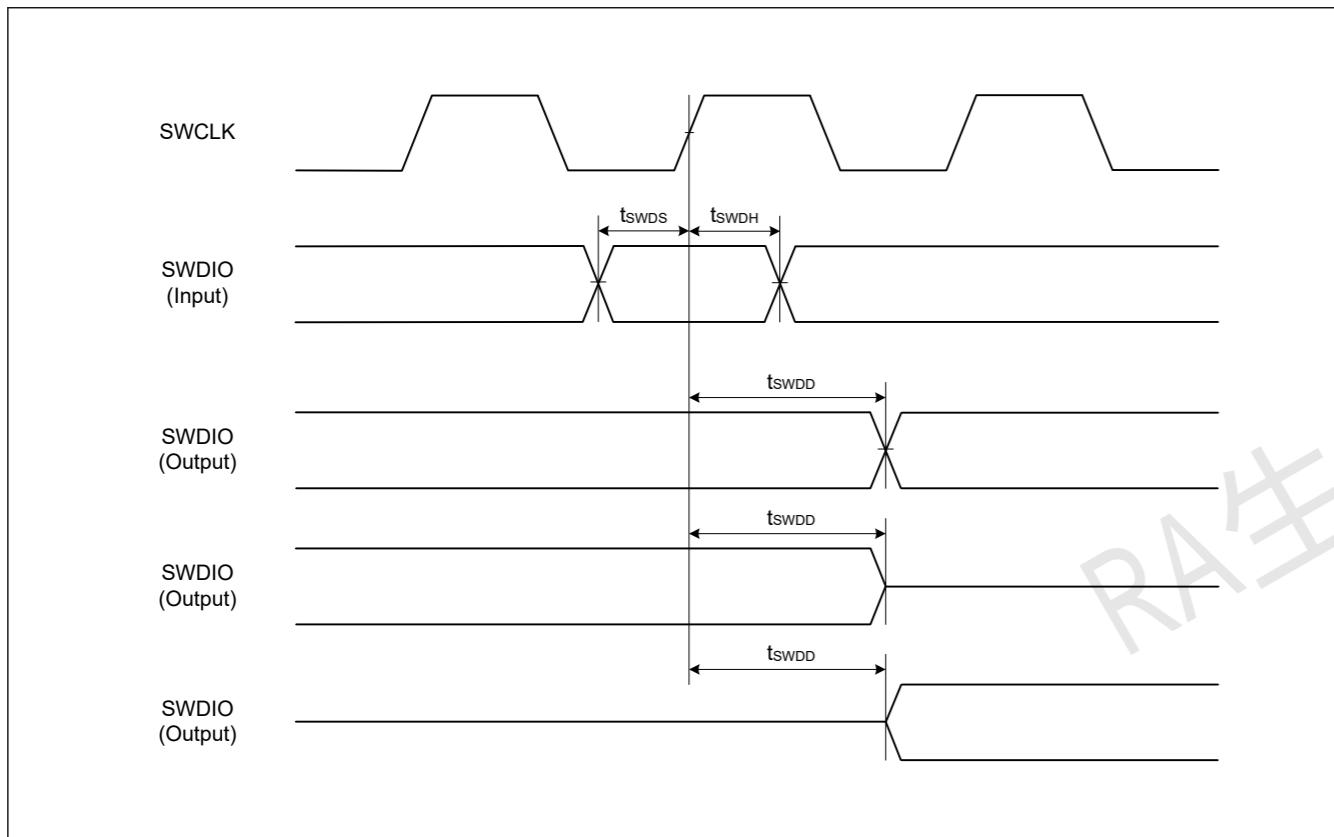


Figure 2.62 SWD input/output timing

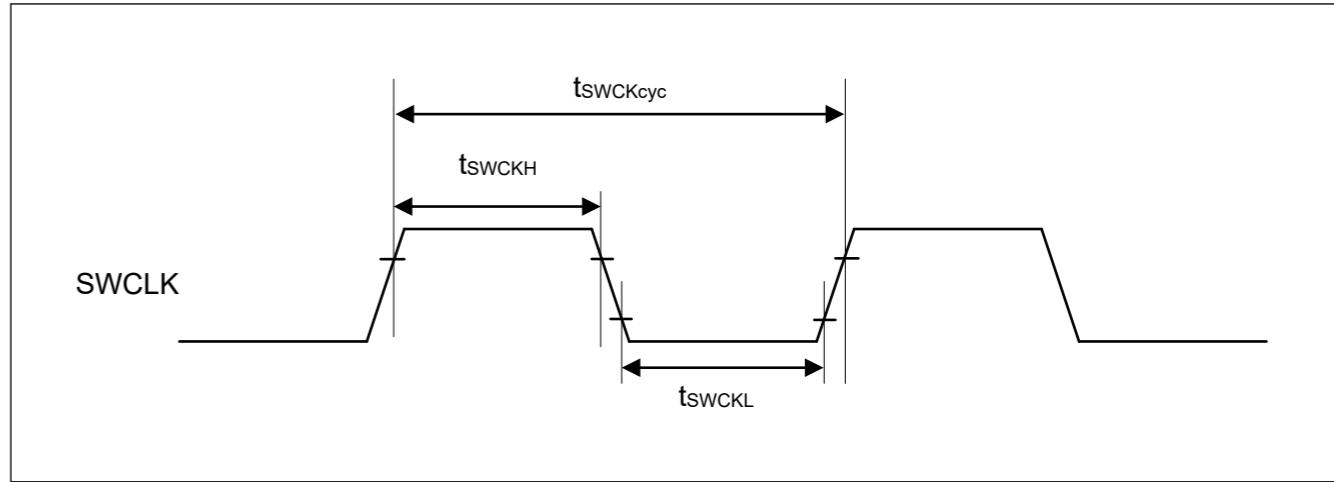


Figure 2.61 SWD SWCLK timing

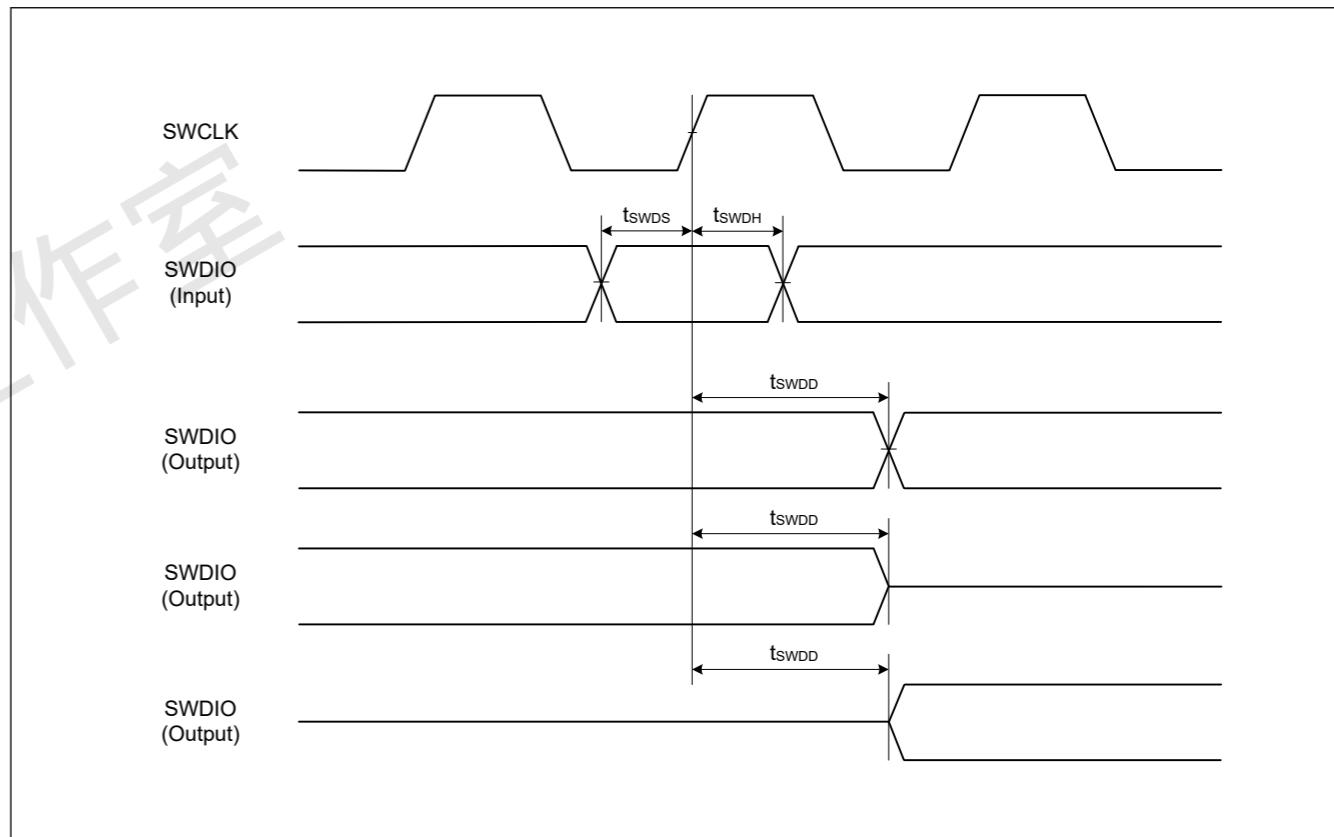


Figure 2.62 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

| Function | Pin function | Reset | Software Standby mode | Deep Software Standby mode | After Deep Software Standby mode is canceled (return to startup mode) | |
|----------|-------------------------|---------|---|----------------------------|---|-------------------------|
| | | | | | IOKEEP = 0 | IOKEEP = 1 ¹ |
| Mode | MD | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| JTAG | TCK/TMS/TDI | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| | TDO | output | Keep-O | Keep | TDO output | Keep |
| IRQ | IRQx | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | IRQx-DS | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| AGT | AGTIOOn | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | AGTIOOn (n=1,3) | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| SCI | RXD0 | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| IIC | SCLn/SDAn | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| USBFS | USB_OVRCURx | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | USB_OVRCURx-DS/USB_VBUS | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| | USB_DP/USB_DM | Hi-Z | Keep-O ⁴ | Keep ³ | Hi-Z | Keep |
| RTC | RTClCx | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| | RTCOUT | Hi-Z | [RTCOUT selected] RTCOUT output | Keep | Hi-Z | Keep |
| CLKOUT | CLKOUT | Hi-Z | [CLKOUT selected] CLKOUT output | Keep | Hi-Z | Keep |
| DAC | DAn | Hi-Z | [DAn output (DAOE = 1)] D/A output retained | Keep | Hi-Z | Keep |
| Others | — | Hi-Z | Keep-O | Keep | Hi-Z | Keep |

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

- Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
 Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
 Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
 Note 4. Input is enabled while the pin is used as an input pin.

Appendix 1. 每种处理模式下的端口状态

| Function | 引脚功能 | Reset | 软件待机模式 | 深度软件待机模式 | 取消深度软件待机模式后（返回启动模式） | |
|----------|-------------------------|---------|---|-------------------|---------------------|-------------------------|
| | | | | | IOKEEP = 0 | IOKEEP = 1 ¹ |
| Mode | MD | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| JTAG | TCK/TMS/TDI | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| | TDO | output | Keep-O | Keep | TDO输出 | Keep |
| IRQ | IRQx | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | IRQx-DS | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| AGT | AGTIOOn | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | AGTIOOn (n=1,3) | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| SCI | RXD0 | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| IIC | SCLn/SDAn | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| USBFS | USB_OVRCURx | Hi-Z | Keep-O ² | Keep | Hi-Z | Keep |
| | USB_OVRCURx-DS/USB_VBUS | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| | USB_DP/USB_DM | Hi-Z | Keep-O ⁴ | Keep ³ | Hi-Z | Keep |
| RTC | RTClCx | Hi-Z | Keep-O ² | Keep ³ | Hi-Z | Keep |
| | RTCOUT | Hi-Z | [RTCOUT selected] RTCOUT output | Keep | Hi-Z | Keep |
| CLKOUT | CLKOUT | Hi-Z | [CLKOUT selected] CLKOUT output | Keep | Hi-Z | Keep |
| DAC | DAn | Hi-Z | [DAn output (DAOE = 1)] D/A output retained | Keep | Hi-Z | Keep |
| Others | — | Hi-Z | Keep-O | Keep | Hi-Z | Keep |

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: 输出引脚保留其先前的值。输入引脚变为高阻抗。
保持: 在软件待机模式期间保持引脚状态。

- 注1.保持IO端口状态直到DPSBYCR.IOKEEP位被清除为0。
 注2.如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
 注3.如果引脚被指定为深度软件待机取消源，则启用输入。
 注4.当引脚用作输入引脚时，输入被启用。

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

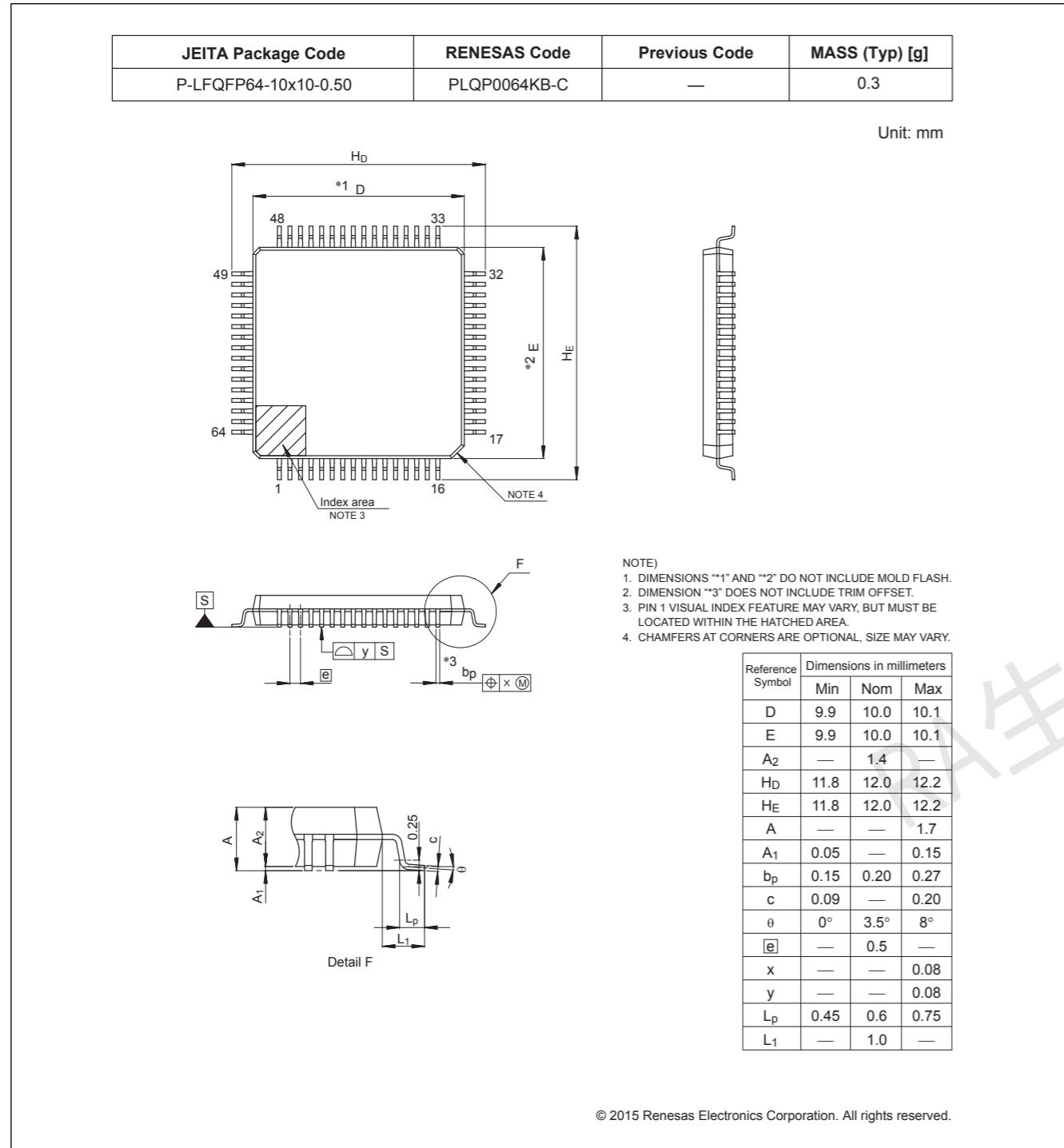


Figure 2.1 LQFP 64-pin

Appendix 2. 包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨电子的“封装”中电子公司网站。

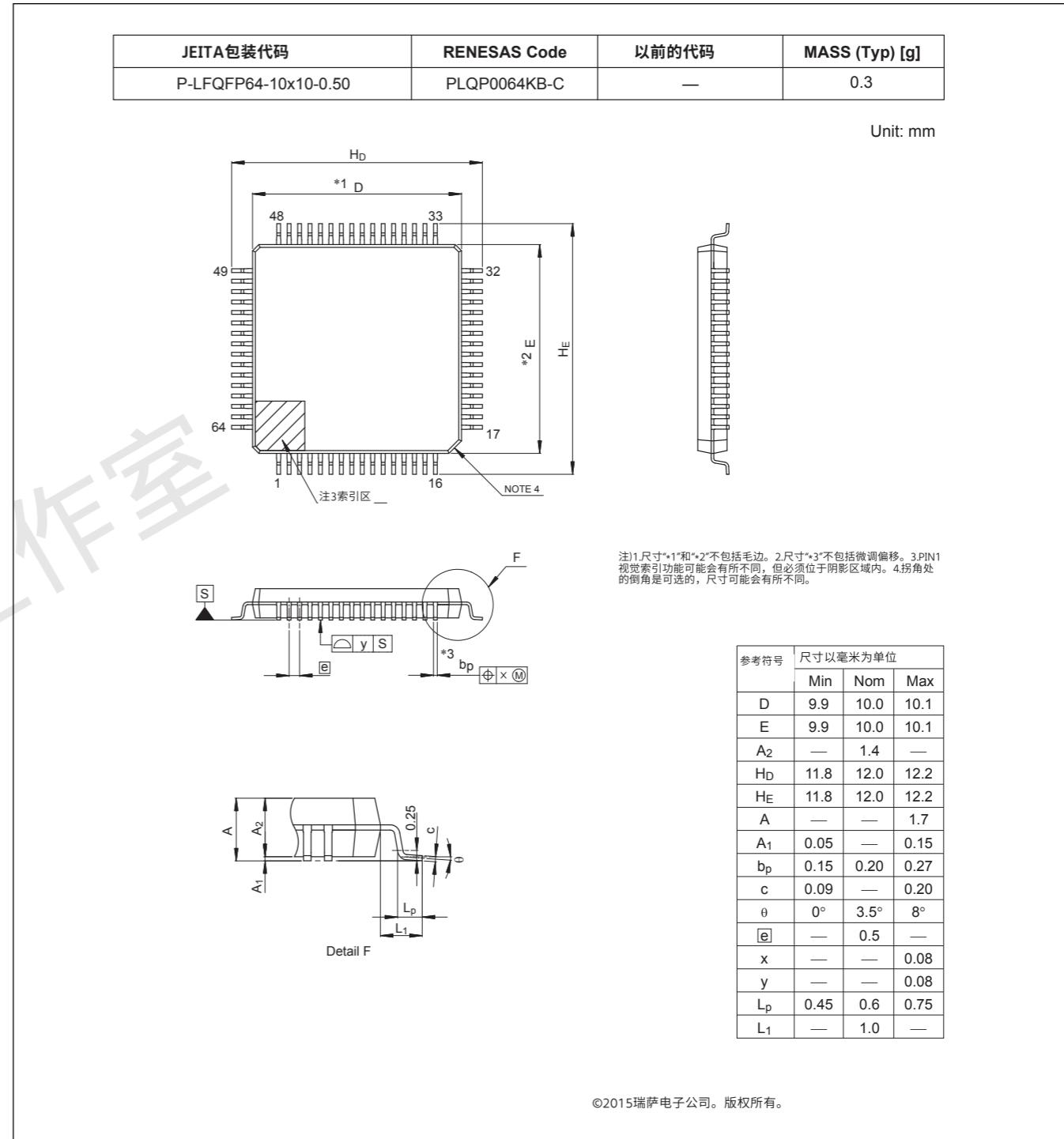


Figure 2.1 LQFP 64-pin

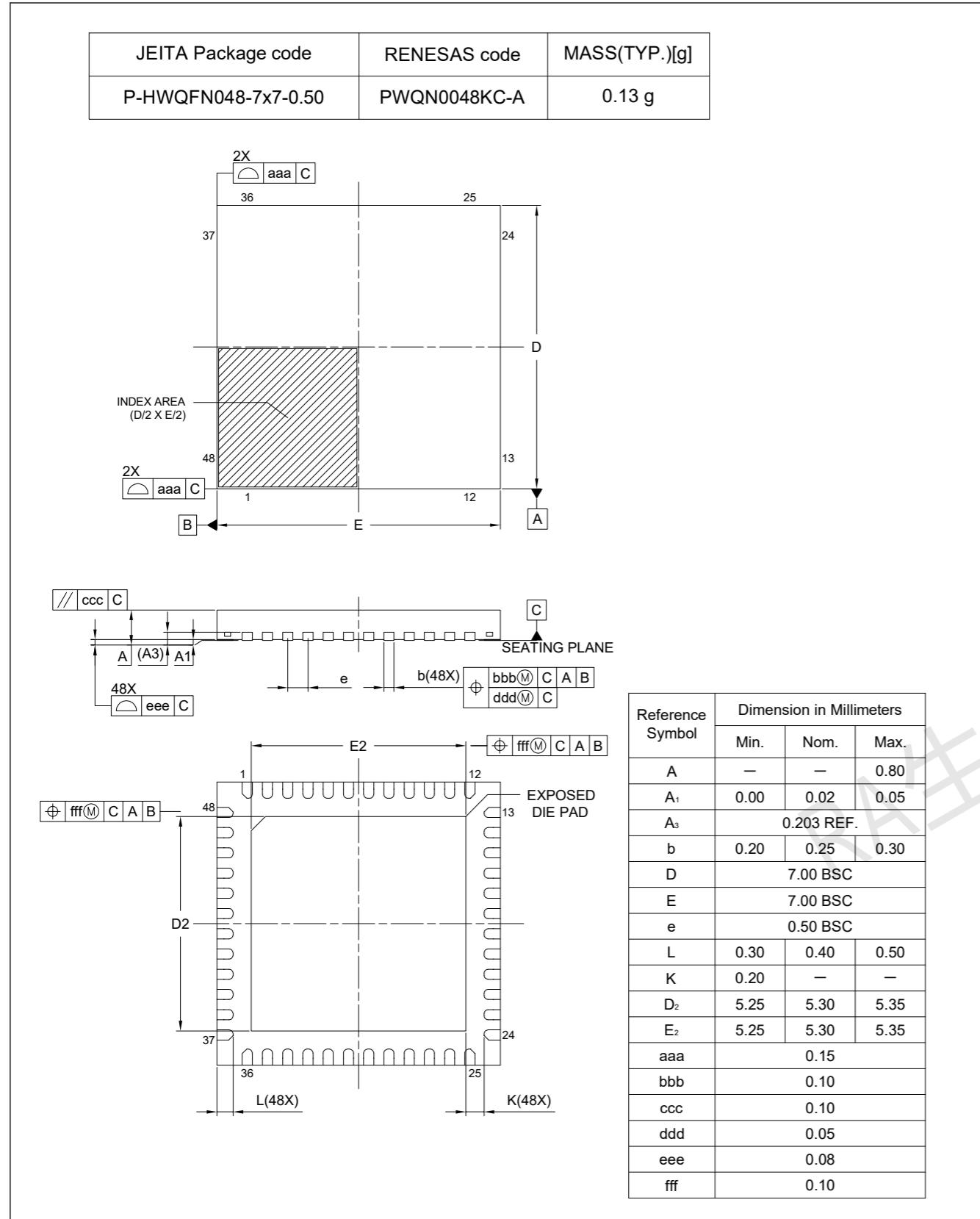


Figure 2.2 QFN 48-pin

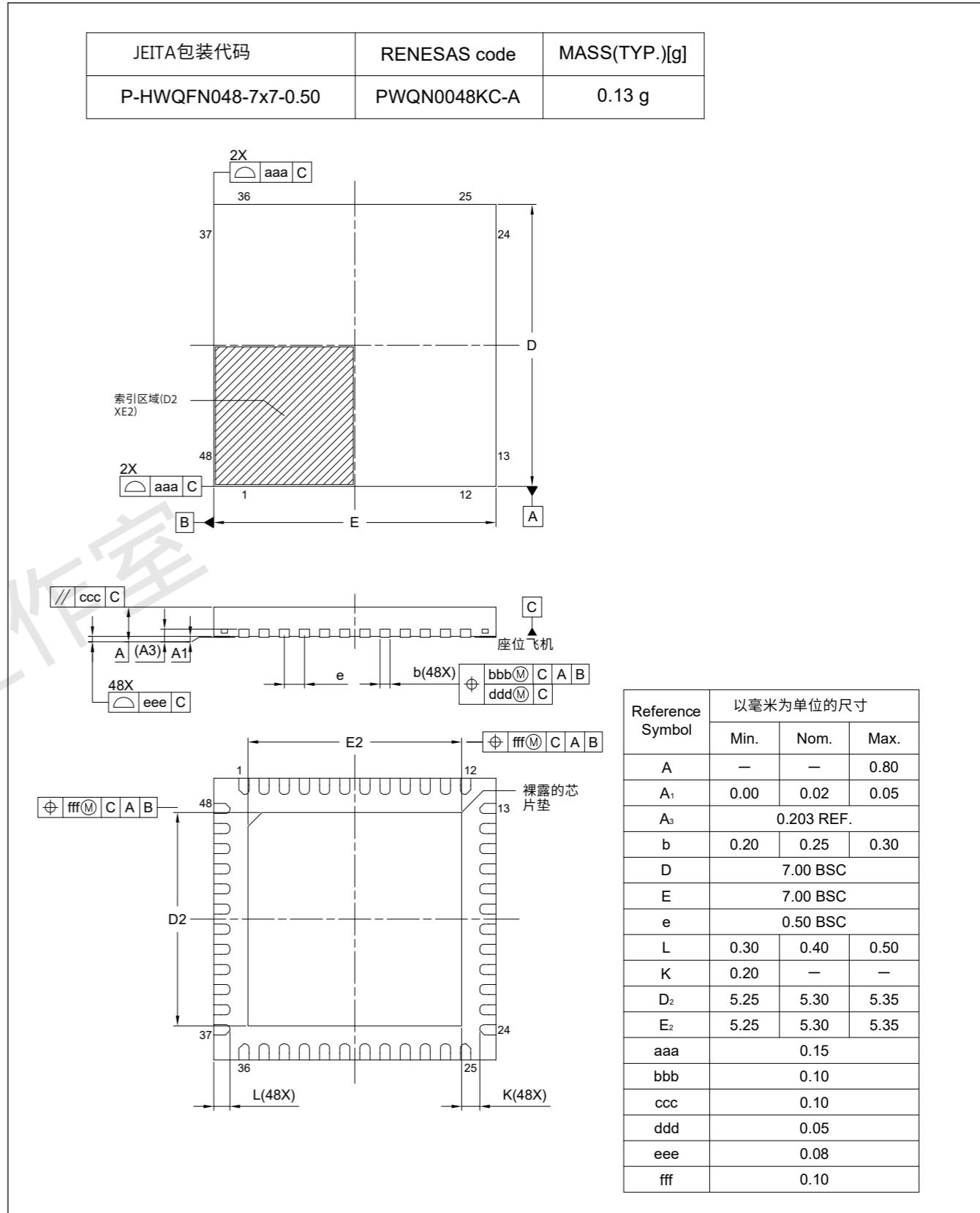


Figure 2.2 QFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. [Table 3.1](#) shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

| Name | Description | Base address |
|--------|--|--------------|
| RMPU | Renesas Memory Protection Unit | 0x4000_0000 |
| TZF | TrustZone Filter | 0x4000_0E00 |
| SRAM | SRAM Control | 0x4000_2000 |
| BUS | BUS Control | 0x4000_3000 |
| DMAC0 | Direct memory access controller 0 | 0x4000_5000 |
| DMAC1 | Direct memory access controller 1 | 0x4000_5040 |
| DMAC2 | Direct memory access controller 2 | 0x4000_5080 |
| DMAC3 | Direct memory access controller 3 | 0x4000_50C0 |
| DMAC4 | Direct memory access controller 4 | 0x4000_5100 |
| DMAC5 | Direct memory access controller 5 | 0x4000_5140 |
| DMAC6 | Direct memory access controller 6 | 0x4000_5180 |
| DMAC7 | Direct memory access controller 7 | 0x4000_51C0 |
| DMA | DMAC Module Activation | 0x4000_5200 |
| DTC | Data Transfer Controller | 0x4000_5400 |
| ICU | Interrupt Controller | 0x4000_6000 |
| CPSCU | CPU System Security Control Unit | 0x4000_8000 |
| DBG | Debug Function | 0x400_1B000 |
| FCACHE | Flash Cache | 0x400_1C100 |
| SYSC | System Control | 0x4001_E000 |
| PORT0 | Port 0 Control Registers | 0x4008_0000 |
| PORT1 | Port 1 Control Registers | 0x4008_0020 |
| PORT2 | Port 2 Control Registers | 0x4008_0040 |
| PORT3 | Port 3 Control Registers | 0x4008_0060 |
| PORT4 | Port 4 Control Registers | 0x4008_0080 |
| PORT5 | Port 5 Control Registers | 0x4008_00A0 |
| PFS | Pmn Pin Function Control Register | 0x4008_0800 |
| ELC | Event Link Controller | 0x4008_2000 |
| RTC | Realtime Clock | 0x4008_3000 |
| IWDT | Independent Watchdog Timer | 0x4008_3200 |
| WDT | Watchdog Timer | 0x4008_3400 |
| CAC | Clock Frequency Accuracy Measurement Circuit | 0x4008_3600 |
| MSTP | Module Stop Control A, B, C, D | 0x4008_4000 |
| POEG | Port Output Enable Module for GPT | 0x4008_A000 |
| USBFS | USB 2.0 FS Module | 0x4009_0000 |
| IIC0 | Inter-Integrated Circuit 0 | 0x4009_F000 |

Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址和访问周期。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of2)

| Name | Description | 基址 |
|--------|----------------------------|-------------|
| RMPU | 瑞萨内存保护单元 | 0x4000_0000 |
| TZF | TrustZone Filter | 0x4000_0E00 |
| SRAM | SRAM Control | 0x4000_2000 |
| BUS | 总线控制 | 0x4000_3000 |
| DMAC0 | 直接内存访问控制器0 | 0x4000_5000 |
| DMAC1 | 直接内存访问控制器1 | 0x4000_5040 |
| DMAC2 | 直接内存访问控制器2 | 0x4000_5080 |
| DMAC3 | 直接内存访问控制器3 | 0x4000_50C0 |
| DMAC4 | 直接内存访问控制器4 | 0x4000_5100 |
| DMAC5 | 直接内存访问控制器5 | 0x4000_5140 |
| DMAC6 | 直接内存访问控制器6 | 0x4000_5180 |
| DMAC7 | 直接内存访问控制器7 | 0x4000_51C0 |
| DMA | DMAC模块激活 | 0x4000_5200 |
| DTC | 数据传输控制器 | 0x4000_5400 |
| ICU | 中断控制器 | 0x4000_6000 |
| CPSCU | CPU系统安全控制单元 | 0x4000_8000 |
| DBG | 调试功能 | 0x400_1B000 |
| FCACHE | 闪存缓存 | 0x400_1C100 |
| SYSC | 系统控制 | 0x4001_E000 |
| PORT0 | 端口0控制寄存器 | 0x4008_0000 |
| PORT1 | 端口1控制寄存器 | 0x4008_0020 |
| PORT2 | 端口2控制寄存器 | 0x4008_0040 |
| PORT3 | 端口3控制寄存器 | 0x4008_0060 |
| PORT4 | 端口4控制寄存器 | 0x4008_0080 |
| PORT5 | 端口5控制寄存器 | 0x4008_00A0 |
| PFS | Pmn引脚功能控制寄存器 | 0x4008_0800 |
| ELC | 事件链接控制器 | 0x4008_2000 |
| RTC | 实时时钟 | 0x4008_3000 |
| IWDT | 独立看门狗定时器 | 0x4008_3200 |
| WDT | 看门狗定时器 | 0x4008_3400 |
| CAC | 时钟频率精度测量电路 | 0x4008_3600 |
| MSTP | 模块停止控制A、B、C、D | 0x4008_4000 |
| POEG | GPT端口输出使能模块 | 0x4008_A000 |
| USBFS | USB2.0FS模块 | 0x4009_0000 |
| IIC0 | Inter-Integrated Circuit 0 | 0x4009_F000 |

Table 3.1 Peripheral base address (2 of 2)

| Name | Description | Base address |
|--------|--|--------------|
| IIC0WU | Inter-Integrated Circuit 0 Wake-up Unit | 0x4009_F014 |
| CAN0 | CAN0 Module | 0x400A_8000 |
| PSCU | Peripheral Security Control Unit | 0x400E_0000 |
| AGT0 | Low Power Asynchronous General purpose Timer 0 | 0x400E_8000 |
| AGT1 | Low Power Asynchronous General purpose Timer 1 | 0x400E_8100 |
| AGT2 | Low Power Asynchronous General purpose Timer 2 | 0x400E_8200 |
| AGT3 | Low Power Asynchronous General purpose Timer 3 | 0x400E_8300 |
| AGT5 | Low Power Asynchronous General purpose Timer 5 | 0x400E_8500 |
| CRC | CRC Calculator | 0x4010_8000 |
| DOC | Data Operation Circuit | 0x4010_9000 |
| SCI0 | Serial Communication Interface 0 | 0x4011_8000 |
| SCI3 | Serial Communication Interface 3 | 0x4011_8300 |
| SCI4 | Serial Communication Interface 4 | 0x4011_8400 |
| SCI9 | Serial Communication Interface 9 | 0x4011_8900 |
| SPI0 | Serial Peripheral Interface 0 | 0x4011_A000 |
| SCE9 | Secure Cryptographic Engine | 0x4016_1000 |
| GPT321 | General PWM 32-Bit Timer 1 | 0x4016_9100 |
| GPT322 | General PWM 32-Bit Timer 2 | 0x4016_9200 |
| GPT164 | General PWM 16-Bit Timer 4 | 0x4016_9400 |
| GPT165 | General PWM 16-Bit Timer 5 | 0x4016_9500 |
| ADC120 | 12bit A/D Converter 0 | 0x4017_0000 |
| DAC12 | 12-bit D/A converter | 0x4017_1000 |
| FLAD | Data Flash | 0x407F_C000 |
| FACI | Flash Application Command Interface | 0x407F_E000 |
| QSPI | Quad-SPI | 0x6400_0000 |

Note: Name = Peripheral name

Description = Peripheral functionality

Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Table 3.1 外设基址 (2个中的2个)

| Name | Description | 基址 |
|--------|-----------------------|-------------|
| IIC0WU | 内部集成电路0唤醒单元 | 0x4009_F014 |
| CAN0 | CAN0 Module | 0x400A_8000 |
| PSCU | 外围安全控制单元 | 0x400E_0000 |
| AGT0 | 低功耗异步通用定时器0 | 0x400E_8000 |
| AGT1 | 低功耗异步通用定时器1 | 0x400E_8100 |
| AGT2 | 低功耗异步通用定时器2 | 0x400E_8200 |
| AGT3 | 低功耗异步通用定时器3 | 0x400E_8300 |
| AGT5 | 低功耗异步通用定时器5 | 0x400E_8500 |
| CRC | CRC Calculator | 0x4010_8000 |
| DOC | 数据运算电路 | 0x4010_9000 |
| SCI0 | 串行通讯接口0 | 0x4011_8000 |
| SCI3 | 串行通讯接口3 | 0x4011_8300 |
| SCI4 | 串行通讯接口4 | 0x4011_8400 |
| SCI9 | 串行通讯接口9 | 0x4011_8900 |
| SPI0 | 串行外设接口0 | 0x4011_A000 |
| SCE9 | 安全加密引擎 | 0x4016_1000 |
| GPT321 | 通用PWM32位定时器1 | 0x4016_9100 |
| GPT322 | 通用PWM32位定时器2 | 0x4016_9200 |
| GPT164 | 通用PWM16位定时器4 | 0x4016_9400 |
| GPT165 | 通用PWM16位定时器5 | 0x4016_9500 |
| ADC120 | 12bit A/D Converter 0 | 0x4017_0000 |
| DAC12 | 12-bit D/A converter | 0x4017_1000 |
| FLAD | 数据闪存 | 0x407F_C000 |
| FACI | Flash应用命令接口 | 0x407F_E000 |
| QSPI | Quad-SPI | 0x6400_0000 |

Note: 名称=外设名称

描述=外围功能

基址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

- 寄存器按相关模块分组。
- 访问周期数是指基于指定参考时钟的周期数。
- 在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。
- IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。
 - 当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。
 - 当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。
 - 写访问周期数是指非缓冲写访问所获得的周期数。

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

| Peripherals | Address | | Number of access cycles | | | | | |
|--|-------------|-------------|-------------------------|-----------------|---------------------------|----------------------|------------|--|
| | | | ICLK = PCLK | | ICLK > PCLK ^{*1} | | Cycle Unit | Related function |
| From | To | Read | Write | Read | Write | | | |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 2 | 2 | 2 | 2 | ICLK | Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller |
| CPSCU, DBG, FCACHE | 0x4000_8000 | 0x4001_CFFF | 4 | 3 | 4 | 3 | ICLK | CPU System Security Control Unit, Debug Function, Flash Cache |
| SYSC | 0x4001_E000 | 0x4001_E3FF | 5 | 4 | 5 | 4 | ICLK | System Control |
| SYSC | 0x4001_E400 | 0x4001_E5FF | 9 | 8 | 5 to 8 | 5 to 8 | PCLKB | System Control |
| PORTn, PFS | 0x4008_0000 | 0x4008_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Port n Control Registers, Pmn Pin Function Control Register |
| ELC, RTC, IWDT, WDT, CAC | 0x4008_2000 | 0x4008_3FFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit |
| MSTP | 0x4008_4000 | 0x4008_4FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Module Stop Control |
| POEG | 0x4008_A000 | 0x4008_AFFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Port Output Enable Module for GPT |
| USBFS | 0x4009_0000 | 0x4009_3FFF | 6 | 5 | 3 to 6 | 3 to 5 | PCLKB | USB 2.0 FS Module |
| USBFS | 0x4009_4000 | 0x4009_4FFF | 4 | 3 | 1 to 4 | 1 to 3 | PCLKB | USB 2.0 FS Module |
| IICn, IIC0WU | 0x4009_2000 | 0x4009_FFFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit |
| CANn | 0x400A_8000 | 0x400A_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | CANn Module |
| PSCU | 0x400E_0000 | 0x400E_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Peripheral Security Control Unit |
| AGTn | 0x400E_8000 | 0x400E_8FFF | 7 | 4 | 5 to 7 | 2 to 4 | PCLKB | Low Power Asynchronous General purpose Timer n |
| CRC, DOC | 0x4010_8000 | 0x4010_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | CRC Calculator, Data Operation Circuit |
| SCI ⁿ | 0x4011_8000 | 0x4011_8FFF | 5 ^{*2} | 4 ^{*2} | 2 to 5 ^{*2} | 2 to 4 ^{*2} | PCLKA | Serial Communication Interface n |
| SPI ⁿ | 0x4011_A000 | 0x4011_AFFF | 5 ^{*3} | 4 ^{*3} | 2 to 5 ^{*3} | 2 to 4 ^{*3} | PCLKA | Serial Peripheral Interface n |
| SCE9 | 0x4016_1000 | 0x4016_1FFF | 6 | 4 | 3 to 6 | 2 to 4 | PCLKA | Secure Cryptographic Engine |
| GPT32n, GPT16n, GPT_OPS | 0x4016_9000 | 0x4016_9FFF | 7 | 4 | 4 to 7 | 2 to 4 | PCLKA | General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller |

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 访问周期(1of3)

| Peripherals | Address | | 访问周期数 | | | | | |
|--|-------------|-------------|-----------------|-----------------|---------------------------|----------------------|------------|--|
| | | | ICLK = PCLK | | ICLK > PCLK ^{*1} | | Cycle Unit | 相关功能 |
| From | To | Read | Write | Read | Write | | | |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 2 | 2 | 2 | 2 | ICLK | 瑞萨内存保护单元、TrustZone过滤器、SRAM控制，总线控制、直接内存访问控制器n、DMAC模块激活、DTC控制寄存器、中断控制器 |
| CPSCU, DBG, FCACHE | 0x4000_8000 | 0x4001_CFFF | 4 | 3 | 4 | 3 | ICLK | CPU系统安全控制单元，调试功能，闪存 |
| SYSC | 0x4001_E000 | 0x4001_E3FF | 5 | 4 | 5 | 4 | ICLK | 系统控制 |
| SYSC | 0x4001_E400 | 0x4001_E5FF | 9 | 8 | 5 to 8 | 5 to 8 | PCLKB | 系统控制 |
| PORTn, PFS | 0x4008_0000 | 0x4008_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | 端口n控制寄存器，Pmn引脚功能控制Register |
| ELC, RTC, IWDT, WDT, CAC | 0x4008_2000 | 0x4008_3FFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | 事件链接控制器，实时时钟，独立看门狗定时器，看门狗定时器，时钟频率Accuracy测量电路 |
| MSTP | 0x4008_4000 | 0x4008_4FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | 模块停止控制 |
| POEG | 0x4008_A000 | 0x4008_AFFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | 端口输出使能GPT模块 |
| USBFS | 0x4009_0000 | 0x4009_3FFF | 6 | 5 | 3 to 6 | 3 to 5 | PCLKB | USB2.0FS模块 |
| USBFS | 0x4009_4000 | 0x4009_4FFF | 4 | 3 | 1 to 4 | 1 to 3 | PCLKB | USB2.0FS模块 |
| IICn, IIC0WU | 0x4009_2000 | 0x4009_FFFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | 集成电路间n, 集成电路间0唤醒单元 |
| CANn | 0x400A_8000 | 0x400A_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | CANn模块 |
| PSCU | 0x400E_0000 | 0x400E_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | 外围安全控制单元 |
| AGTn | 0x400E_8000 | 0x400E_8FFF | 7 | 4 | 5 to 7 | 2 to 4 | PCLKB | 低电量Asynchronous一般用途Timer n |
| CRC, DOC | 0x4010_8000 | 0x4010_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | CRC计算器, 数据运算电路 |
| SCI ⁿ | 0x4011_8000 | 0x4011_8FFF | 5 ^{*2} | 4 ^{*2} | 2 to 5 ^{*2} | 2 to 4 ^{*2} | PCLKA | 串行通信Interface n |
| SPI ⁿ | 0x4011_A000 | 0x4011_AFFF | 5 ^{*3} | 4 ^{*3} | 2 to 5 ^{*3} | 2 to 4 ^{*3} | PCLKA | 串行外设Interface n |
| SCE9 | 0x4016_1000 | 0x4016_1FFF | 6 | 4 | 3 to 6 | 2 to 4 | PCLKA | 安全密钥学Engine |
| GPT32n, GPT16n, GPT_OPS | 0x4016_9000 | 0x4016_9FFF | 7 | 4 | 4 to 7 | 2 to 4 | PCLKA | 通用PWM32位定时器n, 通用PWM16位定时器n, 输出相位开关控制器 |

Table 3.2 Access cycles (2 of 3)

| Peripherals | Address | | Number of access cycles | | | | | |
|---------------|-------------|-------------|-------------------------|---------------------|---------------------------|---------------------|------------|---|
| | | | ICLK = PCLK | | ICLK > PCLK ^{*1} | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| ADC12n, DAC12 | 0x4017_0000 | 0x4017_2FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | 12bit A/D Converter n, 12-bit D/A converter |
| QSPI | 0x6400_0000 | 0x6400_000F | 5 | 14 to ^{*4} | 2 to 5 | 14 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0010 | 0x6400_0013 | 25 to ^{*4} | 6 to ^{*4} | 25 to ^{*4} | 5 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0014 | 0x6400_0037 | 5 | 14 to ^{*4} | 2 to 5 | 14 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0804 | 0x6400_0807 | 4 | 3 | 1 to 4 | 1 to 3 | PCLKA | Quad-SPI |

Table 3.2 Access cycles (3 of 3)

| Peripherals | Address | | Number of access cycles | | | | | |
|-------------|-------------|-------------|-------------------------|-------|---------------------------|--------|------------|---|
| | | | ICLK = FCLK | | ICLK > FCLK ^{*1} | | Cycle Unit | Related function |
| | From | To | Read | Write | Read | Write | | |
| FLAD, FACI | 0x407F_C000 | 0x407F_EFFF | 3 | 3 | 2 to 3 | 2 to 3 | FCLK | Data Flash, Flash Application Command Interface |

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Note 4. The access cycles depend on the QSPI bus cycles.

Table 3.2 访问周期 (2个, 共3个)

| Peripherals | Address | | 访问周期数 | | | | | |
|---------------|-------------|-------------|---------------------|---------------------|---------------------------|---------------------|------------|---|
| | | | ICLK = PCLK | | ICLK > PCLK ^{*1} | | Cycle Unit | 相关功能 |
| | From | To | Read | Write | Read | Write | | |
| ADC12n, DAC12 | 0x4017_0000 | 0x4017_2FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | 12bit A/D Converter n, 12-bit D/A converter |
| QSPI | 0x6400_0000 | 0x6400_000F | 5 | 14 to ^{*4} | 2 to 5 | 14 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0010 | 0x6400_0013 | 25 to ^{*4} | 6 to ^{*4} | 25 to ^{*4} | 5 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0014 | 0x6400_0037 | 5 | 14 to ^{*4} | 2 to 5 | 14 to ^{*4} | PCLKA | Quad-SPI |
| QSPI | 0x6400_0804 | 0x6400_0807 | 4 | 3 | 1 to 4 | 1 to 3 | PCLKA | Quad-SPI |

Table 3.2 访问周期 (3个, 共3个)

| Peripherals | Address | | 访问周期数 | | | | | |
|-------------|-------------|-------------|-------------|-------|---------------------------|--------|------------|---------------|
| | | | ICLK = FCLK | | ICLK > FCLK ^{*1} | | Cycle Unit | 相关功能 |
| | From | To | Read | Write | Read | Write | | |
| FLAD, FACI | 0x407F_C000 | 0x407F_EFFF | 3 | 3 | 2 to 3 | 2 to 3 | FCLK | 数据闪存、闪存应用命令接口 |

注1.若PCLK或FCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2。5是1到3。

注2.访问16位寄存器（FTDRHL, FRDRHL, FCR, FDR, LSR和CDR）时，访问时间比中所示的值多2个周期
表3.2. 访问8位寄存器（包括FTDRH, FTDRL, FRDRH和FRDRL）时，访问周期如下图所示：
Table 3.2.

注3.访问32位寄存器（SPDR）时，访问比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。
注4.访问周期取决于QSPI总线周期。

Appendix 4. Related Documents

| Component | Document Type | Description |
|-------------------------|----------------------------------|--|
| Microcontrollers | Data sheet | Features, overview, and electrical characteristics of the MCU |
| | User's Manual: Hardware | MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions |
| | Application Notes | Technical notes, board design guidelines, and software migration information |
| | Technical Update (TU) | Preliminary reports on product specifications such as restriction and errata |
| Software | User's Manual: Software | Command set, API reference and programming information |
| | Application Notes | Project files, guidelines for software programming, and application examples to develop embedded software applications |
| Tools & Kits, Solutions | User's Manual: Development Tools | User's manuals and quick start guides for developing embedded software applications with Software Packages, Development Kits, Starter Kits, Promotion Kits, Product Examples, and Application Examples |
| | Quick Start Guide | |
| | Application Notes | Project files, guidelines for software programming, and application examples to develop embedded software applications |

Appendix 4. 相关文件

| Component | 文件类型 | Description |
|------------------|-------------------------|---|
| Microcontrollers | 数据表 | MCU的特性、概述和电气特性 |
| | User's Manual: Hardware | MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述 |
| | 应用笔记 | 技术说明、电路板设计指南和软件迁移信息 |
| | 技术更新(TU) | 限制、勘误等产品规格的初步报告 |
| Software | User's Manual: Software | 命令集、API参考和编程信息 |
| | 应用笔记 | 用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例 |
| 工具和套件 解决方案 | 用户手册：开发工具 | 使用软件包、开发套件、入门套件、促销套件、产品示例和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南 |
| | 快速入门指南 | |
| | Examples | |
| 应用笔记 | | 用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例 |

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第一版，已发行

RA生态工作室

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

处理微处理单元和微控制器的一般注意事项 单位产品

以下使用说明适用于瑞萨的所有微处理单元和微控制器单元产品。有关详细的使用说明本文档所涵盖的产品，请参阅文档的相关部分以及为产品发布的任何技术更新。

1. 防止静电放电(ESD)

当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。

2. 上电处理

通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态在通过片内上电复位功能复位的产品中，从供电时间到供电达到指定重置的级别。

3. 断电状态下的信号输入

请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。

4. 处理未使用的引脚

按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。

5. 时钟信号

应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。

6. 输入引脚的电压施加波形

由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在V_{IL}之间的区域(V_{IL}(Max.)和V_{IL}(Min.))由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，输入电平是固定的，并且在输入电平通过V_{IL}(Max.)和V_{IL}(Min.)之间的区域时的过渡期间也是如此。

7. 禁止访问保留地址

禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些不能保证LSI的正确操作。

8. 产品之间的差异

在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。同一组中的微处理单元或微控制器单元产品的特性，但具有不同的部件号，其特性可能会有所不同内部存储器容量，布局模式和其他因素，这些因素会影响电气特性的范围，例如特性值，工作裕度、抗噪能力和辐射噪声量。当更改为具有不同部件号的产品时，实施系统-给定产品的评估测试。

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